EET 3030 Embedded Controllers
Laboratory Report

Lab 1
Voltage Division and Current Division

Presented
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Introduction and Overview

Design and simulate predetermined digital circuit according to instructions from lab 1 for EET3030. This consists of creating schematic diagrams using a variety of gates, inputs, and outputs and testing the schematic with a University Program VWF, which in turn, provides data to analyze wave forms from simulated data.

Circuit is expected to change outputs of 4 different logic gates based on different combinations of 2 inputs.

Equipment and Parts

Laptop, Quartus II software.

Theory

Digital circuit flow, analysis, and construction.

Design Calculations

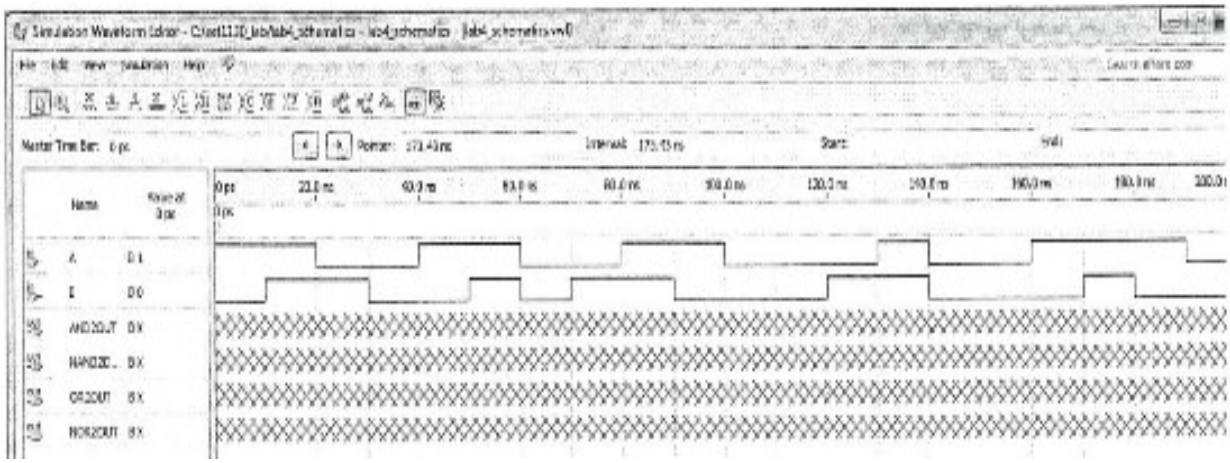
1. Create the schematic
2. Compile the schematic
3. Create University Program WVF
4. Run Functionality and Time Simulations

Schematic Diagram of the Circuits

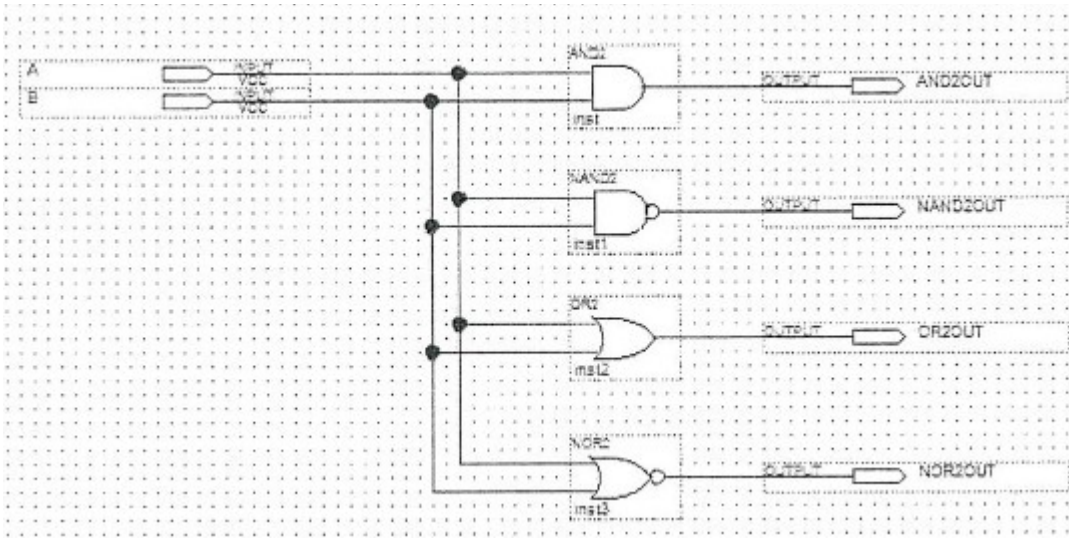
Inputs and Outputs

Name: A	Type: Input	Default Value: GND
Name: B	Type: Input	Default Value: GND
Name: AND2OUT	Type: Output	
Name: NAND2OUT	Type: Output	
Name: OR2OUT	Type: Output	
Name: NOR2OUT	Type: Output	

Inputs: 2 x (Normally open switch) – Inputs set high and low according to below graphical representation.

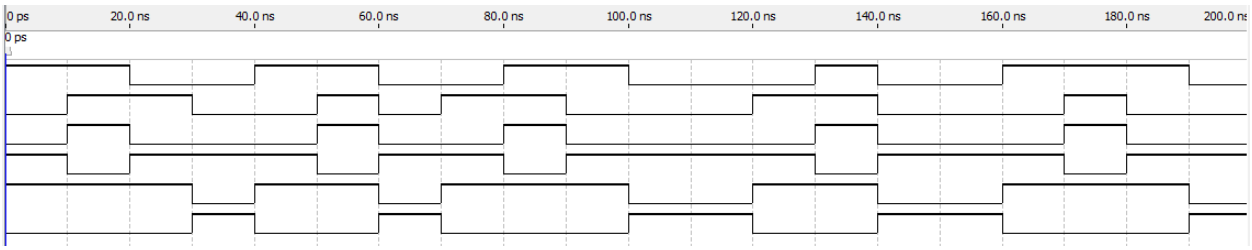


Outputs: 1 x (AND Gate, NAND Gate, OR Gate, NOR Gate)



Results

The results for the circuit are represented by the graphic below. Graphic shows results from simulations of BOTH Functionality and Timing simulations. Circuit is behaving according to design. Logic gates open and close based off the configurations of the two inputs and the wiring of the schematic.



Conclusion

I learned how create schematics using logic components, wire them together, and to test the digital circuit in two different simulations. I had never done anything like that, as I was taught Verilog and went straight to scripting. I like being able to create the diagram because it's a good visual representation of what the circuit is doing and you can visualize how it should act. That's a difficult thing to do with just lines of code.

There was a problem I encountered doing this lab when I was trying to save the .vwf file—it wouldn't run unless it was in the exact same folder as the schematic, so I found that interesting, because I wanted to keep all the .vwf files in a separate folder. Other than that, this lab went smoothly.