FPGA device details:



A. Resource Utilization Graphical user interface, application

Description automatically generated

a. LUTs = 898

b. Slices = 898 (LUTs) + 520 (Registers) = 1,418

c. Flip-flops = 264

d. LUT-FF pairs = NA

e. BRAMs = 6

f. DSP units = 0

g. I/O pins = 394

IO Port errors were generated during synthesis cum implementation. These errors seem to arise from incorporation of AES\_Enc package for implementing Ek block of datapath. Details have been uploaded in attached screenshots. Due to these failures, below 2 steps have not been completed.

Future work would involve decoupling top-level bdi input from input to internal EK block to obtain minimum clock period.

B. Numerical values of the following timing parameters

a. Minimum Clock Period

b. Maximum Clock Frequency

c. Maximum Throughput for processing of a large number of

i. associated data blocks

ii. plaintext blocks

iii. ciphertext blocks

v. hash message blocks (only if your algorithm supports hashing)

based on the minimum clock period after placing and routing.

C. Analysis of the obtained results, observations and conclusions.