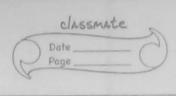
Momework -3 CS2323 - Computer Architecture 1. Given: 6 staged pipeline processer (p)
Delays - 130,125,110,132,135,145 ps.
Pipeline register delay - 12 ps. a) # instruction to be executed - 1000 # cycles required (with pipeline and no state cycles) = n + p - 1 = 1000+6-1 Clock cycle = Delay of the longest Longest delay + pipeline segister delay (if any) Clock cycle = (145+12) ps = 157-ps = 157785 p = 157785 ps

cycles Incur b) Now 20% of the a 1 cycle stall Additional time = 200 x 157 Total time = (157785 + 31400)ps = 189185 ps 2) Given: P1 = 15 a 5 stage ideal processor with 800ps latercy P2 is similar to P1 but viruledes mult intrubbs increasing the latercy of ALU by 250 ps but seduces instruction count by 10%. a) For P1, dode cycle = time for ear stage (as it's equally divided) Min clock cycle = 300 = 160 ps For P2, clock cycle = longest stage delay (i.e. the ALV stage) = 160+250

b) Lets say P1 has to execute x instructions.

P2 executes 0.9 x instructions Tp = I.Cp, x (dock cycle)p1 Tr= I.Cp= x (Worksylle) pr $T_{p_j} = (x + 5 - 1) \times 160 \text{ ps}$ As its a pipelined processor Actual I.C = A + p-1 Tp, = (2c+4)160 = (1602c+640)ps $Tp_2 = (0.9x + 5 - 1) \times 410$ $= (0.9x + 4) \times 410$ = (369x + 1640) psfor any x > 0 , Tp2 y Tp1 o PI executes à given code in smoller time. 51 x 21 x 12 x 13 c 1d x 11 4(x/2) 2 (1 x 13 0(15)

c) Ff = 5000 (Given) Tp1 = I. Cp1 x Clock cylap1 = (5004 x 160) ps = 800640 ps Tp2 = 7. (p2 x Clock cycleps = (4504 x 410)ps = 18 46 640 ps 3. Original code-2 add x14 x 12 x11 2 add x15 x14 x12 3 ld x13 3(x13) 4 1d x 12 0 (x 14) s and x 13 x 15 x 13 2 1d x 11 4(x/3) 2 sd x 13 0(x15)



a) add x 14 x 12 x 11

nop

add x 15 x 14 x 12 # R instruction requires 2 rops data huzerd x14 x12 1d x 13 3(x13) # Only 1 nop
as yd x12 u(x12) O(x14) ld x 12 nop and x13 x15 xx13 alt as an nop. nop 1d x11 4(x13) # Some as above. sd x13 O(x15) i) 2 × 14 data accesses made successively in line I and 2.

2 rope for writeback of line 1.

to be completed before decode of line 2 line 4 acts as a nop and in one more nop is required to avoid data hazard

5 & 6. Handled on in (i)

b) No nops required as pipeline required the forwarding of the required data to the appropriate stage.