VLSI Physical Design INTERVIEW QUESTIONS

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What are sanity checks?

a) Netlist Checks

i. Outputs are connected to vdd or gnd

ii. Inputs are floating

iii. Is there any feedback loop in combinational block

iv. Are there any multiple driver nets

v. Is there any empty module (LEF/LIB not available for module)

vi. Is there any tri-state buffers

vii. Are there any black-boxes present

b) SDC Checks

i. IO Delay constraints are defined or not

ii. There is no clock defined for clock port

iii. Multiple clocks are reaching the flop

iv. There is no input transition or input driver defined for a port

v. There is no load defined for output port

c) Linking related checks

i. LEF Views

1. Cells not defined in library

2. Cells with missing dimension, geometry, direction

ii. LIB Views

1. Timing related information is missing

iii. PG Checks

1. Reports if PG nets are not defined, or not connected to PG terminals

iv. Tie high, Tie low checks

1. Reports if tie high, tie low terminals connected to other nets.

d) Netlist vs SDC Checks

i. For this we do the analysis using ZWLM (zero wire load model)

ii. Use command set zero_interconnect_delay_mode = true to do this

Explain routing in detail?

Routing is the process of creating physical connections based on logical connectivity. Signal pins are connected by routing metal interconnects. Routed metal paths must meet timing, clock skew, max trans/cap requirements and also physical DRC requirements.

There are 3 steps of routing operations: Global routing, track assignment, detailed routing.

Global route: It identifies nets with shortest path and assigns them to specific metal layers and global routing cells. It avoids congestion, detours and blockages. Uses steiner tree or maze algorithm.

Track assignment: It takes the global routed layout, assigns track to all nets. It performs DRC unaware assignment.

Detailed routing: Performs DRC aware routing. It is the final stage of routing

Explain Crosstalk and what commands you used for fixing it ?

Crosstalk occurs when highly switching aggressor net causes victim to change behaviour.

Because of cross-talk, the signal maybe delayed or may reach earlier than expected.

To avoid crosstalk we do shielding of switching nets like crosstalk shielding.

TAP Cell distance, who will give you the number ?

Tap cell distance was 20um and was given from foundary.

What are PD Inputs and Contents.

PD Inputs include the following files:

a) LEF (Physical View of Cell. i.e. its size, area, orientation etc.)

b) Lib (It contains timing and power related information of cells).

c) Upf (It is used in low power design. It contains information related to which power domain being
used, what isolation cells are being used etc.)

d) TF (Technology file, it contains information related to which metal layers are used and what are
their width, resistivity and other parameters.)

e) Netlist File (it's a verilog file containing information related to logical connection between
standard cells)

f) SDC (It's a synopsys design constraints file which contains information related to clocks. Which
clocks are being used. What is max trans, max cap. What is clock definition, latency, uncertainty.
What is path exceptions in design, i.e. false path, multi-cycle path etc.)

g) tluplus file: It contains information related to R & C values.

h) IO Assignment File

How will you highlight the net in the GUI?

Change_selection in ICC

How will you try to minimize the timing in placement and CTS stage ?

Usually placement bounds and path grouping is used to minimize timing in placement stage.

In CTS we can use high driving strength buffers, replace buffers with pair of inverters etc. to minimize timing.

What is Electromigration ?

It is the slow displacement of metal atoms in a semiconductor. It occurs when the current density is high enough to move metal ions in direction of electron flow. This phenomenon causes the eventual loss of connections or failure of a circuit. Hence, the circuit faces reliability issues. To test for reliability, the DUT is put under high temperature operating life conditions, and the data obtained is extrapolated to estimate the durability.

Explain clock gating?

Clock gating is the method of gating clock signal so that we can save clock power by turning off the gate in case a certain gated portion of design is not in function

How you will analyze the congestion?

Report_congestion, it will report grc overflow. For other congestion, we give keep-out margin or partial blockage.

How do you fix congestion?

Congestion occurs when numbers of routing tracks available for routing are less than required routing tracks.

Types of Congestions:

a. Congestion between macros

i. First check fly lines, check net connections, place macros connecting each other closer

ii. If there is more connection from macro to macro, place those macros nearer to each other preferably nearer to core boundaries

iii. If input pin is connected to macro, better to place nearer to that pin or pad

iv. If macros have more connections to std cells, spread the macros and add soft blockage if not added already

b. Congestions in core

i. Local congestion - Check for pin and cell density. Spread cells and insert partial blockage if necessary

Pin density is due to more pins in particular area. For example, OAI, AOI has more pins and it causes pin density

ii. Global congestion - Check for cells causing congestion. Do the cell padding/keep out margin

iii. Module splitting - Tool splits the modules sometimes, causing the congestion by using routing resources

Why clock buffer is used instead of normal buffer in CTS?

Clock buffers have symmetrical rise and fall time.

In CTS which topology you have used?

We used H-Tree in our block

What is latency?

Latency is the delay of clock signal to reach from clock start point to clock end point. To set clock latency, we use the command:

set_clock_latency

In placement what issues you have faced?

In placement, I faced issues related to congestion, timing and module splitting. In congestion, I faced issues because of cell density, pin density and in timing the issues were related to setup timing.

ECO timing fixing commands?

fix_eco_timing -type setup

fix_eco_drc

write_eco_changes filename

How can you get your block size?

The command for block size is get_attribute [get_die_area] bbox

What are the Checks after floorplan.

After floorplan, we check following things:

a) There should not be any overlap between macros. All macros should have required spacing and their placement must be legalized.

b) There should not be any notches in the design and if at all, the notch is present even after performing multiple iterations, a hard blockage must be placed.

c) The pins must be placed in the center of track and legalized.

How can you fix violations using spare cells ?

We can use spare cells to fix violation, usually it is done in functional eco. If there are few changes in RTL, we will get updated netlist, which has to be implemented and this is done using spare cells in design.

In functional eco, after implementing updated netlist, there will be new violations, which needs to be fixed.

What is difference between Graph based and Path based analysis.

GBA Mode is more pessimistic and less time consuming.

PBA is more accurate and more time consuming.

What are the guidelines for routing?

Routing order: Power routing, Clock routing, Signal routing.

How you decided channel distance between macros?

Channel length between macros = $\frac{(\text{pin pitch} * \text{no of pins}) + \text{space between pins}}{\text{Number of horizontal/vertical metal layers}}$

What are tap-cells, end-cap cells?

Tap cells are used to avoid latch up problems. These cells are placed at particular distance in design to avoid latch up.

End cap cells are placed at the edge or end of the row to satisfy well tie off requirements. This will serve as end point of that row.

How do you fix EM issues?

Generally we increase metal layer width wherever we get EM Issues.

How did you fix IR Drop issues in P&R

Static IR - Increase strap width

Dynamic IR - Use decap cells

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Explain Antenna Effect ?

Antenna effect is plasma induced gate oxide damage that can cause reliability problems in manufacturing of MOS ICs. It occurs due to accumulation of charge carriers near the gate of transistor. The tool will calculate if metal area connected to gate is more than gate area then, charge accumulation will occur and may damage the gate. Hence, we need to reduce it. It can be done by use of metal jogging technique (use of higher metal layers), use of standard cells or use of reverse bias diode.

What is difference between keep-out margin and blockage?

Keep out margin is attached to cell/instance, which means if you move cell/instance the keep-out margin also moves along with the cell.
Blockage depends on its coordinate; hence it stays in the same place.

If timing is not met during placement stage, can you still continue for CTS?

We should keep on checking the log continuously, and we will observe the value of WNS. If it keeps on increasing to large value then we need to see our floorplan again.