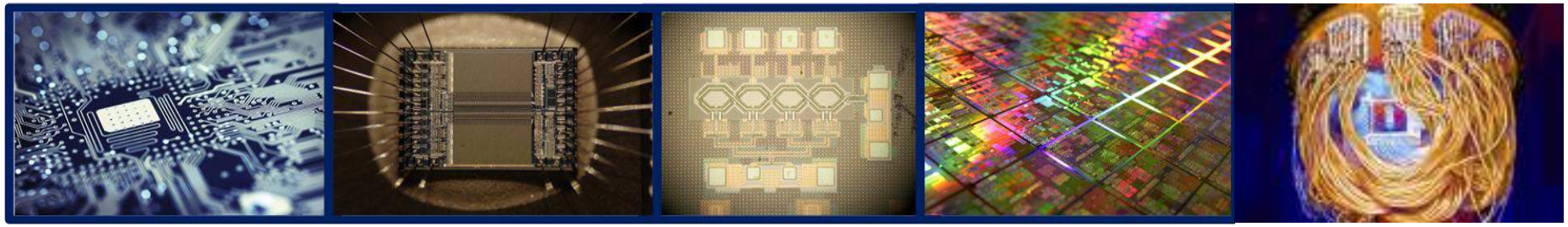

Online Professional Development Course on
INTRODUCTION TO DEVICE AND SYSTEMS PACKAGING

An Introduction to Devices

by

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Outline

1. Introduction to Integrated Circuits (IC)
2. Semiconductors for IC Fabrication
3. Device Characterization
4. Next Generation Computers
5. Microelectronic Devices- PN Junction, MOSFET

What is an IC?

- An integrated circuit (IC) is a piece of semiconductor wafer on which several smaller footprint based electronic devices such as resistors, capacitors, diodes and transistors are fabricated.
- The interconnection of these devices inside the IC forms electrical circuits which can together function as an amplifier, oscillator, timer, counter, logic gate, computer memory, microcontroller, microprocessor, etc.

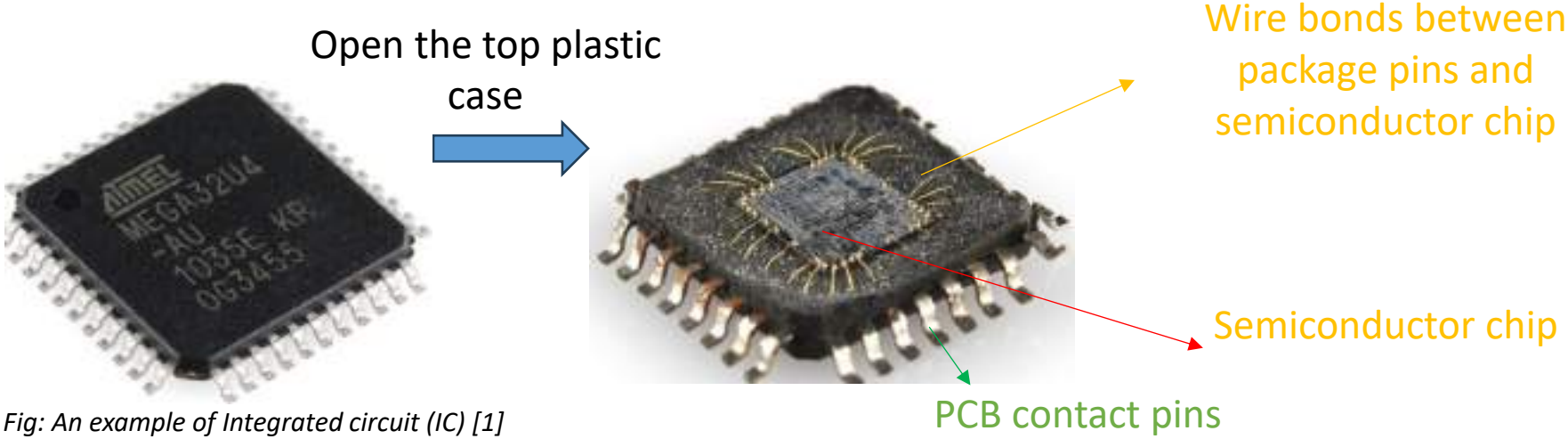
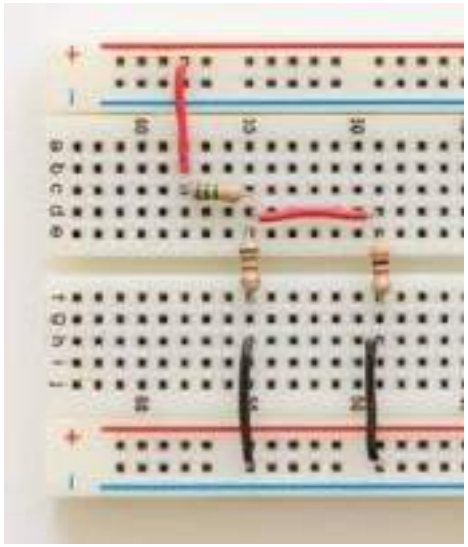


Fig: An example of Integrated circuit (IC) [1]

[1] https://learn.sparkfun.com/tutorials/integrated-circuits/all

What is an IC?

- An IC can also be defined as a complex set of tiny components and their interconnection that are imprinted onto a tiny slice of semiconductor material.



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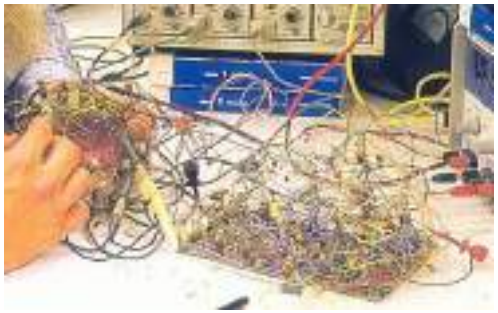


Fig: Demonstration of the complexity and interconnection capabilities of an IC

Application of ICs

- Computer (Arithmetic, logic and memory)
- TV/Radio/video
- Cell phones
- Digital clock
- Robotic systems
- Telecommunication
- Automotive
- Medical equipment
- Aerospace/Navigation
- Remote sensing
- Toys
- Military applications

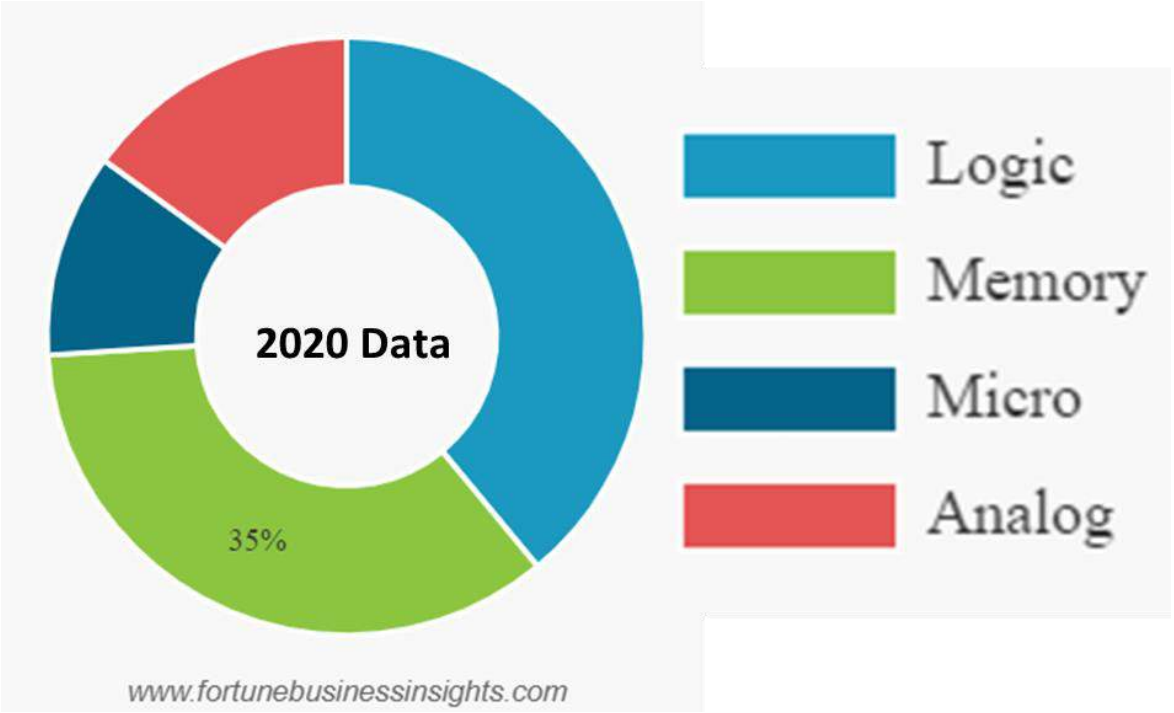
Fig: Some applications of ICs

Advantages of ICs

- Small
- Low cost
- Light weight
- Low power consumption
- Easy replacement
- High reliability
- High speed
- High frequency

Global Status of ICs

- The global IC market is projected to grow from USD 489.31 billion in 2021 to USD 1,136.98 billion in 2028, at a CAGR of 12.8% during the 2021-2028 period
- IoT/AI and Automotive (EV) will drive additional IC demand



Status of ICs in India

- Fabs in India: SCL Chandigarh (0.18 micron CMOS), GAETEC (GaAs), SITAR
- Indian Academia: IIT Bombay (INUP), IIT Delhi (NRF), IISc Bangalore (CENSE), etc.. have clean rooms with basic fabrication and physical/electrical characterization equipment
- India Semiconductor Mission (ISM) launched in 2021 envisions to foster IC manufacturing plants and the entire ecosystem
- Academic R&D is targeting
  - massive R&D in integrated Systems Technologies to attract global IC manufacturing companies to India
  - large scale education and skill development programs, such as this course, to create the required talent pool
  - 12 strategic research areas identified for integrated systems design and manufacturing

IC Flowchart

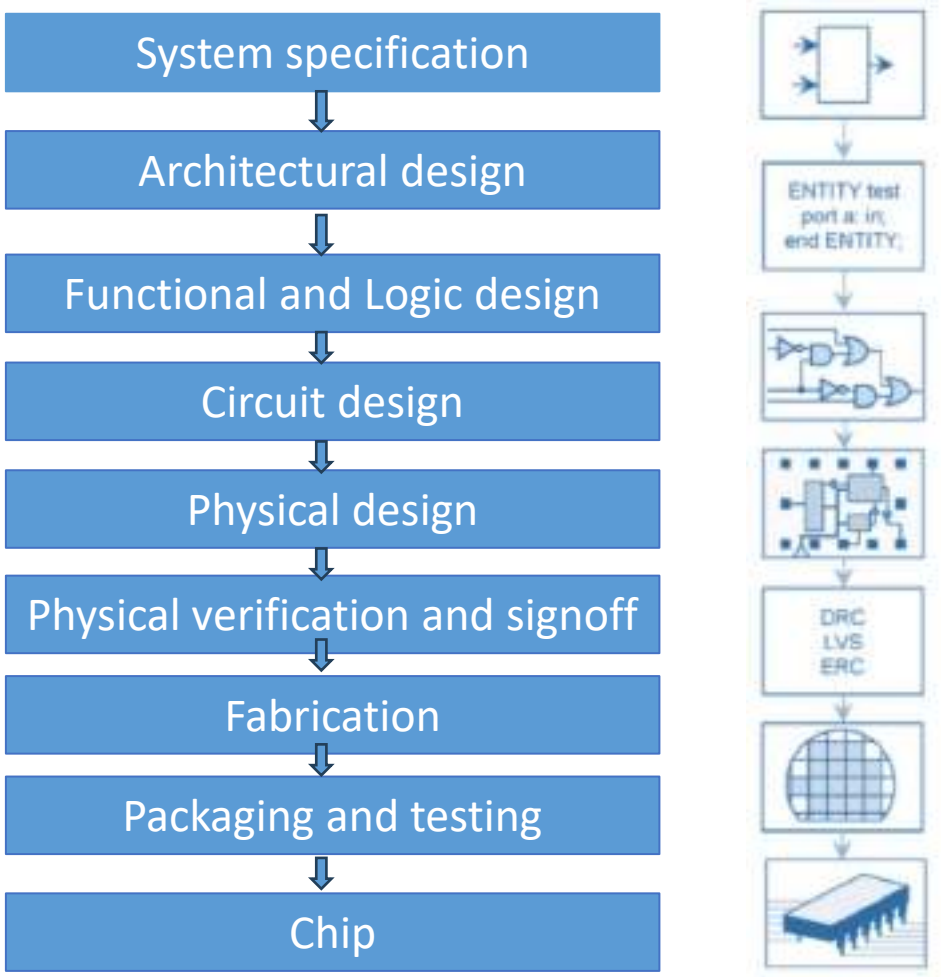


Fig: Process flow for digital IC design

Types of ICs

- The ICs can be classified using several categories. Based on the intended application, the ICs can be classified as under:

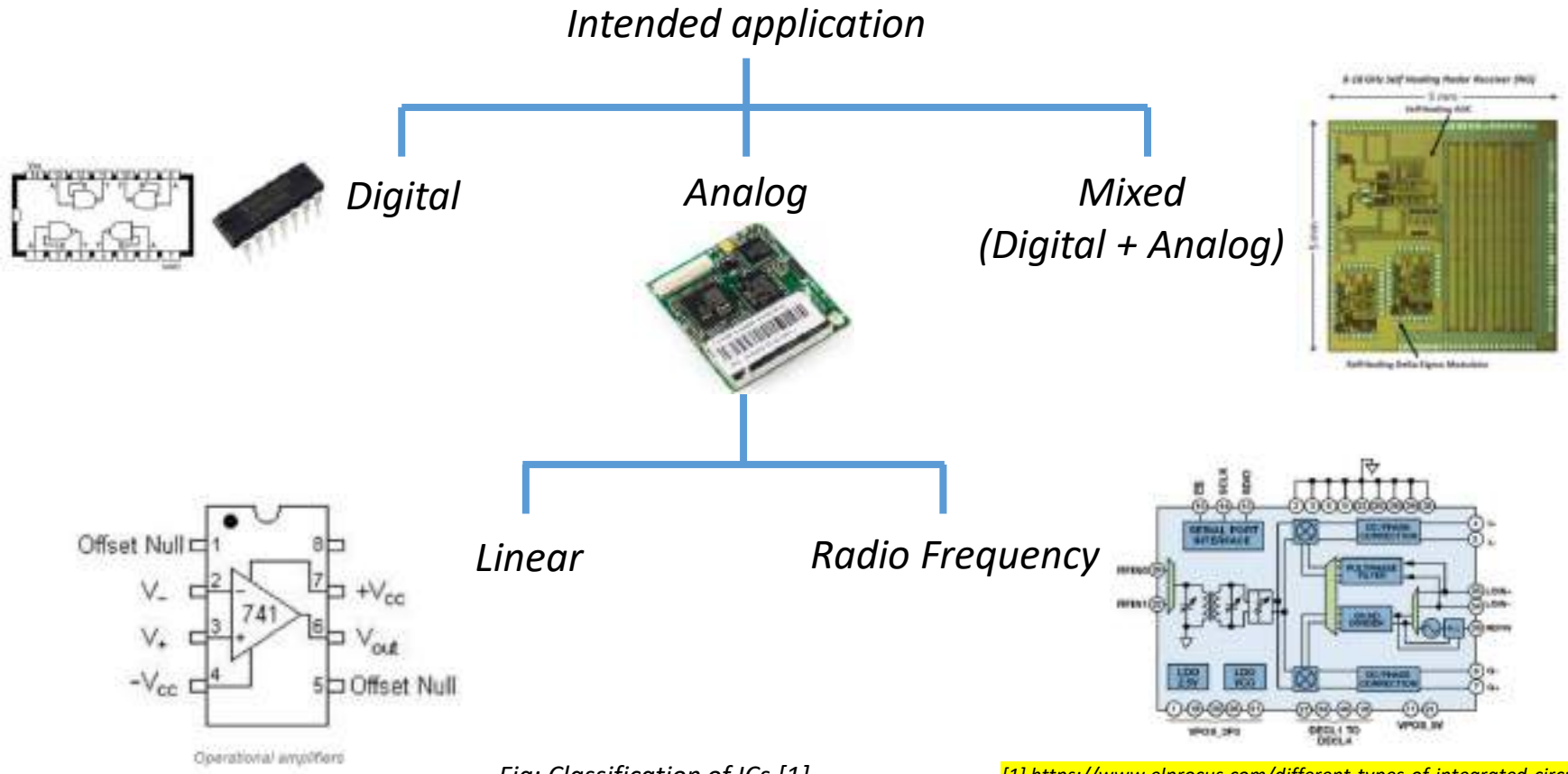


Fig: Classification of ICs [1]

[1] https://www.elprocus.com/different-types-of-integrated-circuits/

Types of ICs

- Based on the type of packaging, the ICs can be classified as under:

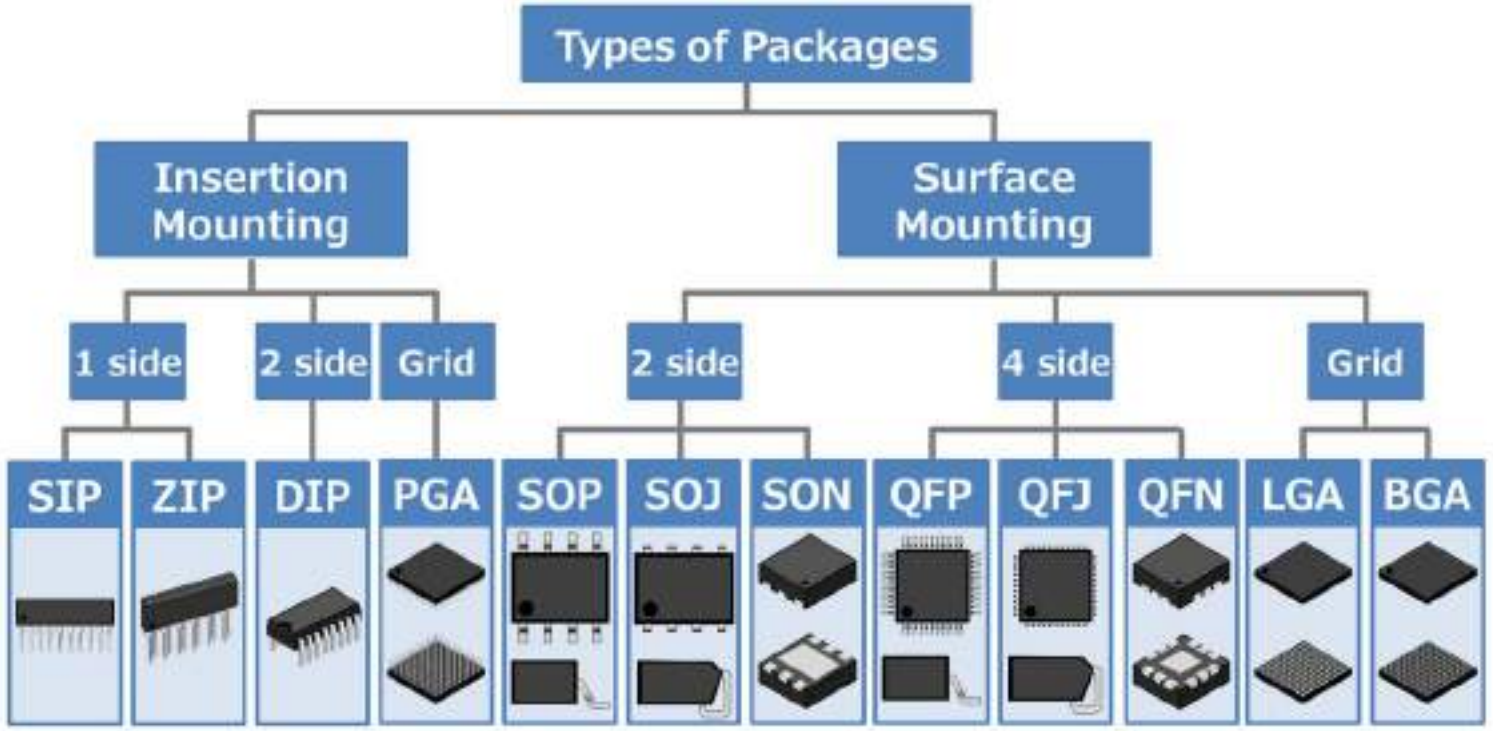


Fig : Classification of ICs based on types of packages [1]

[1] https://electrical-information.com/package-types/

IC-Evolution

❑ICs have traversed a long way from day one until today, undergoing a series of evolution phases:

1. Small Scale Integration (SSI):

- Small-scale integration is a technology that was first used to describe the fabrication of 10 to 100 components on a single chip and was used between 1961 and 1965.
- This was useful for the manufacture of flip-flops and logic gates.

2. Medium Scale Integration(MSI):

- The world witnessed a shift from small-scale integration to medium-scale integration between 1966 and 1970 when the fabrication of 100 to 500 components on a single chip was possible.
- This technology was helpful for multiplexers, counters, and decoders.

IC-Evolution

3. Large-Scale Integration (LSI):

- With the advancement of technology between 1971 and 1979, 500 to 300,000 components could be fabricated over a single chip giving birth to the concept of LSI.
- This technology proved handy in manufacturing RAM, ROM, and microprocessors.

4. Very-Large Scale Integration (VLSI):

- This technology allowed a huge number of components on a single chip- about 300,000 to 1,500,000.
- VLSI made developing RISC, 16 and 32-bit microprocessors, and DSP easy.
- This technology was in use between the years 1980-1984.

IC-Evolution

5. Ultra-Large Scale Integration:

- Following 1985, there was a considerable technical breakthrough that allowed the fabrication of more than 1,500,000 components to billions on a single chip.
- This technology then found its usage in the making of 64-bit processors and is used even today with more devices per chip
  - Current record (2023) is with deep learning processor Wafer Scale Engine 2 by Cerebras having 2.6 Trillion transistors on the chip with TSMC 7-nm process!

IC Materials and Processes

- IC manufacturing is a multistage process.
- The first step is the conversion of quartzite into MGS.
- Then converting MGS into EGS.
- After which pure Silicon Ingot is formed using the CZ/FZ technique.
- Using diamond sawing, Silicon wafers are cut from this ingot.
- Wafers are polished with chemical and mechanical polishers to produce polished wafers used for making devices.

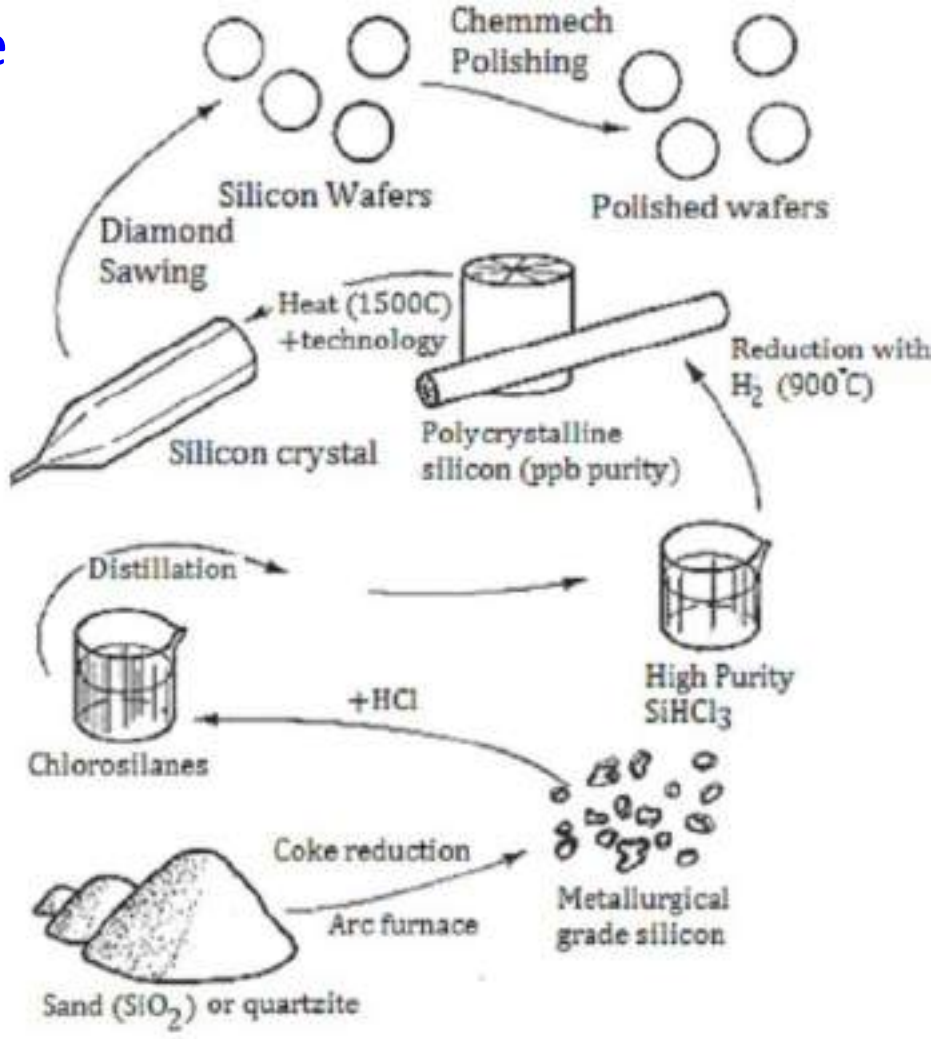


Fig : wafer process flow [1]

[1] https://shop62001.sosoutremer.org/category?name=from%20sand%20to%20silicon

IC Manufacturing process

- After the wafer is ready, the following steps are used in the IC manufacturing process:

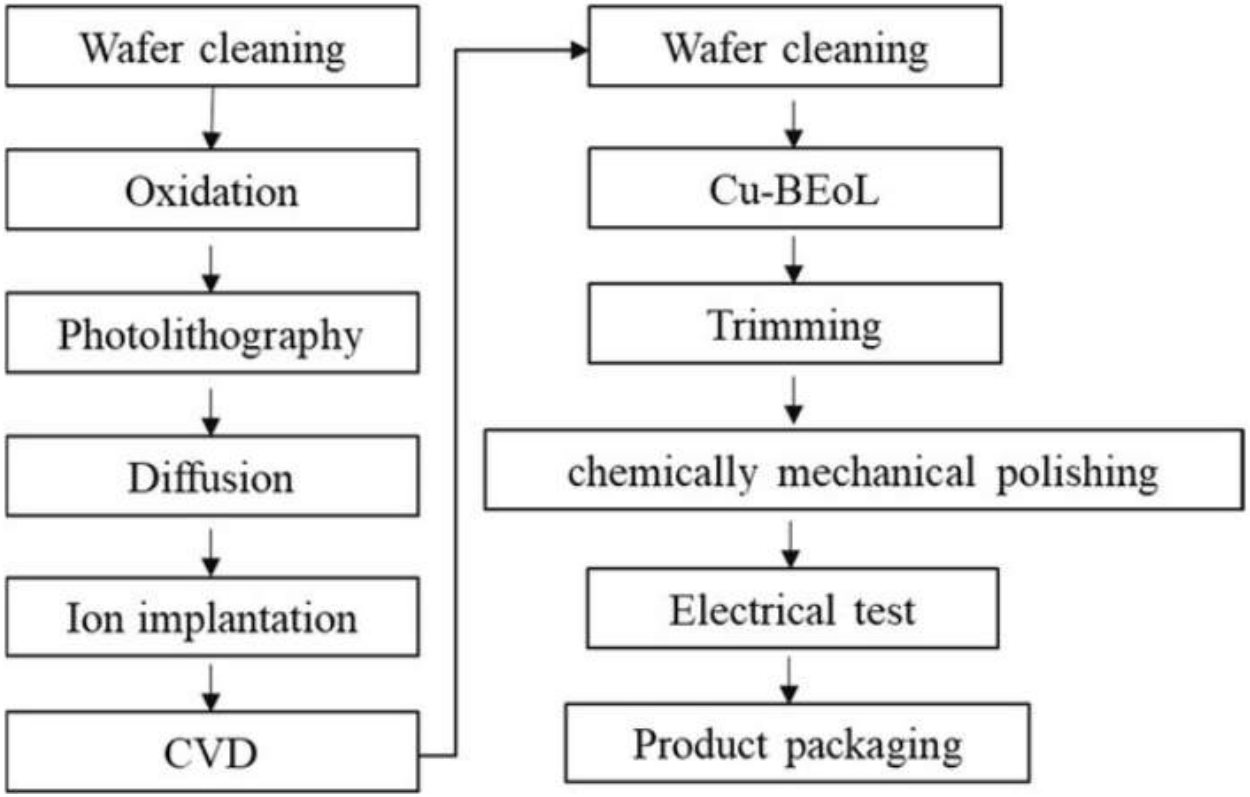
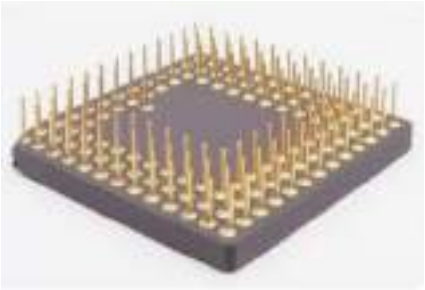


Fig : Process flow chart of typical IC [1]

[1] Shen, L.; Xiang, P.; Liang, S.; Chen, W.; Wang, M.; Lu, S.; Wang, Z. Sources Profiles of Volatile Organic Compounds (VOCs) Measured in a Typical Industrial Process in Wuhan, Central China. Atmosphere 2018, 9, 297. https://doi.org/10.3390/atmos9080297

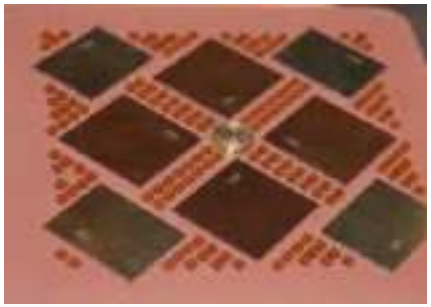
IC Packaging

- IC packaging refers to the encapsulation of semiconductor material in "package", a strong supporting case that prevents physical damage and provides electrical contacts between device and circuit board.
- For IC packaging, electrical contact materials and package material are crucial design factors. For electrical contacts; low resistance, capacitance, and inductance materials are preferred to prevent parasitics, whereas packaging materials are preferred to be physically robust, moisture-free, and have greater heat dissipation capabilities.
- Types of IC package: Lead-frame and dual-inline, chip scale, pin-grid array, Quad flat pack, Quad flat no-lead, Multichip package.



Pin-grid array

Quad flat pack



Multichip package

IC Packaging

- The Die can be attached to the package either via soldering or gluing to the substrate. The two important operations for packaging are:

- IC bonding: Interconnections are made between IC and packaging. The choice for the type of bonding depends on the package type. Some of the IC bonding schemes are listed below:
  - Wire bonding
  - Thermosonic bonding
  - Flip Chip
  - Tape automated bonding
- IC encapsulation: IC encapsulants are the final pieces of IC package that protects the conductor and wires from external environment. IC encapsulation materials can be epoxy or silicone resins.

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What are semiconductors?

- Elements in periodic table can be divided into three major sections depending on their electrical conductivity: metals (high), insulators (low or near to 0) and semiconductors (moderate).

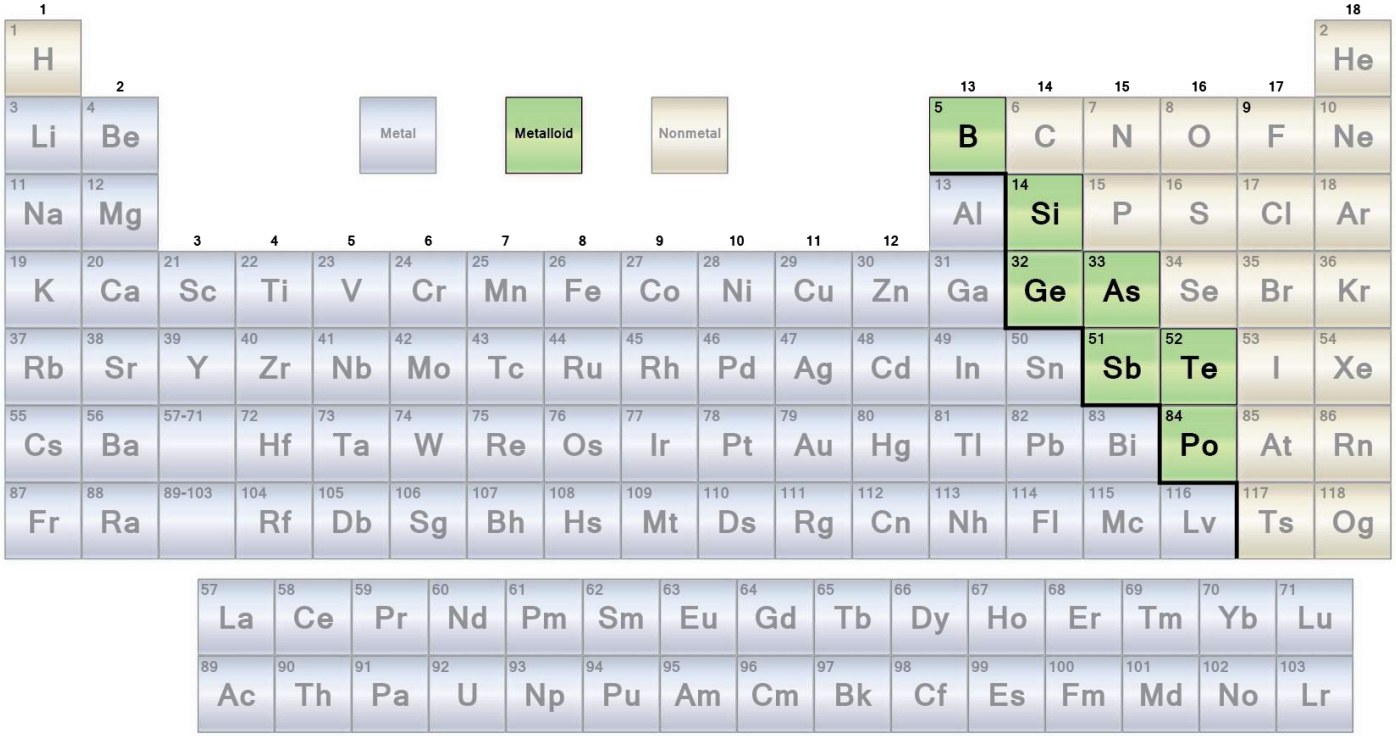

Fig: Periodic table showing position of semiconductor(metalloids)[1]

[1]: https://sciencenotes.org/printable-periodic-table/

What is the basis of this classification

- Looking at the atomic level, when atoms form a lattice the discrete energy states (orbits) of the electrons in the atom merge to form a quasi-continuous band of energies in lattice. During this process, some energy intervals are left, these are known as forbidden energy bands (or band-gap).
- Depending on the bandgap we decide whether a material is a metal (≈0 eV), insulator (>>5eV) or semiconductor (1eV – 4eV).
- The atoms forming lattice can be from a single element (Si, Ge) or different elements (III-V, II-VI)

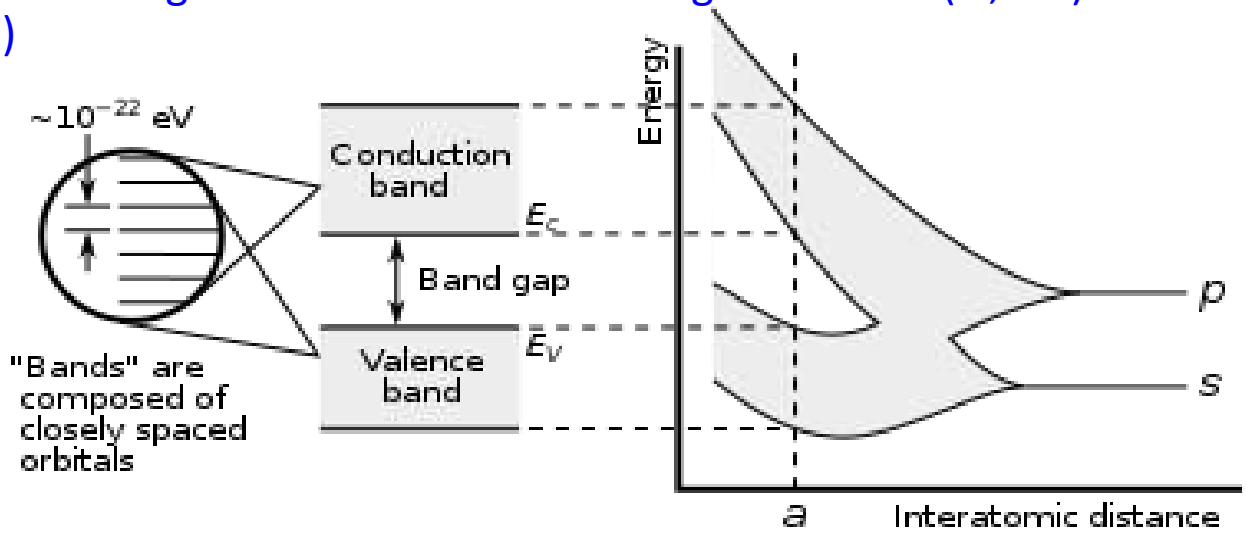

Fig: Energy levels in atom as a function of interatomic spacing[1]

[1] https://physics.stackexchange.com

Why Silicon?

- There are many semiconducting elements, but when someone talks about the semiconductor industry, its mostly about the use of Silicon.
- The first successful transistor was made from Germanium in mid-1900s.
- Si cannot be used in optoelectronic devices due to its indirect band gap
- Then what makes Silicon the most preferred semiconductor material in electronics?

Fig: First transistor made from Ge [1]

[1] https://collections.museumsvictoria.com.au

Why Silicon?

- One of the most abundant elements on earth- easily available as compared to other elements. Also, various processes are present to produce electronic grade Si from ore.
- Si has high melting point of around 1400 ^{o}C- it can withstand high temperature processes during manufacturing.

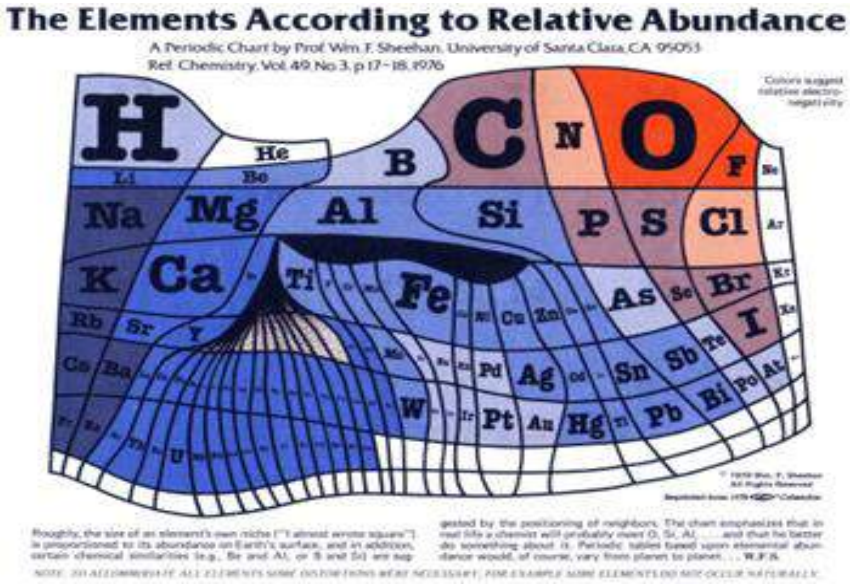

Fig: Relative abundance of elements [1]

[1] https://www.openculture.com

Why Silicon?

- Si forms SiO_2 (silica) with ease and the Si-SiO_2 interface is highly stable and better understood than any other semiconductor-insulator interface, e.g., GeO_2 dissolves in water and has low melting point!
- SiO_2 is a very good insulator with band gap of 8.9 eV and hence very low leakage current. It can sustain high fields (MV/cm).
- Lattice of Si is face centered cubic with 34% packing density which allows easy substitution of impurity atoms in the empty spaces of the lattice.

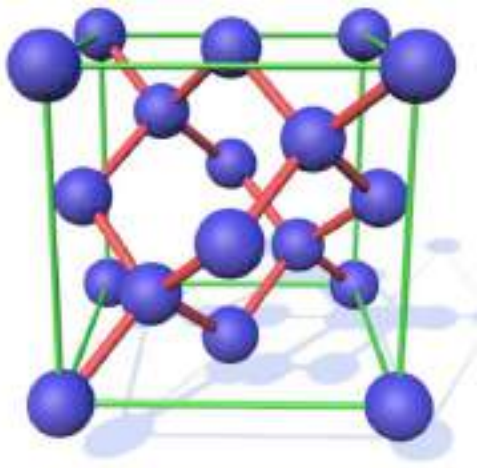

Fig: Si crystal lattice [1]

[1] https://www.turbosquid.com

Compound Semiconductors

- Materials composed of two or more elements from the same or different groups of the periodic table.
- Classification based on no. of elements:
  - Binary: SiGe
  - Ternary: AlGaAs
  - Quaternary: InGaAlAs
- Classification based on periodic table groups:
  - III-V group: GaAs, InP, GaN
  - II-VI group: ZnS, ZnSe
  - IV-IV group: SiC, SiGe

II	III	IV	V	VI
	B	C	N	
	Al	Si	P	
Zn	Ga	Ge	As	Se
Cd	In	Sn	Sb	Te

Why Compound Semiconductors?

- Compound semiconductors can achieve different bandgaps to achieve desired properties. Bandgap can be tuneable based on mole fraction in compound semiconductor.

$$Eg = h\nu$$
$$\Rightarrow Eg = h\frac{c}{\lambda}$$
$$\Rightarrow \lambda = \frac{hc}{Eg}$$

- Carrier mobility is higher.
- Low power consumption.
- High speed devices can be designed.
- At high temperatures, compound semiconductors are thermally stable.
- Compound semiconductors are direct bandgap material, so optoelectronics applications are possible.

Properties of Compound Semiconductors

- Bandgap Engineering:
  - Wide range of bandgaps possible by selecting different elements.
  - Enables control over energy levels and device characteristics.
- High Electron Mobility:
  - Faster electron movement compared to traditional semiconductors.
  - Essential for high-frequency and high-speed applications.
- Optoelectronic Properties:
  - Efficient light emission and absorption, crucial for LEDs and lasers.

SiGe

- SiGe is a solid solution formed by blending Silicon (Si) and Germanium (Ge) in varying proportions. The mixture of these elements imparts specific properties to the resulting material.
- SiGe's properties bridge the gap between silicon and germanium, offering a combination of benefits from both elements. This includes enhanced electrical and thermal performance compared to pure silicon.

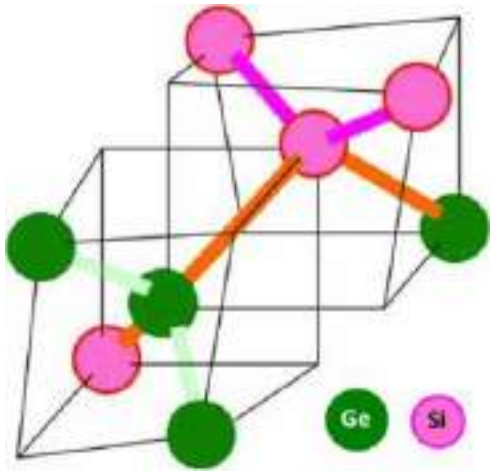

Fig: SiGe lattice [1]

- One of SiGe's notable features is the ability to engineer its properties by adjusting the ratio of silicon to germanium. This adjustability allows for tailoring its characteristics to suit different applications.

[1] I. Yonenaga, "SixGe1-x Bulk Crystals," in Reference Module in Materials Science and Materials Engineering, Elsevier, 2016.

Properties of SiGe

❑ Tunable Bandgap:

- By adjusting the ratio of silicon to germanium, the bandgap can be tailored to suit specific applications for optoelectronics and high-speed circuits.

❑ Thermal Expansion Matching:

- SiGe thermal expansion coefficient closely matches that of silicon when SiGe is integrated with silicon-based devices. This reduces stress and strain at the interface, contributing to improved device reliability and performance.

❑ Enhanced Carrier Mobility:

- SiGe offers higher carrier mobility compared to pure silicon resulting in improved transistor performance in high-frequency applications.

❑ Compatibility with Silicon Technology:

- SiGe's compatibility with standard silicon fabrication processes enables the creation of hybrid structures that leverage the benefits of both materials.

Applications and Future Prospects of SiGe

❑ RF and Microwave Applications:

- SiGe's high carrier mobility makes it well-suited for devices like RF amplifiers, mixers, and oscillators which operate at high frequencies.

❑ Optoelectronic Devices:

- SiGe's ability to emit and detect light in the near-infrared range aligns with the wavelengths used in optical communication.

❑ High-Speed Circuits:

- Data centers rely on SiGe-based high-speed circuits to process and transmit large volumes of data quickly and efficiently.

❖ Future Directions:

- Researchers are exploring SiGe's potential contributions to quantum computing, where its properties could be leveraged for qubit manipulation and control.

GaN for High Freq. Medium Power Applications

- GaN's high electron mobility and wide bandgap make it well-suited for high-frequency applications in the range of 1 GHz to several GHz.
- GaN-based transistors are highly efficient at amplifying high-frequency signals, making them essential components in RF power amplifiers for wireless communication systems.
- GaN devices exhibit lower conduction and switching losses at high frequencies compared to traditional materials like silicon (Si) making them ideal for medium-power applications where minimizing power dissipation is crucial.

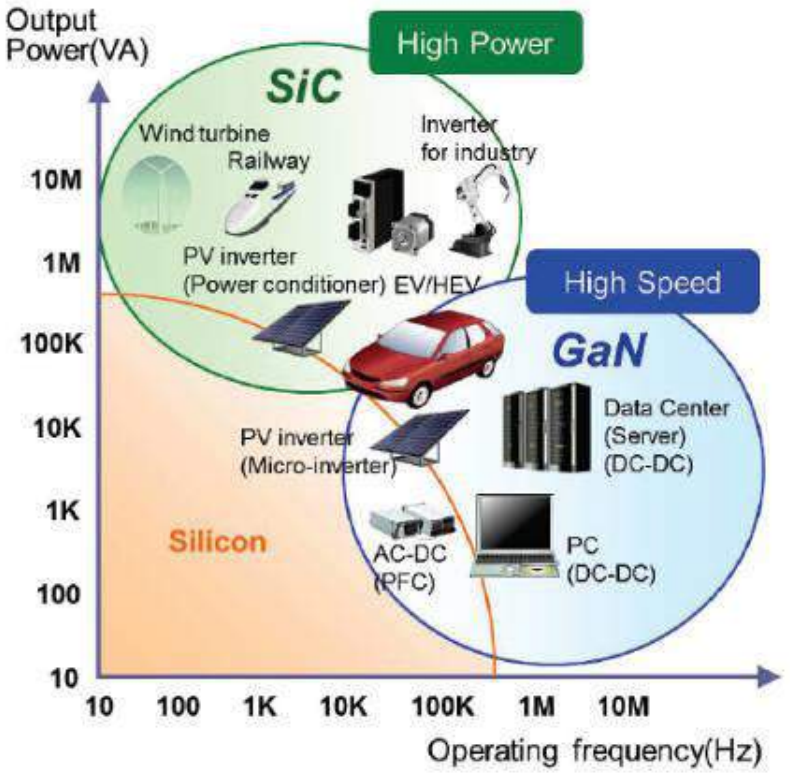

Fig: Applications of GaN materials in medium power and high frequency domain [1].

[1]: C. Langpoklakpam et al., "Review of silicon carbide processing for power MOSFET," Crystals (Basel), vol. 12, no. 2, p. 245, 2022.

SiC for Medium Freq. High Power Applications

- SiC is known for its exceptional voltage-handling capability, making it well-suited for high-power applications at low to medium frequencies.
- SiC devices offer low on-resistance, which means they experience minimal power losses when conducting high currents, crucial for high-power applications.
- SiC's superior thermal conductivity enables efficient heat dissipation, crucial for maintaining device reliability in high-power scenarios.
- SiC is a wide bandgap semiconductor which allows it to operate efficiently even at medium frequencies while maintaining high-temperature stability.

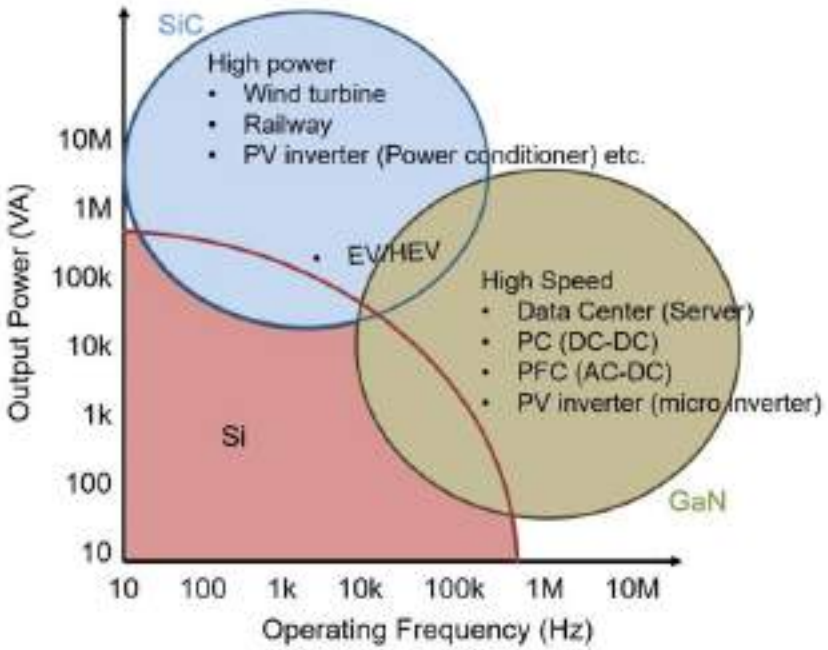

Fig: Applications of SiC materials in high power and low frequency domain [1].

[1]: C. Langpoklakpam et al., "Review of silicon carbide processing for power MOSFET," Crystals (Basel), vol. 12, no. 2, p. 245, 2022.

Comparison between GaN and SiC for Power Applications

Fig: Possible applications of GaN and SiC power devices as a function of the voltage. [1]

[1]: F. Roccaforte, G. Greco, P. Fiorenza, and F. Iucolano, "An overview of normally-off GaN-based high electron mobility transistors," Materials (Basel), vol. 12, no. 10, p. 1599, 2019.

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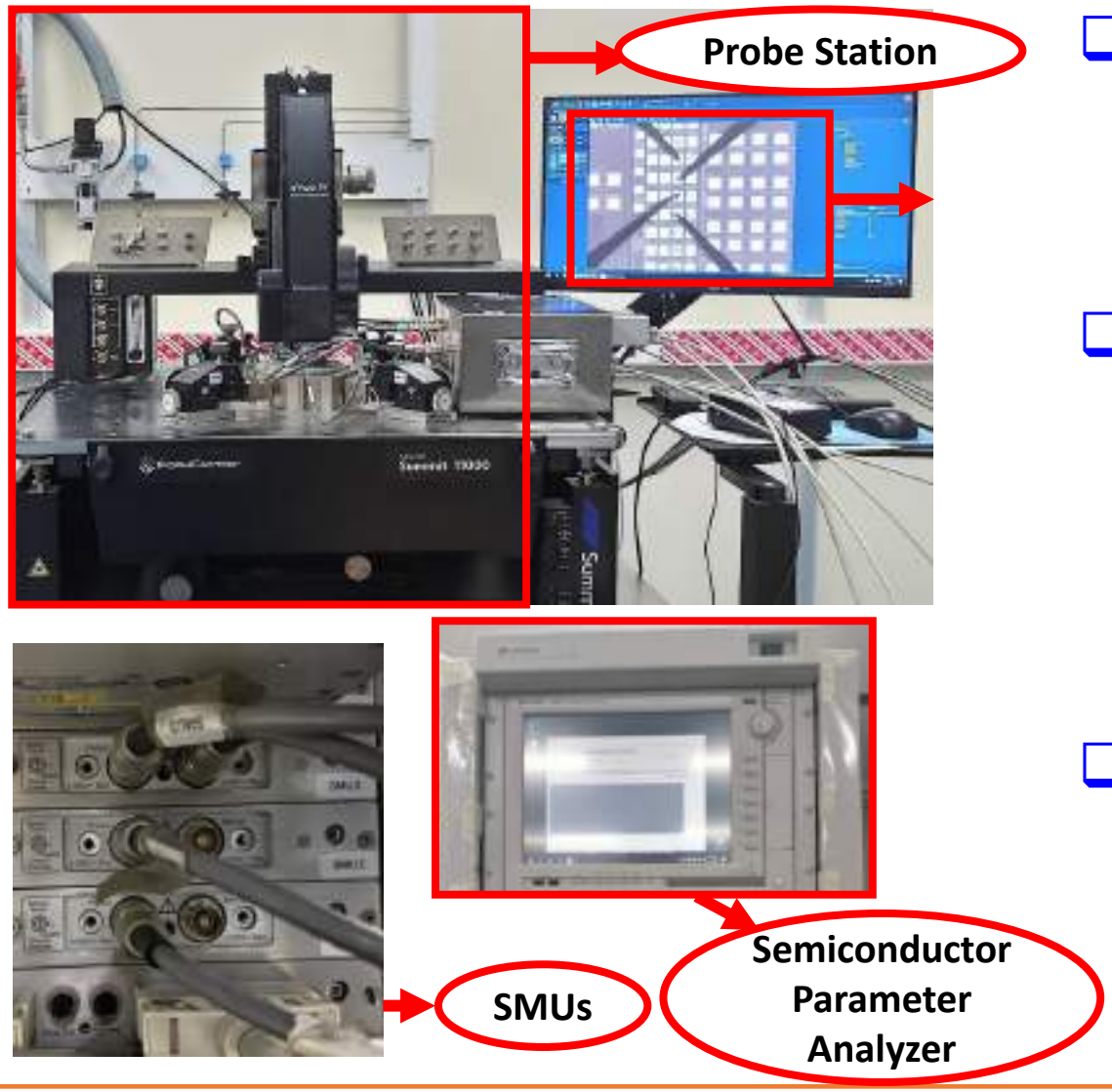
DC Characterization

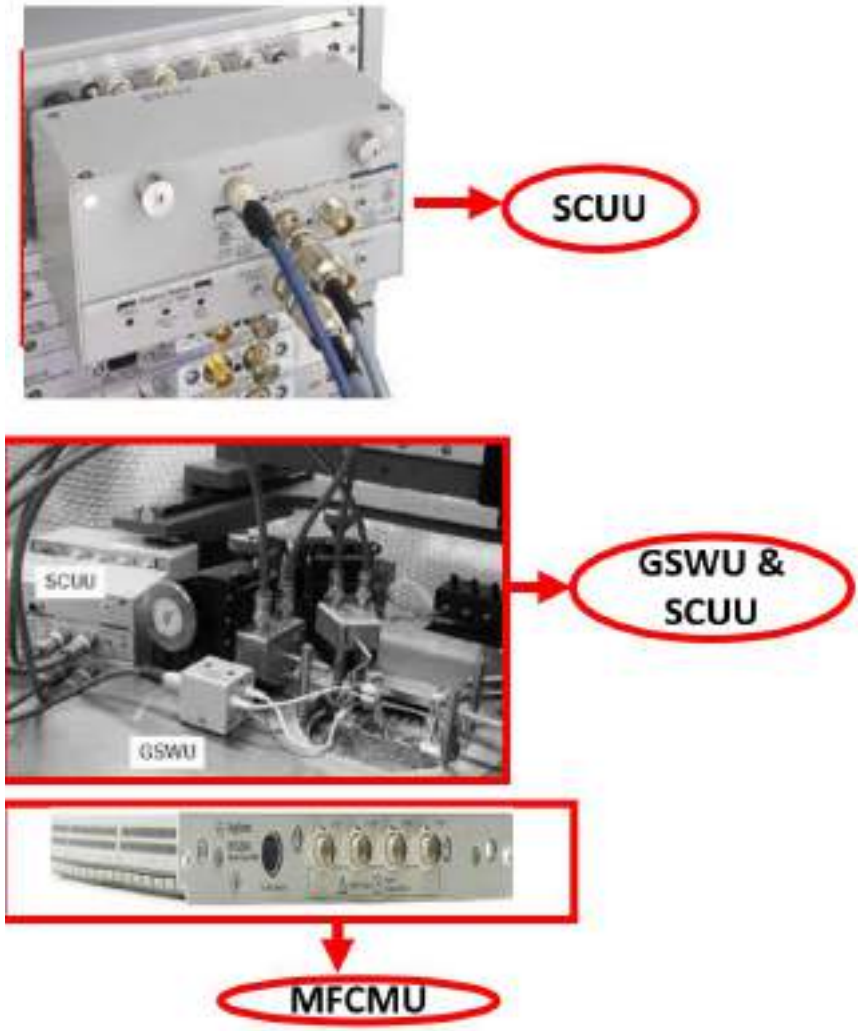
- The DC characteristics of the Devices under test (DUTs) such as MOSFETs, diodes, resistors etc. can be measured employing DC characterization technique and setup.
- The important DC characteristics that can be measured are: DC IV and CV measurements.
- On-wafer DC measurement flow:

DC Characterization setup assembly



- The die containing samples is placed on sample stage (chuck) of probe station.
- Keysight B1500A parameter analyzer with source-monitor-unit (SMUs) used for electrical characterization.
- DUTs can be characterized in all 4 quadrants through SMUs based on 4-wire method.

DC Characterization setup assembly

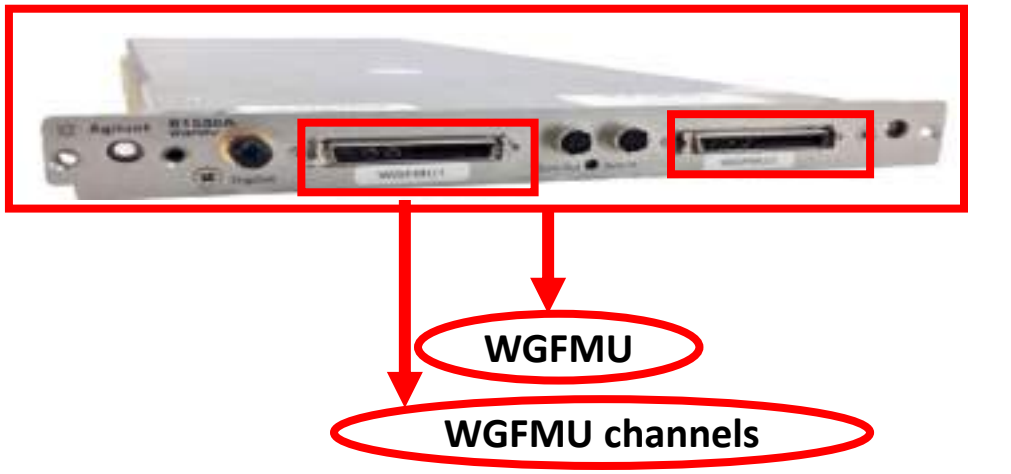


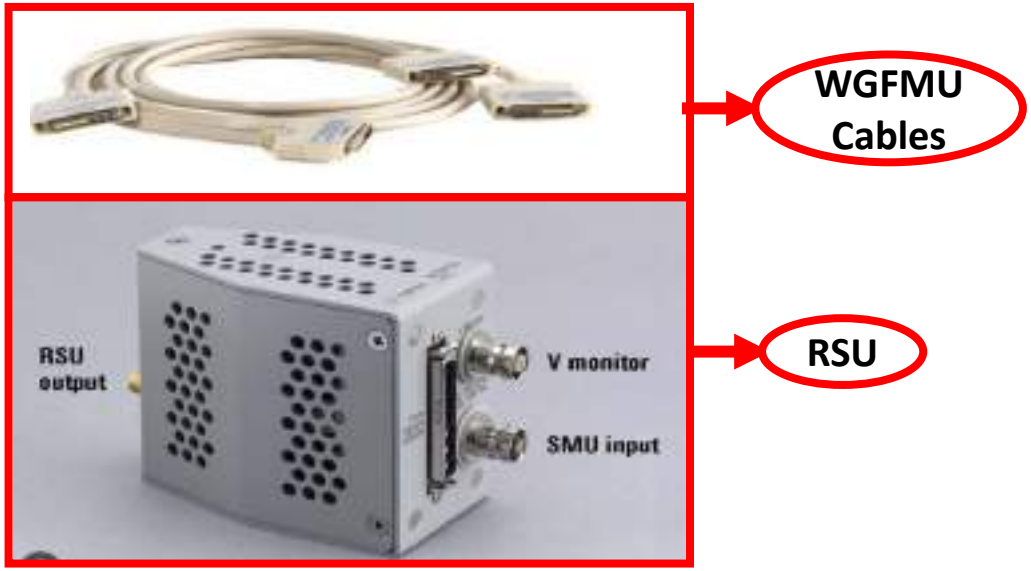
- CV measurements are performed using Multifrequency capacitance measurement unit (MFCMU) through SCUU and GSWU
- SCUU (SMU CMU unify unit) multiplexes outputs from two SMUs and CMU. It enables easy switching between IV and CV measurements.
- GSWU (Guard Switch Unit) forms a guard return path to improve CV measurement accuracy.

Pulsed Characterization

- For state-of-the art technologies, understanding the device performance under dynamic conditions is essential.
- Pulsed characterization is performed to analyze self-heating, trapping phenomena, NBTI/PBTI, TDDB, RTS Noise measurement for the devices and many more
- Keysight B1530A Waveform Generator/Fast Measurement unit enables fast pulsed measurements. It offers the combination of arbitrary linear waveform generation with synchronized fast current or voltage measurements.
- DC as well as different AC waveforms such as pulsed, staircase and staircase pulsed sweeps can be provided as inputs to the gate or drain or both terminals of the MOSFET DUT under study.

Pulsed Characterization setup





- The DUTs on the probe station are connected to WGFMU unit for applying Pulsed biasing through RSUs (Remote-Sense and switch Unit) .
- RSU has SMU input and WGFMU channel input that enables easy switching between DC and pulsed measurements.
- The RSU output connects to the DUT through probe arm assembly.

RF Characterization Techniques

RF frequency range: 30kHz-300GHz

Applications:

Communications (5G/6G)

Wireless Sensing Systems

Wireless Power Systems

RF Characterization: Small-signal and large-signal analysis

S-parameter measurements: Extracted information includes (i) Cut-off frequency (f_T), (ii) Maximum oscillation frequency (f_{max}), etc.

Challenges in RF Characterization:

- ❑Interconnects mimic transmission line characteristics
- ❑Additional parasitics like inductances may be needed

RF Characterization Techniques

Calibration

- **Calibration of measurement setup needs to account for parasitics associated with connection of VNA to a device under test (DUT)**
  - Connection results in additional losses, reflective discontinuities, and phase shifts
- **Calibration Techniques:**

Open Short, SOLT (Short-Open-Load-Thru), SOLR (Short-Open-Load-Reciprocal), TRL (Thru-Reflect-Line), LRM/LRRM (Line-Reflect-Match/Line-Reflect-Reflect-Match)

- **A special Impedance Standard Substrate (ISS) with precisely defined standards is used**

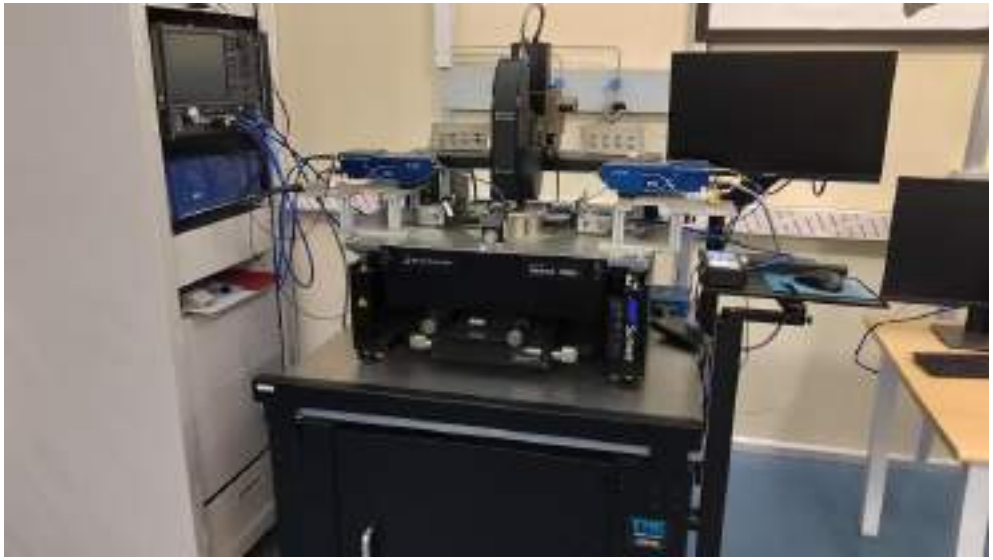
RF GSG Probes :

ACP Probes

Infinity Probes

RF Load Pull Characterization

- Load pull: Technique for RF device characterization.
- It involves tuning the load impedance while measuring device characteristics.
- RF circuits are essential components in 5G and 6G communication, mobile phones, Wi-Fi routers, satellite communication, Bluetooth devices, and more.



Load Pull Methodology

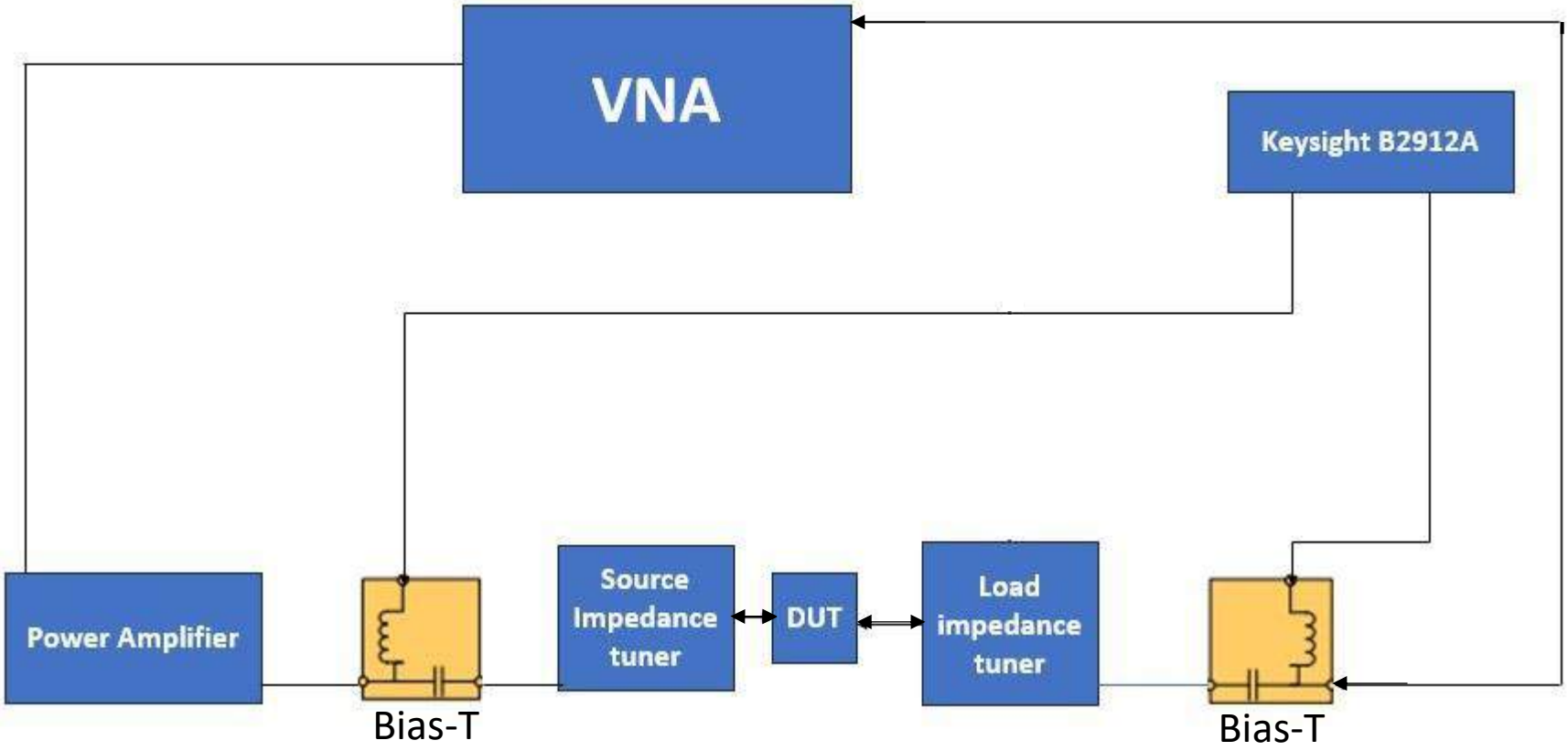


Fig: A typical load full characterization setup

RF Frequency Bands

Frequency Bands

Letter Designation	Frequency Range	Wavelength Range
L band	1 to 2 GHz	15 cm to 30 cm
S band	2 to 4 GHz	7.5 cm to 15 cm
C band	4 to 8 GHz	3.75 cm to 7.5 cm
X band	8 to 12 GHz	2.5 cm to 3.75 cm
Ku band	12 to 18 GHz	16.7 mm to 25 mm
K band	18 to 26.5 GHz	11.3 mm to 16.7 mm
Ka band	26.5 to 40 GHz	5.0 mm to 11.3 mm
Q band	33 to 50 GHz	6.0 mm to 9.0 mm
U band	40 to 60 GHz	5.0 mm to 7.5 mm
V band	50 to 75 GHz	4.0 mm to 6.0 mm
W band	75 to 110 GHz	2.7 mm to 4.0 mm
F band	90 to 110 GHz	2.1 mm to 3.3 mm
D band	110 to 170 GHz	1.8 mm to 2.7 mm

Applications of Load Pull Characterization

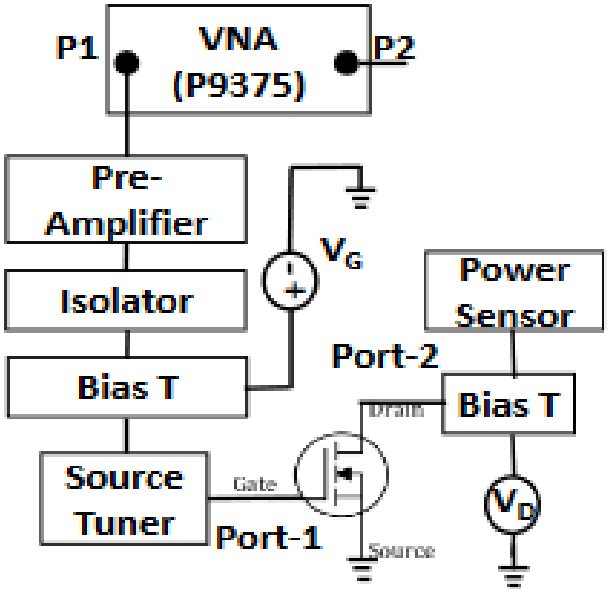


Fig: Measurement setup for the large-signal reliability characterization

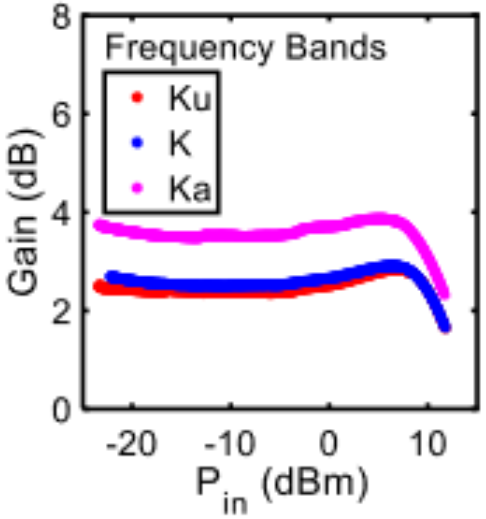


Fig: Comparison of Gain (dB) of PA cell at different frequency bands biased at $V_{GS} = 0.5\ V$ and $V_{DS} = 1.5\ V$

A. Rathi, P. Srinivasan and A. Dixit, "Impact of RF Frequency Bands on the DC and Large Signal Reliability of a 45nm RFSOI NFET based Power Amplifier Cell," 2023 7th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), Seoul, Korea, Republic of, 2023, pp. 1-3, doi: 10.1109/EDTM55494.2023.10102985.

CRYOGENIC CHARACTERIZATION

- Electrical characterization of devices down to cryogenic temperatures.
- Cryogenic temperatures: below 120K (-153^{o} C)
- Need proper cooling systems along with cryogenic compatible characterisation setup.
- Two types of cooling systems:
  - Open cycle Refrigeration : Direct contact of coolant with the substrate to be characterised.
  - Closed cycle Refrigeration : Indirect contact of coolant with the substrate to be characterised.
- Coolant : Fluids with boiling points of few Kelvin.

Coolant	Boiling Point (K)
Helium 3	3.19
Helium 4	4.214
Nitrogen	77.09

CRYOGENIC CHARACTERISATION

- Device characteristics change as the temperature is ramped down from room temperature to cryogenic temperatures.
- Threshold voltage of the devices (FETs) increases and tends to saturate.
  - consolidated effect of bandgap widening, dopant freezeout, uniform and Gaussian interface traps near the band edge.
- SS (mv/decade) decreases and saturates after a certain temperature.
  - interface trap charges and surface roughness introduce exponential band tail in the conduction band.
- Change in mobility:
  - lattice vibrations with decrease in temperature →decreases the overall phonon scattering.
  - temperature reduction further below a critical temperature result in increased surface roughness and coulombic scattering.

CRYOGENIC CHARACTERISATION

❑Cryogenic charaterisation facality CRF, IIT Delhi.

- Lakeshore CRX-VF
- He 4 based CCR
- 300K – 10K

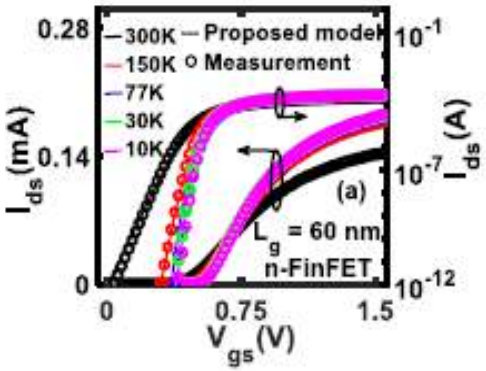


Fig: ID-VG Over Temperature Characterization and modeling

Device Reliability Characterization

- Techniques for evaluating and quantifying system and device reliability are known as reliability characterization techniques.
- These methods assist scientists and engineers in comprehending how various stress circumstances affect a device's behavior, locating probable failure causes, and estimating the device's projected lifetime or performance over time.
- Accelerated Lifetime Testing

- **To understand device life and reliability, devices are subjected to accelerated stress conditions such as higher temperature, voltage, or mechanical loads.**
- **Engineers can determine a device's estimated lifespan under typical working conditions by analyzing how devices break under accelerated conditions.**

Outline

1. Introduction to Integrated Circuits (IC)
2. Semiconductors for IC Fabrication
3. Device Characterization
4. Next Generation computers
5. Microelectronic Devices- PN Junction, MOSFET

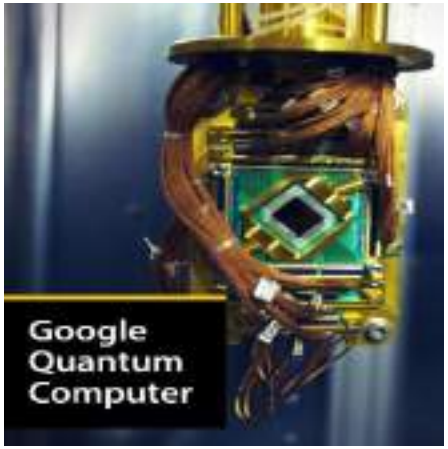
Computing beyond Von Neumann

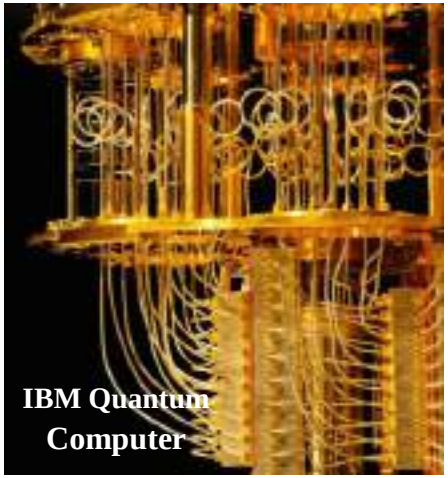
1. Optical Computing
2. Molecular Computing
3. DNA Computing
4. Quantum Computing

Quantum Computers

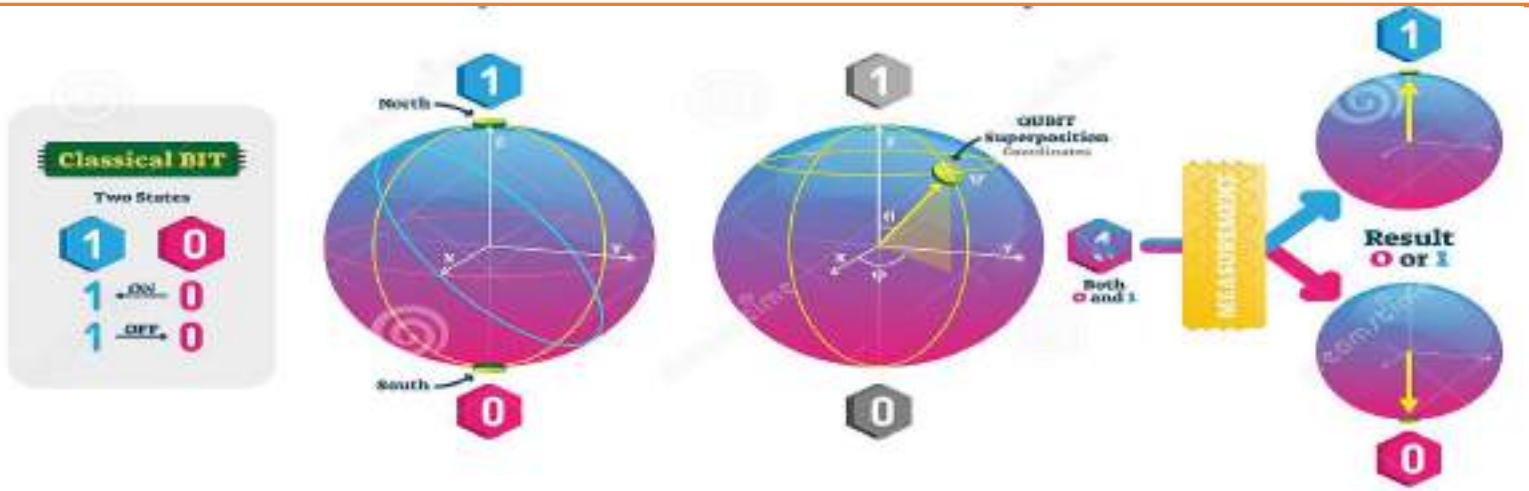
Quantum computers

- Quantum Computer has the capability of solving very complex problems with exponentially large computation power. Quantum computers are not versatile devices like conventional personal computers but excellent for certain tasks.
- Quantum computers rely on Quantum bits (Qubits) as opposed to bits for classical computers.
- They utilize two important properties of quantum mechanics: Quantum Superposition and Quantum Entanglement.
- Solid state realizations, typically silicon qubits have attracted the R&D industry the most because of its compatibility with CMOS foundries.





Quantum Bits: implementation



- Qubits also store binary value of 1 or 0 as classical bits; however, they are implemented in the form of two state quantum entity. They can be manifested as the electronic state of an atom or ion, horizontally or vertically polarized photon, as a spin-up or spin-down electron.
- Qubits typically stay in place and the control signals for their manipulation are brought to the qubits.

https://www.dreamstime.com/qubits-vector-illustration-infographic-superposition-entanglement-states-comparison-classical-one-polarization-bit-image126322079.

Quantum Bits: Properties

❑Quantum Superposition:

- A Qubit always exists in a continuous state between 0 and 1 until it is measured. When measured, superposition state of the qubit is destroyed, and it settles with the outcome of either 0 or 1.
- Qubit representation:

$$|\psi> = \alpha|0> + \beta|1>$$

Where |0> and |1> are the two basis vectors and are written in "Dirac" or "bra-Ket" notation

- For better understanding about quantum information and computing, Bloch sphere is used.

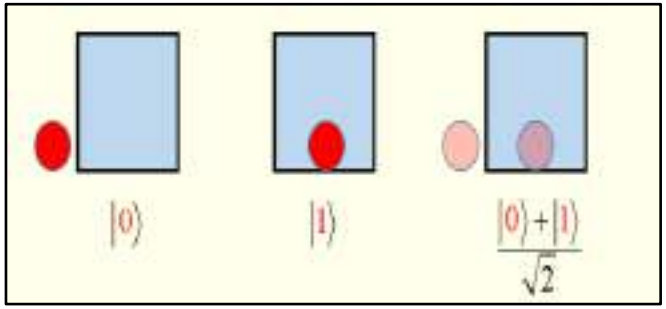


Fig: Quantum Superposition

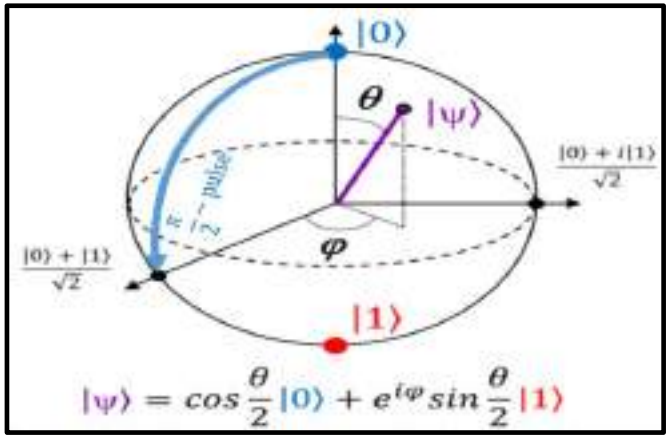


Fig: Bloch Sphere

https://www.microcontrollertips.com/what-are-the-basics-of-quantum-computing-faq/.

Quantum Bits: Properties

❑Quantum Entanglement:

- Another important property of qubits.
- Quantum mechanical phenomena represented by qubits that describes the correlation between them such that the quantum state of each particle of the pair depends on state of the other, even when particles are physically separated.
- Example: if there is a pair of entangled particles such as electrons such that their total spin is zero, and one electron has spin-up; then other particle (electron) will have spin-down on measurement

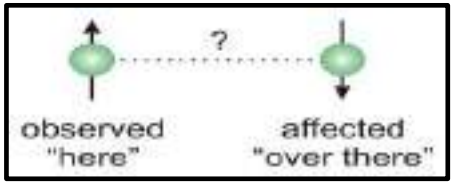
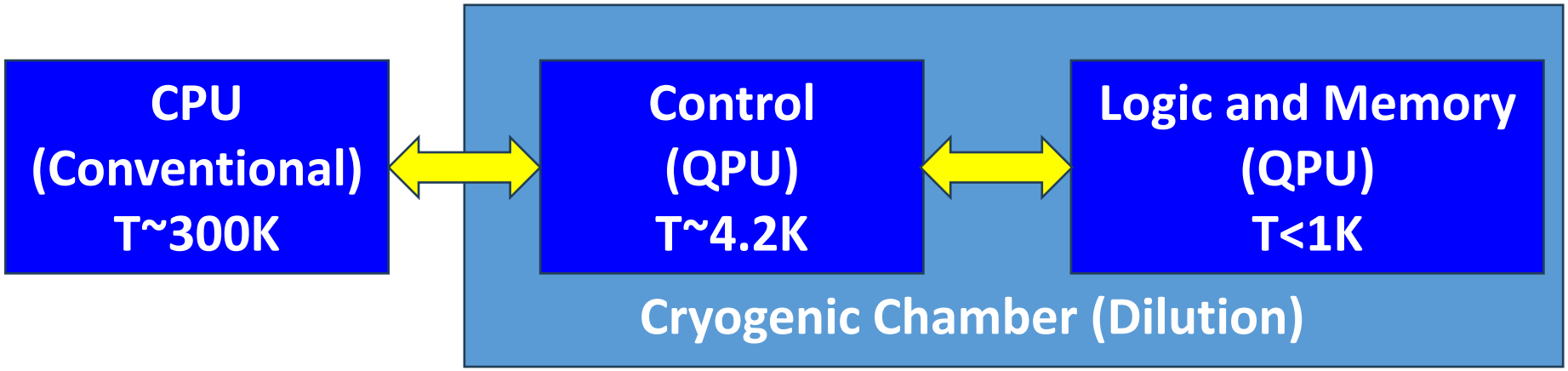


Fig: Quantum Entanglement

https://www.nasa.gov/audience/forstudents/postsecondary/features/23jan_entangled_prt.htm

A Quantum Computer Architecture



- Other designs possible
- Variations in QPU architecture based on qubits as per their operating temperatures and coherence (t1, t2)
- Control and Logic/Memory are two separate chips, each with own thermal and bandwidth considerations
- Accordingly, two separate boards/packages required to hold control and logic/memory chips, different sizes, thermal, and bandwidth considerations

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Integrated Devices- Active and Passive

❑ Active Devices

- ✓Diodes, BJT, FETs, etc.
  - Always fabricated using the front-end-of-the-line (FEOL) process

❑ Passive Devices: Capacitors, Resistors, Inductors, e-fuse, etc. are fabricated using both FEOL and BEOL processes

Component Type	Range of Values	Absolute Accuracy	Relative Accuracy	Temperature Coefficient	Voltage Coefficient
MOSFET gate Cap.	6-7 fF/μm^2	10%	0.1%	20ppm/°C	±20ppm/V
Poly-Poly Capacitor	0.3-0.4 fF/μm^2	20%	0.1%	25ppm/°C	±50ppm/V
Metal-Metal Capacitor	0.1-1fF/μm^2	10%	0.6%	??	??
Diffused Resistor	10-100 Ω/sq.	35%	2%	1500ppm/°C	200ppm/V
Ion Implanted Resistor	0.5-2 kΩ/sq.	15%	2%	400ppm/°C	800ppm/V
Poly Resistor	30-200 Ω/sq.	30%	2%	1500ppm/°C	100ppm/V
n-well Resistor	1-10 kΩ/sq.	40%	5%	8000ppm/°C	10kppm/V
Top Metal Resistor	30 mΩ/sq.	15%	2%	4000ppm/°C	??
Lower Metal Resistor	70 mΩ/sq.	28%	3%	4000ppm/°C	??

PN Junction Diode

- Standalone P type or N type semiconductors have limited use. However, the junction of these two types of semiconductors forms a PN junction diode and provides interesting properties for wide range of applications such as:

- Rectifier
- Amplifier
- Switching, etc.

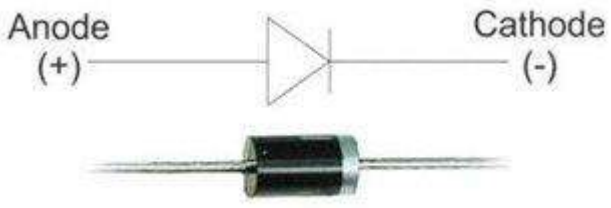


Fig : Symbolic representation of a PN junction diode and its physical image [1]

[1] https://www.atlearner.com/2019/07/pn-junction-diode.html

What is a PN junction

- A PN junction can be defined as a metallurgical junction between p-type and n-type semiconductor
- Just after the junction formation, majority carriers diffuse across the junction.
- The diffusion leaves behind immobile charge carriers (Donor and acceptor ions) generating space charged region / depletion region

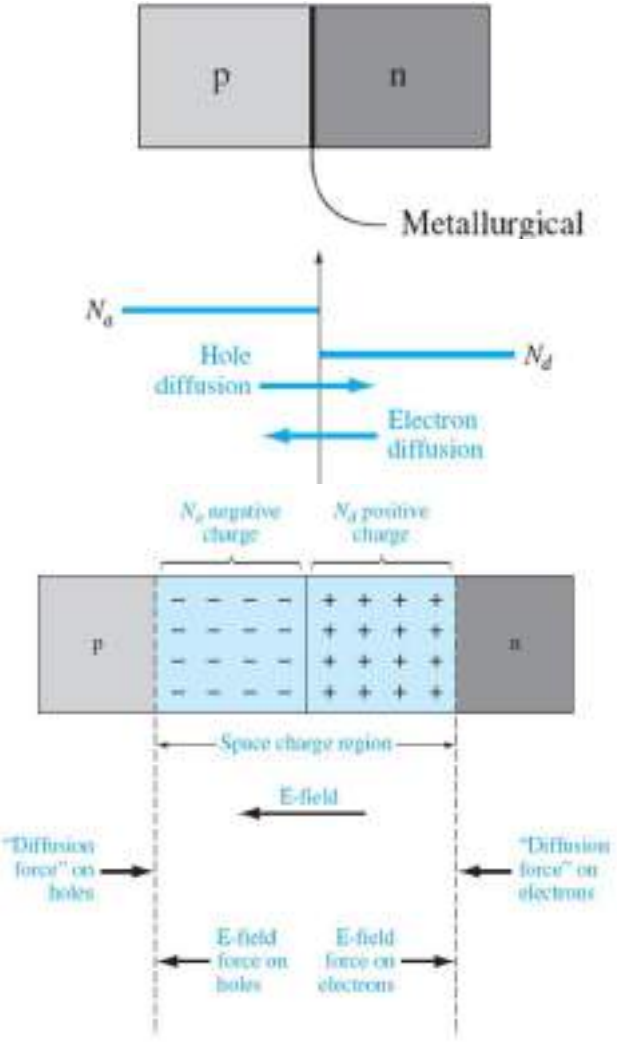
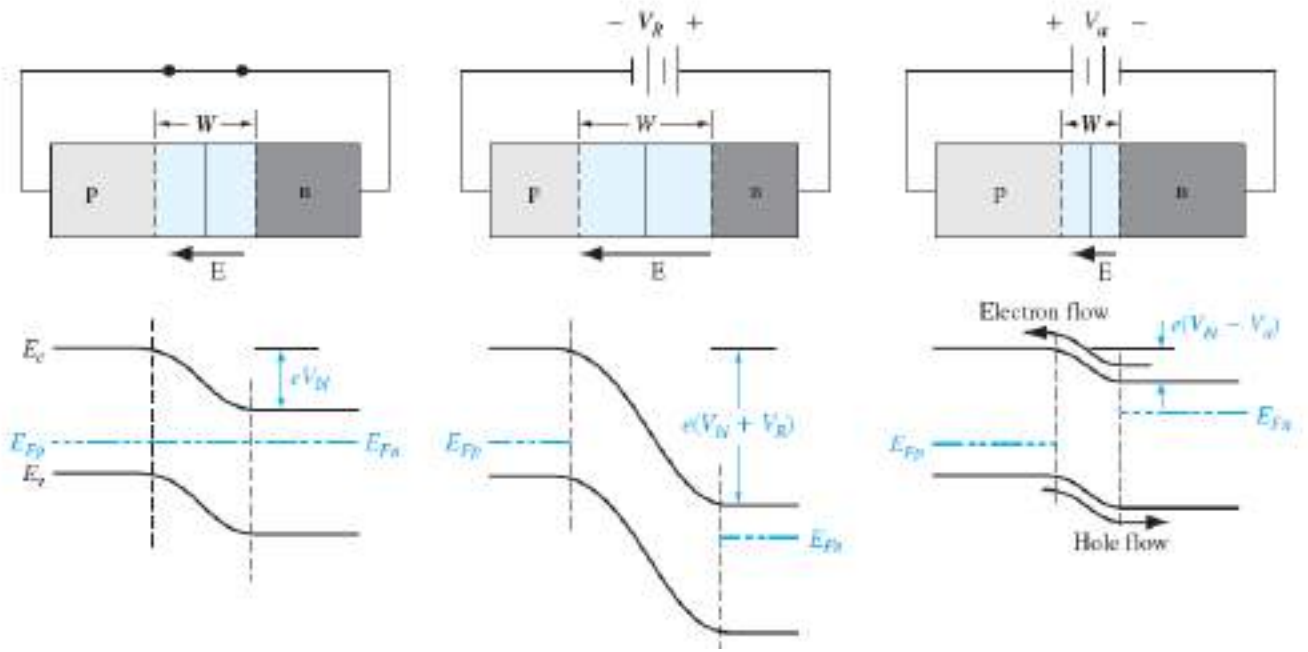


Fig: Operational description of a PN junction [1]

[1] *Sedra, A., Smith, K.C., Carusone, T.C. and Gaudet, V., 2020. Microelectronic circuits 8th edition. Chapter, 14, pp.1235-1236.*

PN junction biasing

- The three-biasing condition for the PN junction and their corresponding energy band diagram are shown below:



Unbiased Reverse biased Forward biased

Fig : PN junction under different biasing conditions

IV characteristics of a PN junction diode

- In the unbiased condition (Zero bias), there is no effective flow of current in any direction and thus the current is zero
- In Reverse bias condition, the barrier height is increased which further restricts the flow of majority carriers
- However, the increased electric field allows more minority carriers to pass through the barrier and thus contribute to some current, J_s (Reverse saturation current)
- The current is dependent on the flow of minority carriers and thus is small in magnitude and approximately independent of reverse bias

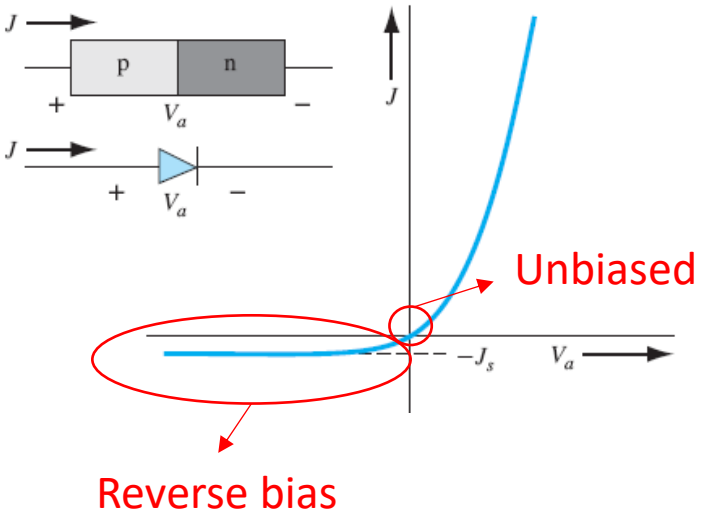


Fig : IV characteristics of a PN junction diode

IV characteristics of a PN junction diode

- In Forward bias condition, the barrier height is reduced which allows the majority carriers to diffuse through the barrier and contribute to the current
- As this current is dependent on the flow of majority carriers, it is exponentially dependent on the applied external bias, V_a as shown below:

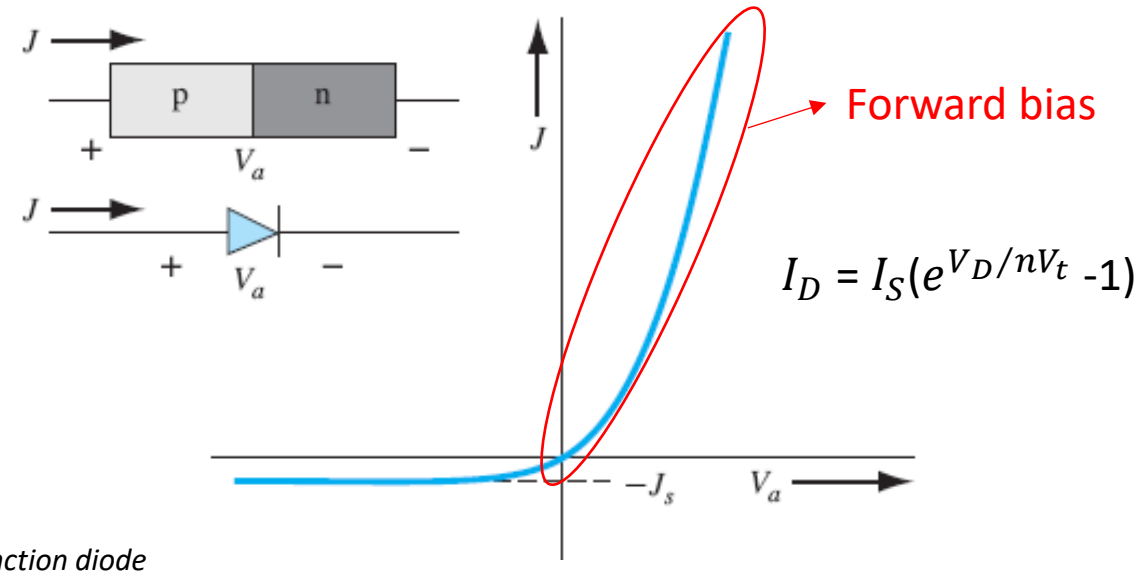


Fig : IV characteristics of a PN junction diode

Junction Breakdown

- Under extremely high Reverse bias, the PN junction may breakdown which results in a heavy flow of current in the direction of the reverse bias
- Two popular mechanisms for breakdown are:

(a) Zener breakdown (b) Avalanche breakdown

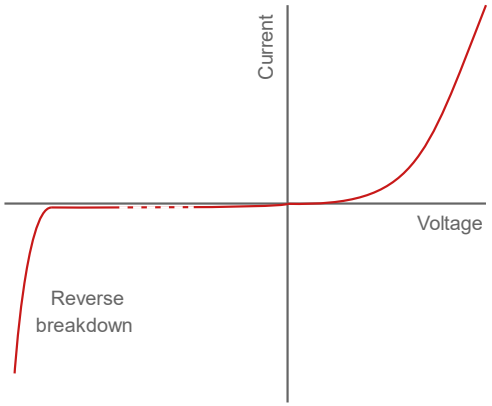


Fig : IV characteristics of a PN junction diode demonstrating reverse breakdown

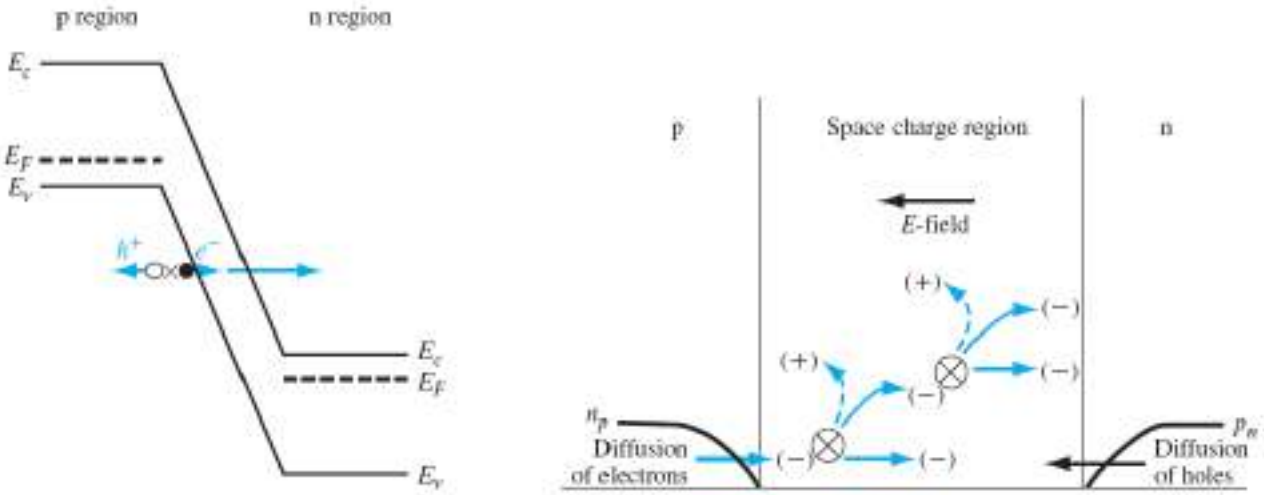


Fig : Two prominent breakdown mechanisms in diode

Junction capacitance

- The depletion region acts like a dielectric placed in between the two plates of a parallel plate capacitor
- The junction/depletion layer capacitance of a PN junction is given as:

$$C' = \left\{ \frac{q \in_s N_a N_d}{2(V_{bi} + V_R)(N_a + N_d)} \right\}^{1/2}$$

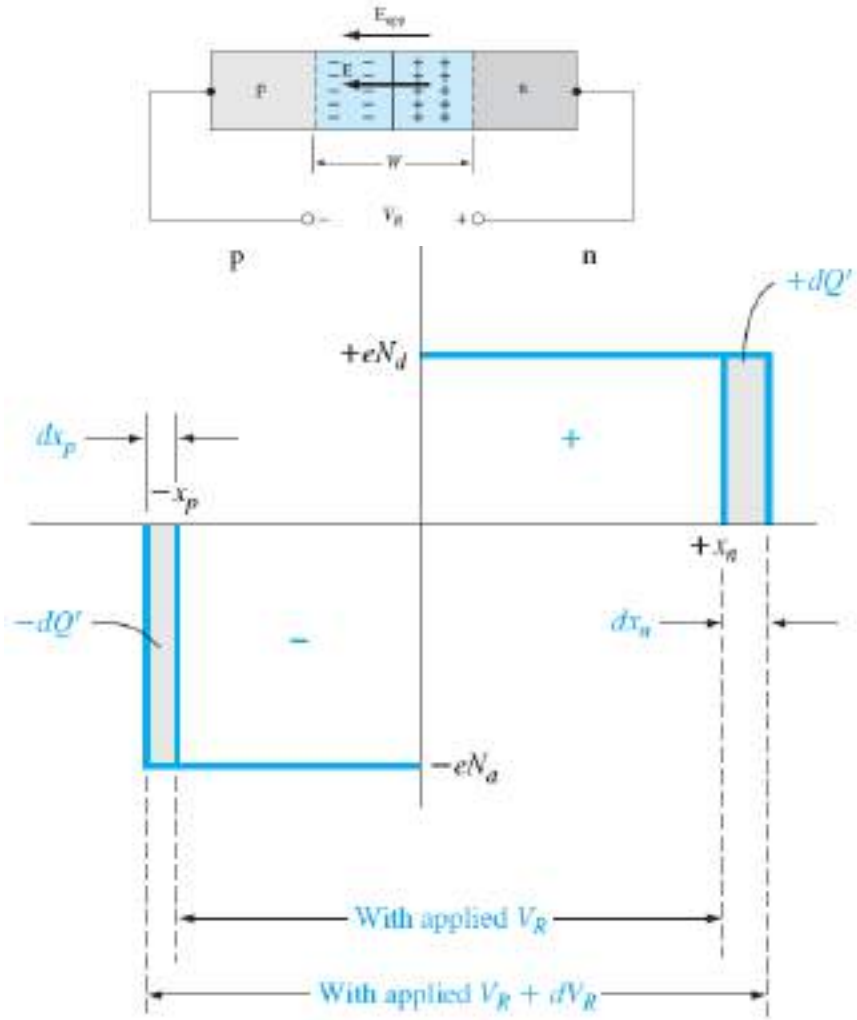


Fig : Space charge across PN junction

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Transistors

- The transistor is a three-terminal semiconductor device in general with the capability to control current at one terminal with the help of applied voltage at another terminal.
- Possible to have current gain, voltage gain when used with other circuit components.
- Two major types:
  - Bipolar Junction Transistor (BJT).
  - Metal-oxide-semiconductor field-effect transistor (MOSFET).

Most widely used electronic devices

Bipolar Junction Transistor(BJT): Introduction

- The Bipolar Junction Transistor (BJT) is a three-terminal device, that features two p-n junctions and three independently doped regions.
- BJT is an active device that in conjunction with other circuit elements, is capable of current gain, voltage gain, and signal power gain.
- BJTs are current controlled devices.
- Three regions that form terminal connections are:
  - Emitter: highly doped region
  - Base: narrow-width region
  - Collector: lightly doped

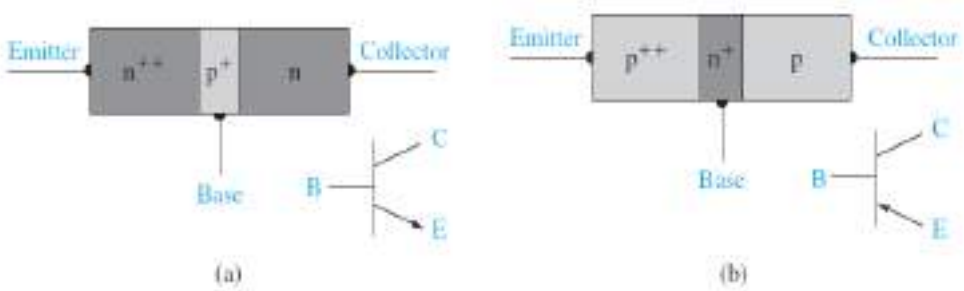


Fig: Block diagrams and circuit symbols of bipolar transistors (a) npn and (b) pnp [1]

[1] Donald A. Neamen, Semiconductor Physics and Devices Basic Principles, Fourth Edition.Chapter 12, pp 491-560

MOSFETs

- BJT is a bipolar, current controlled device and hence consumes more power as compared to voltage controlled devices such as MOSFETs.
- Due to its small sizes, MOSFETs are used extensively in digital circuit applications and IC design.
- Analog circuits and mixed-signal design are some other applications of MOSFETs.

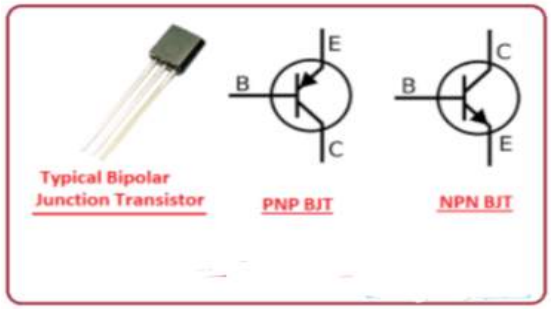


Fig. BJT: NPN, PNP

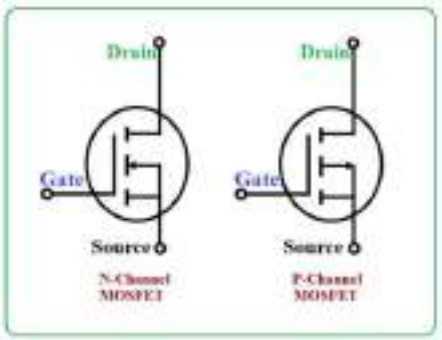
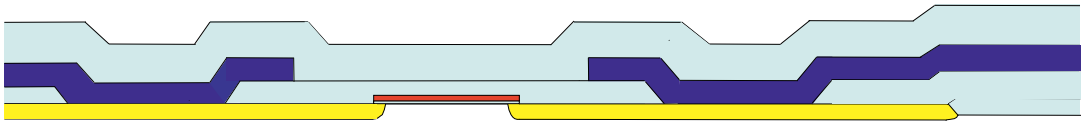


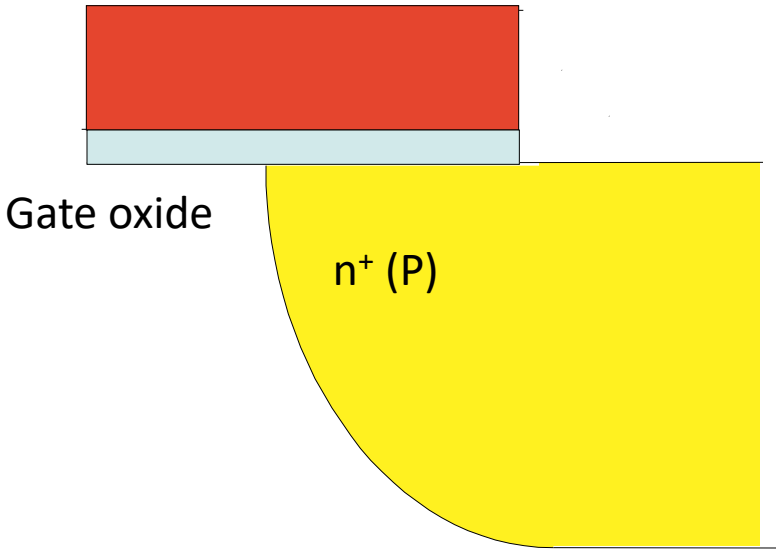
Fig. MOSFET

How it all got started...

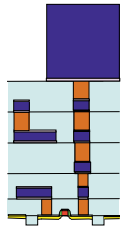
1973 : 6µm nMOS



Magnified



1998 : 0.25µm CMOS



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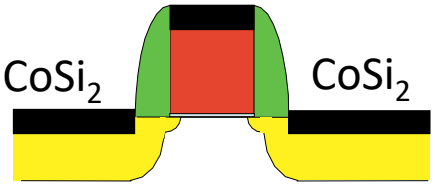

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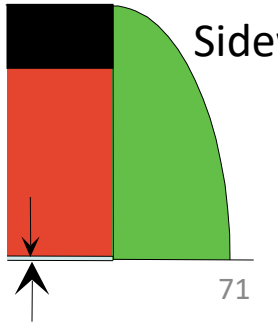
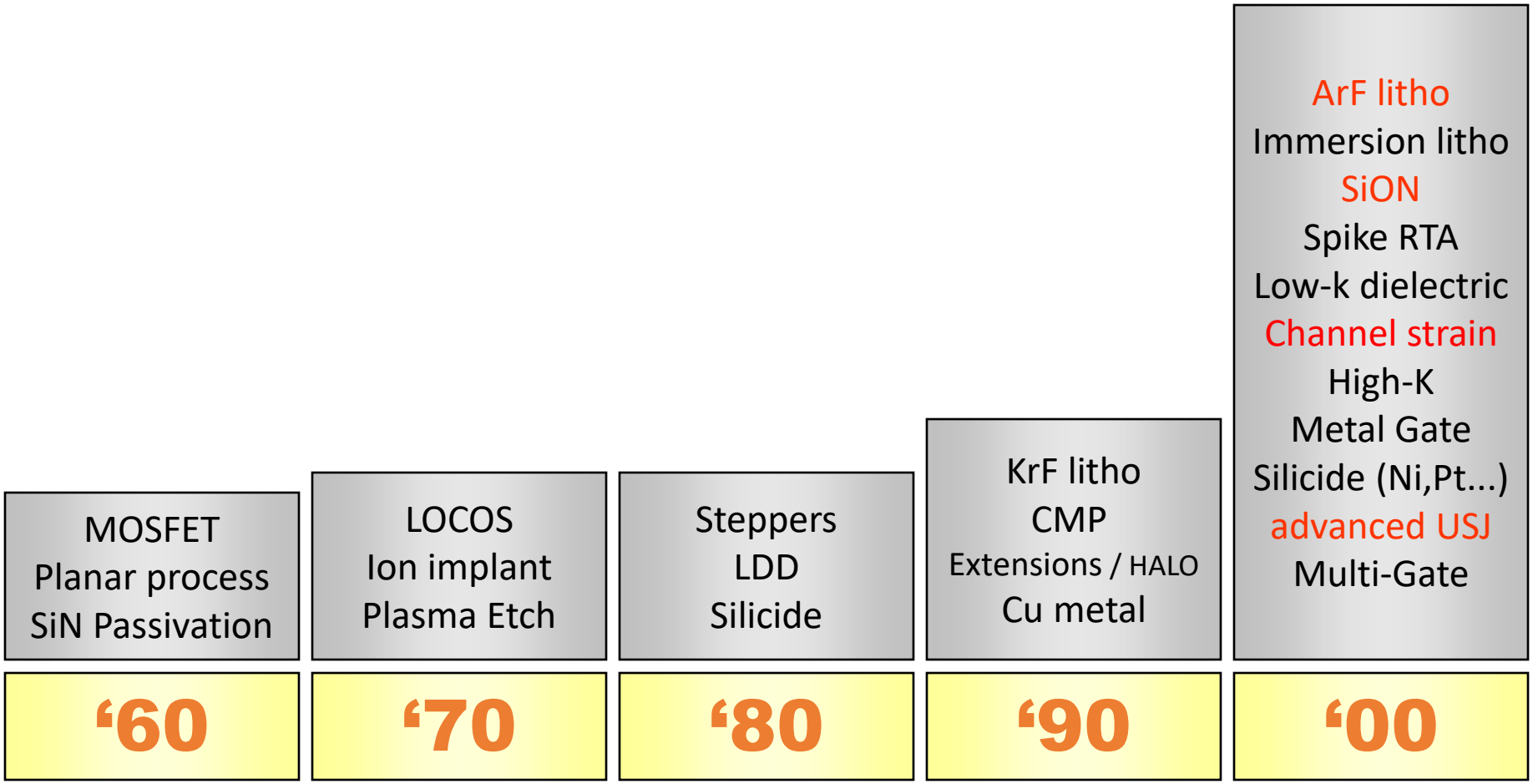


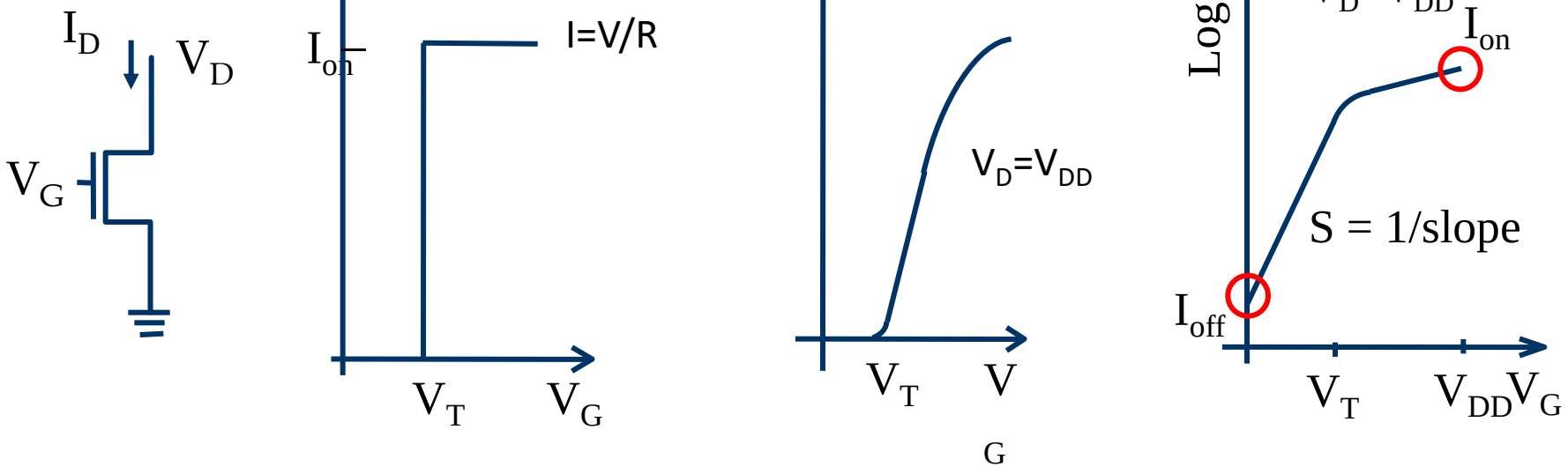
Enabling R&D Breakthroughs



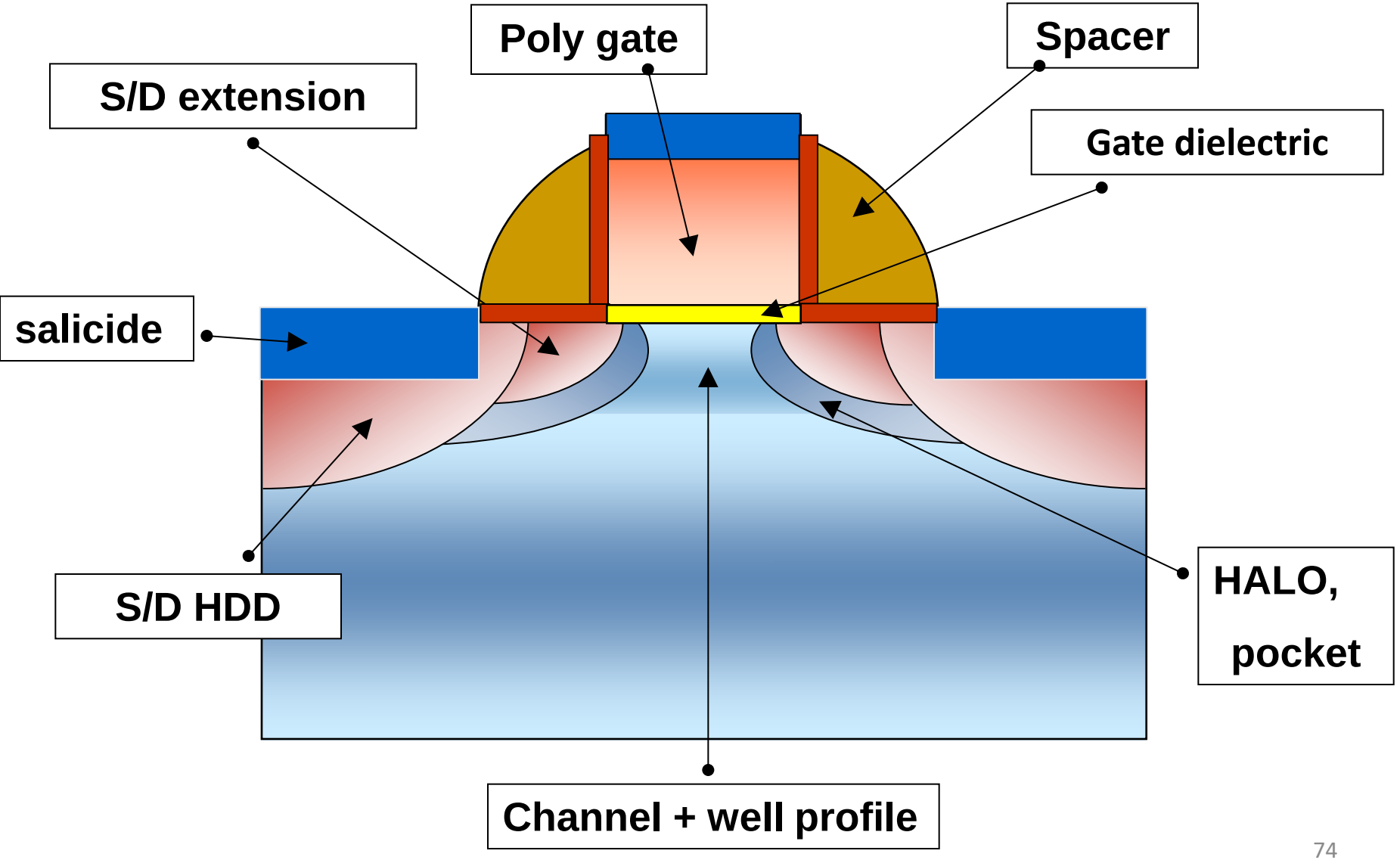
What is a transistor ?

CMOS transistors in digital CMOS circuits

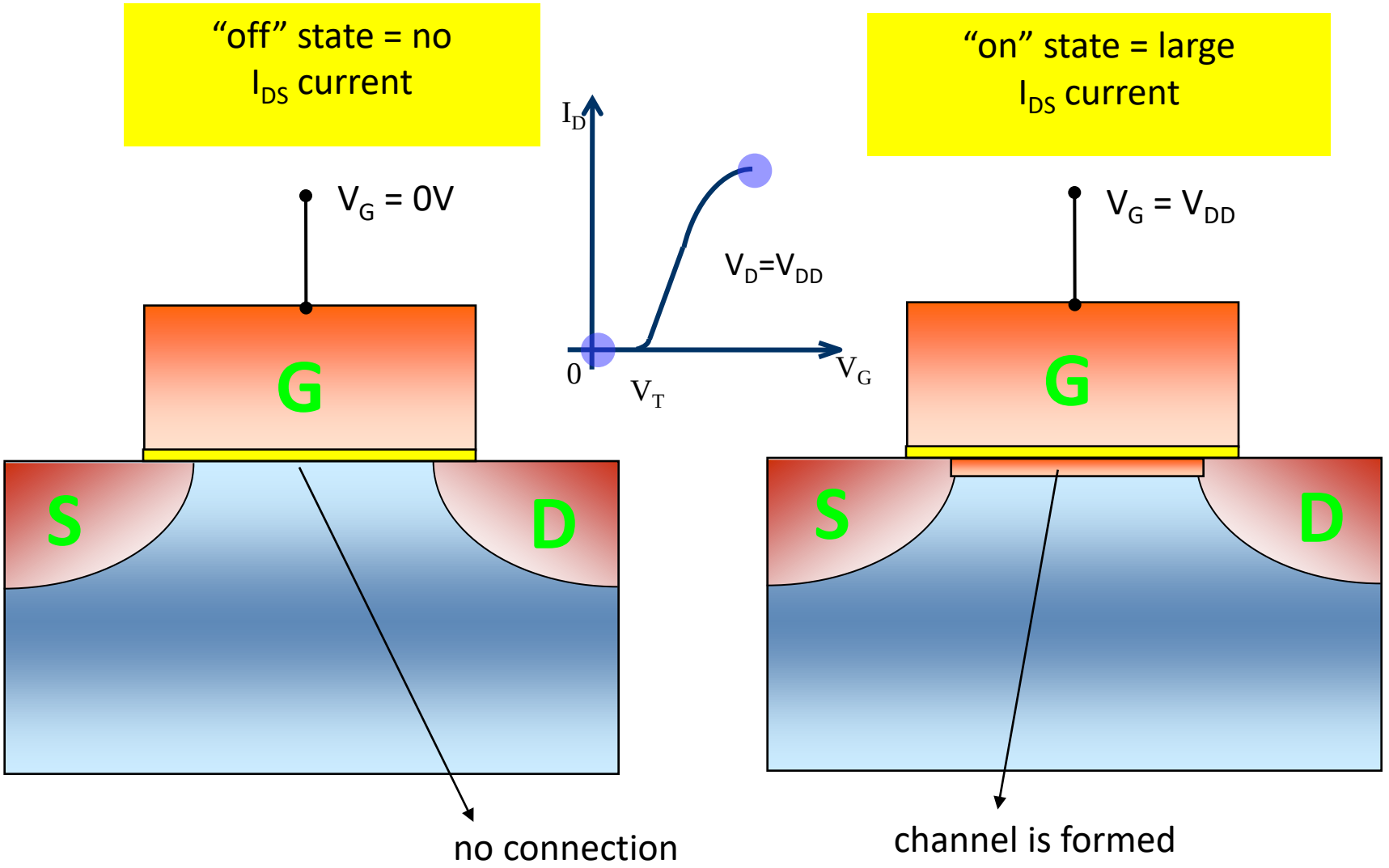
SWITCH



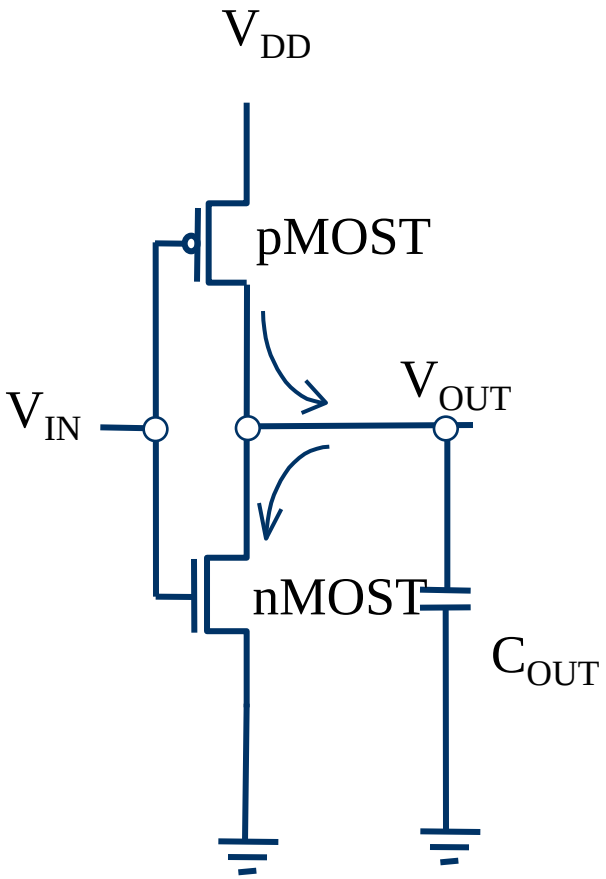
Typical Advanced MOSFET Structure

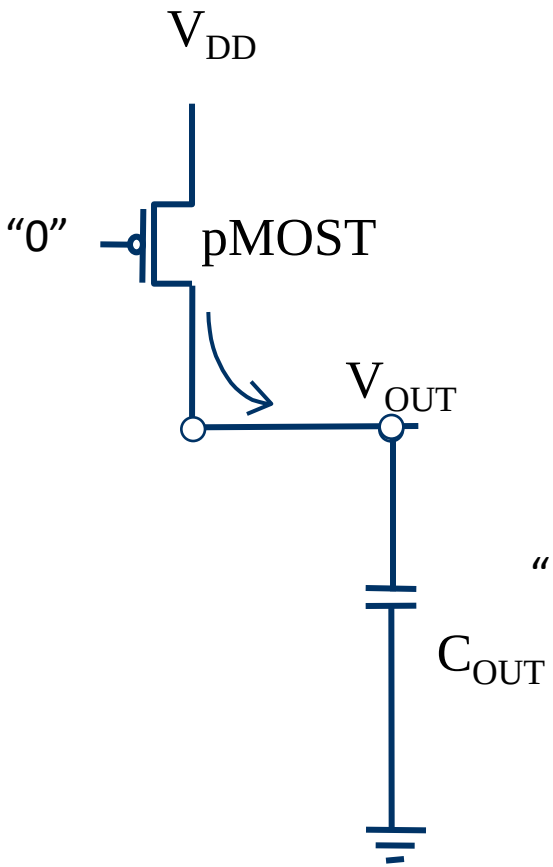


MOSFET ‘digital’ operation

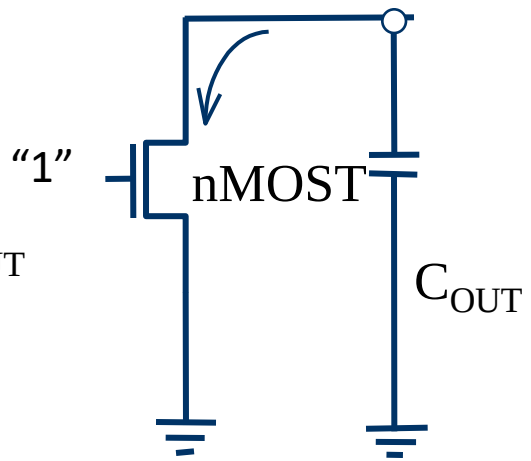


A Digital Circuit



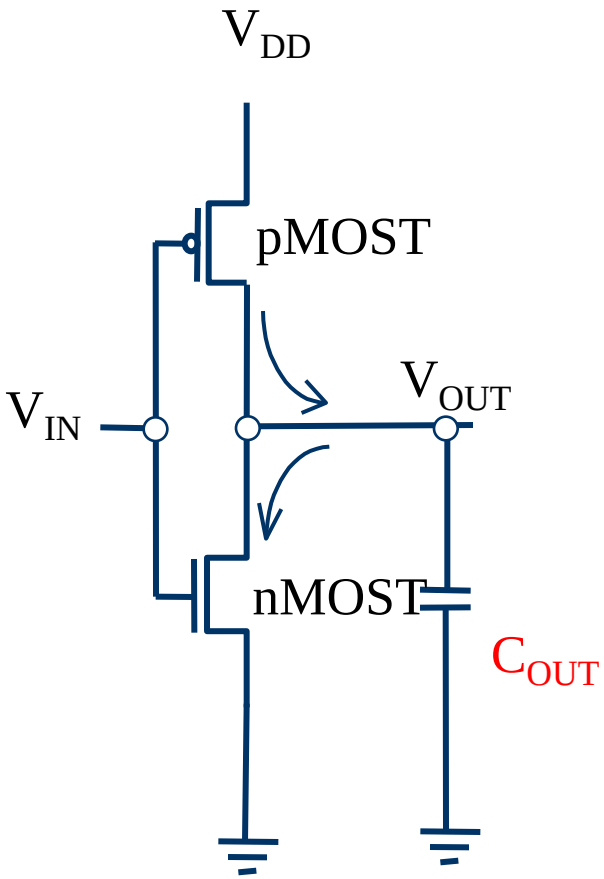


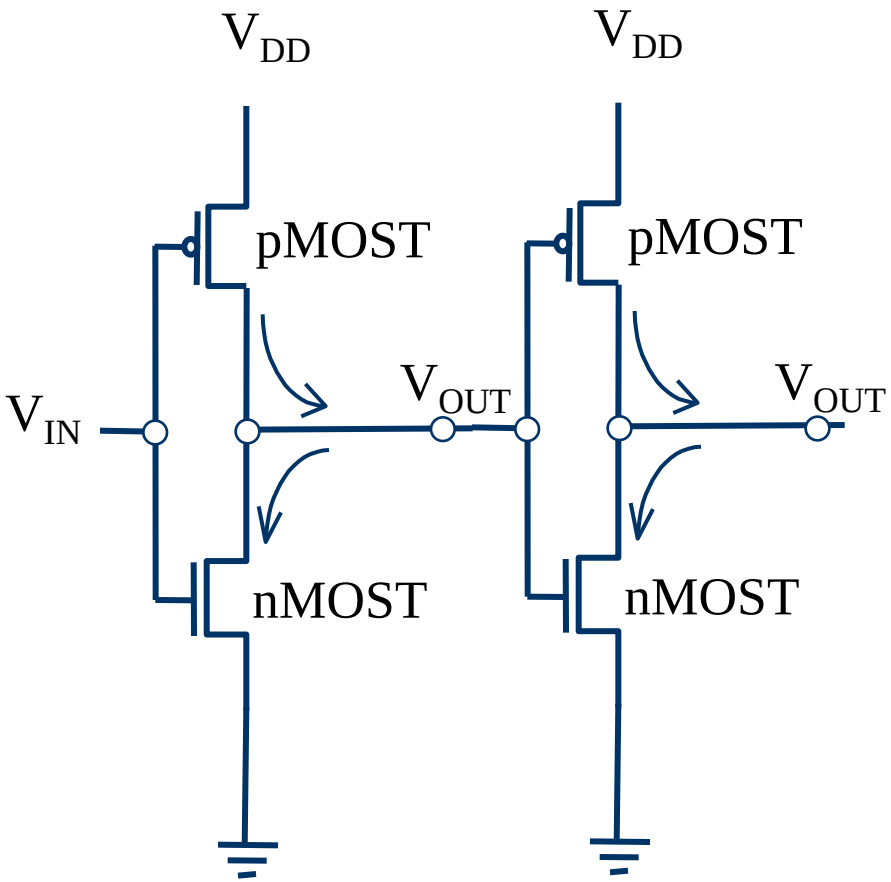
Creates '1'
Q = C * Vdd



Creates '0'
Q=0

A Digital Circuit





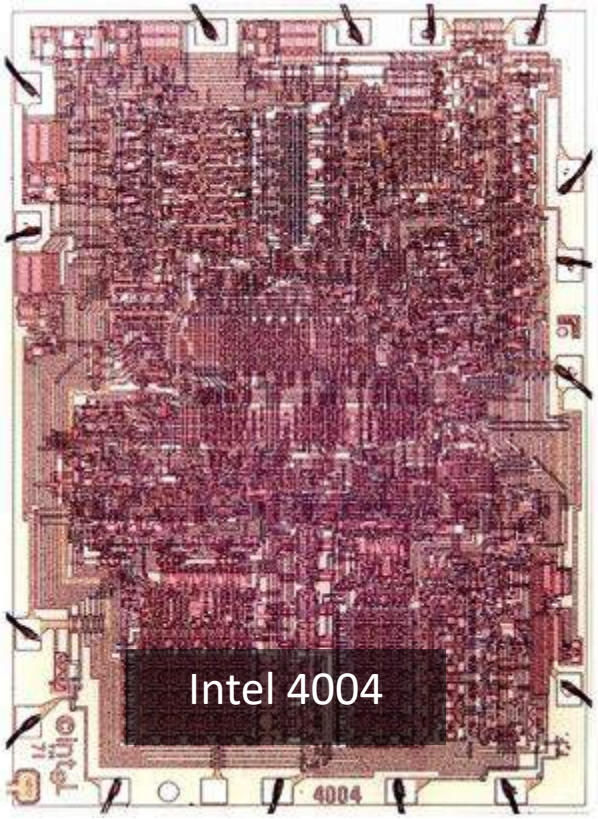
Cout = next MOSFET stage

Technology evolution - scaling

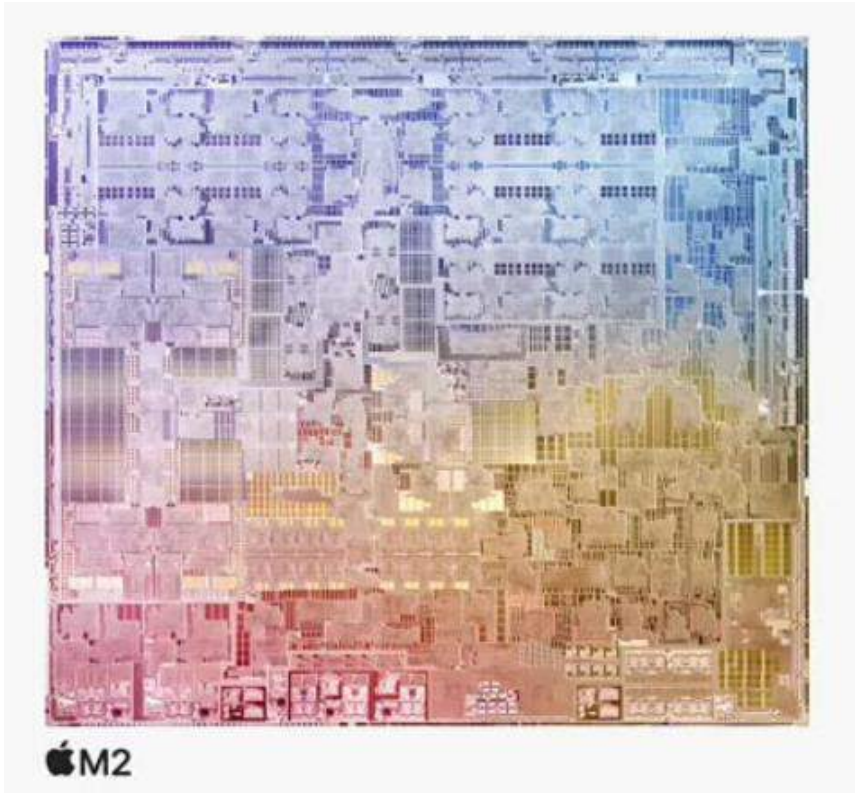
Year	1971	2023
Transistors	2,300	134 B
Speed (kHz)	108	3.5M
CD	10 µm	5 nm

x 58 million
x 32,407
/ 2,000

!!



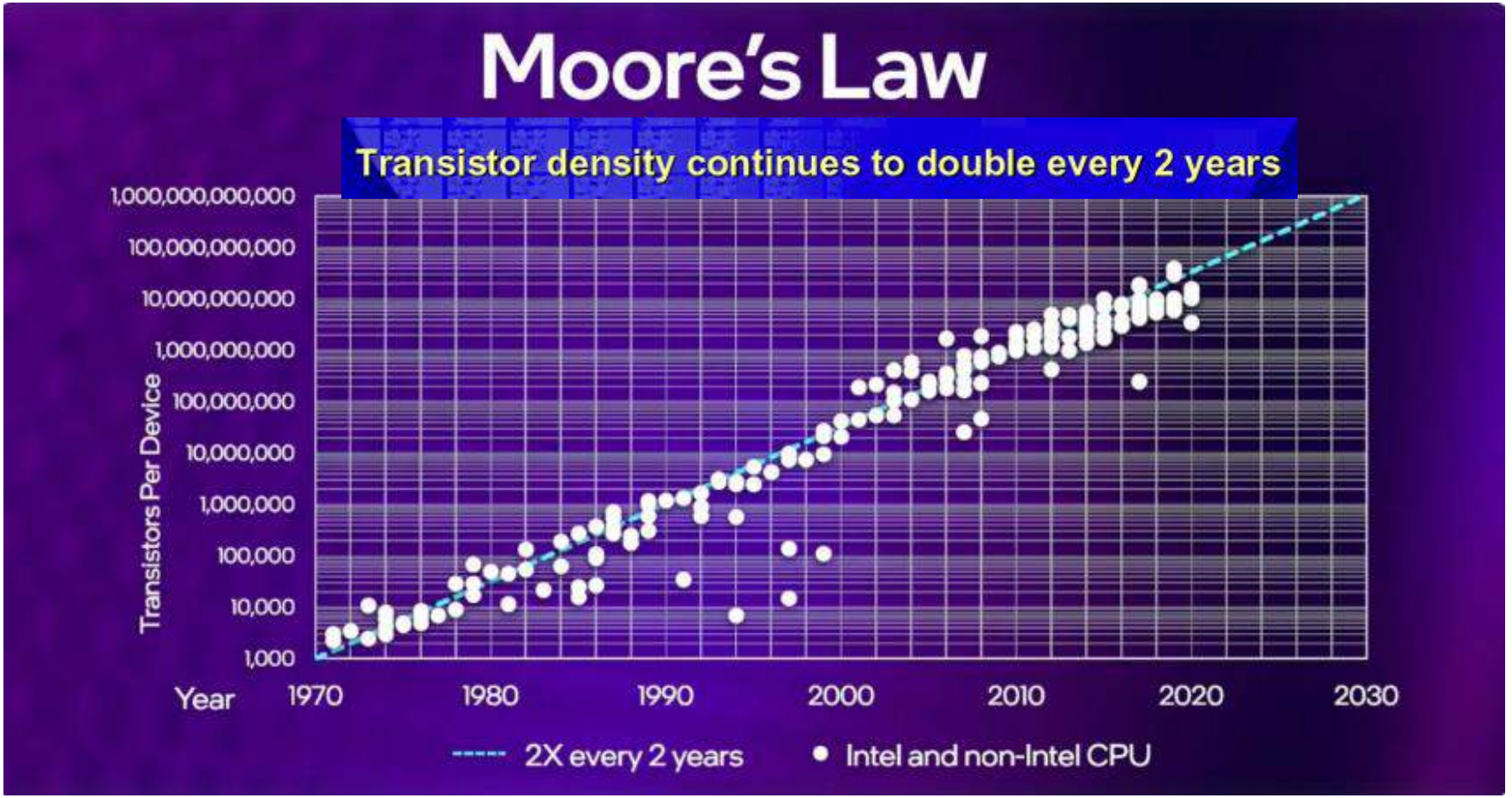
50+ years of scaling



Historical trend – packing density

The Moore's law

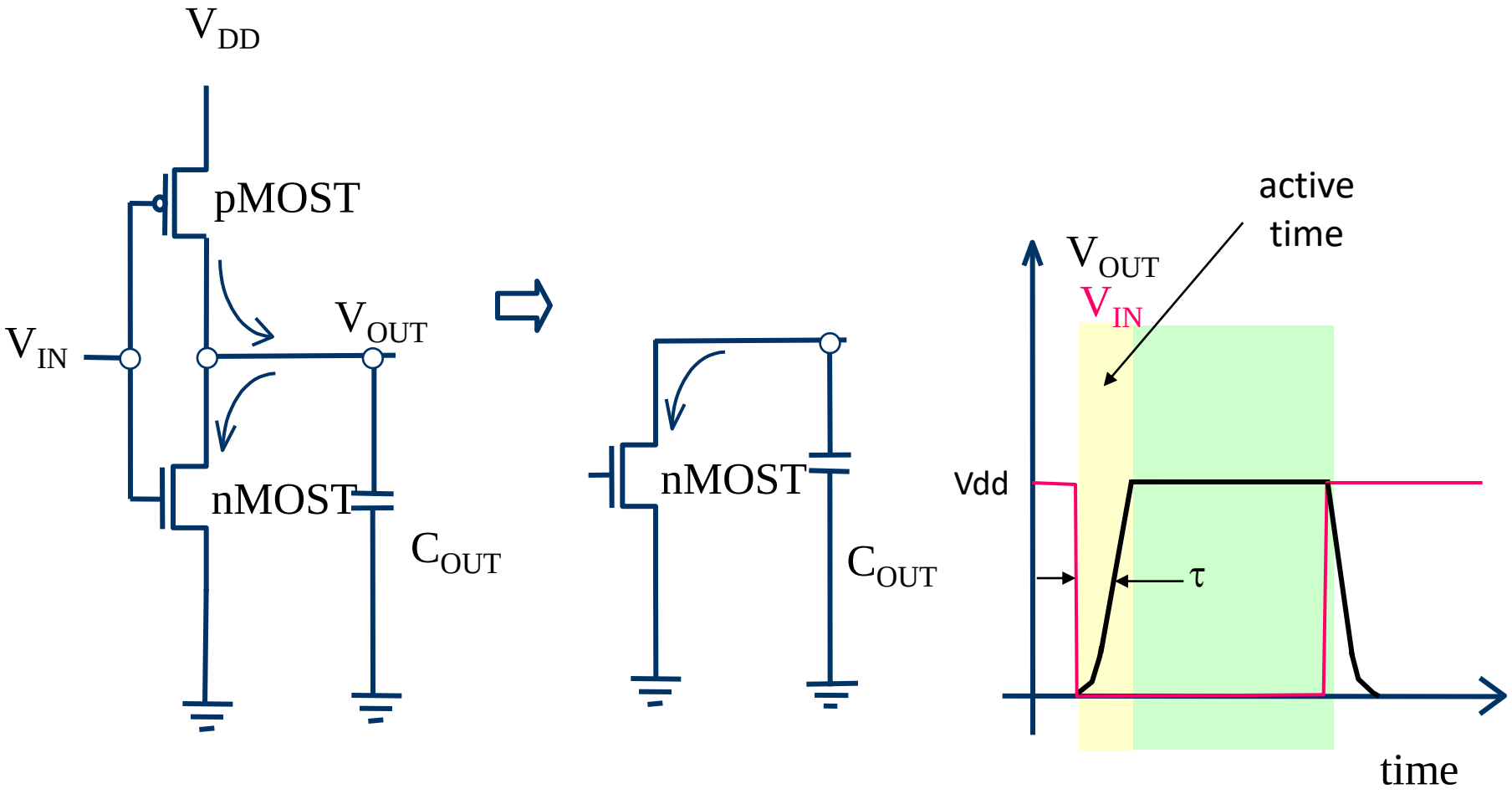
Author: Gordon E. Moore
Publication: Electronics, April 19, 1965



Source : http://www.intel.com/research/silicon/mooreslaw.htm

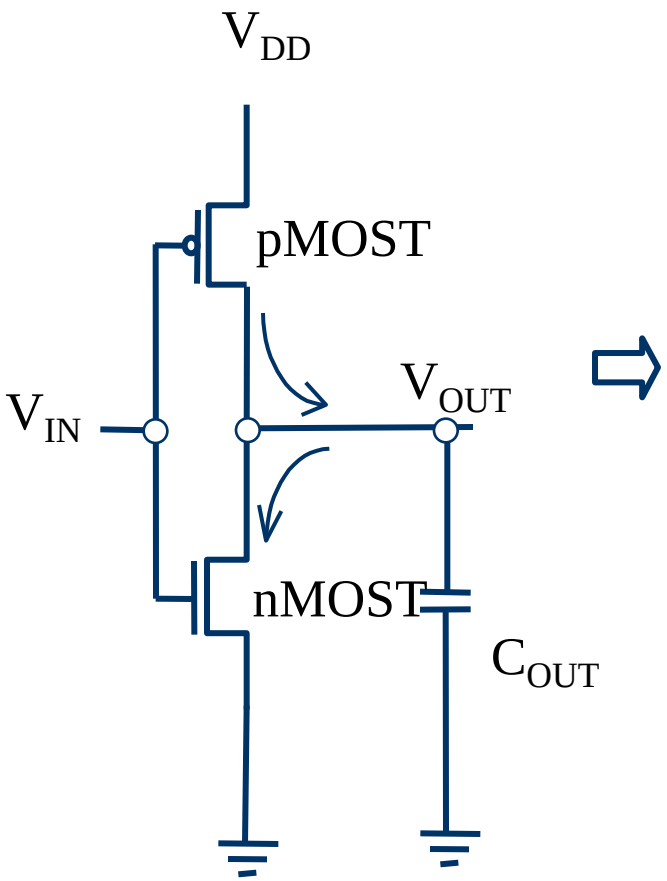
Digital Circuits -Speed

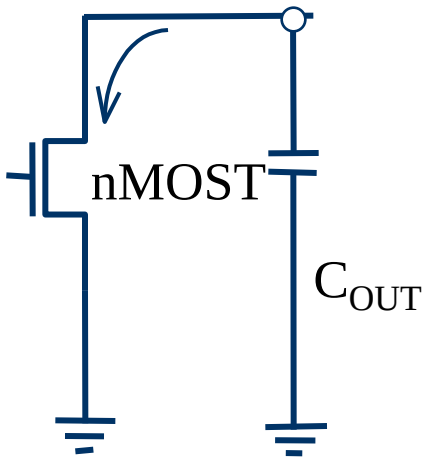
Inverter delay



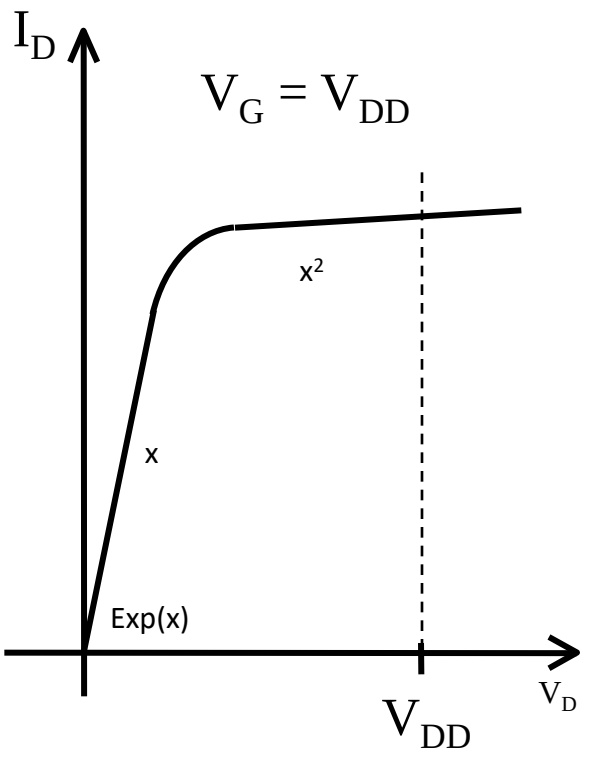
Digital Circuits -Speed

$$dt = \frac{C(V)dV}{I(V)} \Rightarrow \tau = \int_0^{V_{DD}} \frac{C_{OUT}(v)}{I_D(v)} dv; \quad \tau \propto C_{OUT} \frac{V_{DD}}{I_{ON}}$$



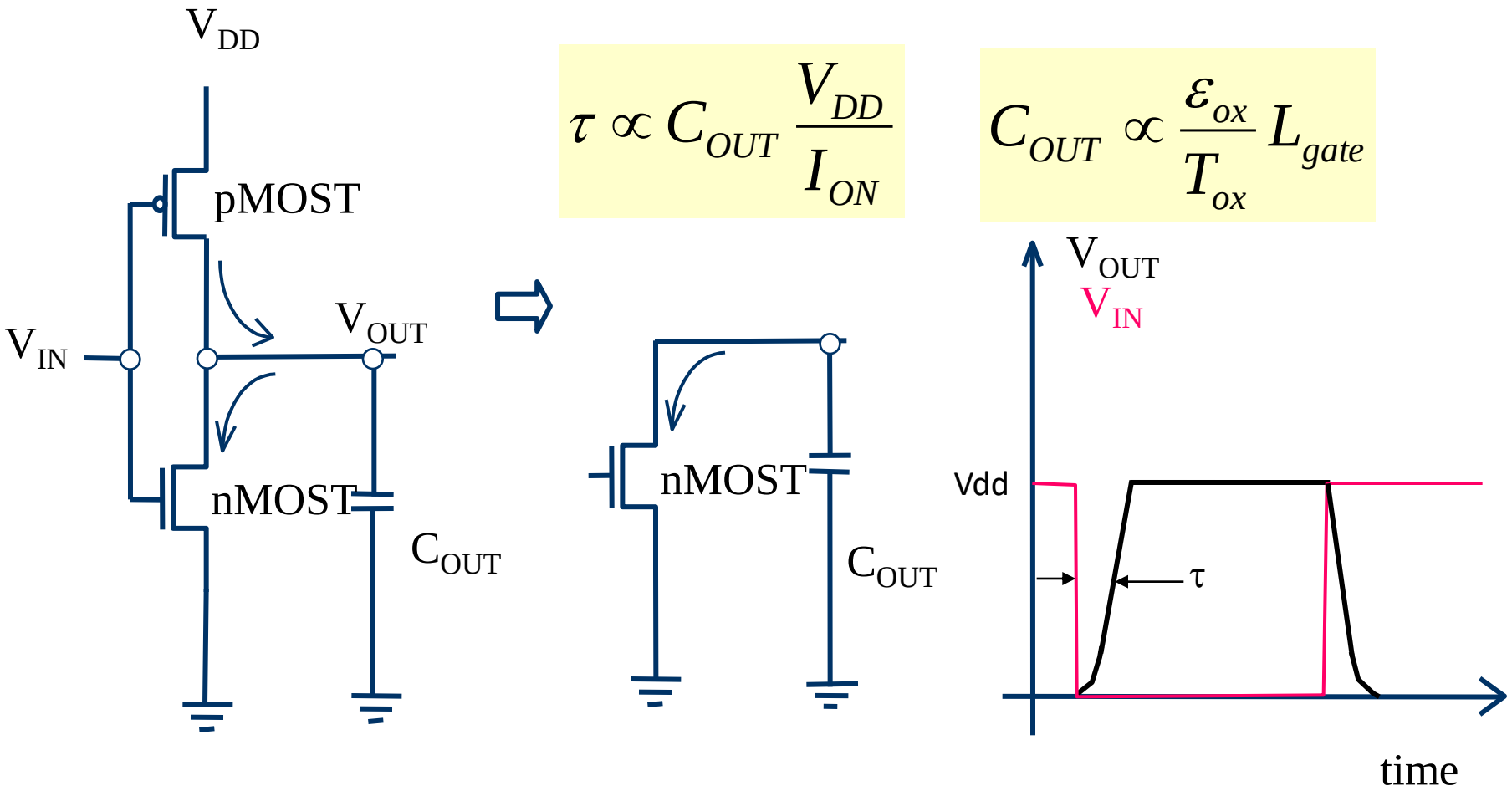


I_D-V_D characteristics



Scaling

Inverter delay

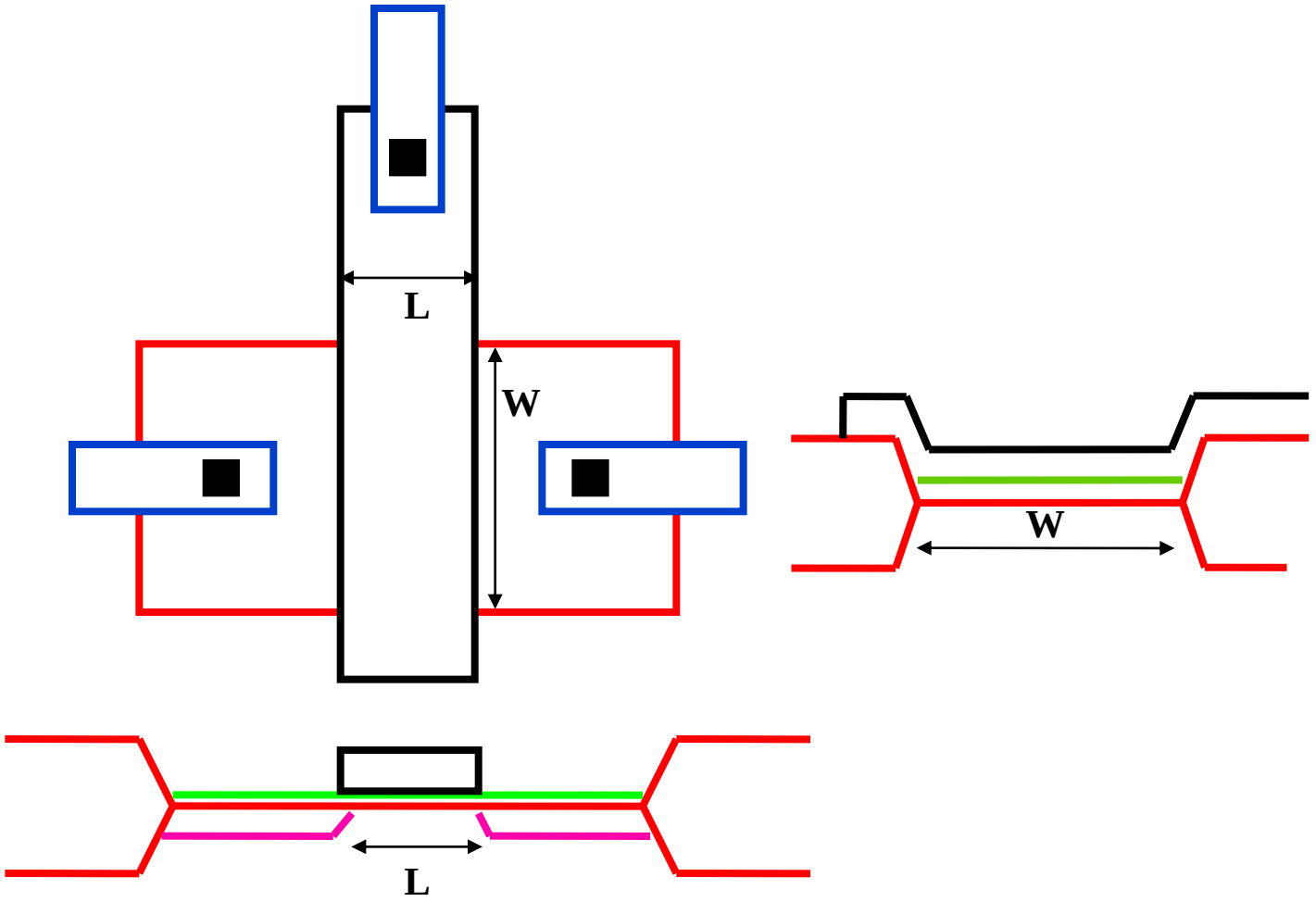


$$\tau \propto C_{OUT} \frac{V_{DD}}{I_{ON}}$$

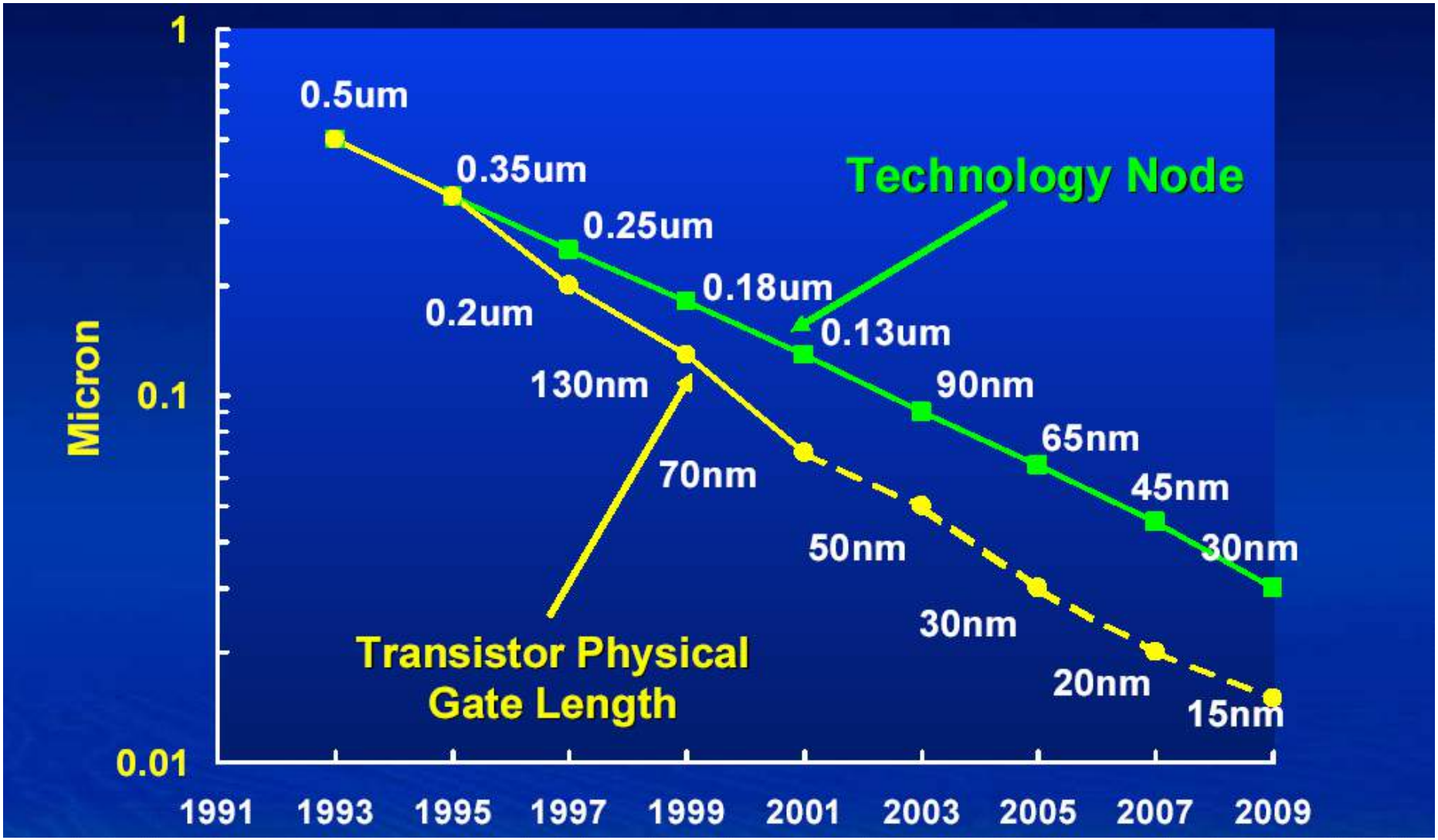
$$C_{OUT} \propto \frac{\varepsilon_{ox}}{T_{ox}} L_{gate}$$

Scaling

reduction of device dimensions in ALL directions

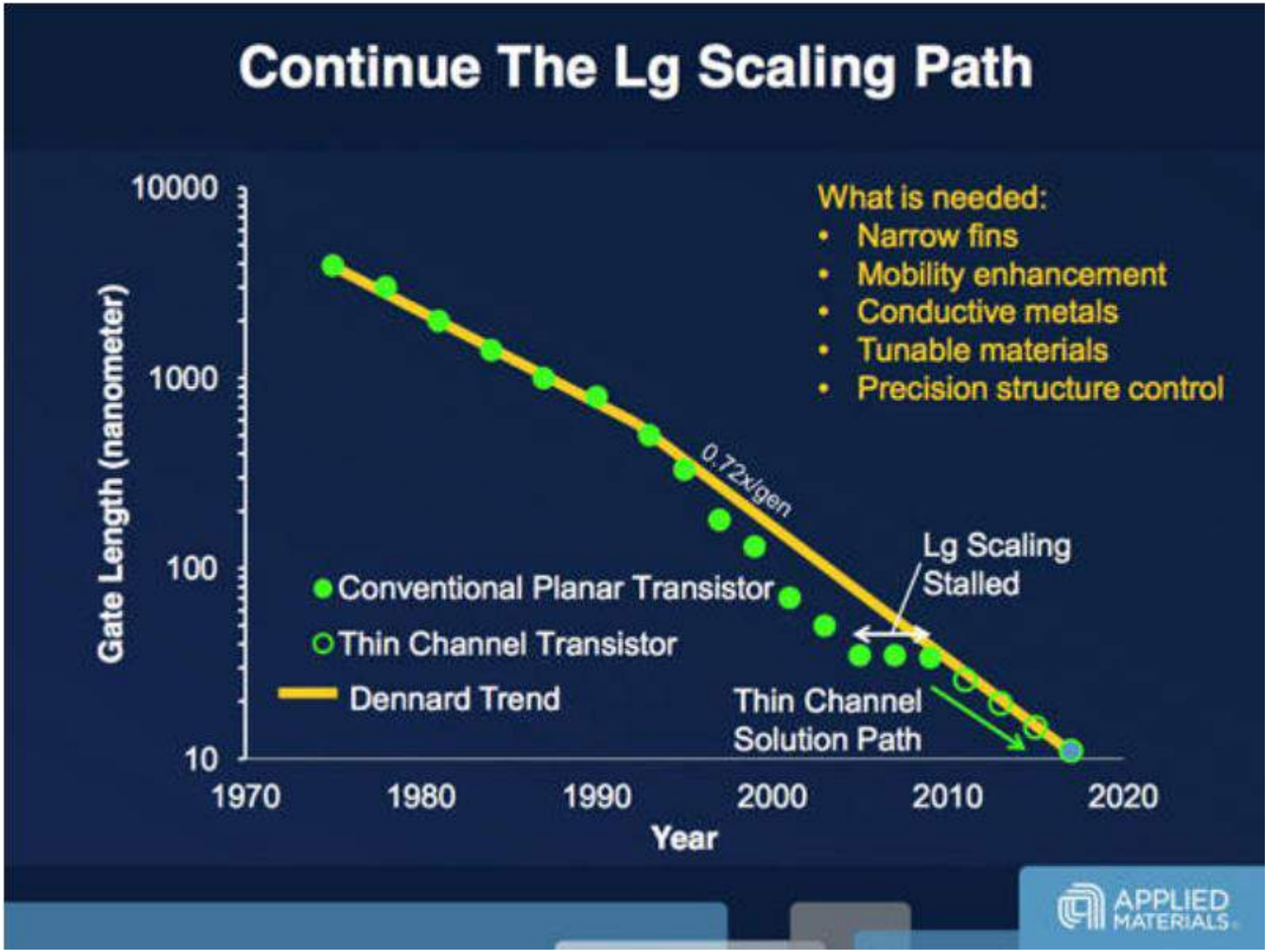


Technology nodes & Lg



Yung, Intel : ESSCIRC'02, presentation

Technology nodes & Lg



Scaling

What is the goal of scaling ?

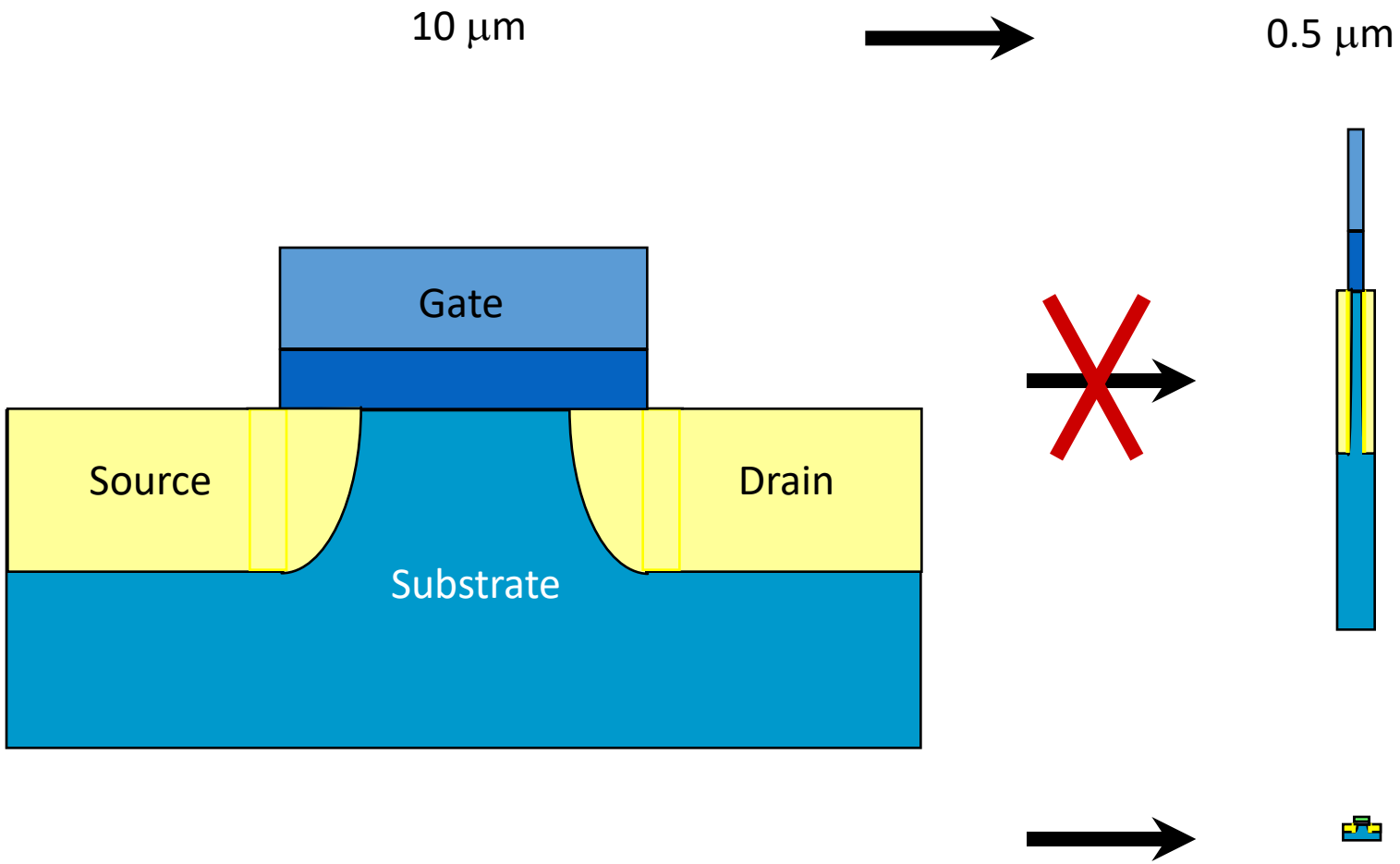
- increase in packing density
- higher speed

GOAL : more performance for reduced cost per function

What are the problems, limitations ?

- physical (HCE, **SCE**, tunneling, poly depletion, B penetration …)
- technological (availability of tools, processes, …)
- economical (cost of new technology development)

Device down scaling



digital CMOS circuits - Inverter

Inverter power dissipation

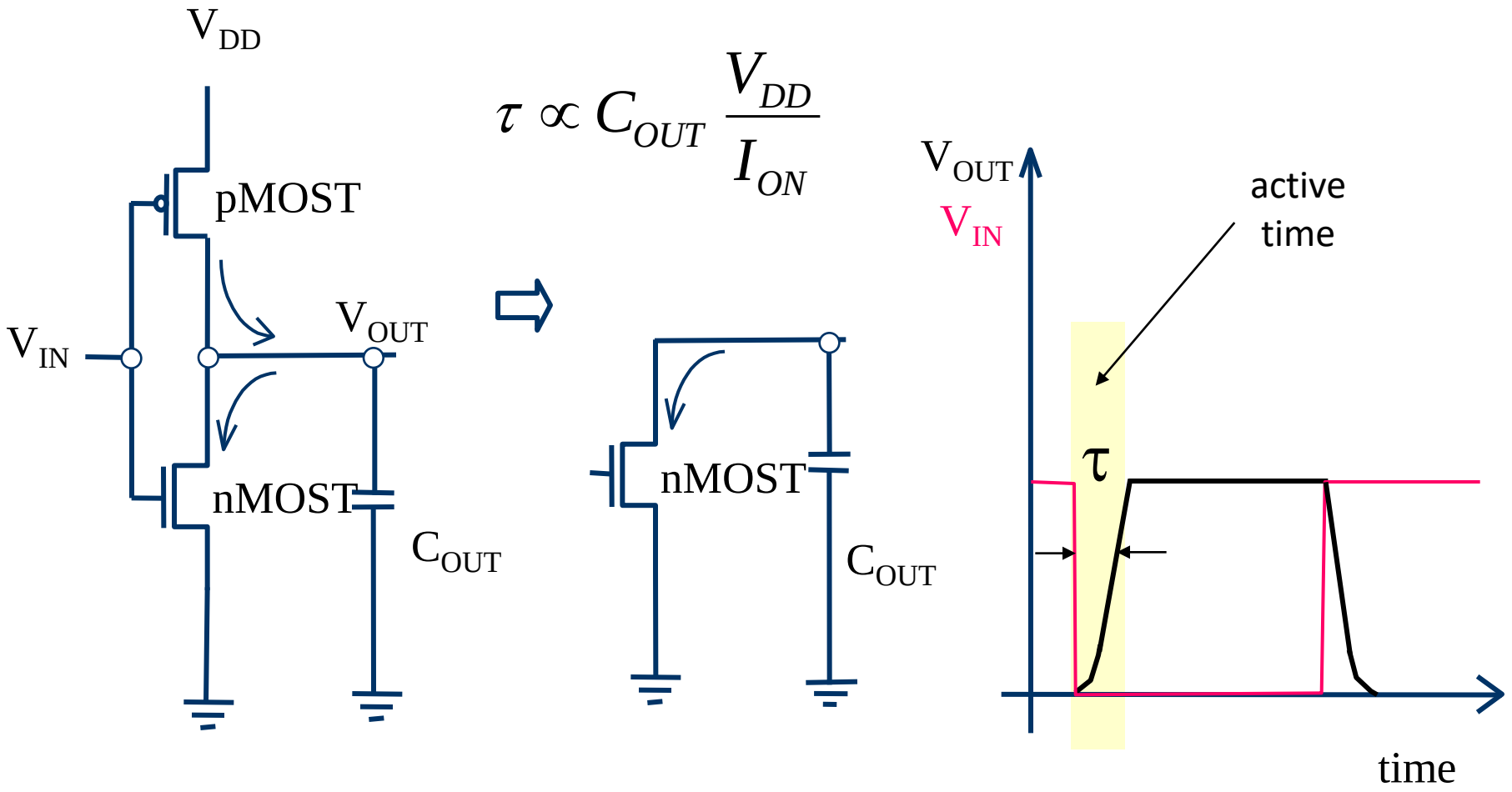
Active power:

$$P_{ac} = C_{OUT} V_{DD}^2 f$$

Discharging a capacitor

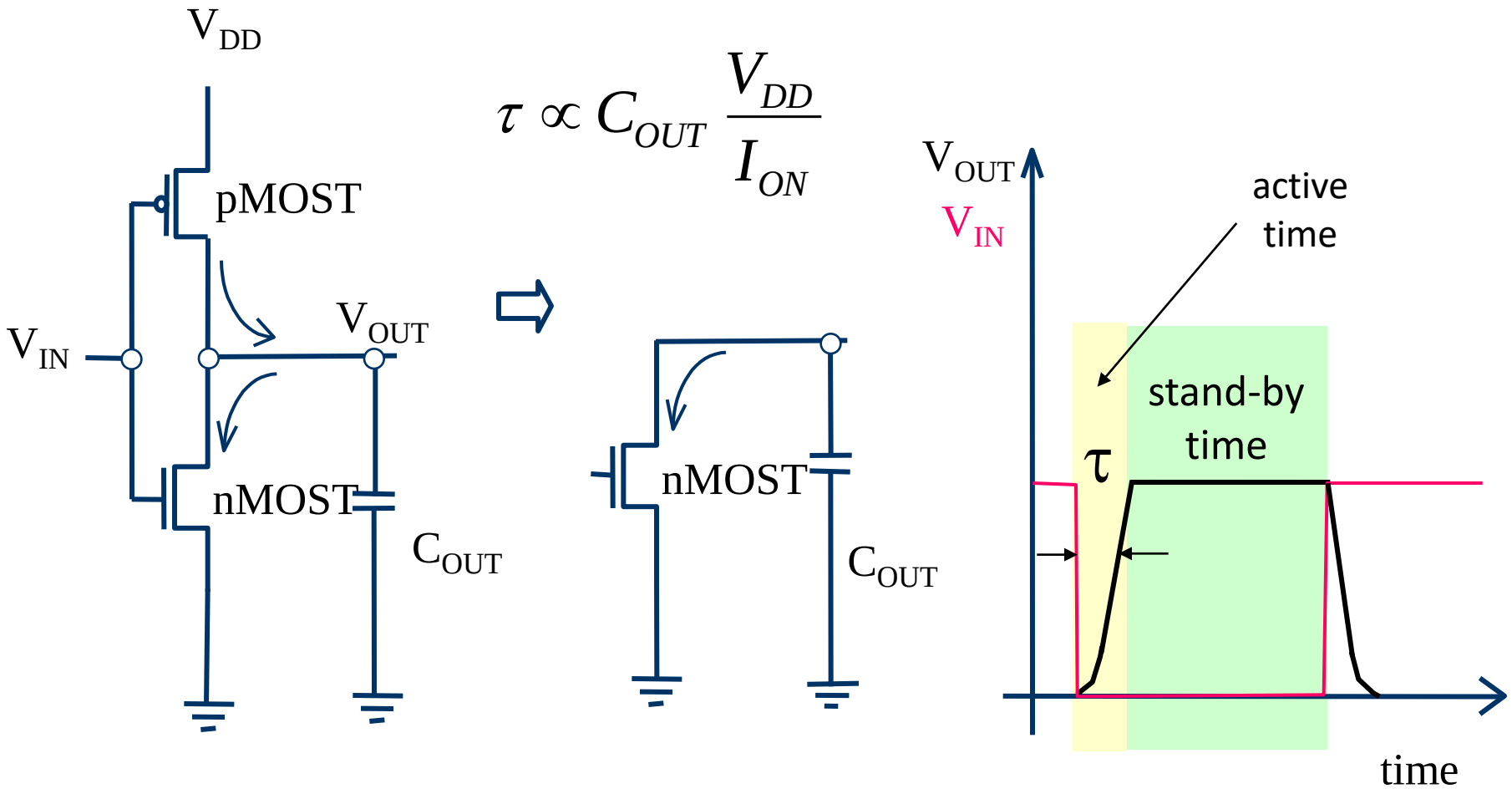
digital CMOS circuits - Inverter

Inverter delay - active



digital CMOS circuits - Inverter

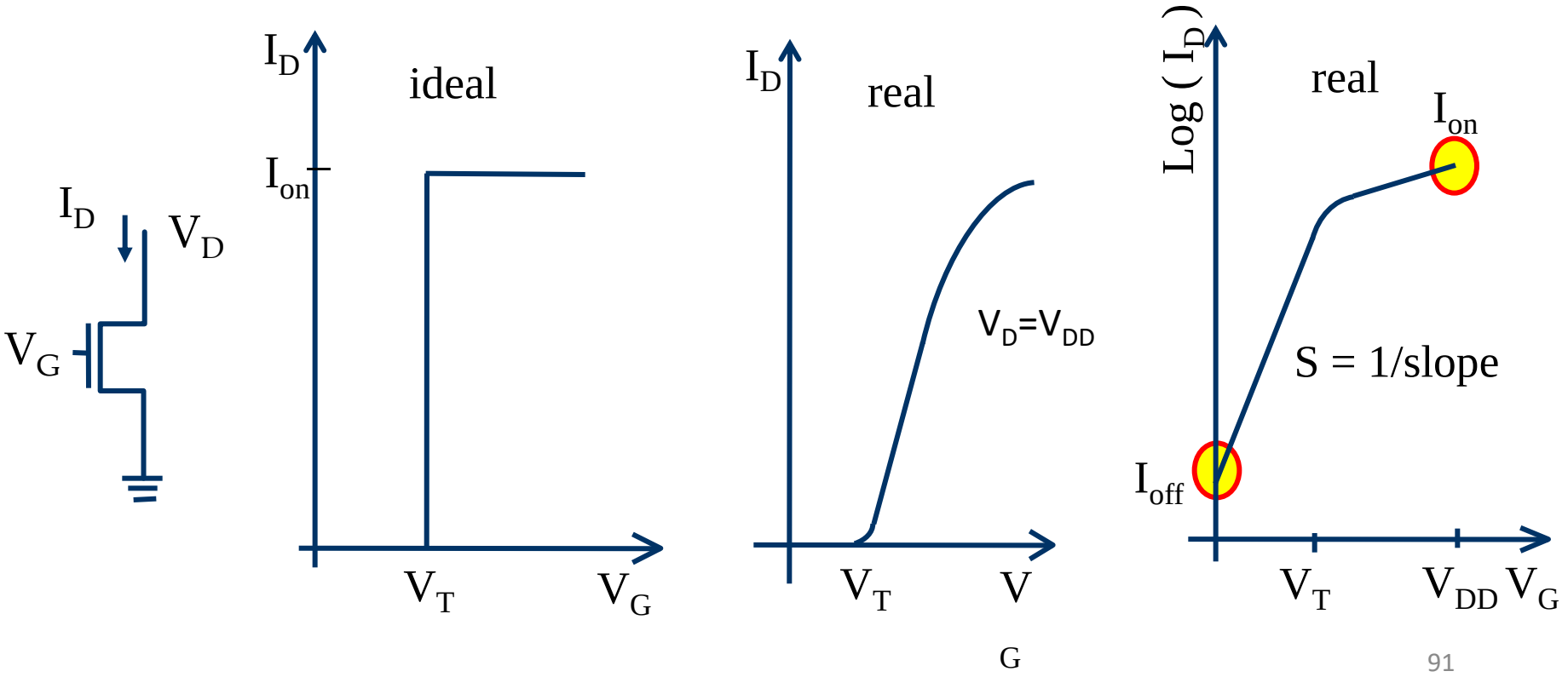
Inverter delay – stand-by



Origin Standby Power

CMOS transistors in digital CMOS circuits

SWITCH



digital CMOS circuits - Inverter

Inverter power dissipation

Ideally only active:

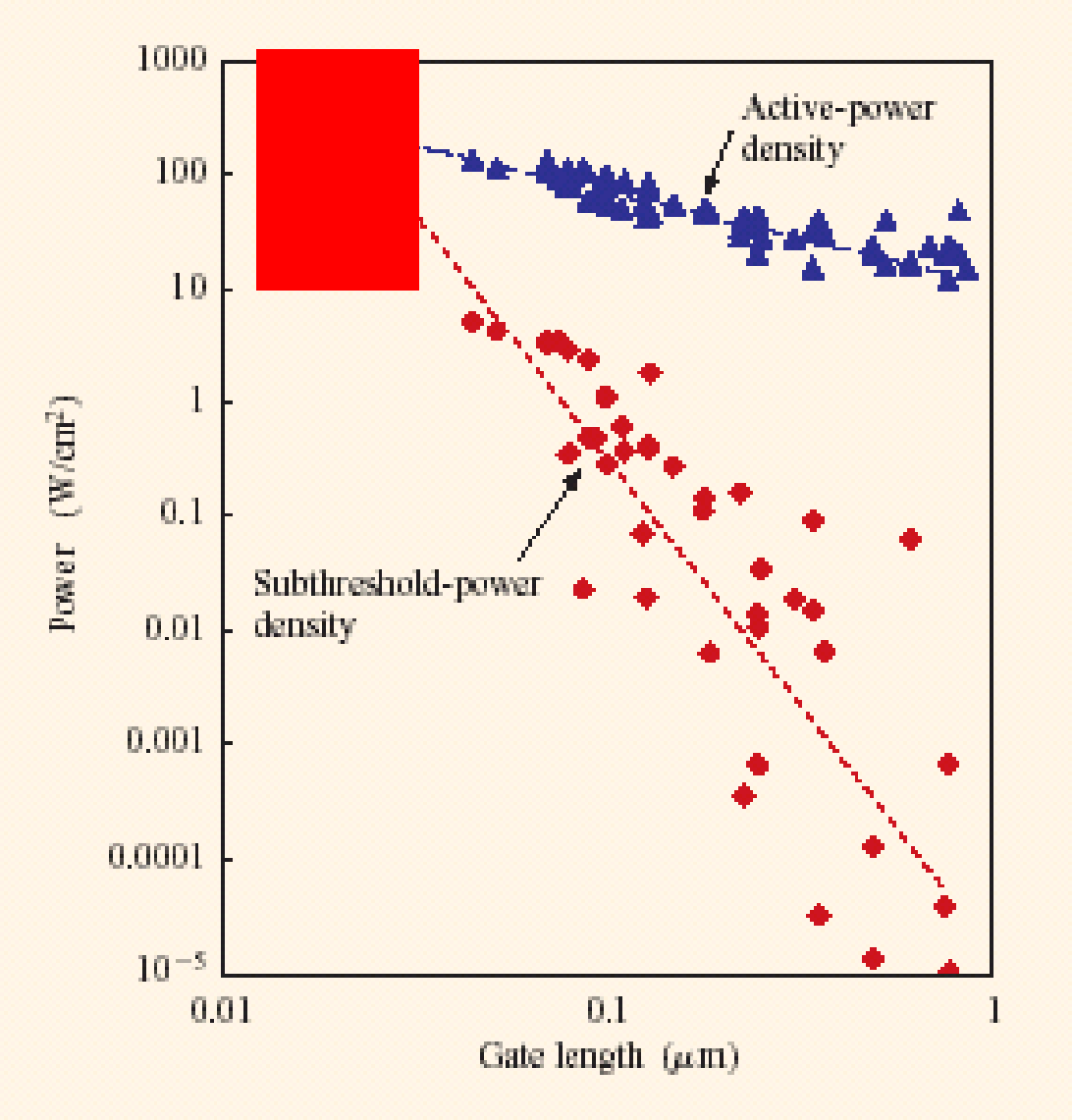
$$P_{ac} = C_{OUT} V_{DD}^2 f$$

In reality also static:

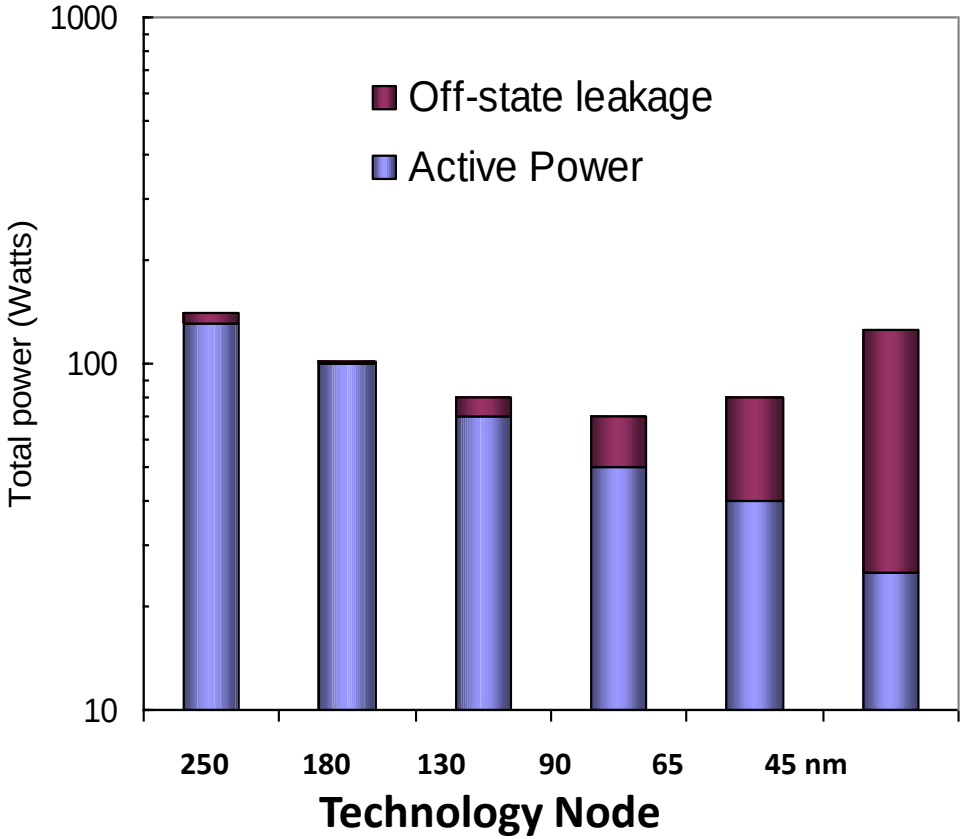
$$P_{off} = V_{DD} W_{TOT} I_{OFF} = V_{DD} W_{TOT} I_0 exp\left(-\frac{qV_T}{mkT}\right)$$

$$P = \underbrace{C \cdot V^2 \cdot f}_{\text{Active power}} + \underbrace{I_{off} \cdot V}_{\text{Sub-threshold power}}$$

Power


1000
100
10
1
0.1
0.01
0.001
0.0001
10^{-5}
Power (W/cm^2)
Active-power density
Subthreshold-power density
0.01
0.1
1
Gate length (μm)

Where does it lead?
…in terms of off-state power



- Increasing importance of off-state current as technology scales

Scaling consequences

$$P = \underbrace{C \cdot V^2 \cdot f}_{\text{Active power}} + \underbrace{I_{off} \cdot V}_{\text{Off-state power}}$$

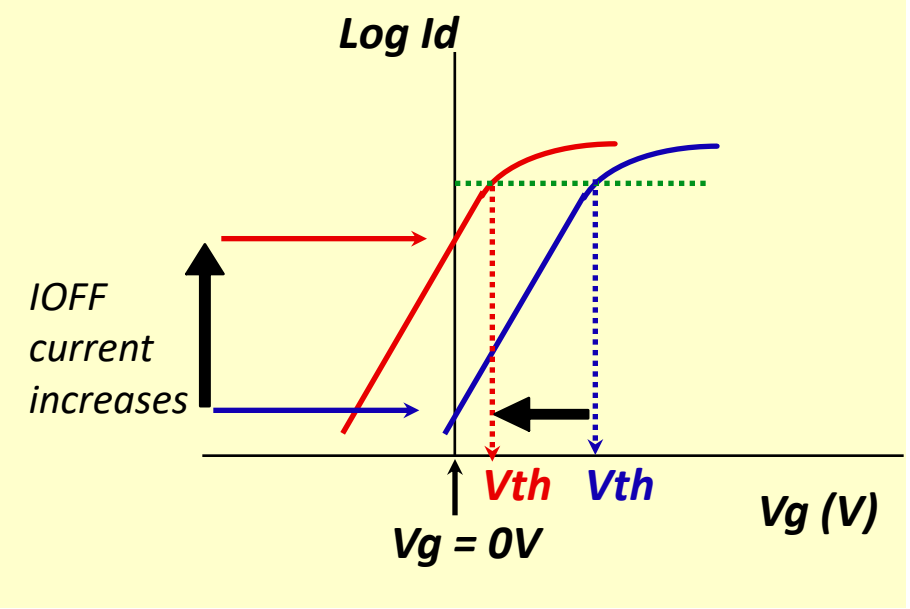
V – supply voltage ↘

If I_{ON} = const → VT ↘ → IOFF ↗

↓

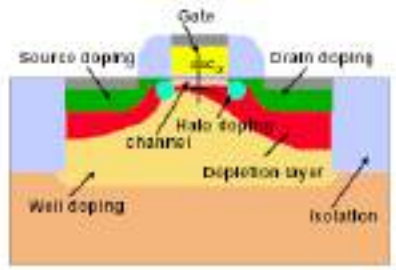
Increase in

off-state power

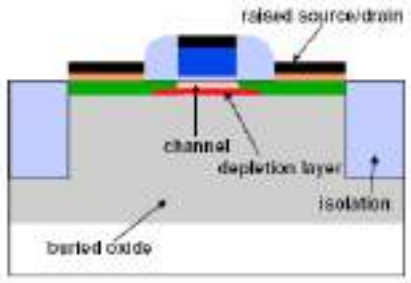


Device Architecture

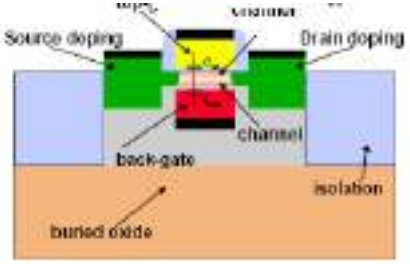
From Bulk to SOI to Multi-Gate



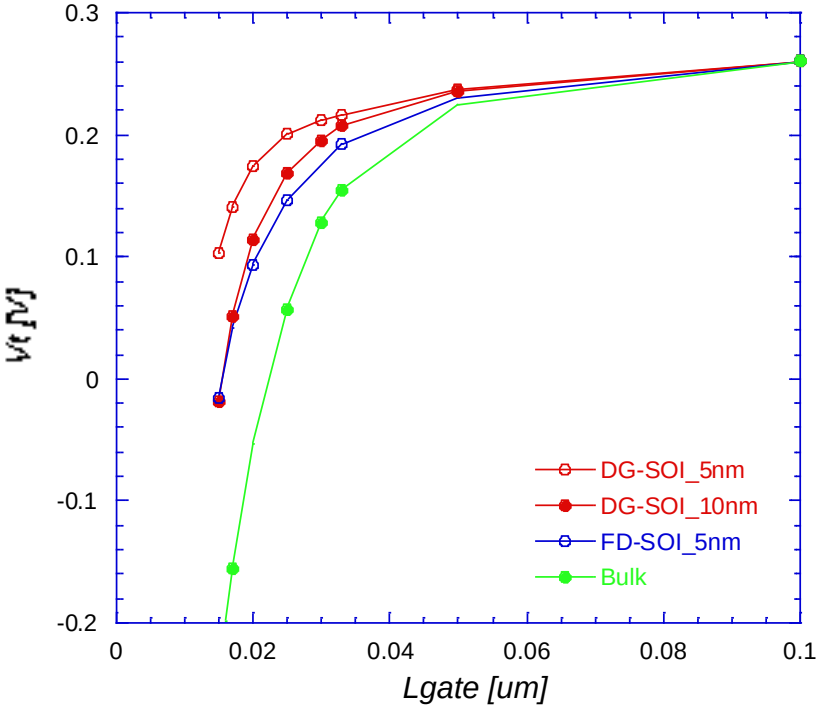
Bulk MOSFET



Thin Body SOI MOSFET



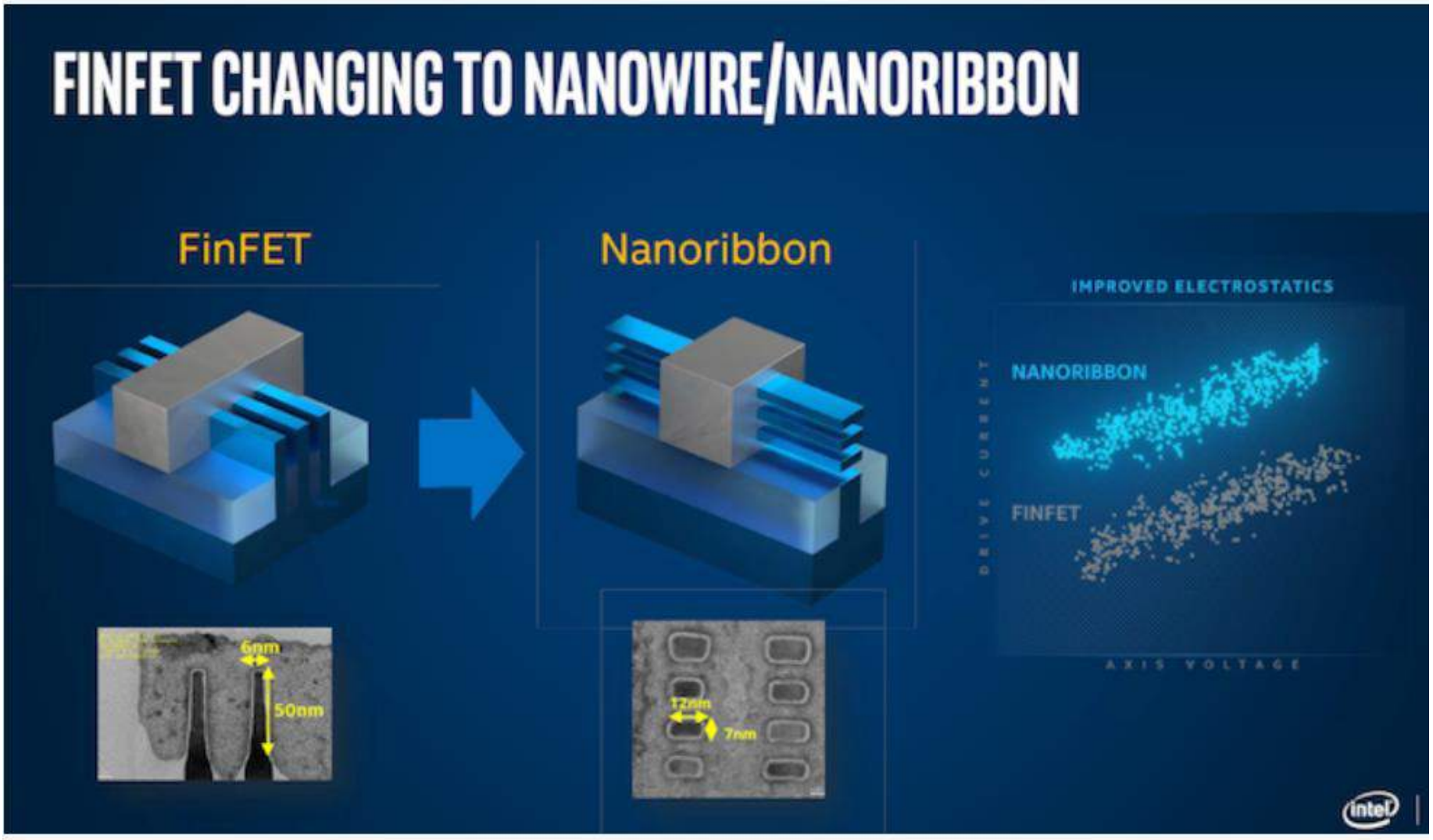
Double Gate MOSFET



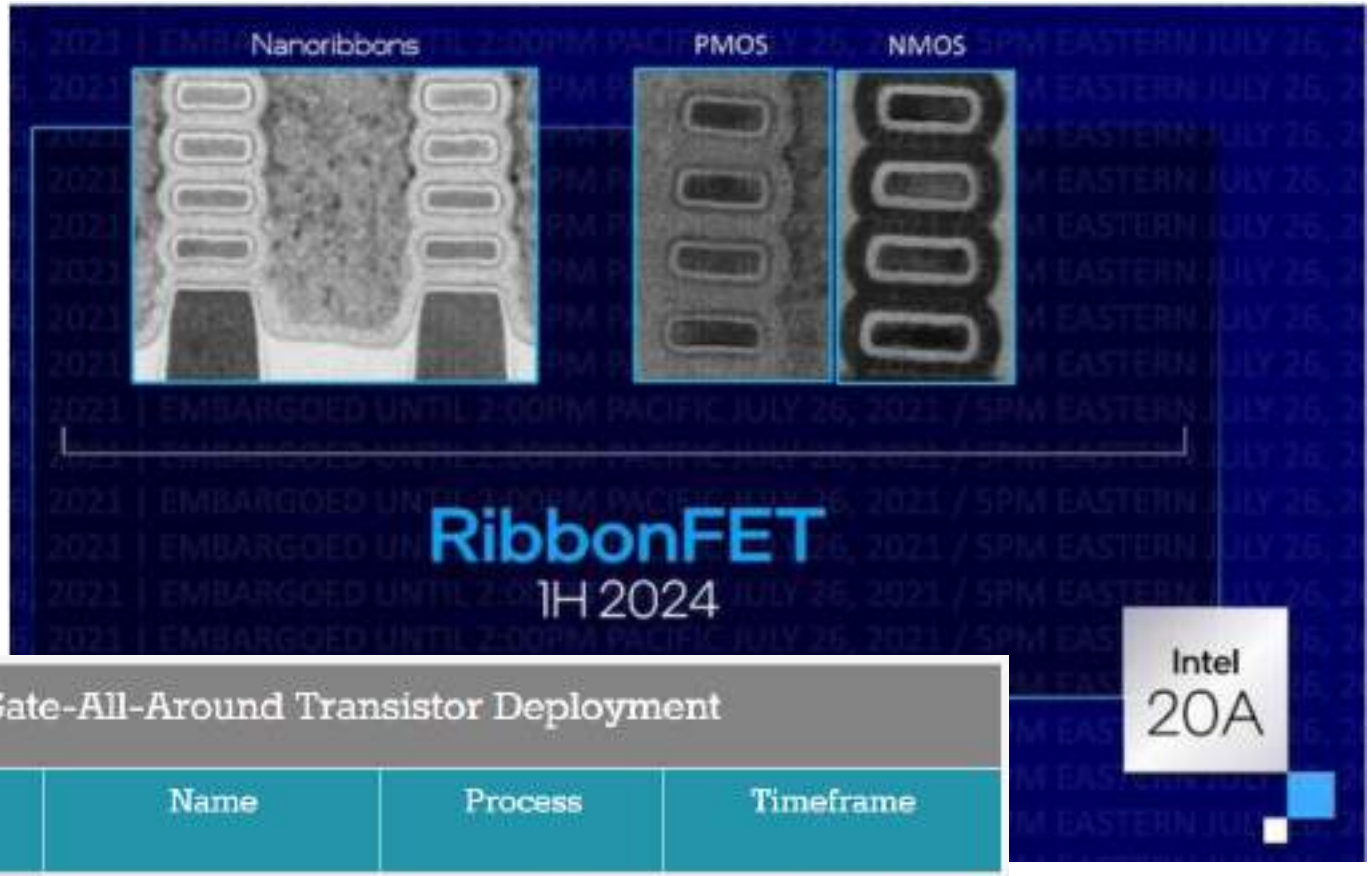
Improves:

- **Short channel effect**
- **Sub-threshold slope**
- **Mobility**

Device Architecture



Device Architecture



Gate-All-Around Transistor Deployment			
AnandTech	Name	Process	Timeframe
Intel	RibbonFET	20A	2024
		18A	2025
TSMC	GAAFET	N2 / 2nm	EoY 2023?
Samsung	MBCFET	3GAE	2022
		3GAP	2023

Thank you