

Fundamentals of Chip-to-Package Interconnections and Assembly

The short course will focus on providing the basic concepts involved in interconnection and assembly of electronics systems, across many applications.

The short course will cover the following topics:

- 1) Technology and process overview
- 2) Fundamentals of wire bonding
- 3) Fundamentals of flip-chip bonding
 - Adhesive bonding
 - Metallurgical bonding with Au and solder bumps
- 4) Characterization, performance and reliability
- 5) Guide to interconnection and process design
- 6) Emerging technologies such as all-Cu interconnections

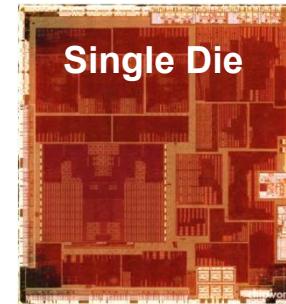
Short course taught by Vanessa Smet, Assistant Professor in the George W. Woodruff School of Mechanical Engineering at Georgia Tech – vanesa.smet@me.gatech.edu

Interconnection hierarchy in electronic systems

- Several levels of packaging may be needed from active/passive components to human “interface”
 - From nm to μm to mm^3 to m^3
 - Levels mitigate risk, if one sub-system fails it can be replaced rather than the entire system
 - Levels have different materials and process limitations
- **Level 0 – still on chip**
 - Redistribution within the chip
 - Fan-out (embedding)
- **Level 1 – off-chip interconnections**
 - Chip-level interconnections
 - Chip to substrate (discrete or multichip module)
- **Level 2 – to board**
 - Board-level Interconnections
 - Package to motherboard or daughter card
- **Level 3 – to human interface**
 - Via sockets or connectors
 - Motherboard to backpanels



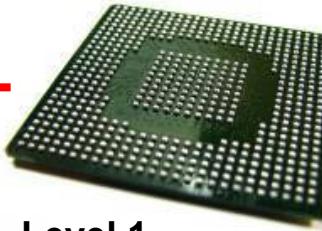
Wafer



Single Die



Level 2



Level 1



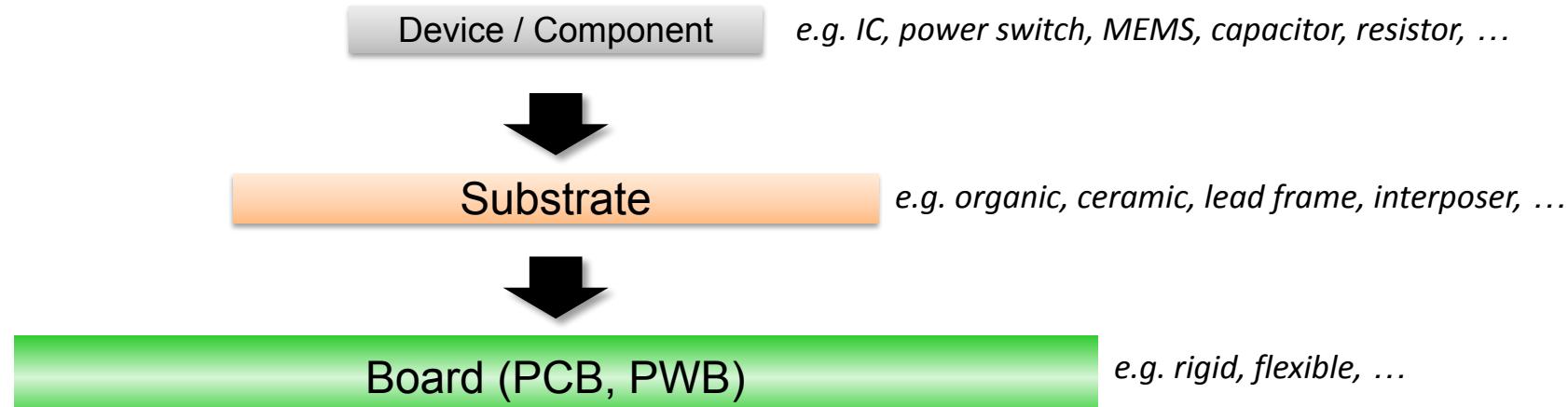
Level 3



Level 4

What are interconnections and assembly?

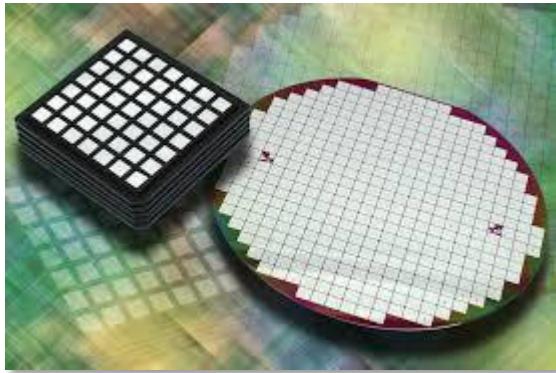
- **Interconnections:** electrically and mechanically connect active devices and passive components, substrate and board, from the device to the “human” interface. Also provides a path for heat transfer. *Examples: wires, pins, bumps, ...*
 - ❖ Contact-based: e.g. in sockets (*not covered in this short course*)
 - ❖ Physical attach: e.g. adhesive bond, metallurgical joining, ...
- **Assembly:** process by which interconnections are formed. *Examples: wire bonding, tape automated bonding, flip-chip bonding, ...*



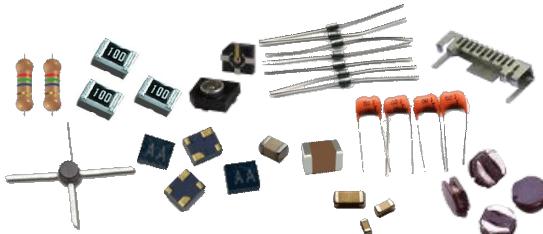
The very basics

CONNECT

Semiconductor devices



Passive components



WITH

Interconnections

Adhesive / Metal

&

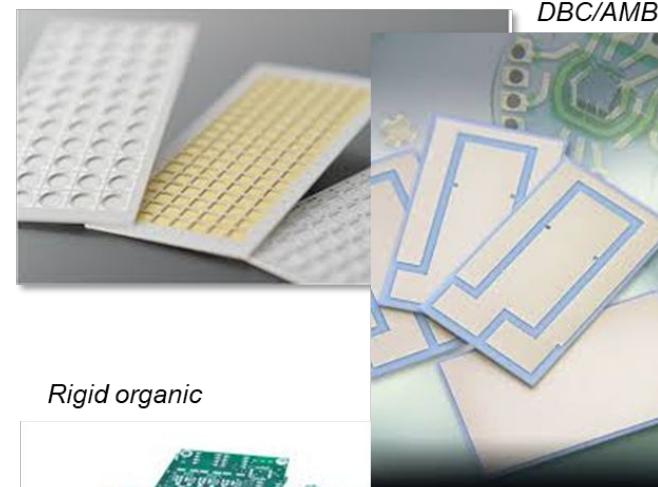
Assembly

Contact + Energy

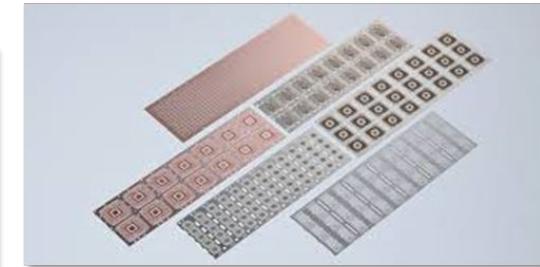
TO

Substrates

Ceramic



Lead frame



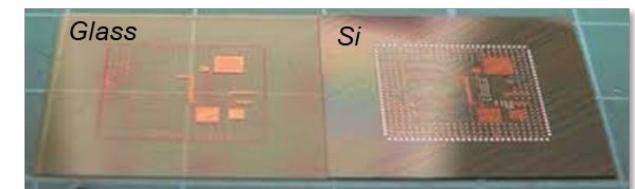
Flexible



Rigid organic



Interposer



Characteristics of interconnections

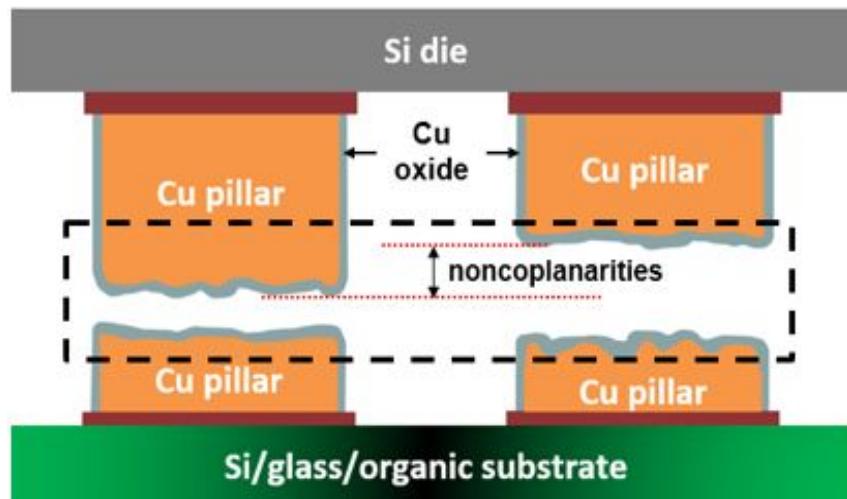
- Materials (metals & conductive adhesives) & their processability both for bumping and assembly
- Geometry
 - Standoff height
 - Density (I/O per cm²) – pitch – diameter
 - Footprint
- Electrical performance
 - Resistance (R), parasitic inductance and capacitance (L, C)
 - Current carrying capability – electromigration performance (EM)
- Thermal performance
 - Thermal conductivity
 - Thermal boundary resistance
- Mechanical performance
 - Compliance of interconnections in assembly
 - Bond strength
 - Long-term reliability (e.g. thermal expansion mismatch, shock, vibrations, ...)
- Cost



Understanding of coupling & trade-offs critical to developing a comprehensive solution that addresses ALL requirements!

Bonding mechanisms

- **Adhesive bonding:** mechanical bond typically formed by mechanical interlocking (in absence of surface functionalization), cross-linking of resin providing adhesion strength.
- **Metallurgical bonding:** chemical bond enabled by the motion (transport) of atoms of one metal into another, provided external energy is brought into the system to overcome the energy barrier to diffusion. Atomic contact between clean and oxide-free surfaces is required.

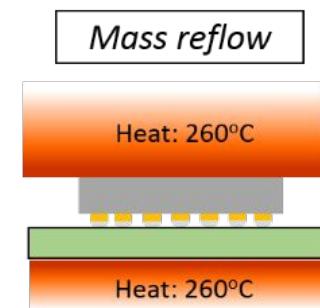


Challenges

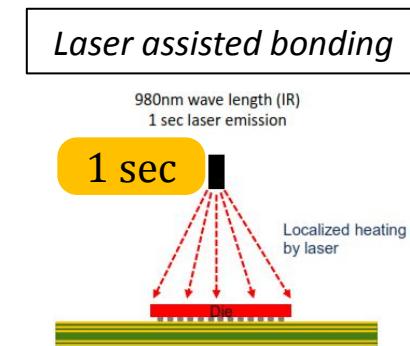
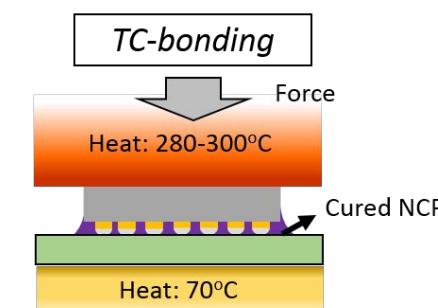
- Non-coplanarities and surface roughness
- Surface oxides and their management
- Relatively high melting point of highest conductivity metals (e.g. Ag, Cu, Au)
- Diffusion kinetics: solid vs. liquid state, effect of scale

Characteristics of assembly processes

- Classification by interconnection type: e.g. wire bonding, flip-chip bonding, sintering
- Classification by energy type: reflow (isothermal heating), thermocompression (heat, pressure), thermosonic (heat, ultrasonic agitation, pressure), hybrid bonding (thermocompression + self-compression), laser-assisted bonding, magnetically-assisted bonding, resistance welding, mechanical caulking, reactive bonding (exothermic reaction), ...
- Bonding parameters: temperature, pressure, time, ...
- Required placement accuracy: self-alignment, degrees of alignment
- Throughput: batch (many parts assembled in one process step, generally > 50,000 UPH) vs. sequential (individual components, generally < 1,000 UPH) processing
- Resulting warpage
- Yield
- Tools and infrastructures



VS.

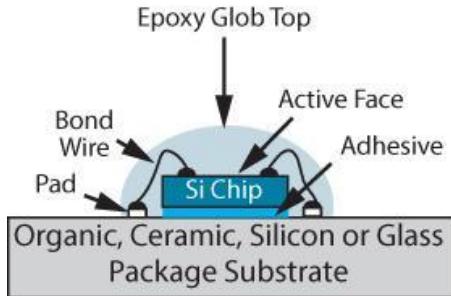


- *Isothermal heating*
- *High throughput*
- *High warpage – low control of joint microstructure*

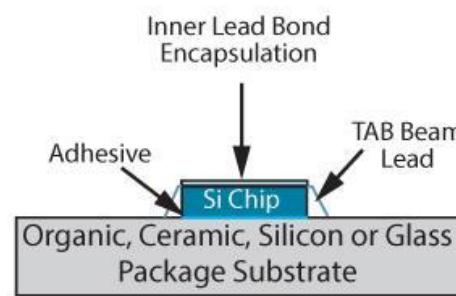
- *Directional heating*
- *Low throughput*
- *Low warpage – high control of joint microstructure*

Assembly technologies

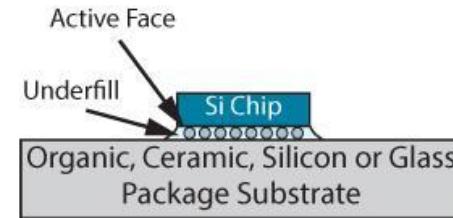
(a) Wire Bonding



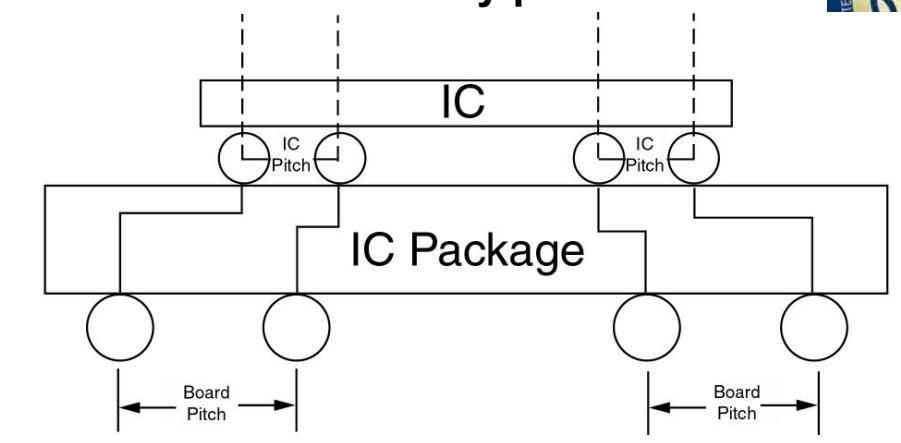
(b) Tape Automated Bonding



(c) Flip-Chip Bonding



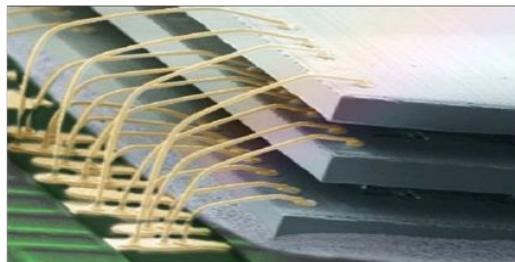
Assembly pitch



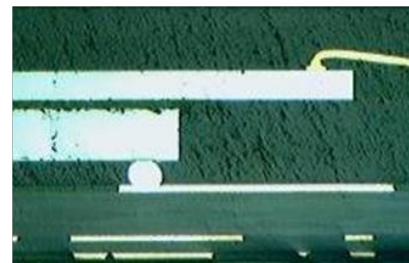
Rule of thumbs:

Interconnection diameter $\sim \frac{1}{2}$ pitch

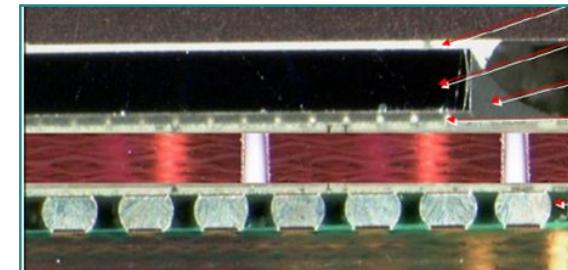
Wire-bonded package



Hybrid package



Flip-chip package

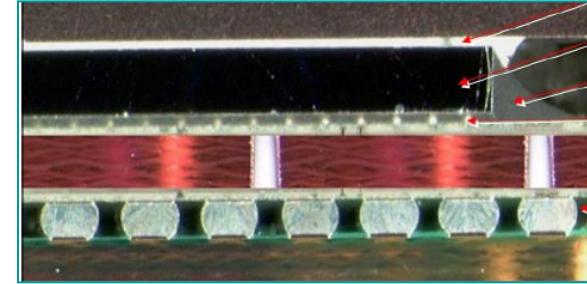


Assembly technologies often mixed for optimal system integration: performance, footprint and cost decides!

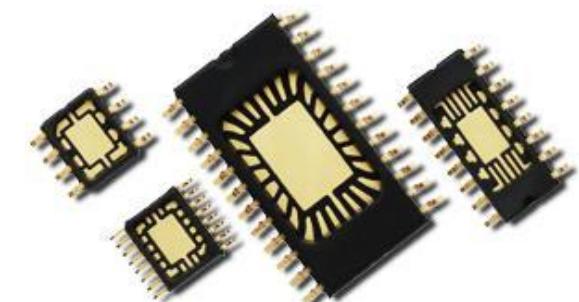
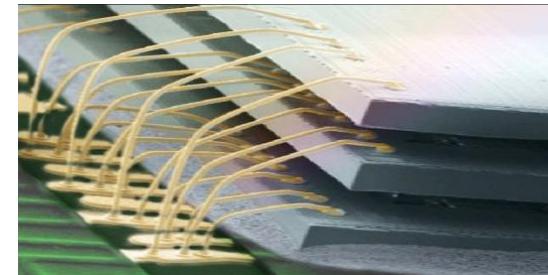
In products

- The majority of chips are wire bonded on lead frames
- Higher level of integration:
 - Increased I/O density
 - Higher electrical & thermal performance require more advanced packaging technologies
- Advanced packaging uses:
 - High-density organic, silicon & glass substrates
 - Wire bonding, flip-chip and/or thermocompression bonding
 - Advanced system integration:
 - 2.5 and 3D assembly
 - Interposers

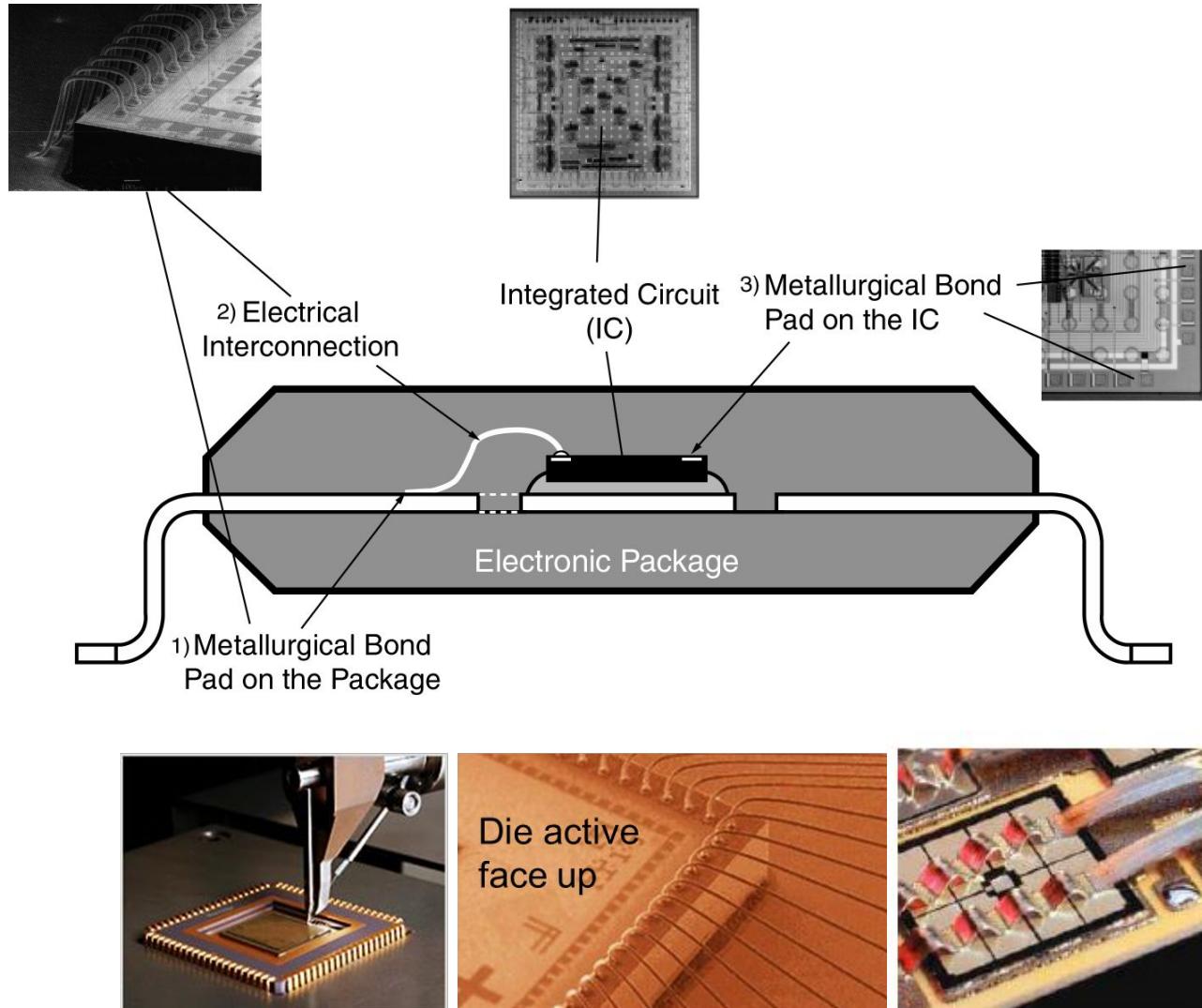
Performance



Cost

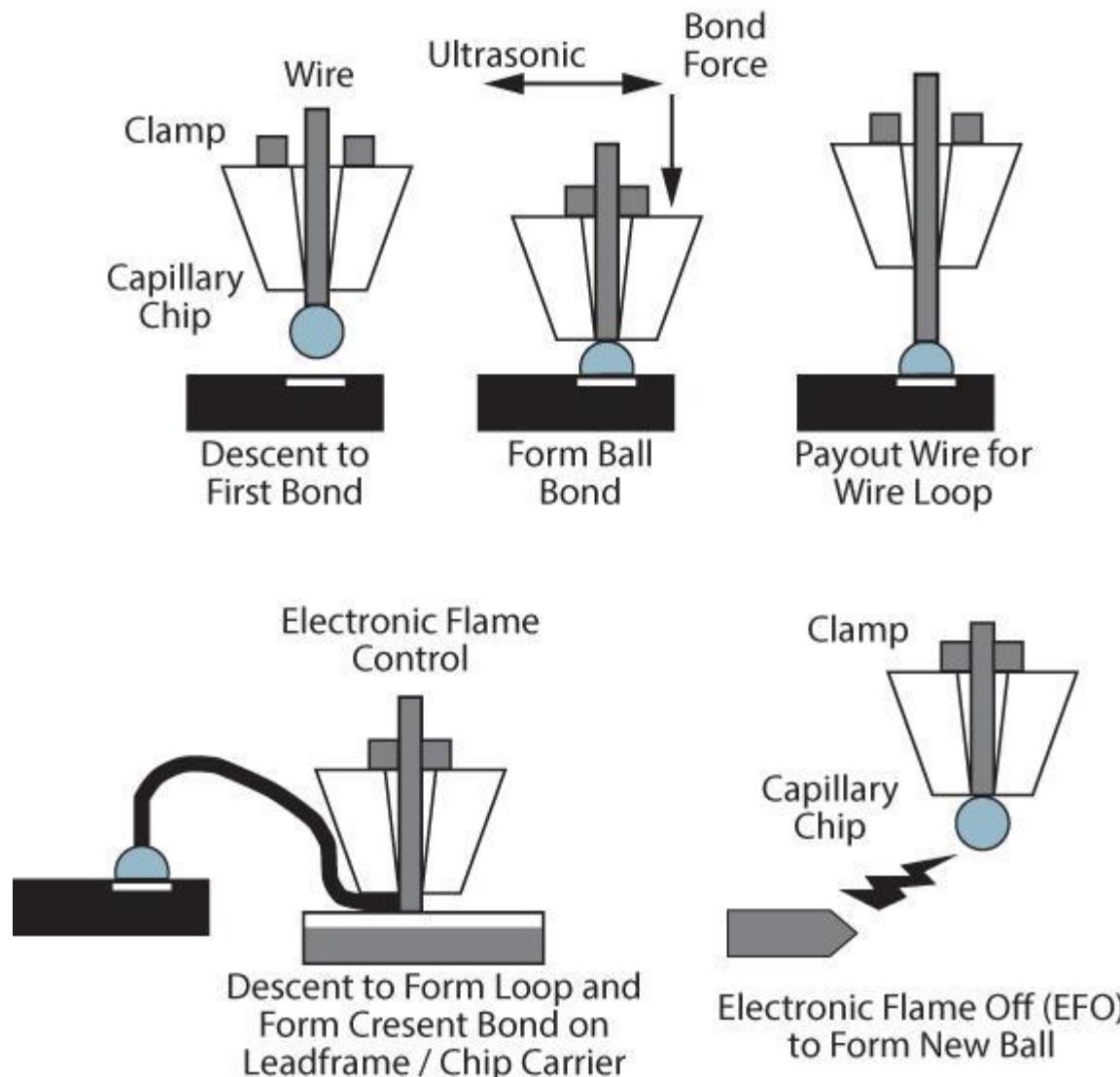


Fundamentals of wire bonding



- Die active face up, no underlying active circuitry
- **Peripheral** point-to-point interconnection up to 3 rows – *design flexibility but large footprint + limited density*
- **Min pitch of 35 µm** using 15 µm-diameter wires
- **Wire materials:** Au, Cu, Al
- **Wire diameter:** 25 µm (typical) – 15 to a few 100 µm
- **Bond pad materials:** ENIG-coated Cu, Cu alloys
- Two main processes: ball (thin wires) or wedge bonding (thick wires or ribbons)

Ball bonding process



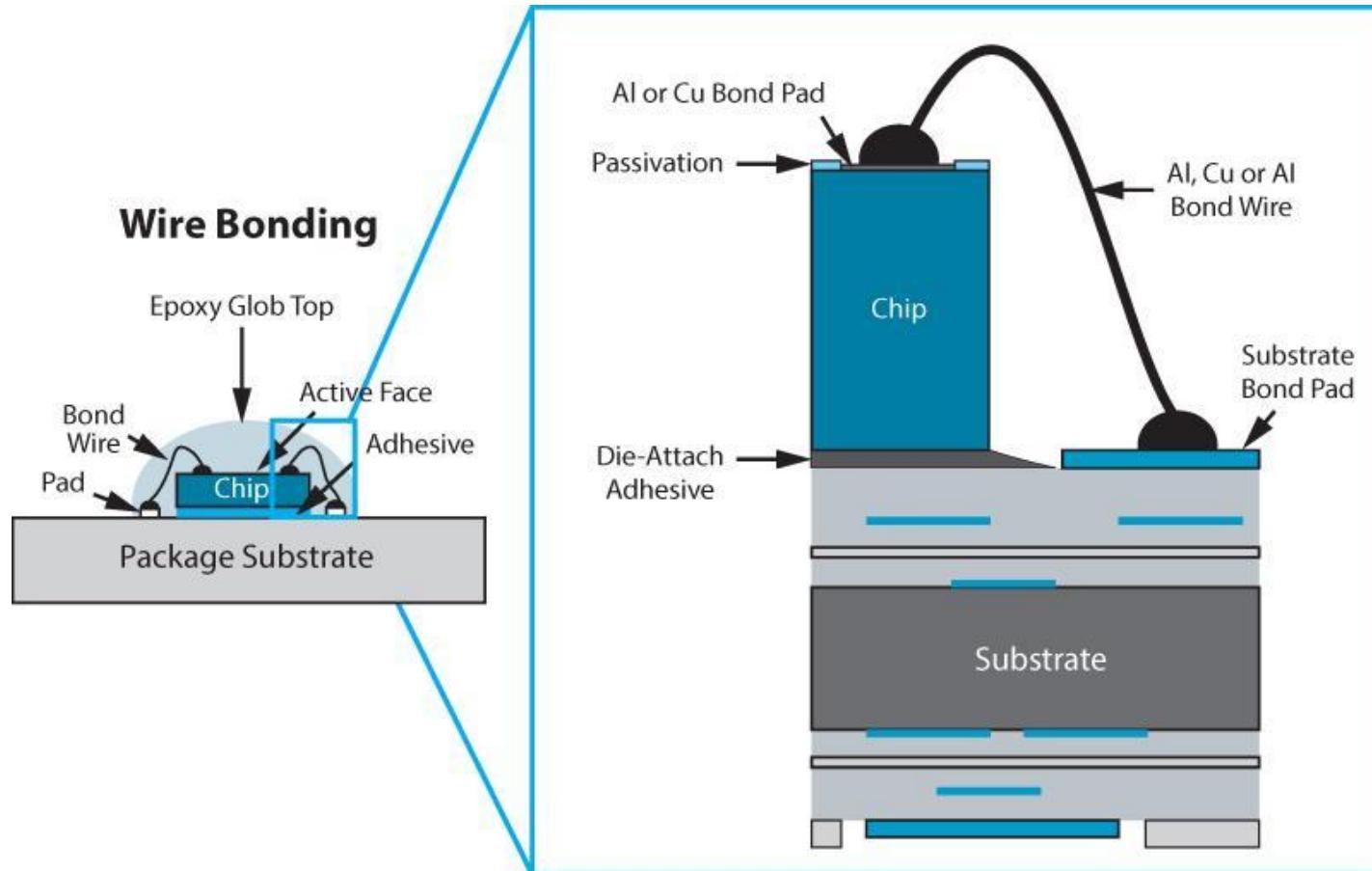
Thermosonic bonding typical parameters (Au wires):

- Temperature: 150-200°C
- Force < 100 g
- Ultrasonic excitation at 60-120kHz
- Cycle time: 20ms
- High yield: 40 – 1000 ppm

Post-processing: encapsulation (e.g. glob top, overmolding)

Note on flexible substrates: require substrate permanent / temporary stiffeners in bonding area & pad reinforcement

Ball bonding process



Thermosonic bonding typical parameters (Au wires):

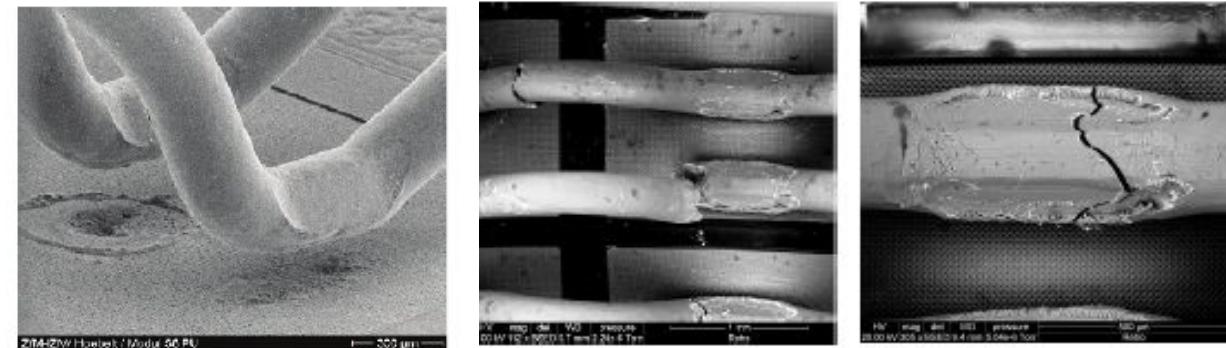
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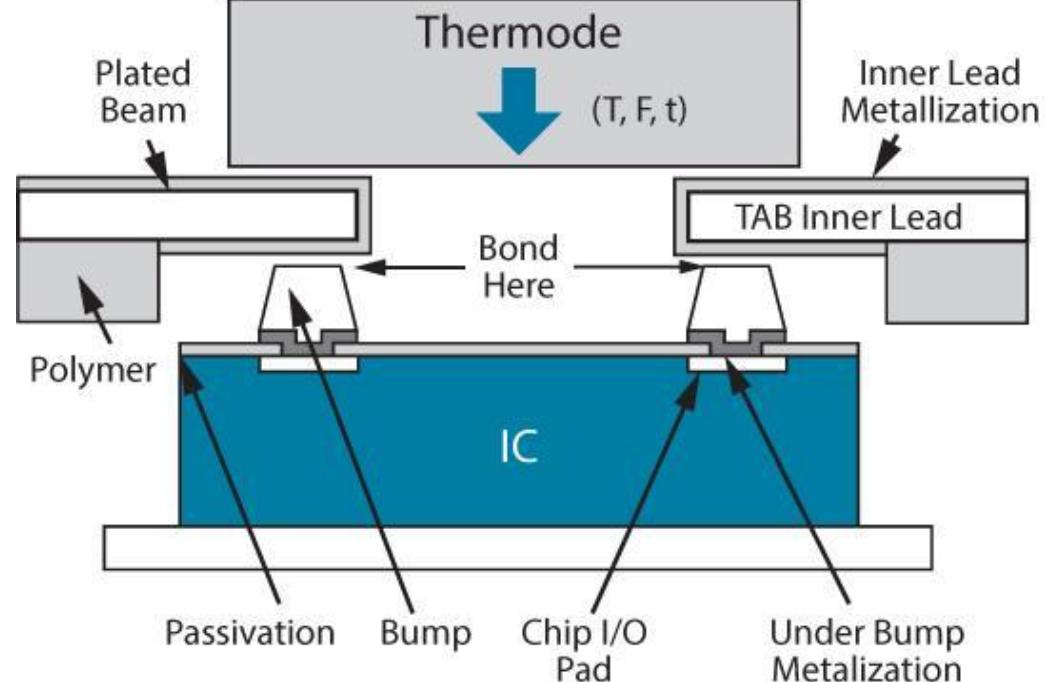
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Performance, characterization & reliability

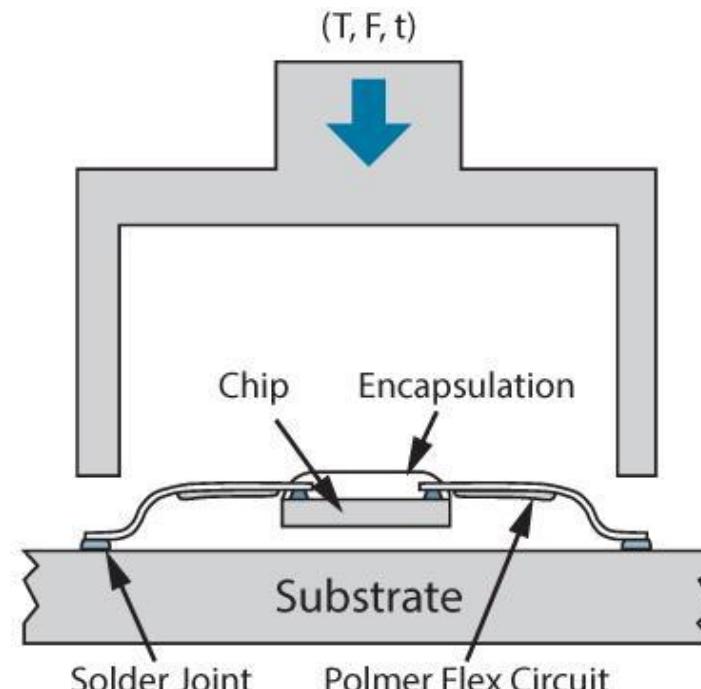
- Electrical:
 - ❖ DC resistance: $R = \rho \times \frac{l}{A}$ where ρ is the resistivity of the wire metal in $[\Omega \times m]$, l is the length of the wire in [m] and A is the cross-section of the wire in $[m^2]$
 - ❖ Long interconnection length: high impedance – susceptibility to inductive coupling
- Mechanical strength: wire bond shear / pull test according to JEDEC standards



Fundamentals of tape automated bonding (TAB)



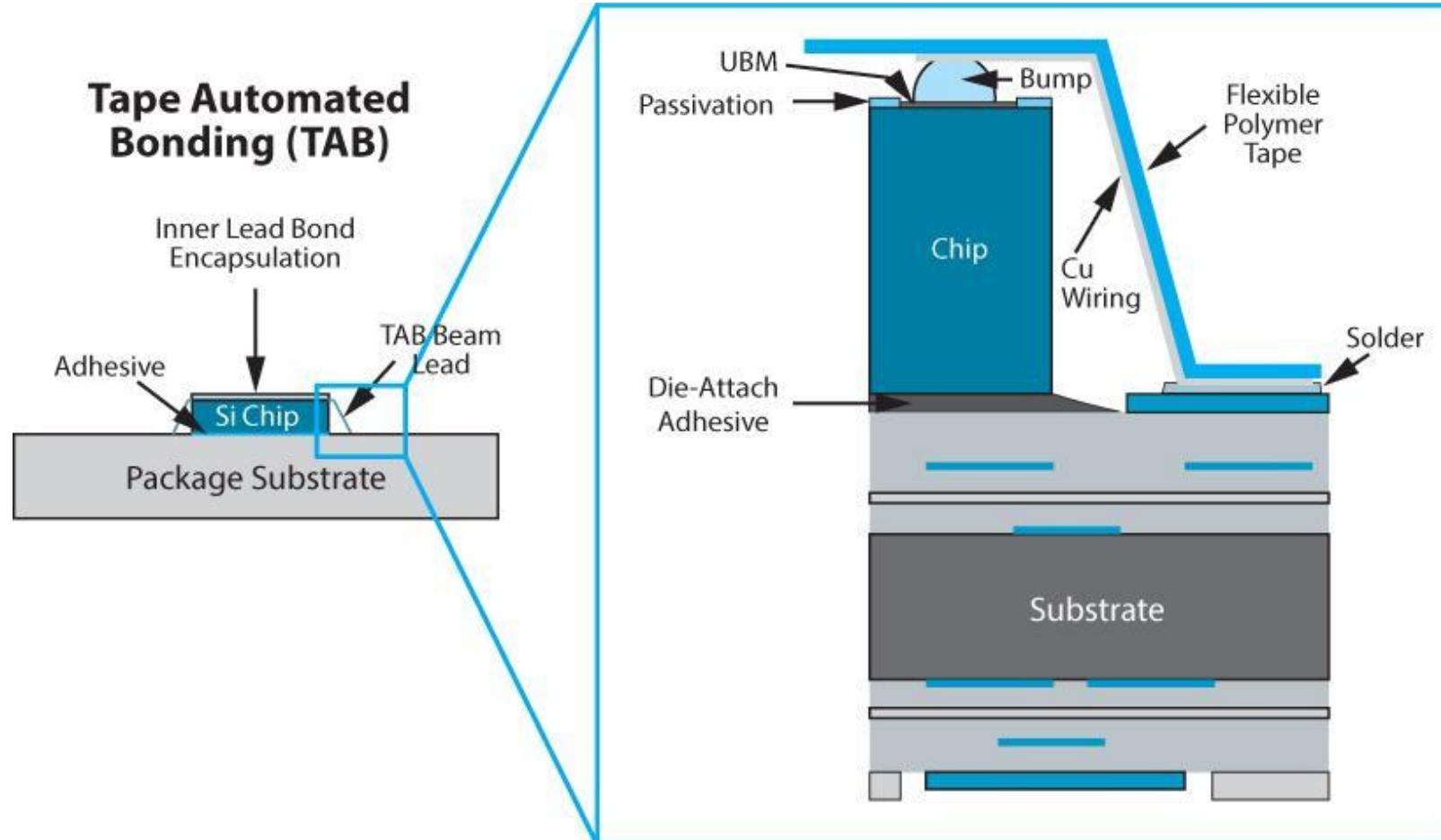
(a) Inner Lead Bonding



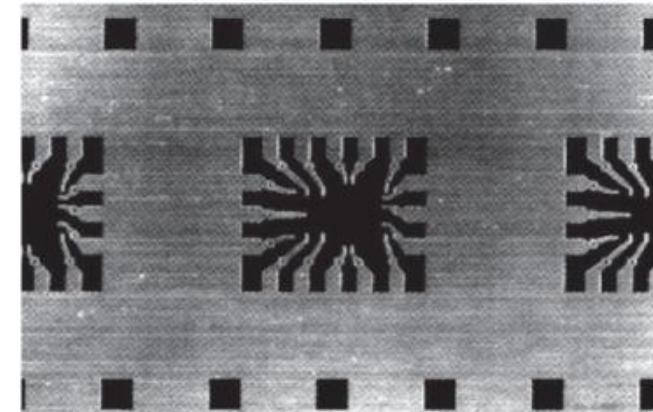
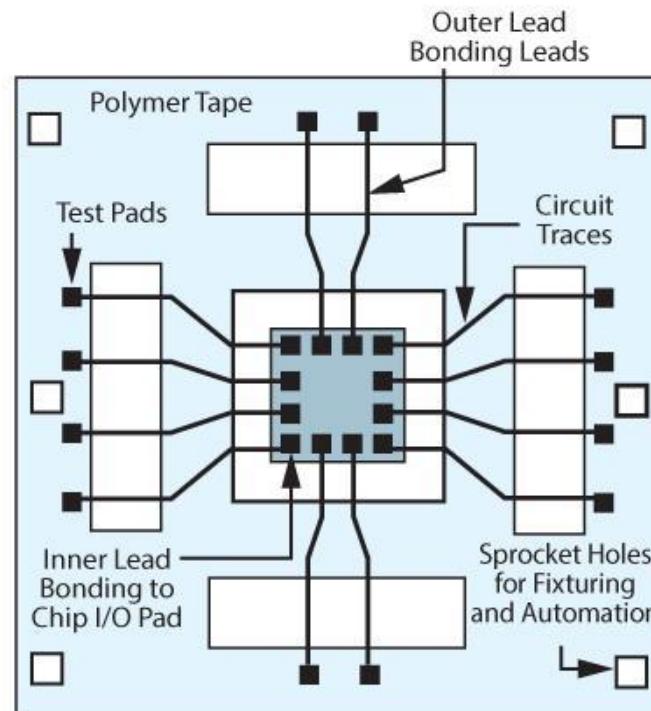
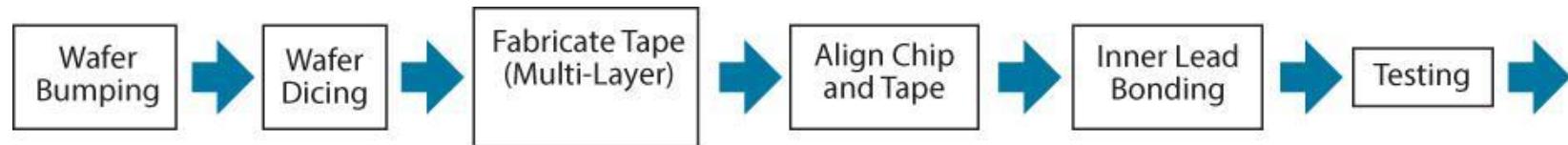
(b) Outer Lead Bonding

- Derived from wire bonding, goal is to increase throughput through “gang” bonding
- Wiring created on flexible (e.g. polyimide) substrate – finer pitch capability than wire bonding
- All connections are made at once but requires a bumped wafer
- IC can be active face up or down
- Peripheral bump arrangement – limited I/O density

Anatomy of a TAB cross-section



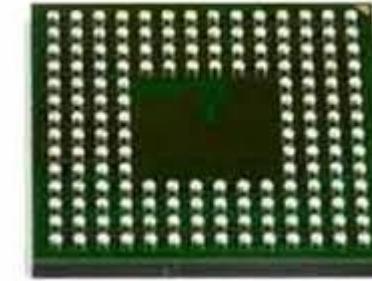
Typical TAB process flow



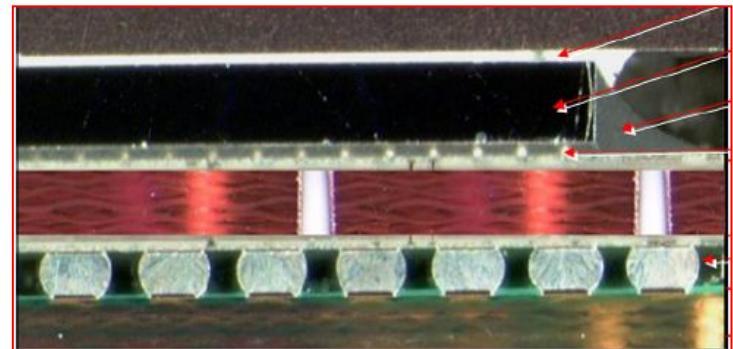
Fundamentals of flip-chip bonding

- **Die assembled active face down:** chip-scale package, reduced interconnection length, thermal management through chip backside possible
- **Interconnection arrangement:** area array for high-density and fine-pitch interconnections
- **Interconnection technology:**
 - ❖ Adhesives (ICA, ACA)
 - ❖ Metal bumps (Au, Cu, solder)
- **Batch assembly:** all connections made in a single step
- **Applicable at chip & board levels**

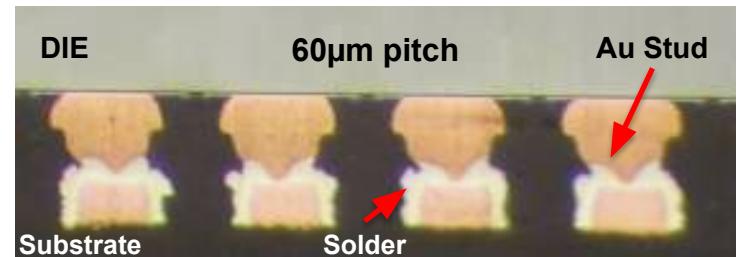
Area array bump configuration



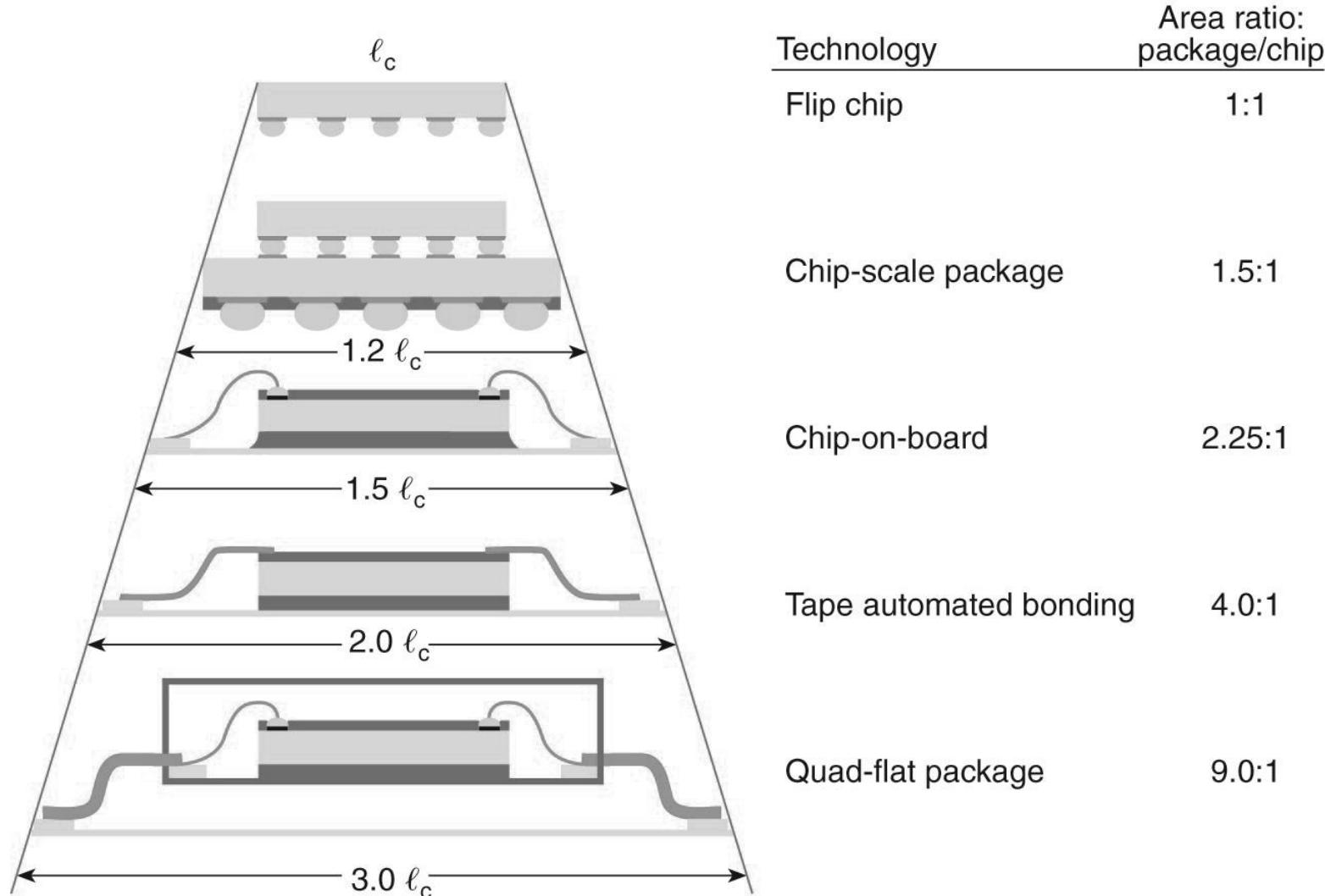
C4 package



Stud-bumped package

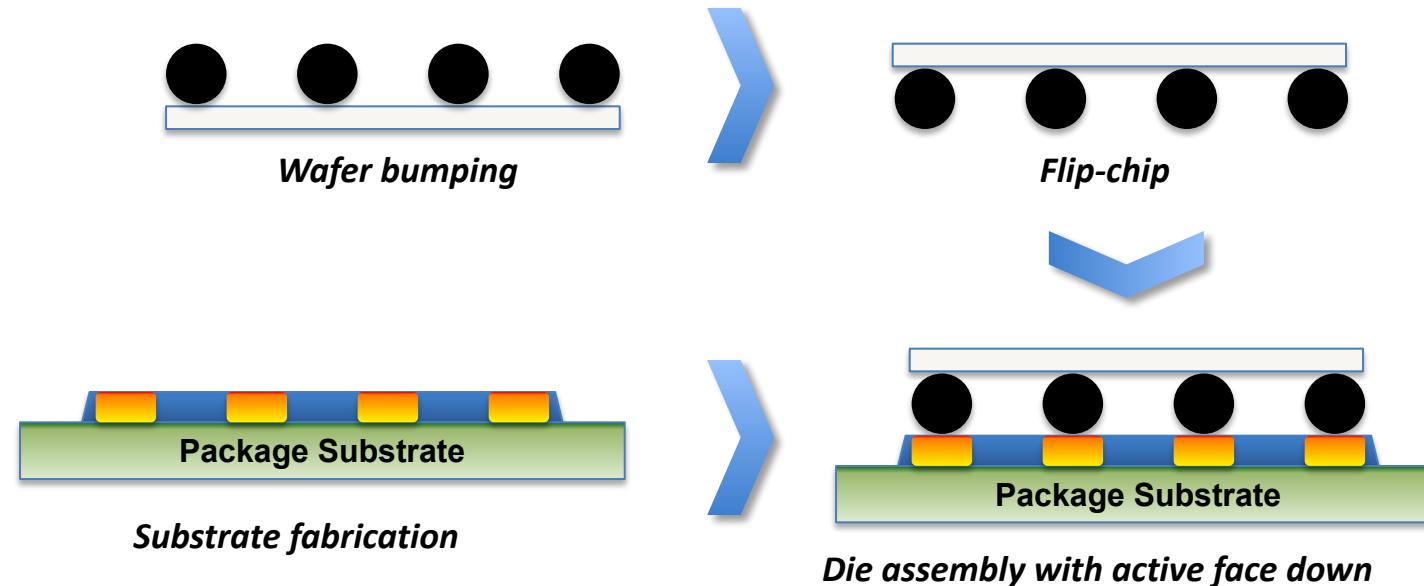


Size comparison – Chip-scale package



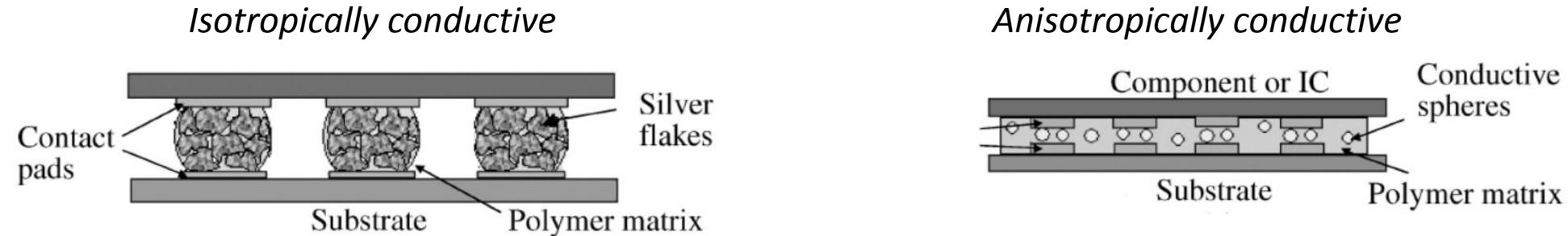
Flip-chip bonding concept

- Wafer bumping
- Die-to-wafer, wafer-to-wafer, die-to-substrate, substrate-to-board process
- Fine alignment capability with HVM tools ($\pm 3 \mu\text{m}$ at chip level)
- Chip-last approach:

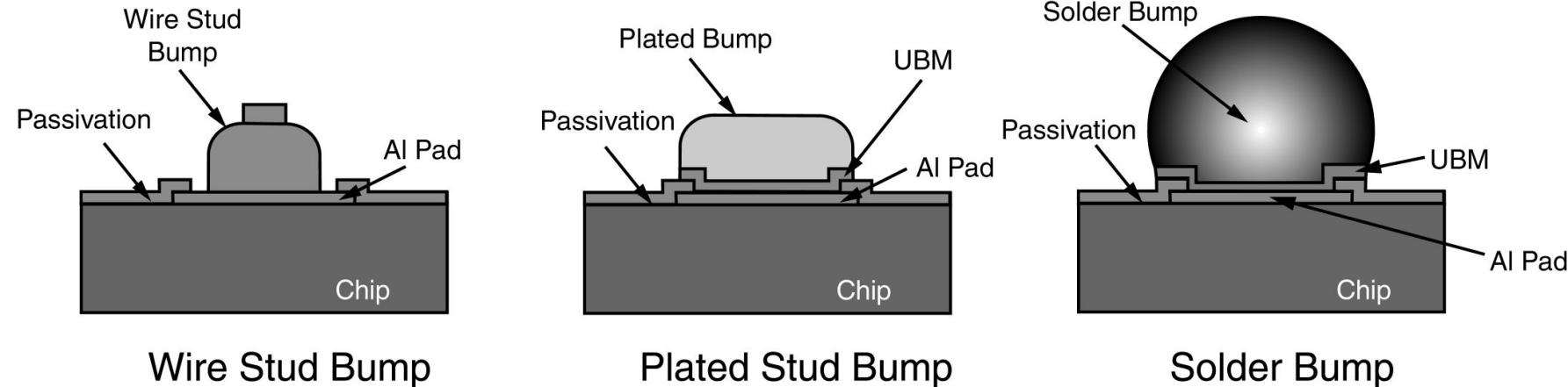


Flip-chip interconnection types

- **Adhesives**



- **Bumps**



❖ Chip level – C4: controlled collapse chip connection

Liquid-phase vs. solid-state bonding



Solder – liquid-phase

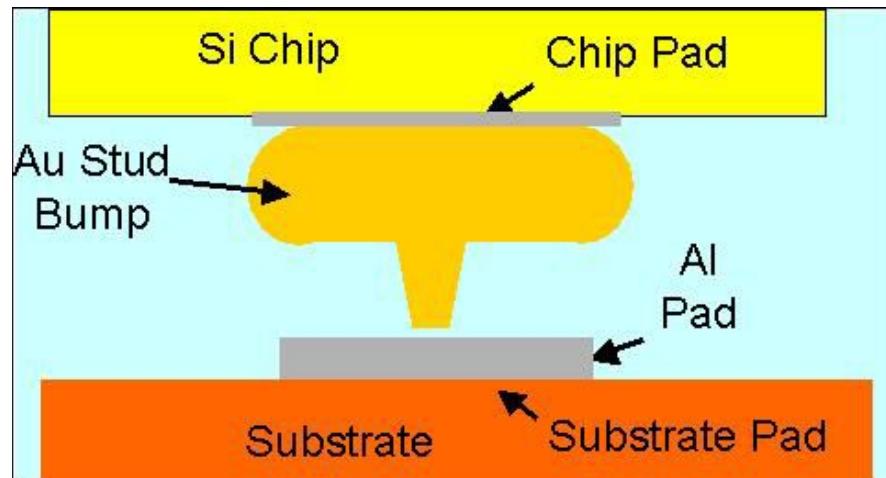
- Low melting point
- Solder melting:
 - ❖ Collapse (high tolerance to non-coplanarities)
 - ❖ Self-alignment
- High interdiffusion rates – fast bonding
- Risks of bridging

VS.

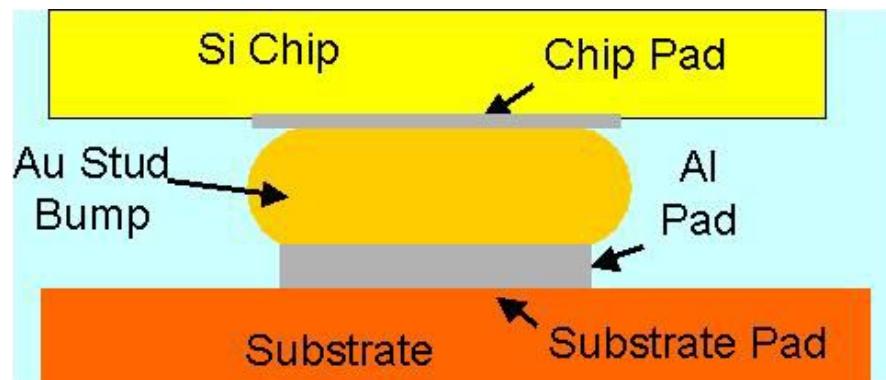
Au-Au, Cu-Cu – solid-state bonding

- High melting point
- No viscous phase in assembly
 - ❖ Mitigation of non-coplanarities through plastic deformation under compression or surface planarization
 - ❖ Alignment accuracy more critical
- Reasonable to low self-diffusion rates – surface activation, post anneal step
- No risk of bridging

Stud bumping & Au-Au bonding



↓ Flip-chip bonding



Au Stud Bump on Chip Pad
 ~ 75 microns diameter
 Does not require UBM

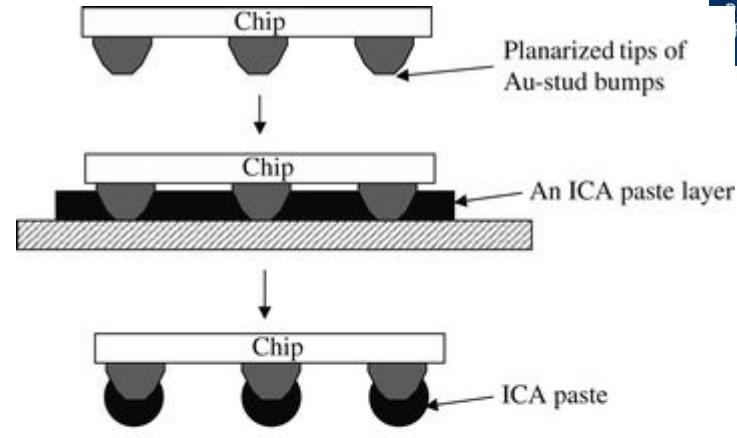
- Directly derives from wire bonding, so infrastructure readily available
- Bump material: Au (most common), Cu (hard to coin, oxidation)
- No need for UBM (under bump metallization) as no risk of electromigration

- Bumps can be coined to flatten the wire “tail”
- Assembly by thermosonic or thermocompression bonding: heat + ultrasonic energy + applied pressure – metallic bonding relies on self-diffusion

Au-Au bonding is very popular in analog and consumer power applications: variable pitch and bump diameter, high current density

Conductive adhesives – Classification

- **Composite materials:** resin binder + conductive fillers
- **Isotropic adhesives or films (ICA or ICF)** – e.g. silver epoxies
 - ❖ High filler content – conduct in all 3 directions
 - ❖ Paste form – patterning through screen/stencil printing or through dip transfer on stud bumps
- **Anisotropic adhesives or films:**
 - ❖ Low filler content – relies on trapping of particles to conduct in z-direction
 - ❖ Bumping required
 - ❖ Film or paste form – lamination on wafer or substrate

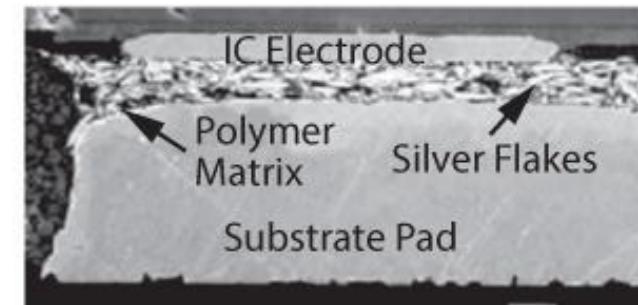
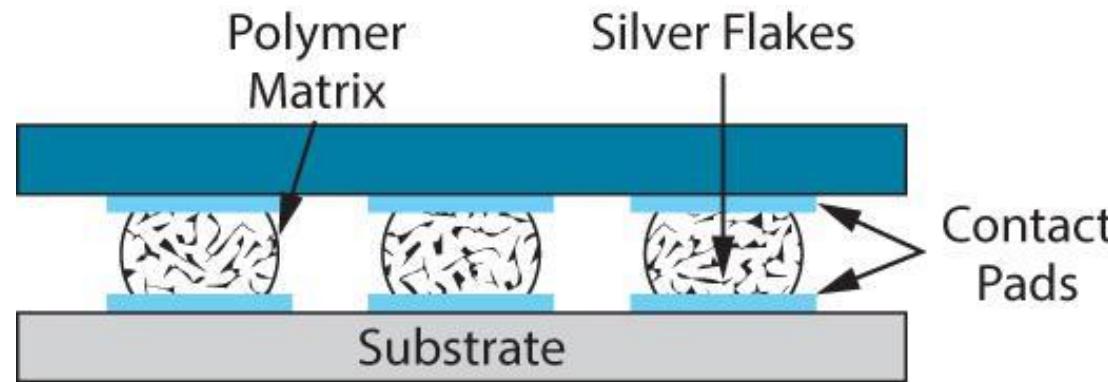


- **Relatively poor electrical / thermal performances**

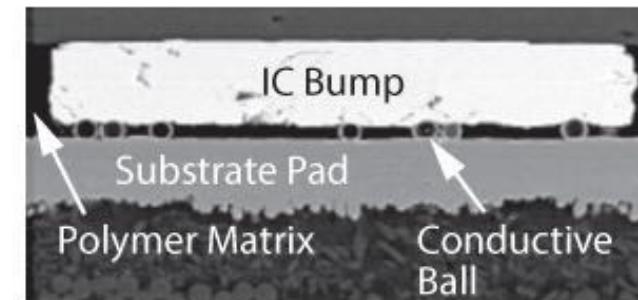
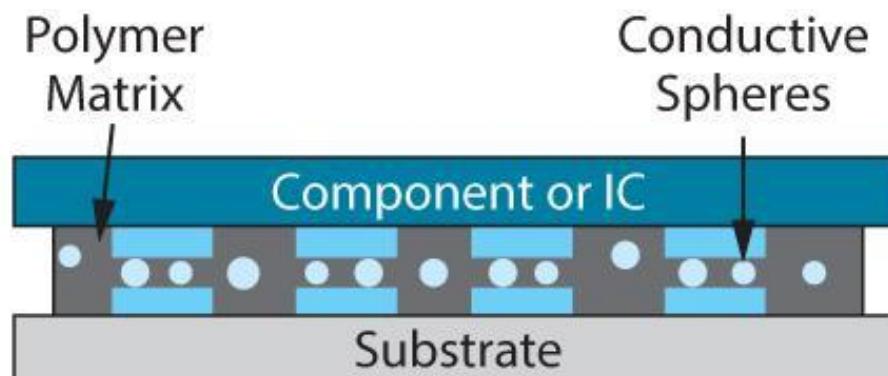
Characteristic	ICA	SnPb eutectic
Volume resistivity ($\Omega \text{ cm}$)	0.00035	0.000015
Typical junction resistance ($\text{m}\Omega$)	<25	10-15
Thermal conductivity (W/mK)	3.5	30
Shear strength (MPa)	13.8	15.2
Min processing temperature ($^{\circ}\text{C}$)	150-180 (flexible electronics)	215
Environmental impact	Very minor	Negative

Conductive adhesives - Classification

- Isotropic Conductive Adhesive

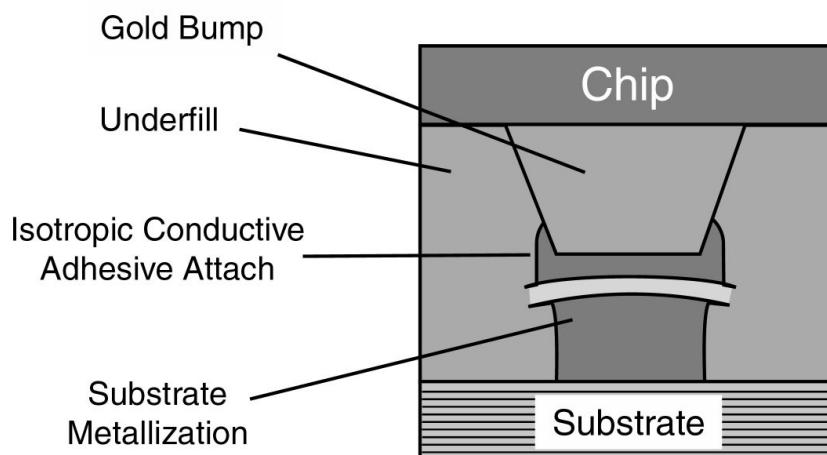
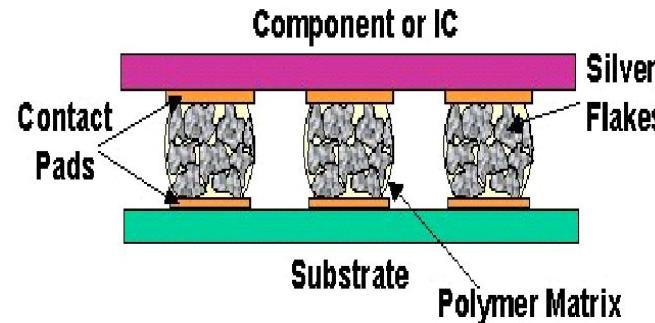


- Anisotropic Conductive Adhesive

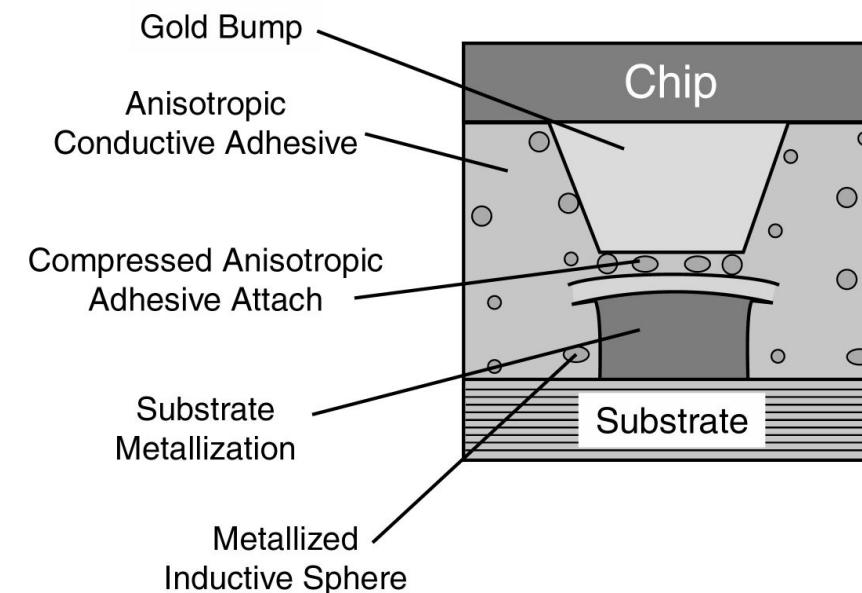
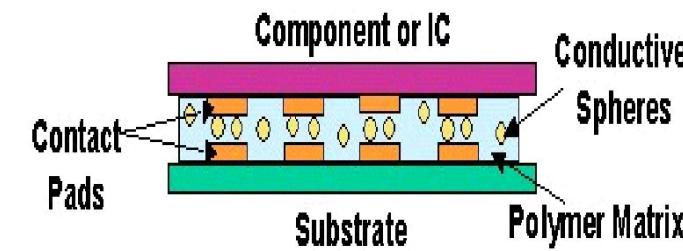


Adhesive bonding process

Isotropic Conductive Adhesives



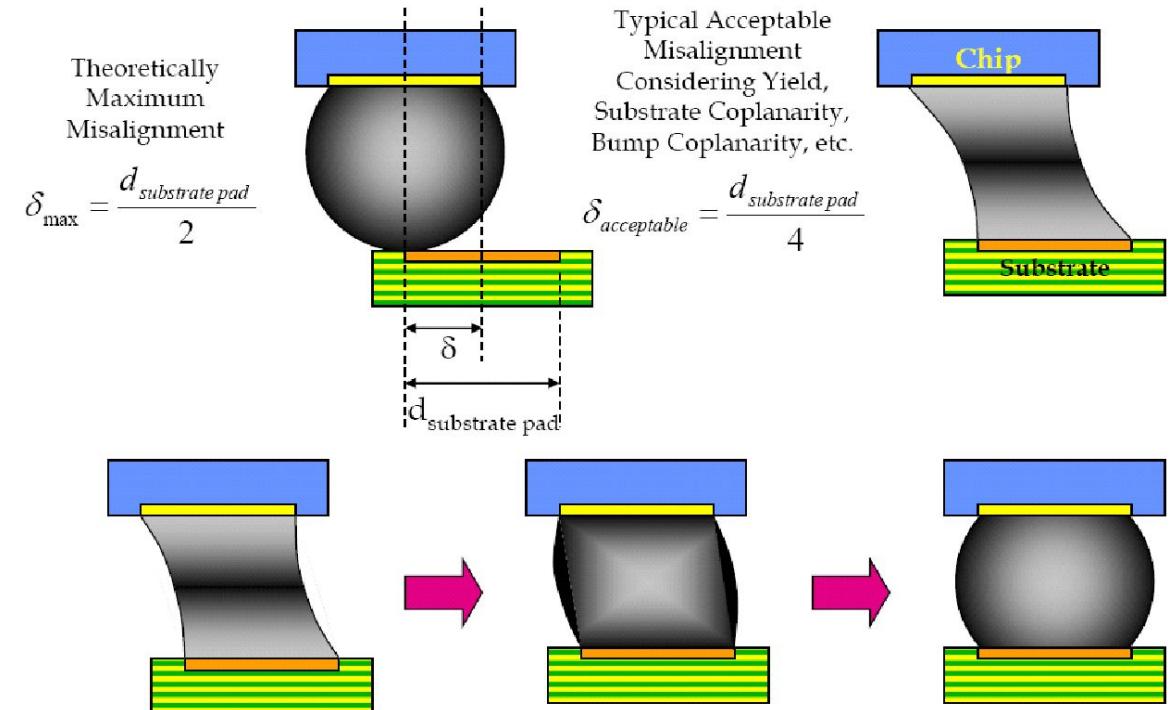
Anisotropic Conductive Adhesives



Assembly is typically carried out at 180°C – 50kgf/cm^2 for a few tens of seconds (thermocompression)

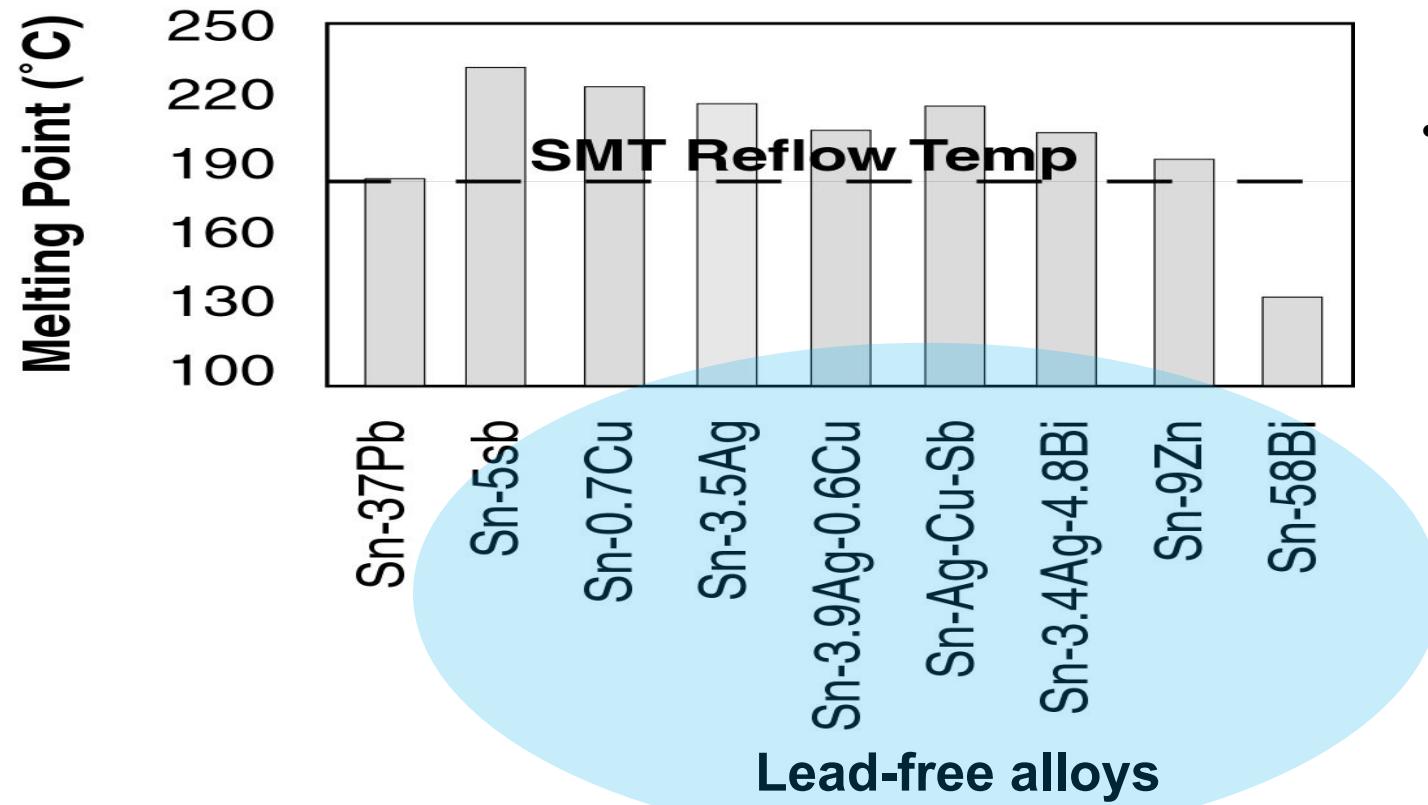
Why use solders?

- Adequate electrical / thermal properties
- Relatively low melting point, giving low processing temperature
- High capacity to absorb CTE-mismatch induced deformation
- Collapse and self-alignment of solders provide tolerance to:
 - ❖ Bumps and pads non-coplanarities
 - ❖ Substrate and die warpage
 - ❖ Slight misalignment



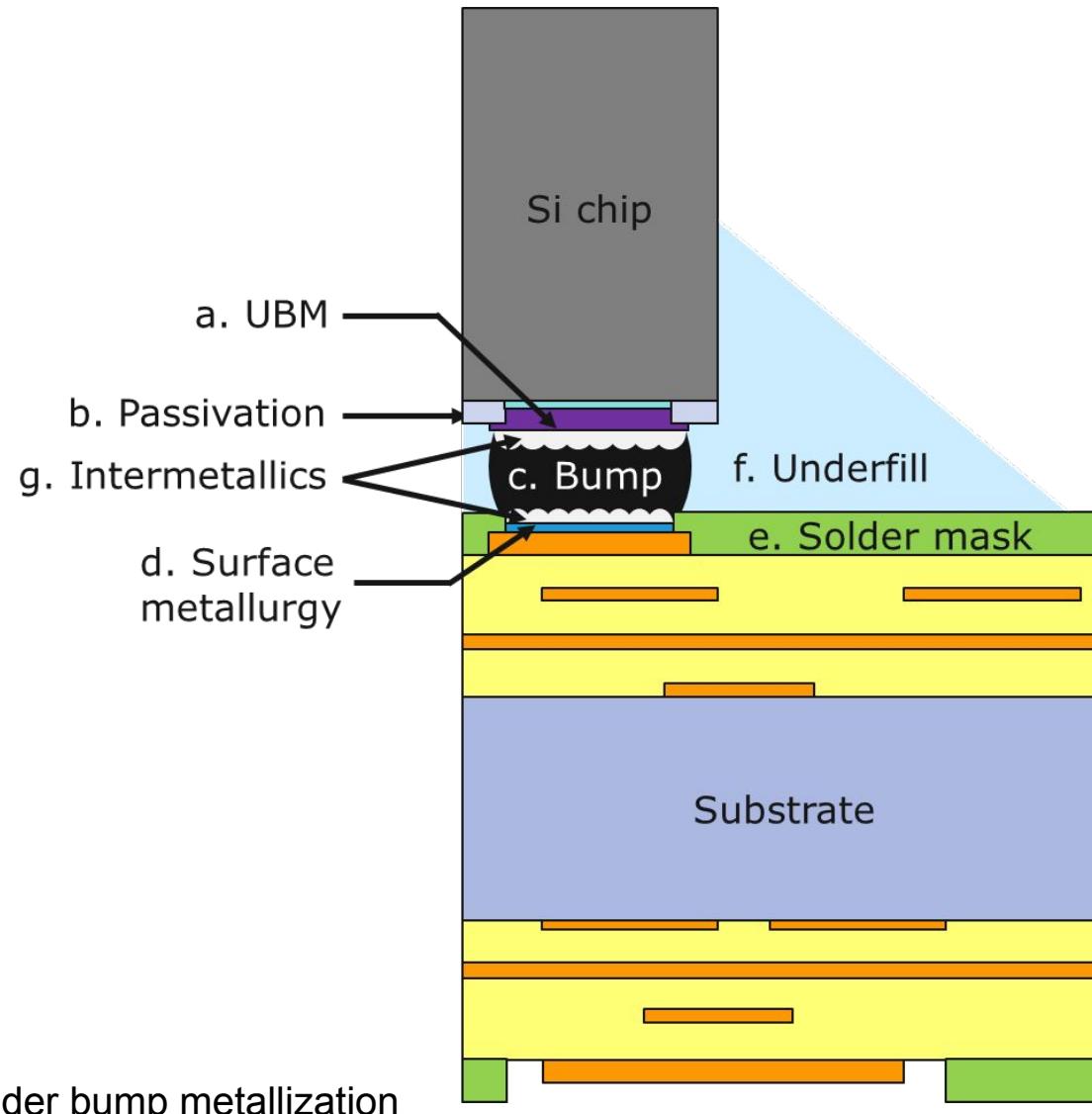
Solder materials: the lead-free transition

- Shift from leaded solder (SnPb eutectic) to lead-free alloys due to Pb toxicity
- Higher melting point → increased warpage and thermal expansion stresses
- Mechanical behavior (i.e. reliability) highly dependent on microstructure



- Favored lead-free solders:
 - Chip level: Sn, SnAg (2.0-3.5 at.% of Ag), SnCu (e.g. Sn0.7Cu), AuSn eutectic (high temp., photonics)
 - Board level: SAC alloys (e.g. SAC105, SAC305, SAC405)

Solder Bump Structure



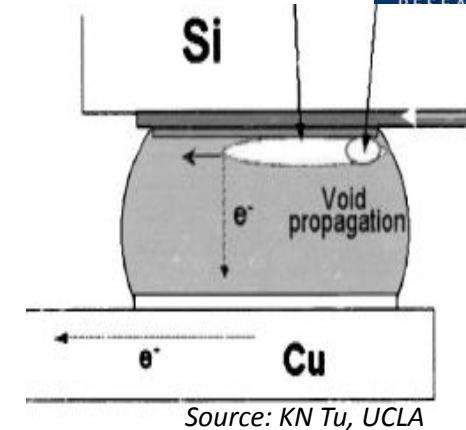
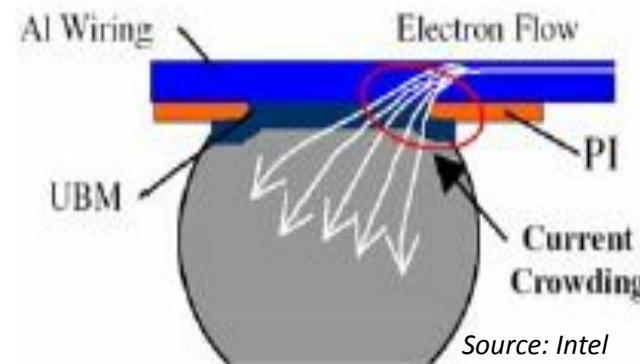
Interconnection system to be designed consists of:

- Bump material
- Reacting interfaces: UBM and surface finish metallurgy

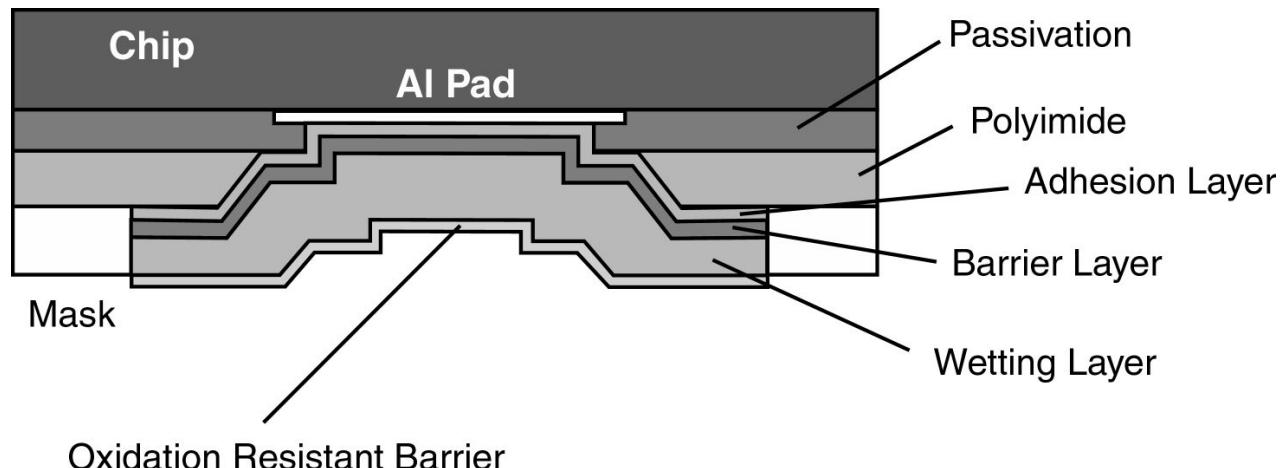
During assembly, the solder melts and reacts with the UBM / surface finish metallurgy to form intermetallic compounds. The reacting interfaces provide a way to control the microstructure, hence physical properties of the joint (e.g. shear strength, long-term reliability)

Need for UBM: Electromigration in Solder

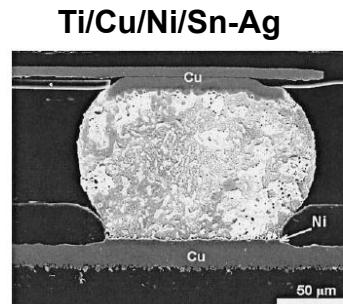
- High current densities heats up the bump
- Enhanced atom flux (diffusion)
- Leads to electromigration-related failures:
 - ❖ Voids
 - ❖ Aggressive intermetallic formation



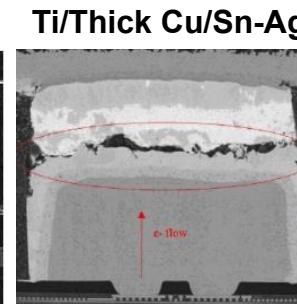
Details of UBM



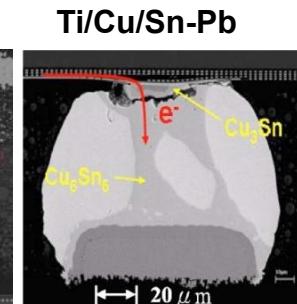
Material-dependent limitations on current carrying capability



Source: Freescale



Source: Intel

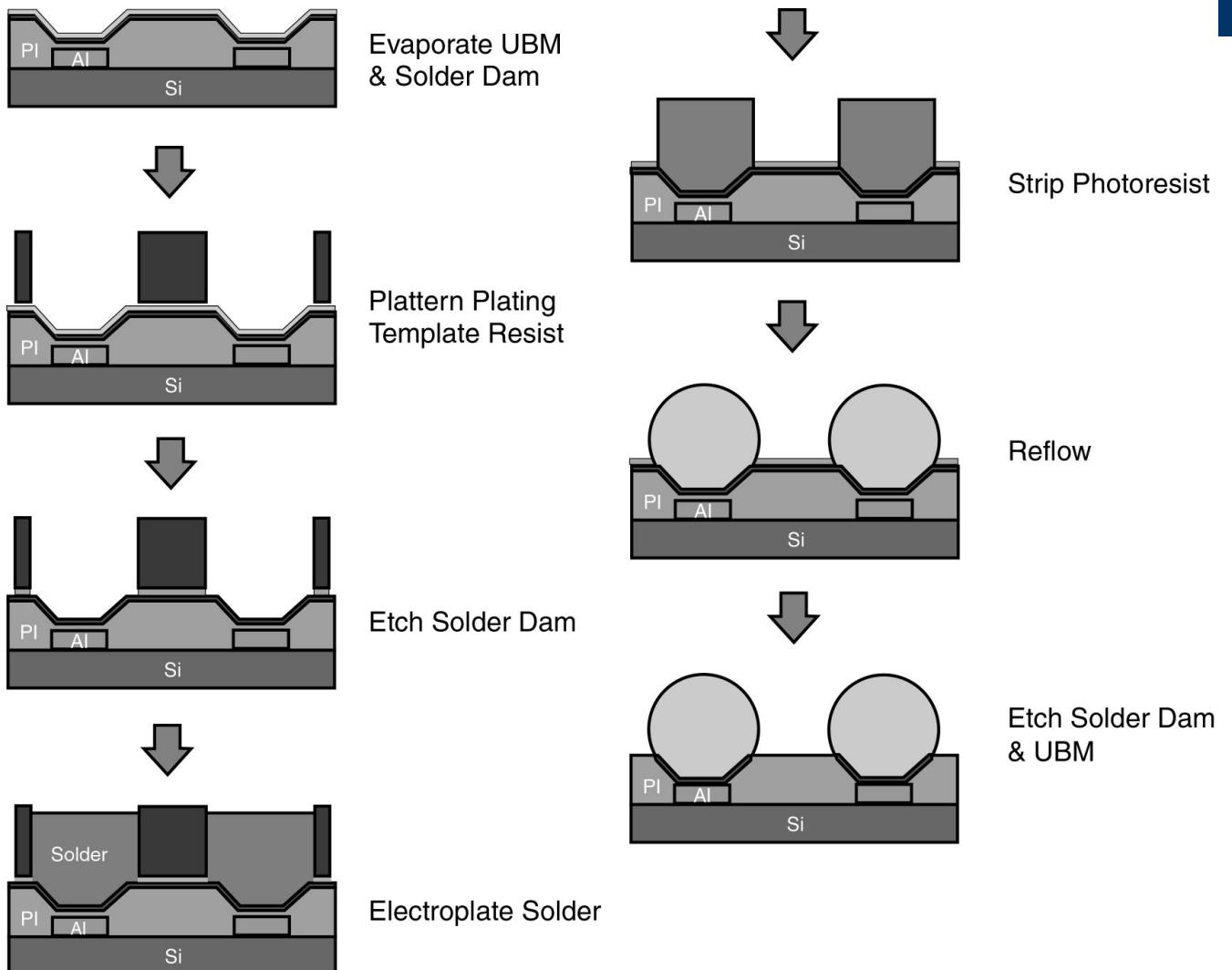


Source: UCLA

With conventional Sn-based solders, current density $< 0.5 \times 10^4 \text{ A/cm}^2$

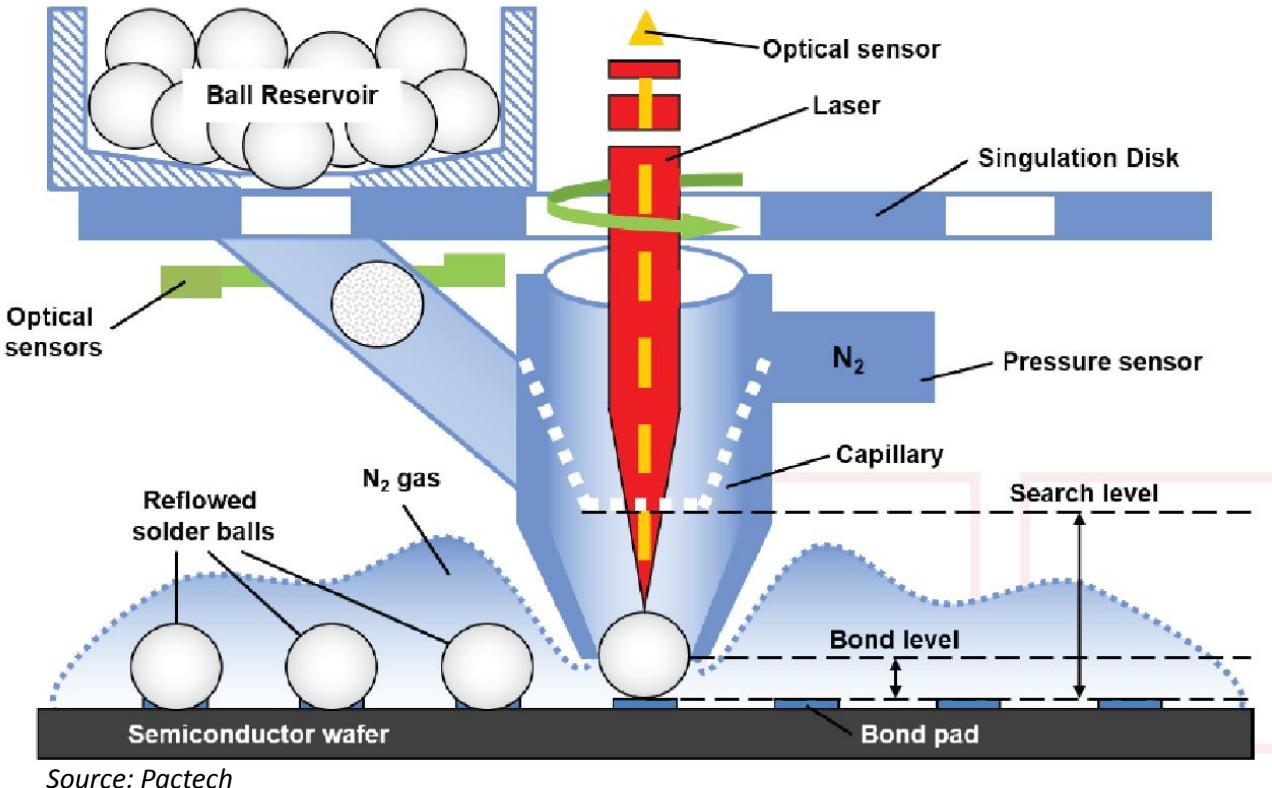
Wafer bumping by electrodeposition (main)

- Semi-additive processing
- Fine feature capability
- Limited to binary alloys (SnAg, SnCu)
 - stack plating possible for ternary alloys or more complex stack-ups



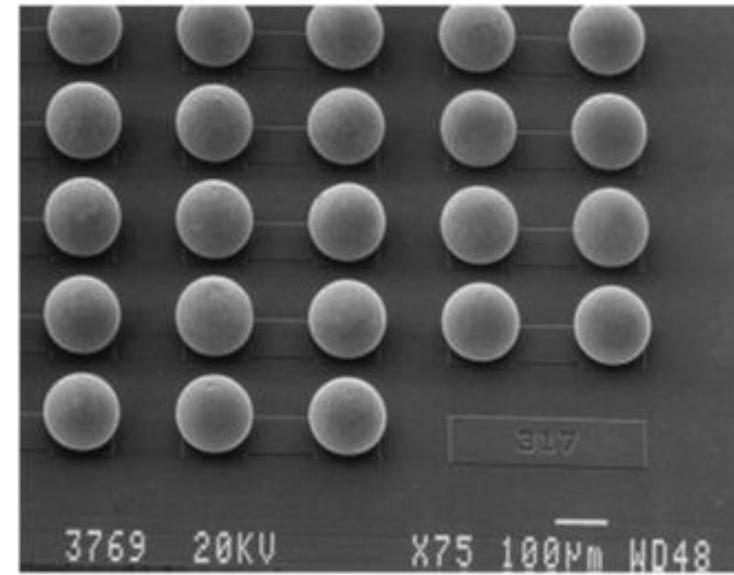
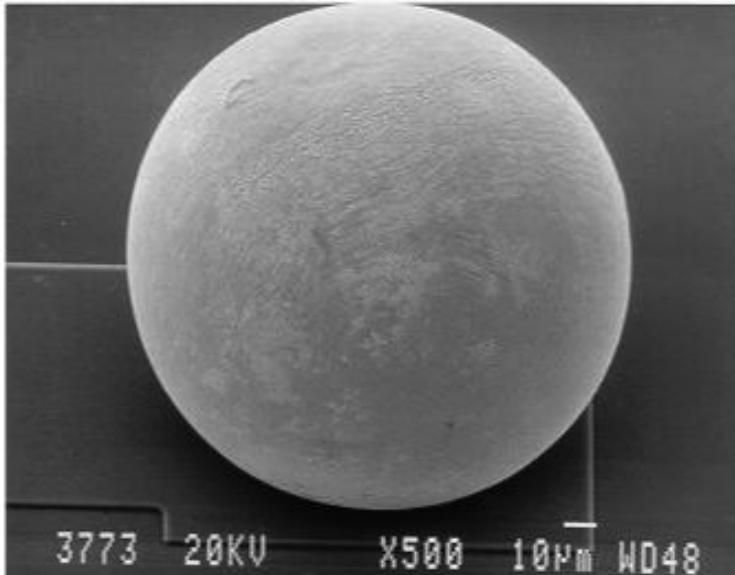
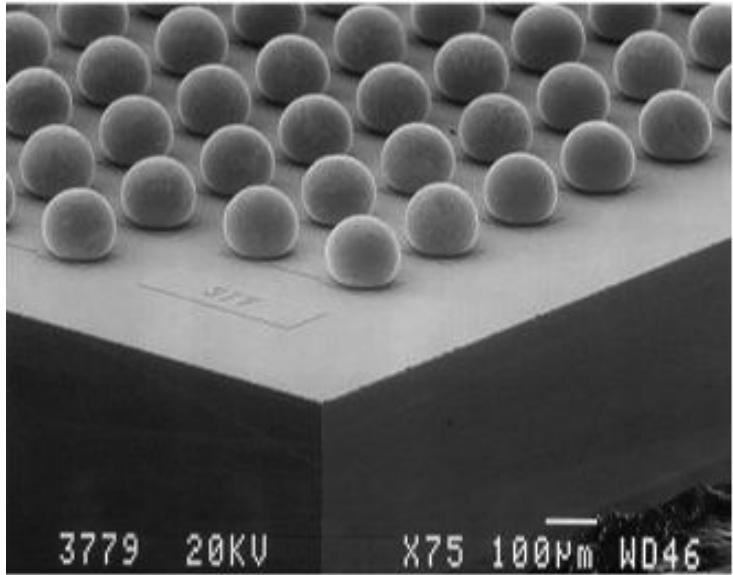
Wafer bumping by solder jetting (low volume)

- Flexible solder ball placement and laser reflow
- Flexibility in solder alloy
- Pitches down to 80 μm



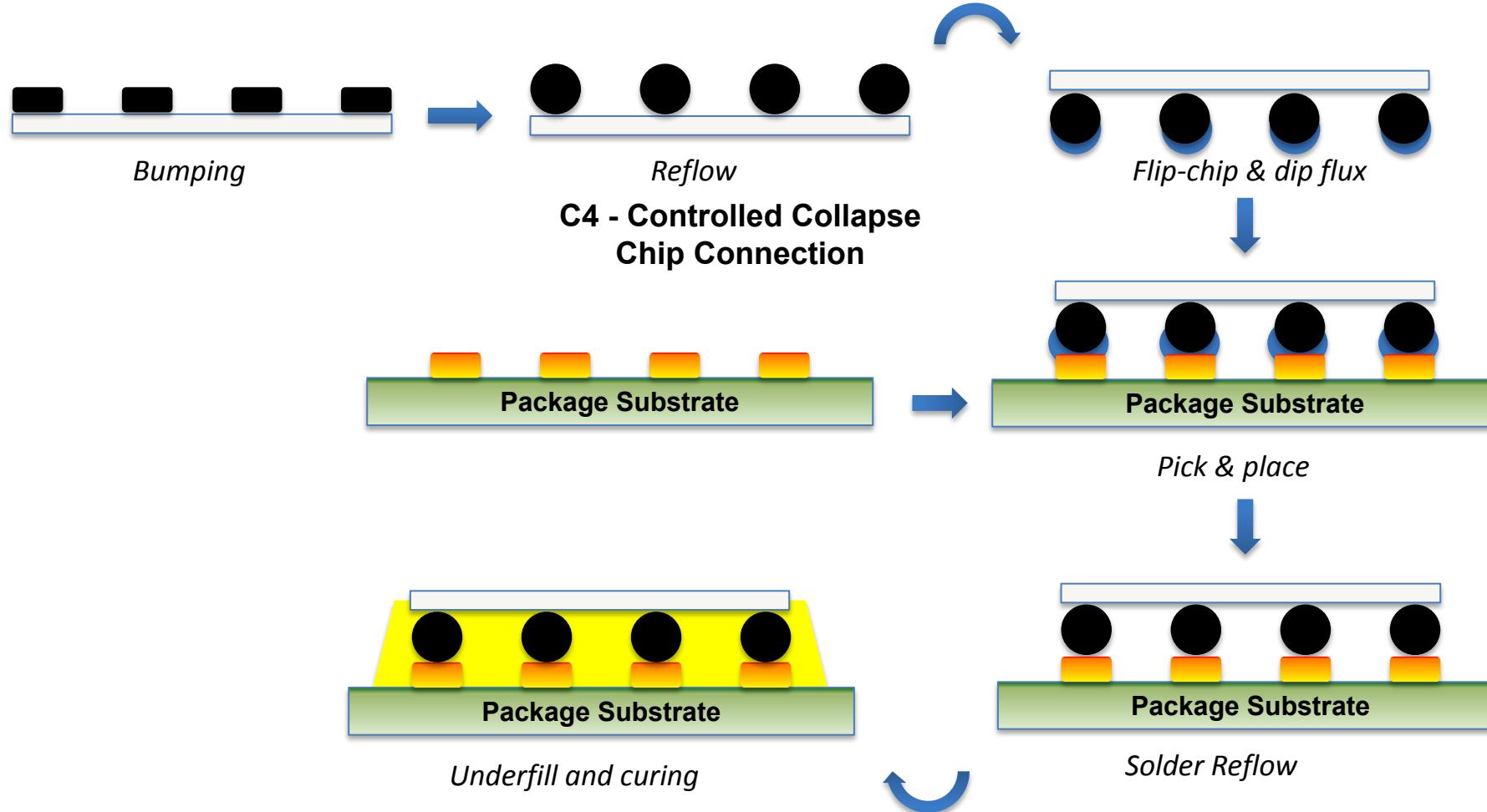
Source: Pactech

Typical area array solder bumps on chip

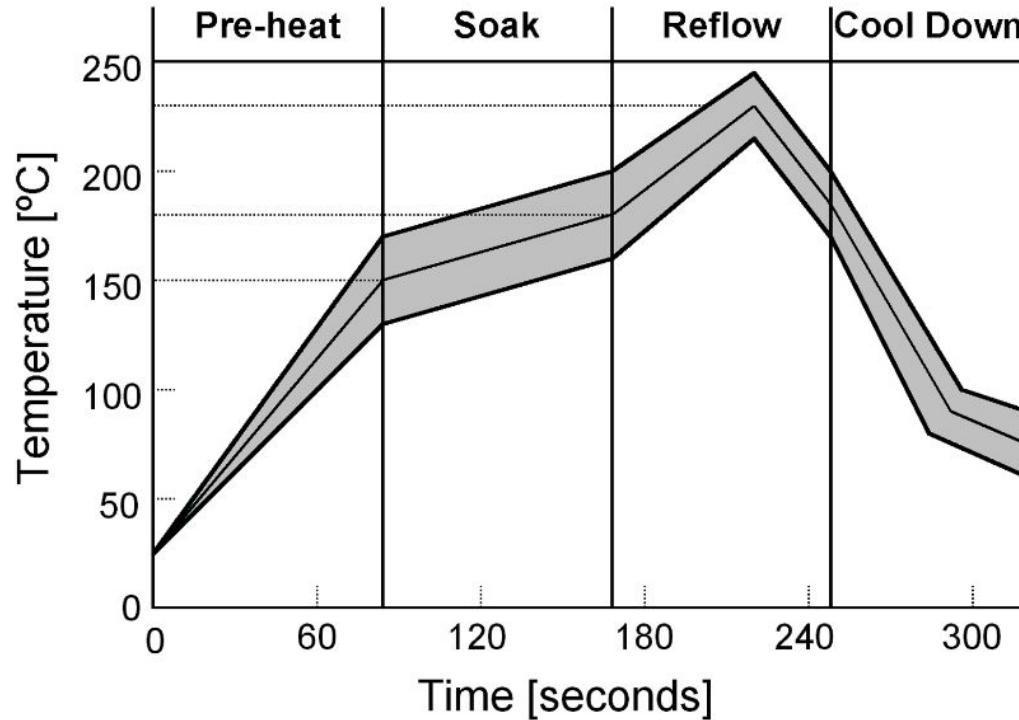


Flip-chip bonding with solder bumps

Chip-level flip-chip process with solder-based C4 bumps



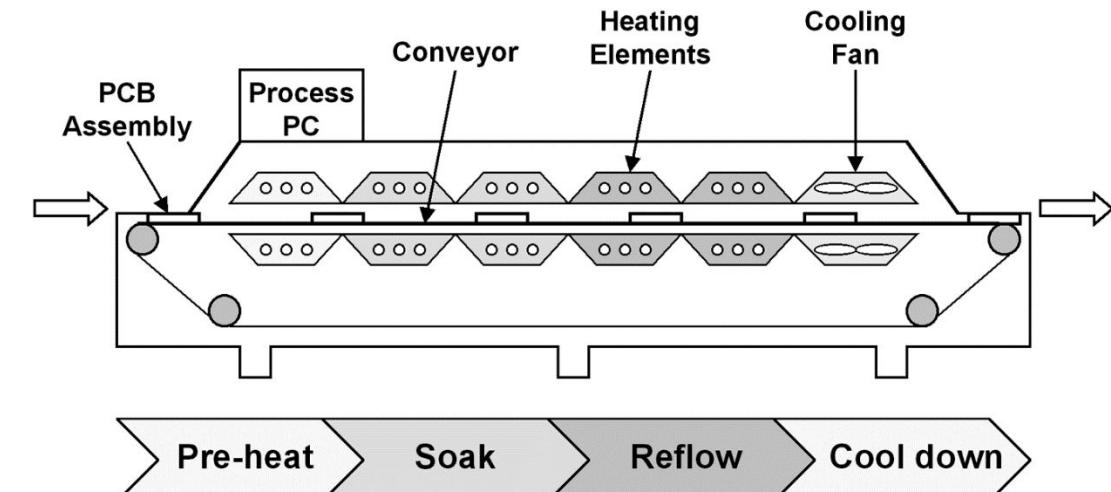
Reflow process



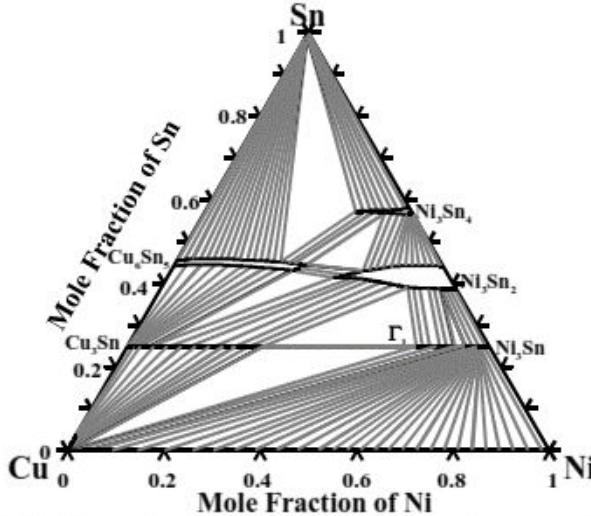
Guide to optimize reflow profile: "Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP and Flip Chip Technologies", Ning-Cheng Lee, Indium Corp.



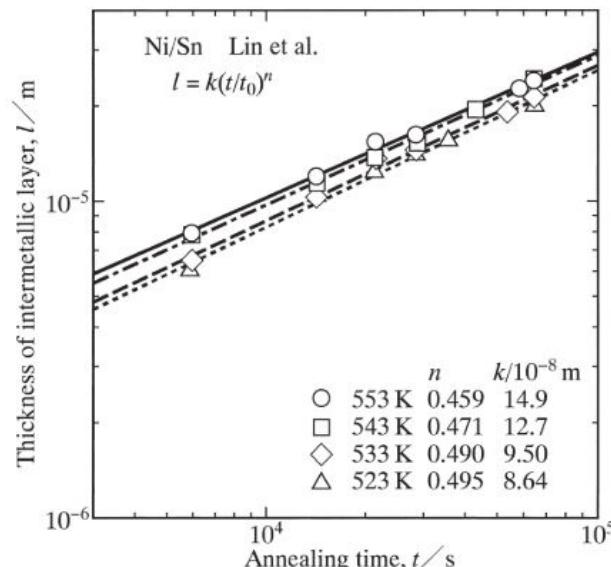
- Assembly is heated in oven above solder liquidus temperature and cooled to attach components to the package
 - ❖ Time above liquidus to be controlled – IMC growth
 - ❖ Cool down affects IMC growth, distribution and grain size, along with thermal expansion stresses
- With conventional SnAgCu alloys, melting points in 215-230°C range → peak temperature ~250°C



Interfacial reactions during reflow



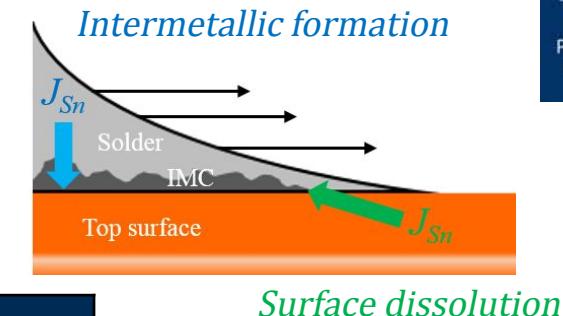
Example of phase diagram: Cu-Ni-Sn system



- Solder reacts with UBM and surface finish metallurgies to form IMCs, primarily during time above liquidus (TAL)
- Microstructure controls joint properties and reliability!!
- Intermetallic compounds continue to grow through both liquid- and solid-state diffusion: all process steps / normal conditions of use to be accounted for in design of interconnection system
- Design of interconnection stack-up:** use phase diagram and empirical diffusion models to calculate intermetallic thickness. Based on mass conservation and atomic percentage of key elements (e.g. Sn, Ni, Cu) in the expected IMCs, back calculate thickness of solder / surface finish metallurgy consumed

Surface finish metallurgy on substrate pads

- **Wetting** (surface dissolution): ImAg > ENIG > HASL > ImSn > OSP
- **Joint strength** (intermetallic thickness): OSP > HASL > ImAg > ImSn > ENIG



	ENIG	ENEPIG	Cu-OSP	ImSn
Advantages	<ul style="list-style-type: none"> • Ideal wettability • High bonding strength and reliability 	<ul style="list-style-type: none"> • Ideal wettability • Improved reliability than ENIG 	<ul style="list-style-type: none"> • Pitch scalability • Low cost • High drop test reliability 	<ul style="list-style-type: none"> • High as-deposited wettability • Low cost
Limitations	<ul style="list-style-type: none"> • Hyperactive corrosion • Pitch scalability • Dimensional accuracy • High insertion loss 	<ul style="list-style-type: none"> • Brittle interface with limited solder • Pitch scalability • Dimensional accuracy • High insertion loss 	<ul style="list-style-type: none"> • Incompatibility to TC-NCP process • Lack of barrier layer 	<ul style="list-style-type: none"> • Surface oxidation • Thermal stability • Tin whisker growth

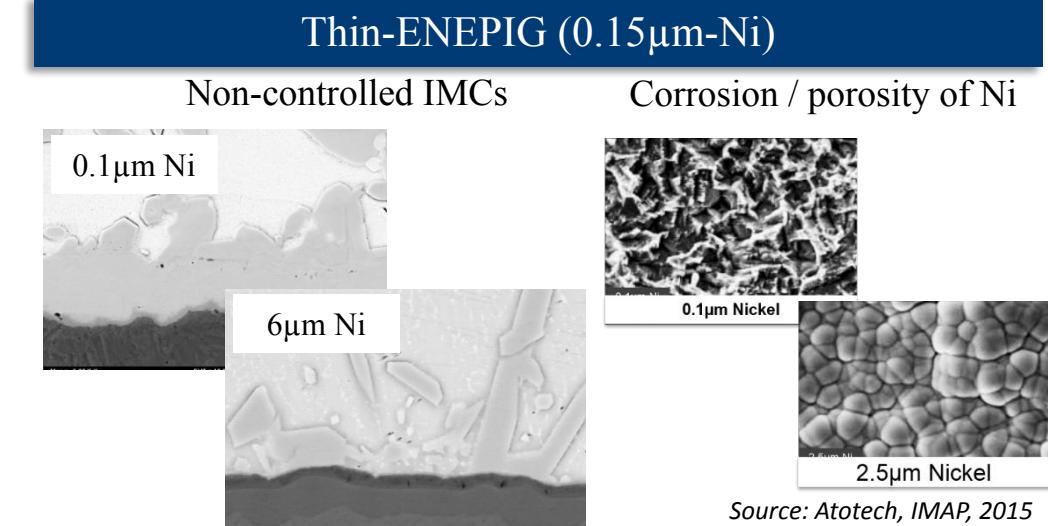
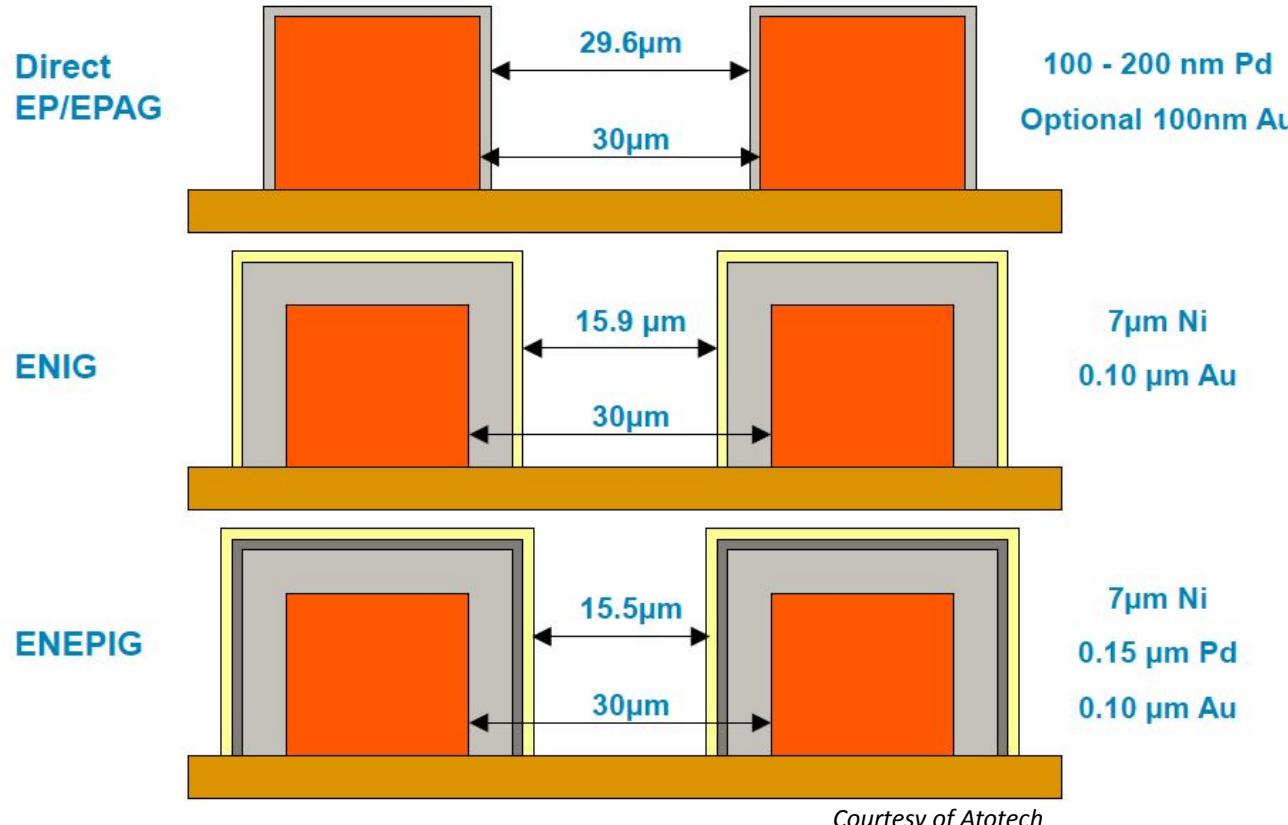
Popular in HPC

Popular in Mobile

ImAg: Immersion Ag
 ENIG: Electroless Ni, Immersion Au
 HASL: Hot Air Solder Leveling
 ImSn: Immersion Sn
 OSP: Organic Solderability Preservative
 EP: Electroless Pd
 EPAG: Electroless Pd, Autocatalytic Au

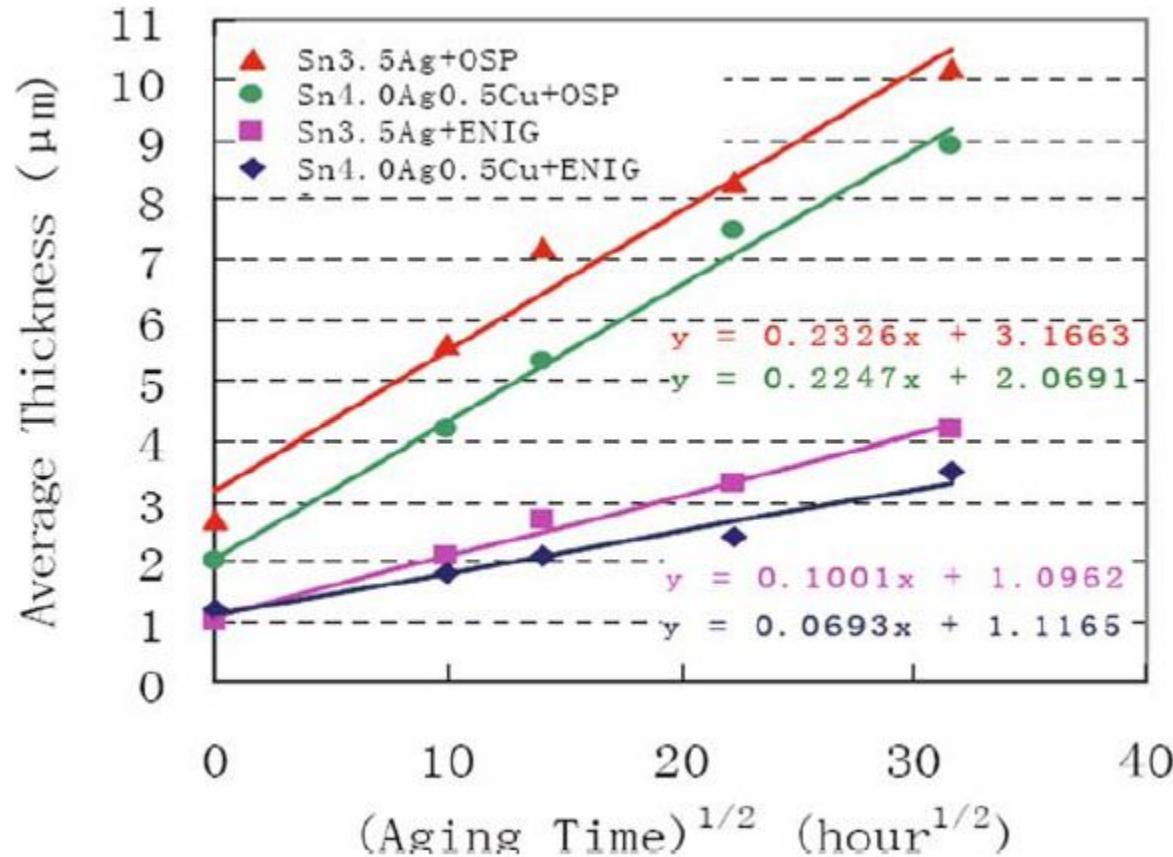
Scalability of surface finish metallurgies

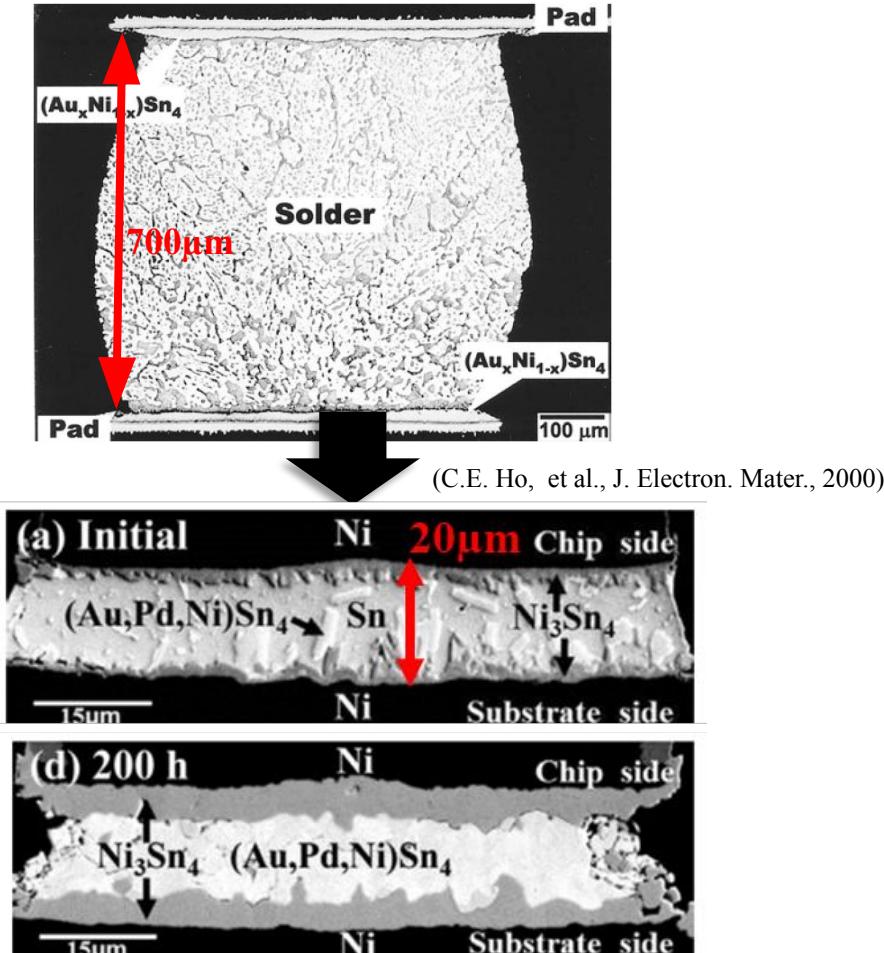
- Limited scalability of ENIG / ENEPIG to high-density RDL



Intermetallic growth with surface finish

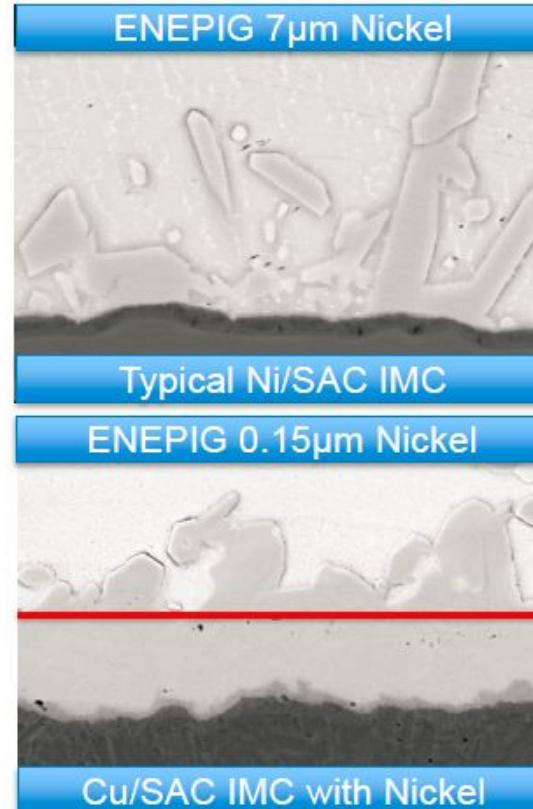
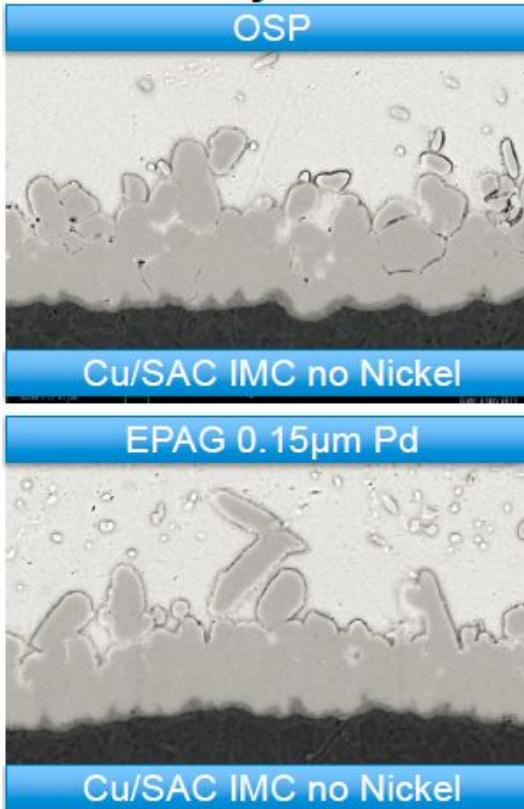
- Diffusion barrier layers such as Ni are great tools to control IMC growth
- With pitch scaling, Au/Pd embrittlement becomes a critical challenge



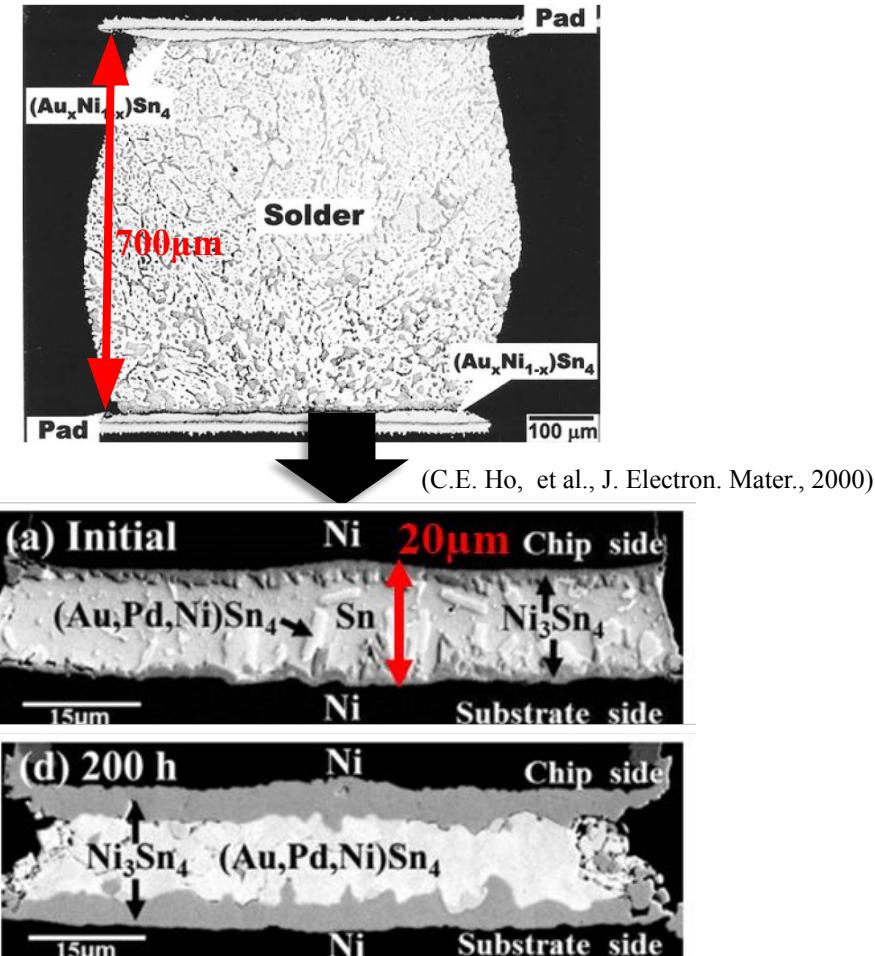


Intermetallic growth with surface finish

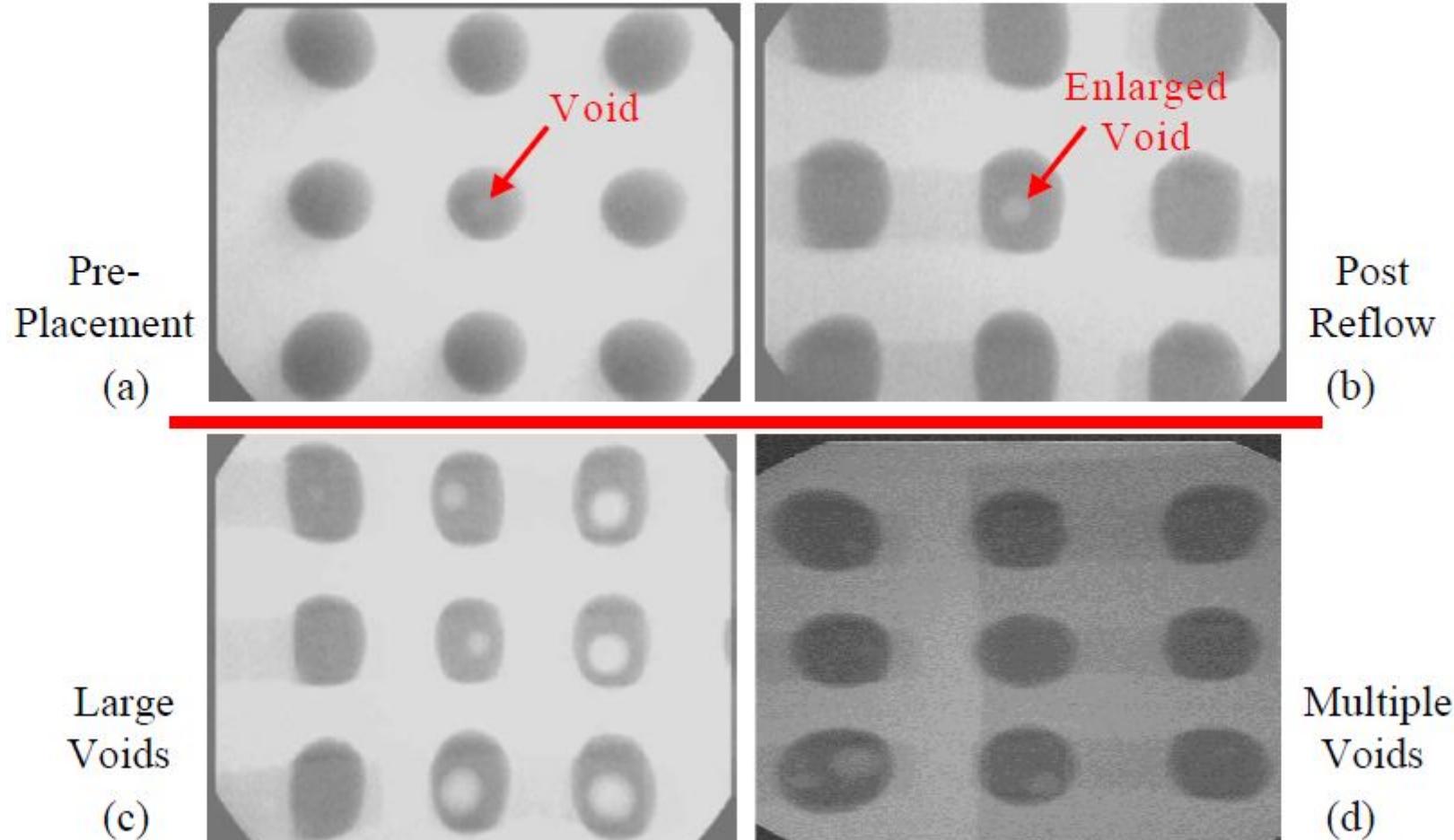
- Diffusion barrier layers such as Ni are great tools to control IMC growth
- With pitch scaling, Au/Pd embrittlement becomes a critical challenge



Demarcation
Line



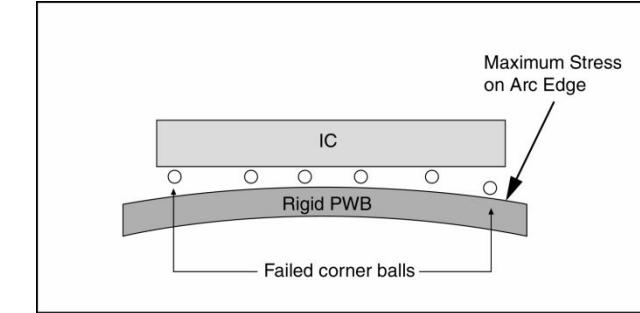
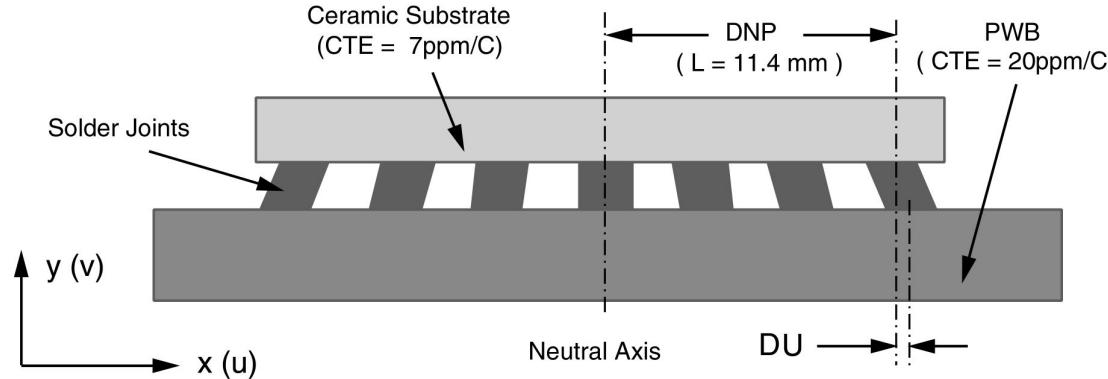
X-Ray characterization: voiding, alignment, shorting defects



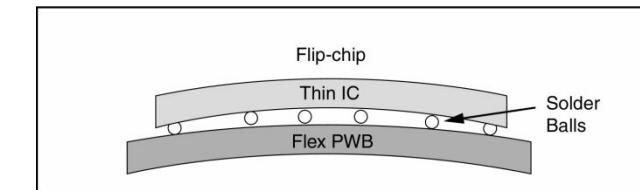
CTE-mismatch induced stress-strain in solders

Substrate warpage

**CTE mismatch: maximum shear strain is related
to: $DNP \times \Delta\alpha \times \Delta T/h$**



a) Rigid

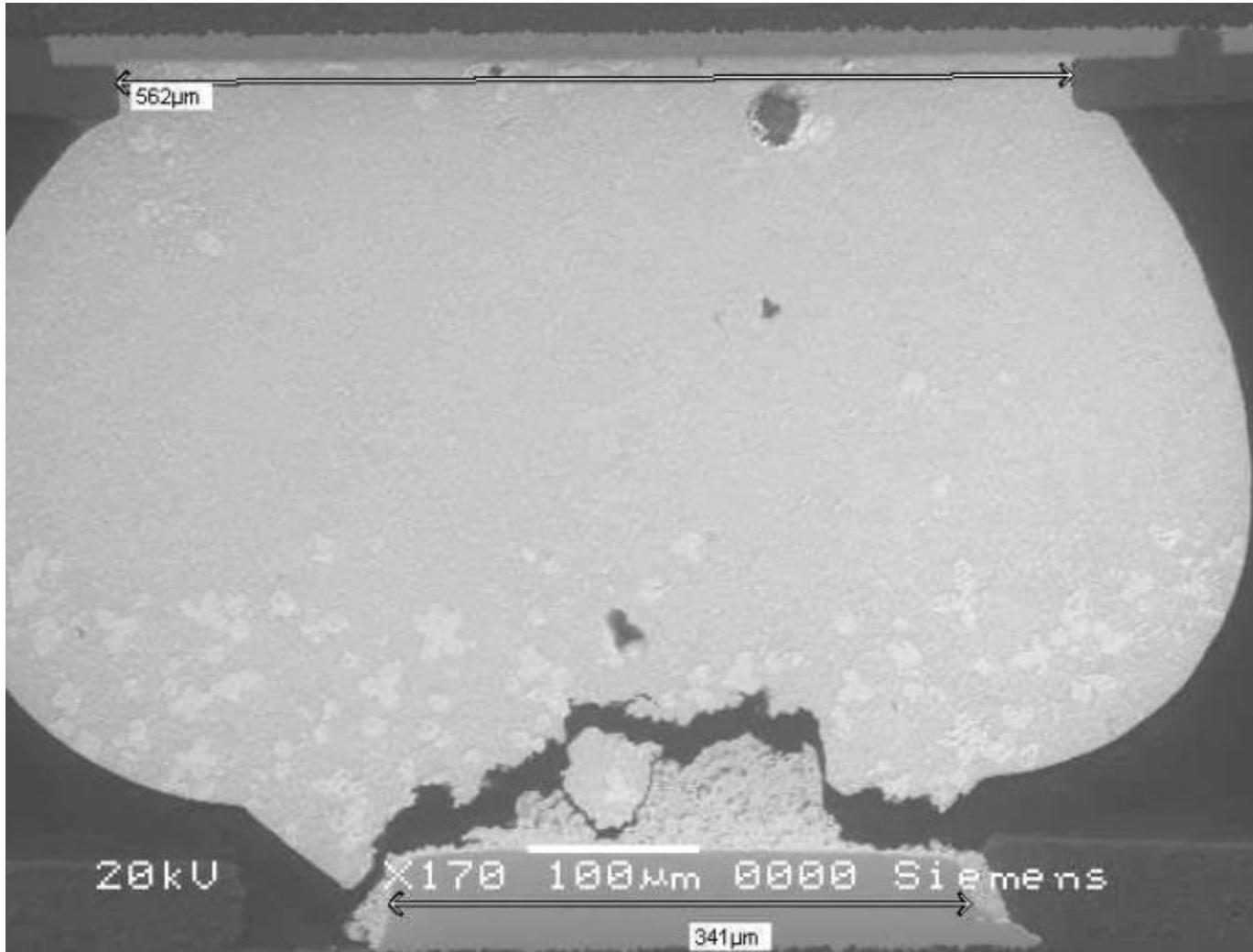


b) Thin or Compliant

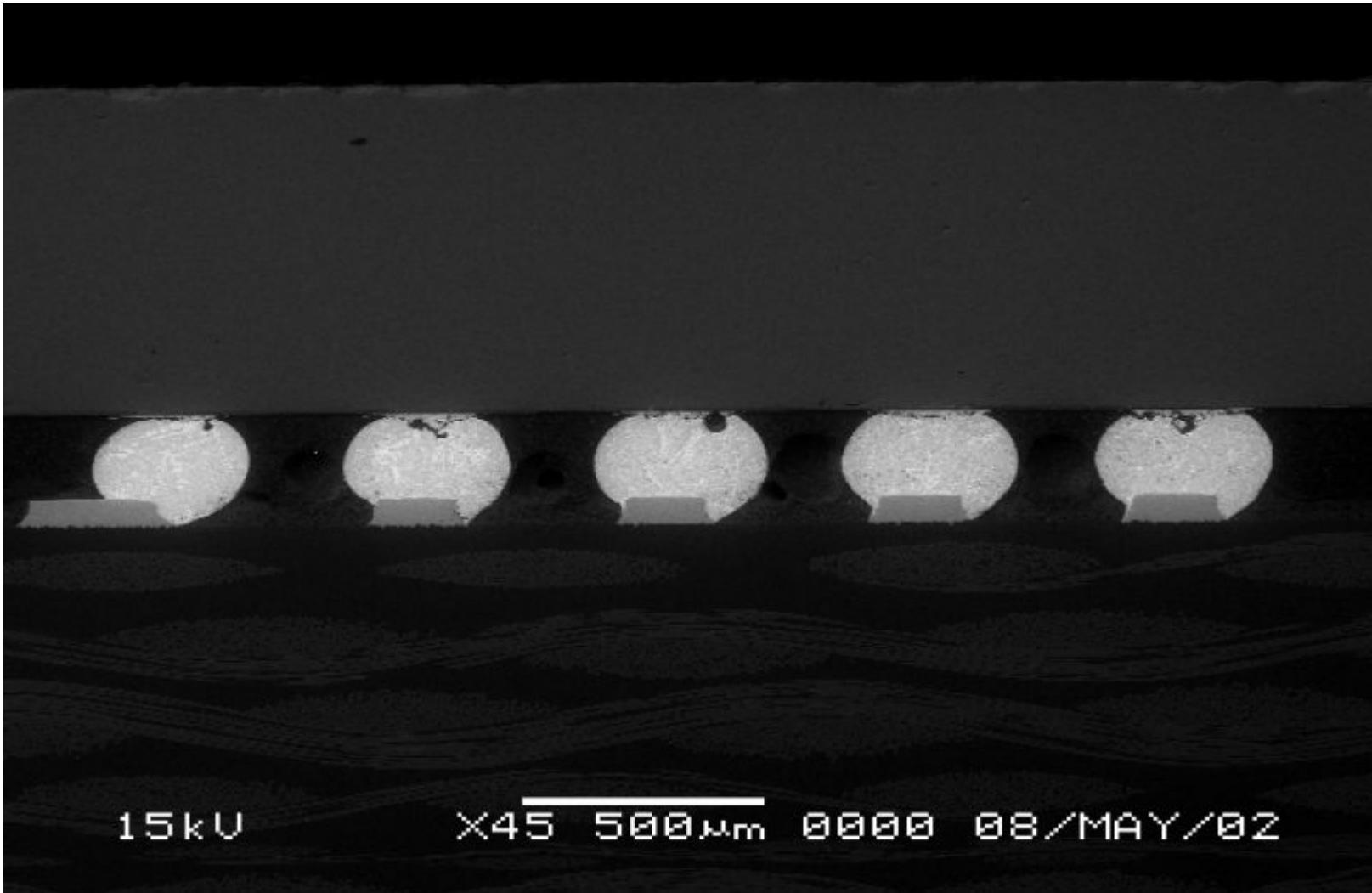
- CTE mismatch between chip and substrate causes stresses and strains in solders (lateral displacement)
- Solders undergo thermomechanical fatigue due to thermal cycling (viscoplastic behavior – time-dependent plasticity)

→ **Reliability concern!!!!** even more so as die size increases, while pitch & standoff height decrease

SEM: cold cracking due to warpage

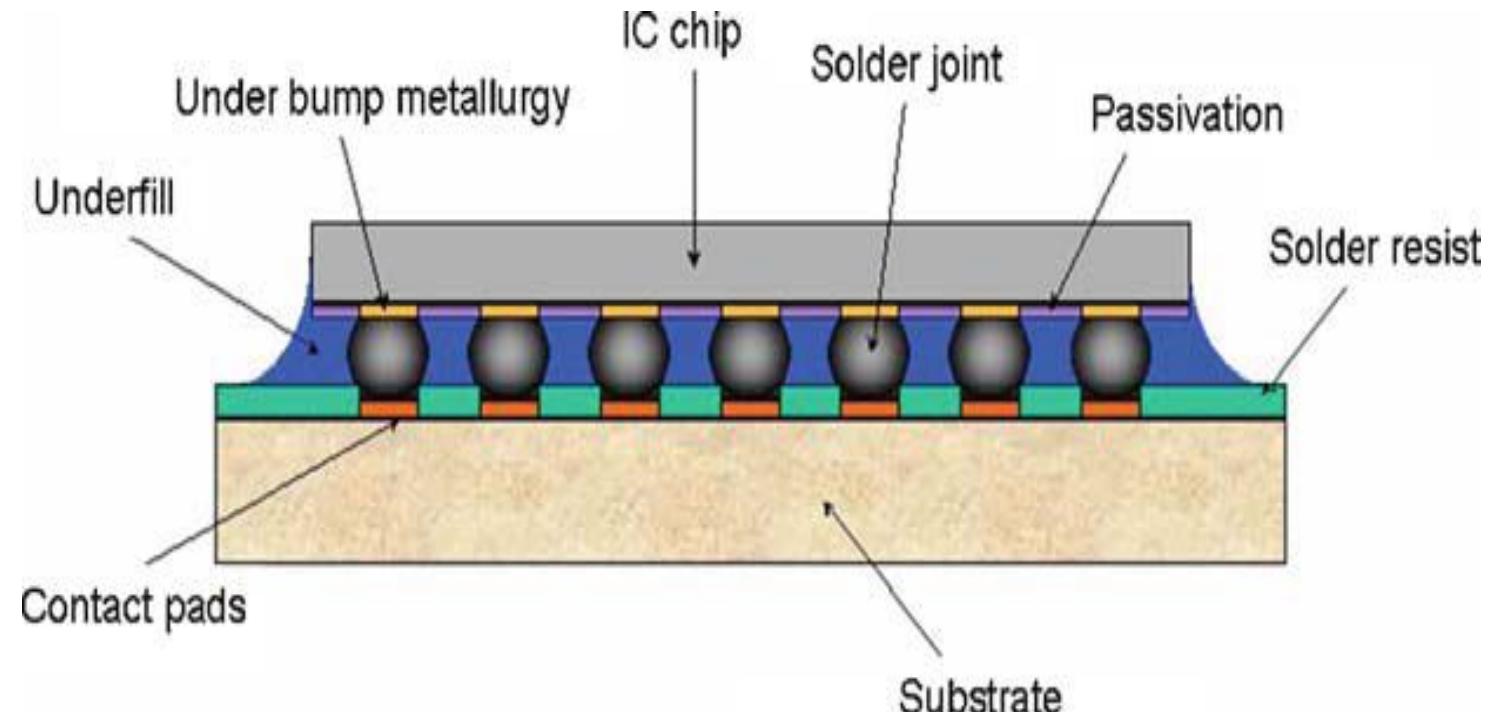


SEM: solder cracking due to fatigue

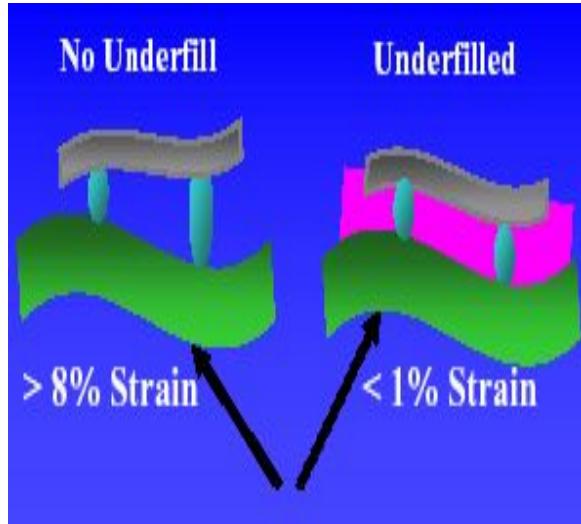


Underfill to enhance thermomechanical reliability

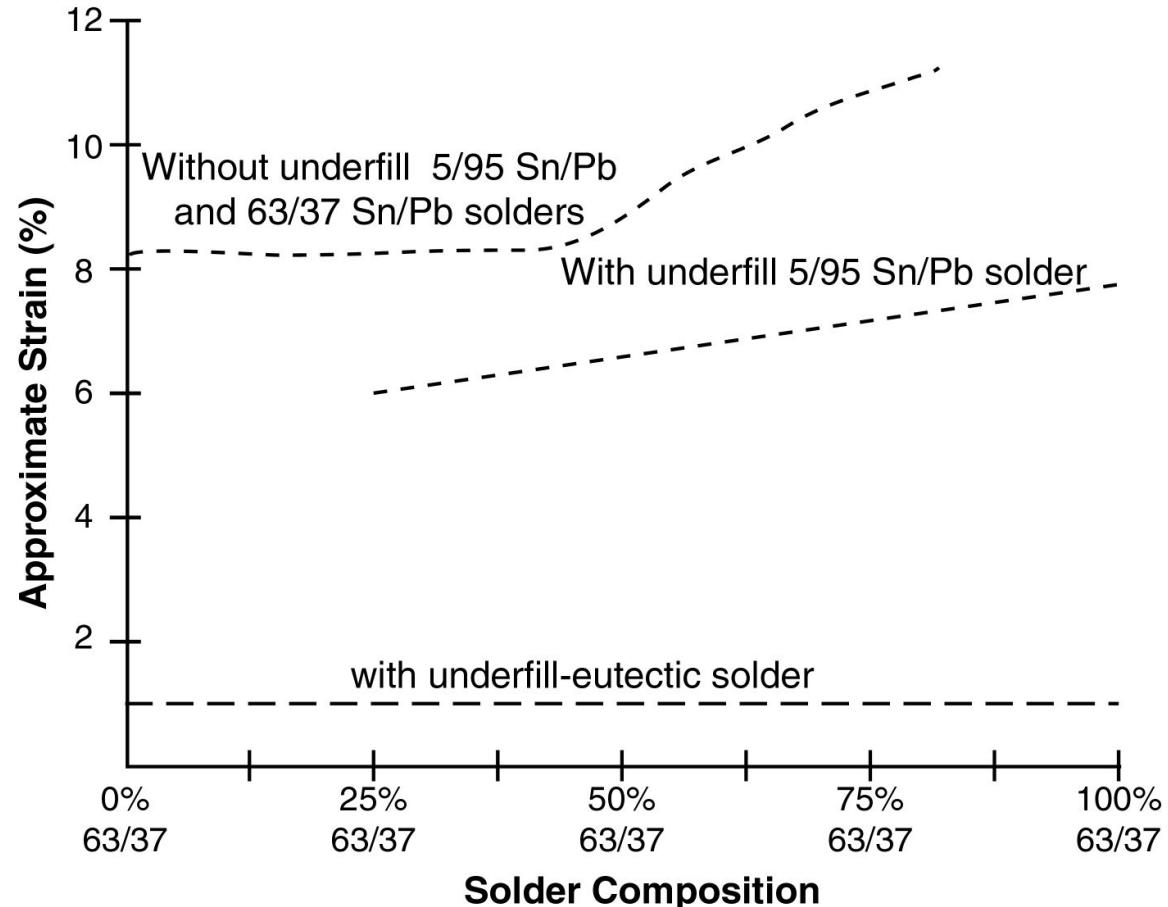
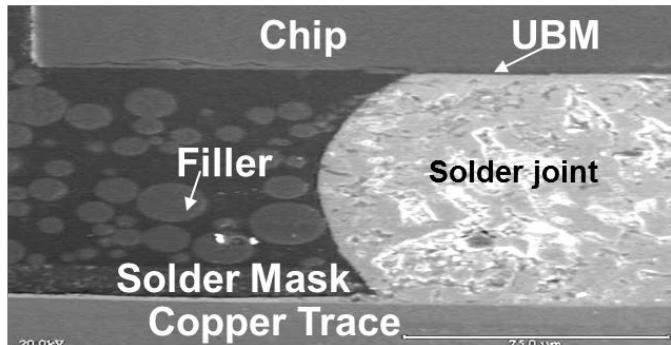
- Underfill encapsulants protect solder joints and the active surface of dies
- To prevent damage to the solder bumps due to CTE mismatch, epoxy-based materials are used to fill in the gap between the flipped chip and the substrate



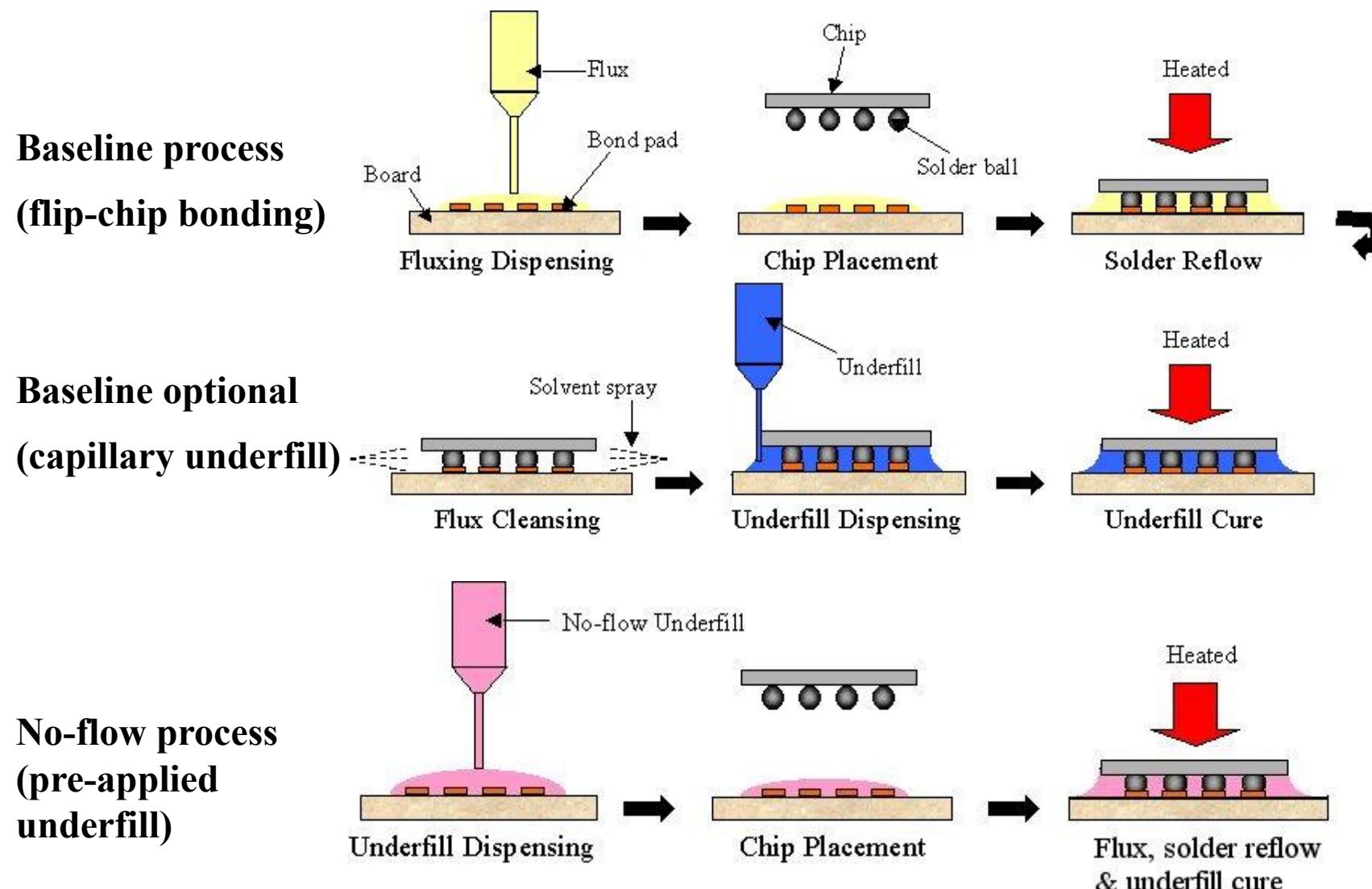
Strain reduction in solders with underfill



Underfill with silica fillers: low CTE and high modulus

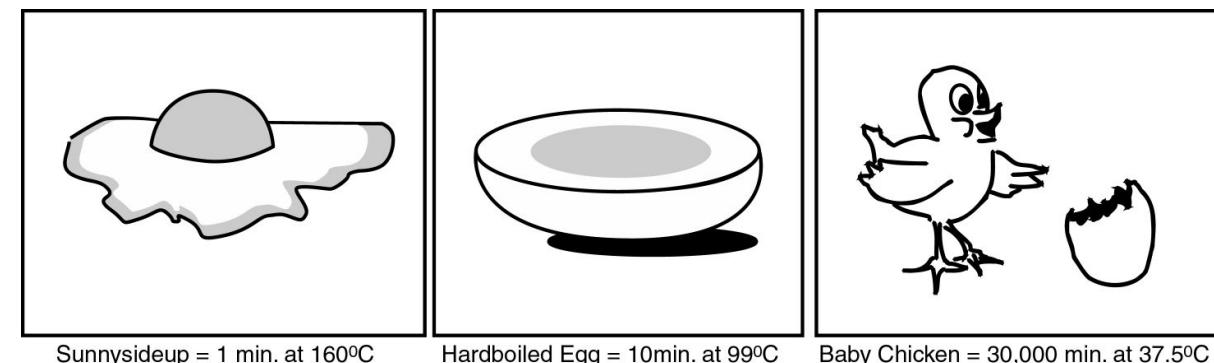


Underfill types & dispense process



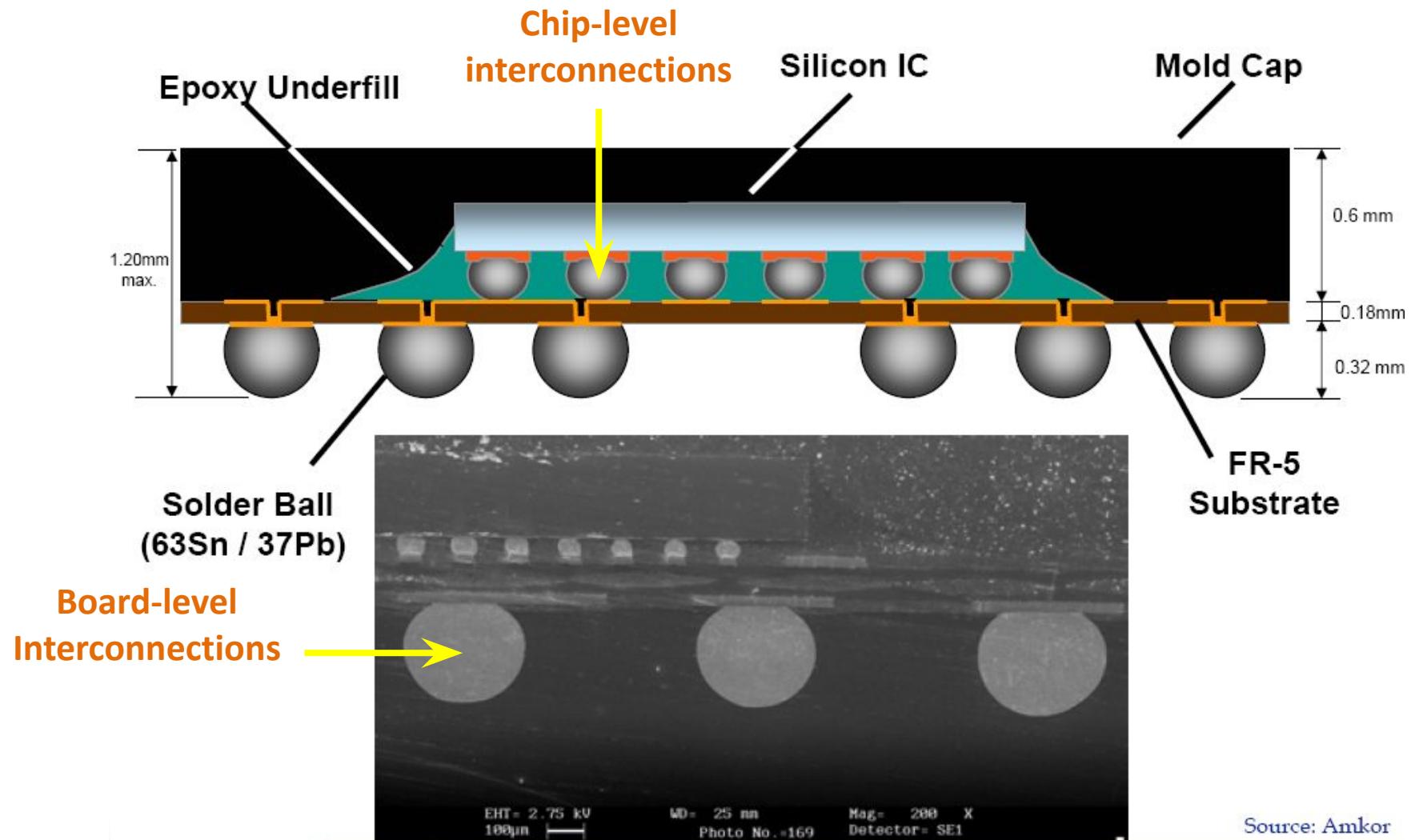
Reliability Characterization

- Accelerated life testing – environmental stress tests
 - ❖ A reliability test where one or more stress conditions are used to reduce the required time to failure
 - ❖ Intent of the test is to accelerate a given physical mechanism without introducing new failure mechanisms that would not occur in the use environment
 - ❖ Standard test conditions defined by common standards (JEDEC, ISO, AEC ...)
- Examples of reliability tests:
 - ❖ Temperature cycling: thermal cycling test (TCT)
 - ❖ High-temperature storage
 - ❖ Highly accelerated stress test (HAST)
 - ❖ Electromigration (EM)
- Failure analysis performed after test to determine the predominant failure modes and fundamental failure mechanisms



Finite element modeling (e.g. thermomechanical analysis) is a great tool to design interconnection system and assembly process for reliability

Flip-chip package cross-section



Source: Amkor

Advantages of flip-chip bonding

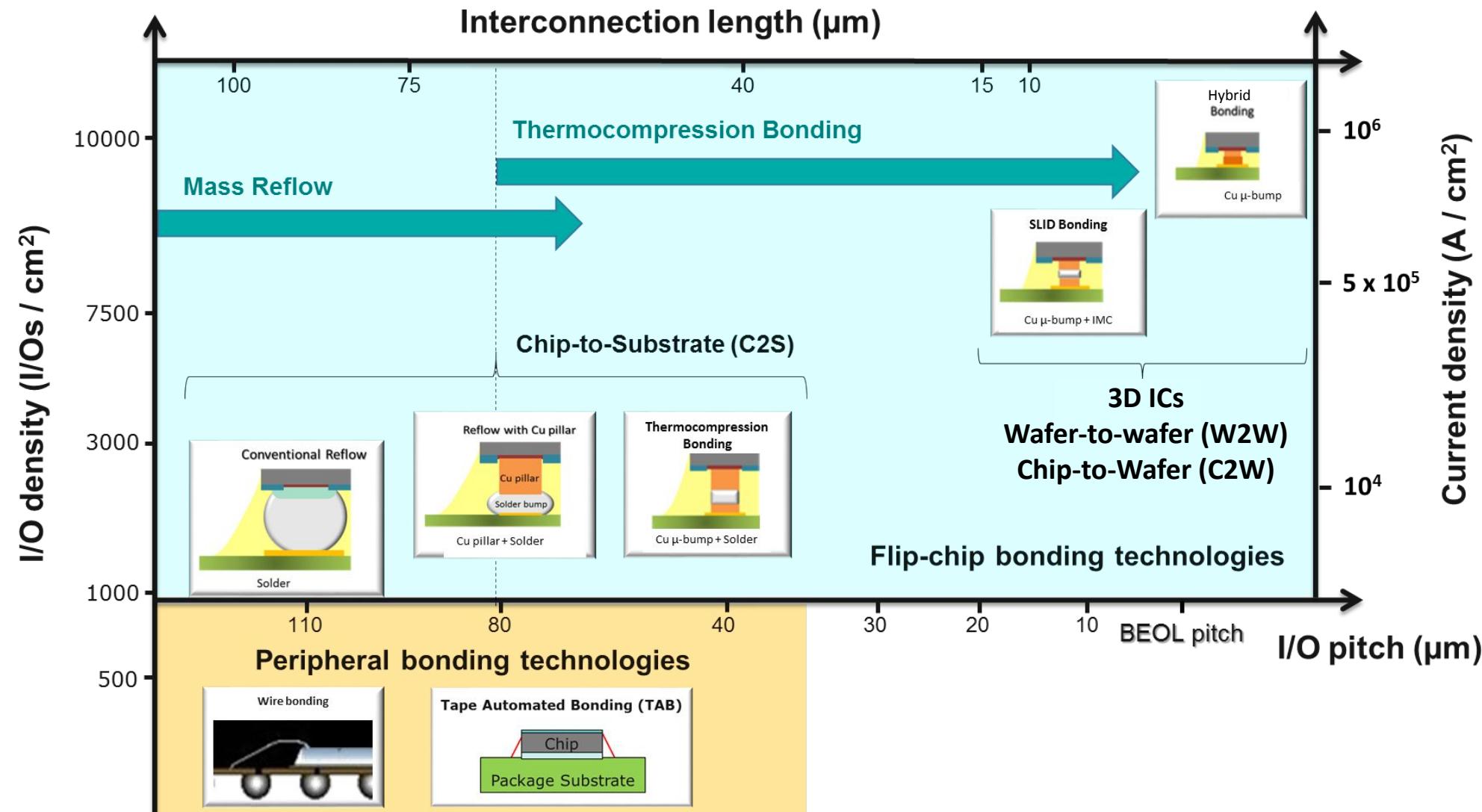
- Electrical – parasitics R, L
- Size – Footprint
- Thermal – Heat dissipation
- Increased functional density
- Lower cost in high volume manufacturing
- Self alignment (with solder reflow)
- Ability to use conductive adhesives
- Current carrying capacity of bumps
- Reworkability to some extent

Challenges of flip-chip bonding



- Reliability – joint microstructure (e.g. intermetallics, unreacted solder volume)
- Reliability – CTE-mismatch induced solder fatigue
- Alignment and cost with smaller pitches on high-density substrates
- Underfill process
- Industry infrastructure

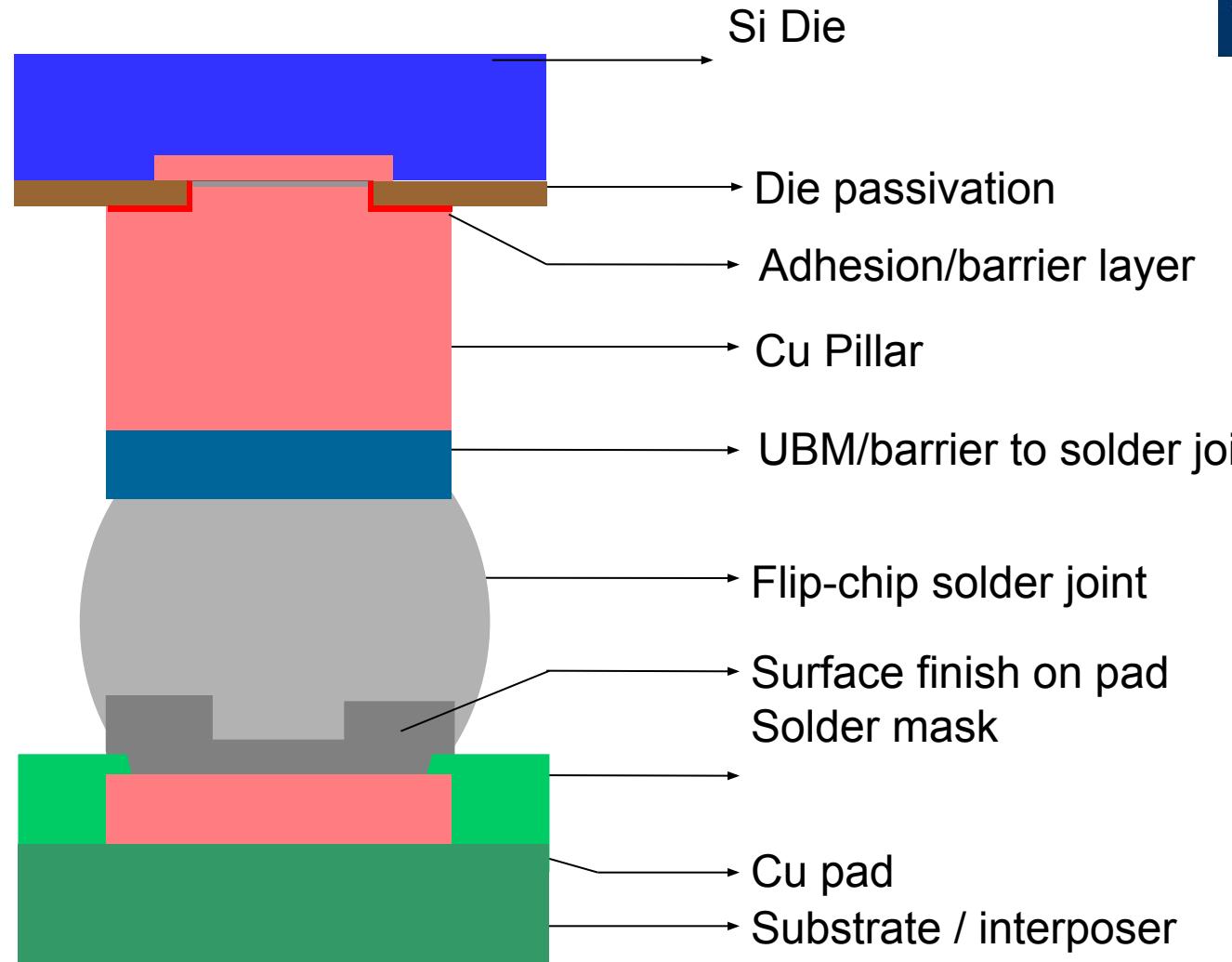
Technology roadmap



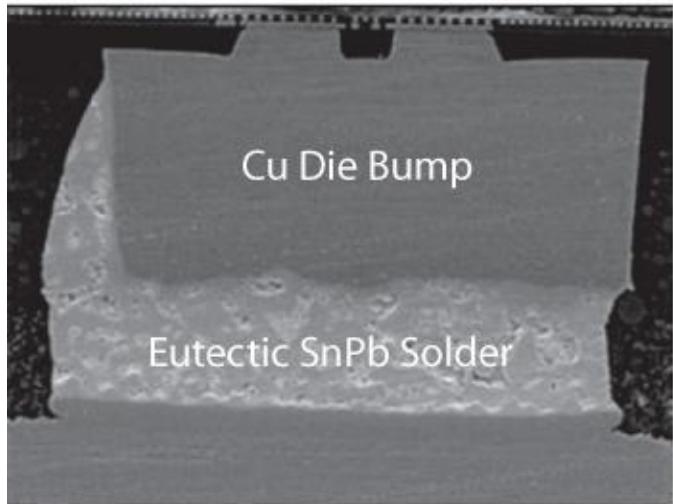
Pitch scaling with solders: the Cu pillar technology

Pitch scaling is accompanied by a reduction in solder volume

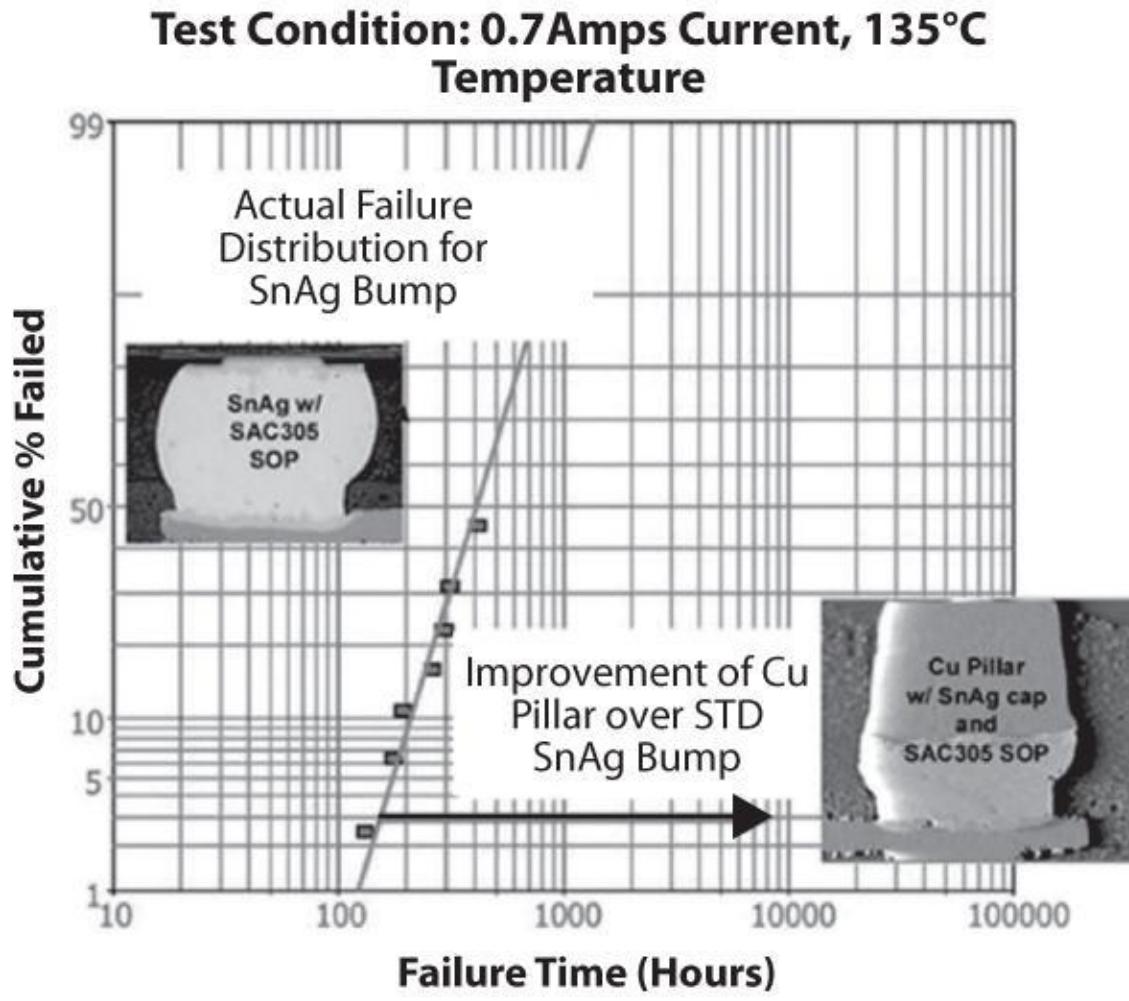
- ❖ Cu pillar introduced to increase standoff height
- ❖ Shift from reflow to thermocompression bonding (TC-NCP)
- ❖ Finer control of reaction required



Improved electromigration performance with Cu pillars



(a)

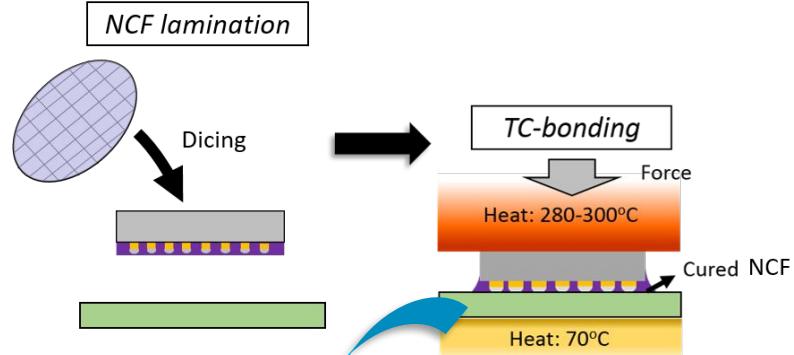


(b)

Shift to thermocompression (TC) bonding

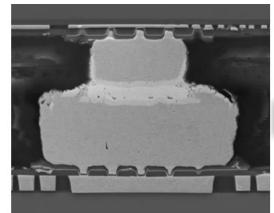
Reaction control at fine pitch

TC-bonding with wafer-level underfill



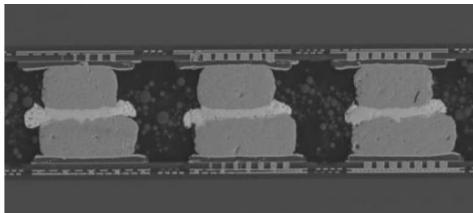
40µm pitch (TC-NCP)

(Chip-to-substrate)



20µm pitch (TC-NCE)

(3D-ICs)

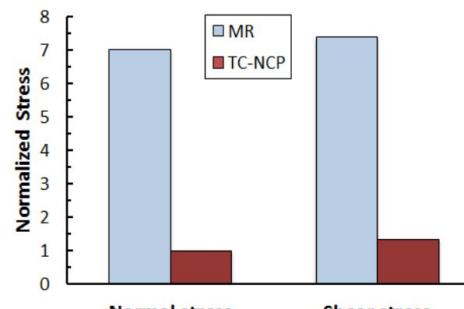


(IMEC, IMAPS, 2016)

Localized heating for
CTE-mismatched architecture

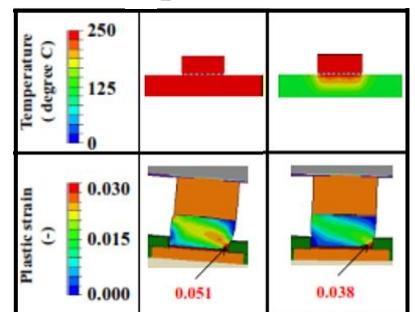
Improved stress management

ULK cracking

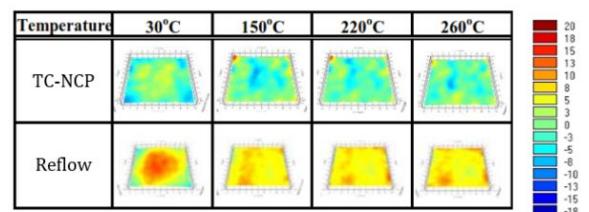


(Global Foundry: J.K. Cho , ECTC, 2015)

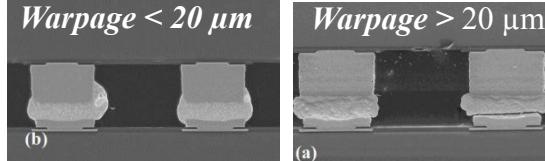
Solder plastic strain



Warpage



Warpage < 20 µm



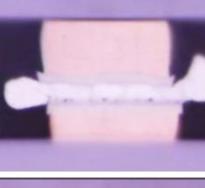
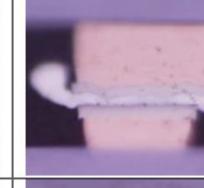
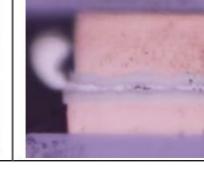
(Invensas: L. Wang, IMAP, 2014)

Throughput improvements

- Assembly throughput: **TC-NCP < 1,000 UPH** vs. **> 40,000 UPH** for mass reflow

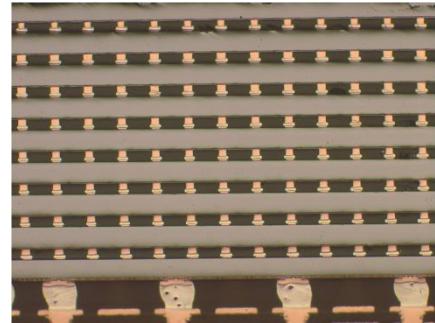
Gang bonding with 8-dies

(Qualcomm/Amkor, 2015)

Die	40um Pitch	80um Pitch
Large Die (6x10)		
Small Die (4x10)		

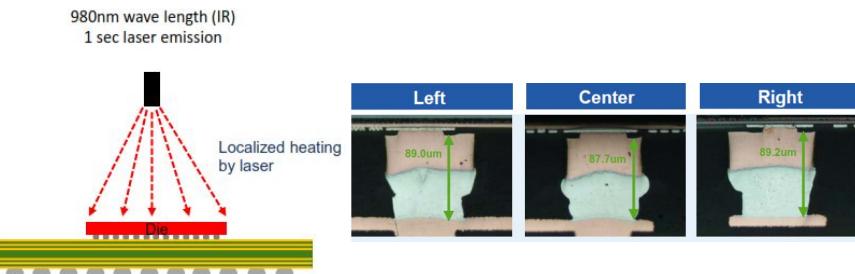
Collective bonding of 7 memory dies with 350°C peak temp.

(K&S, 2015)



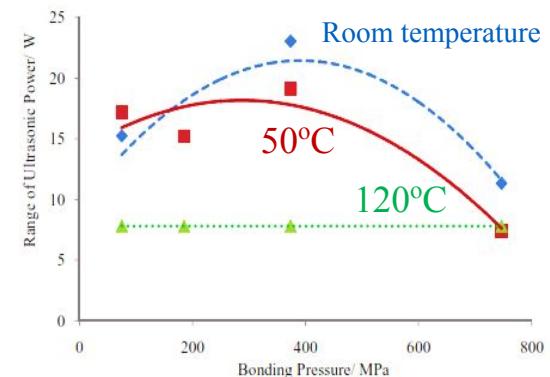
Laser assisted bonding (LAB): 2,200 UPH

(Amkor 2015)



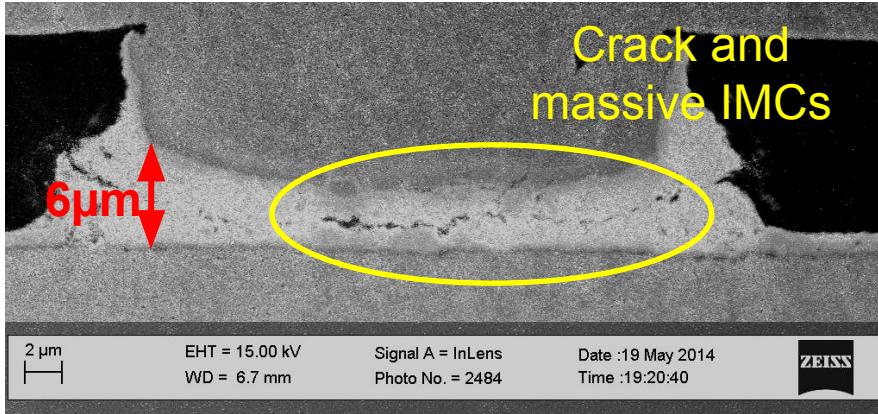
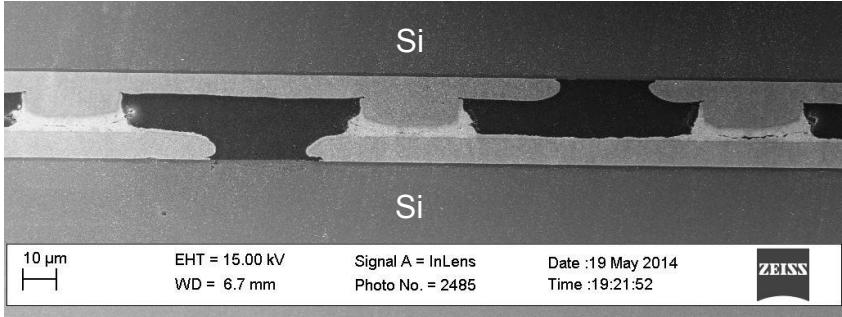
Ultrasonic bonding

(GGI by A*STAR 2013)

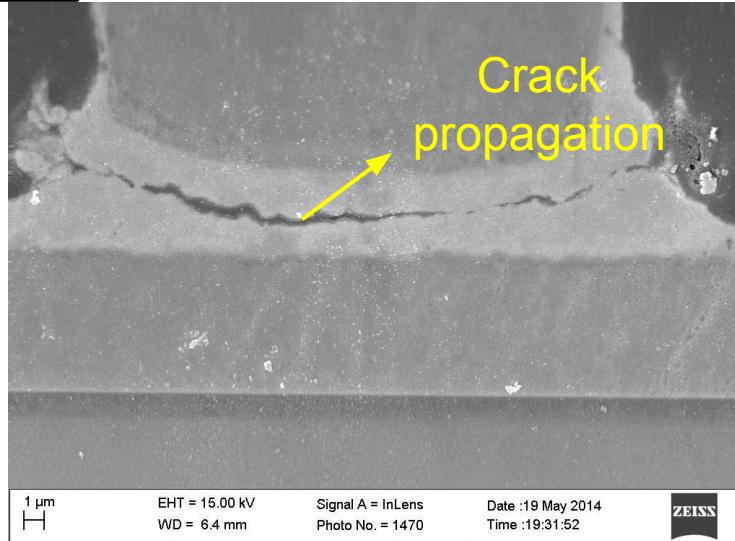
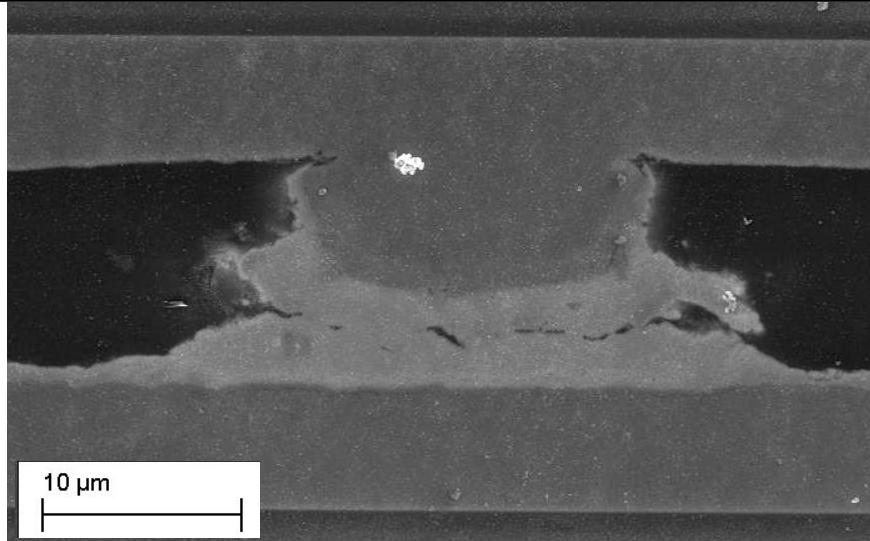


The challenge with reducing solder height

As-assembled

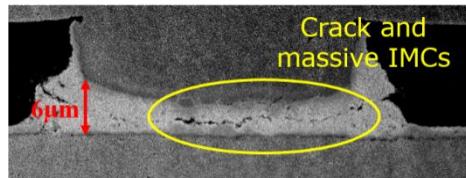


After reflow 3 times (Peak temp.= 260C)

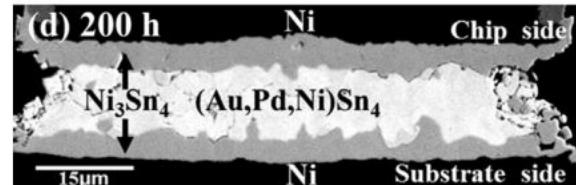


Limitations of standard Sn-based solders

- Limited pitch scalability
 - ❖ Increased risks of bridging
 - ❖ Difficult control of interfacial reaction with limited solder volume



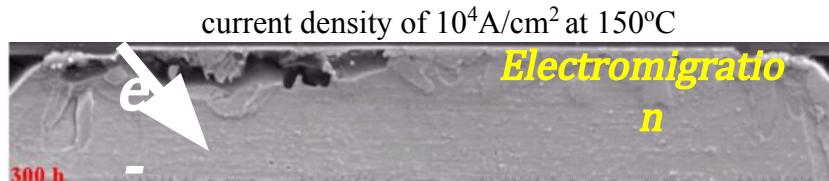
Severe interfacial stresses



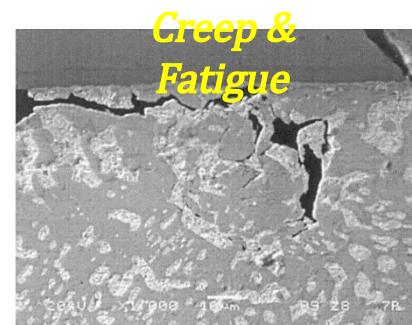
Au embrittlement

- Fundamental material limitations

- ❖ Max. operating temperatures: $0.3\text{-}0.5 T_m \rightarrow$
- ❖ Current carrying capability $< 0.5 \times 10^4 \text{ A/cm}^2$



M.H. Jen, et al., CPMT, 2009.

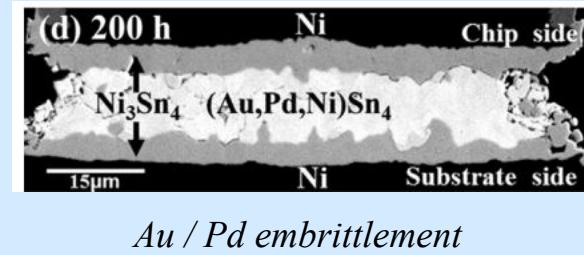
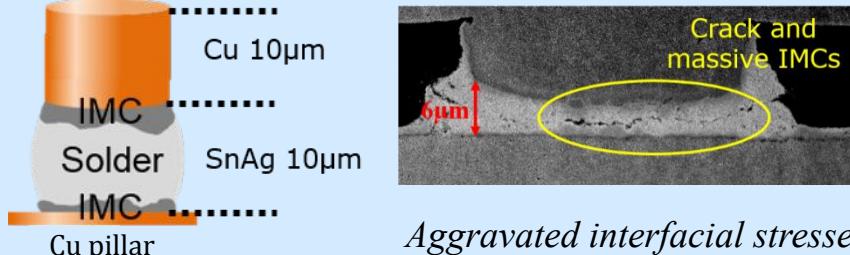


H.L.J. Pang, et al., Mat. Sci. Eng., 2001.

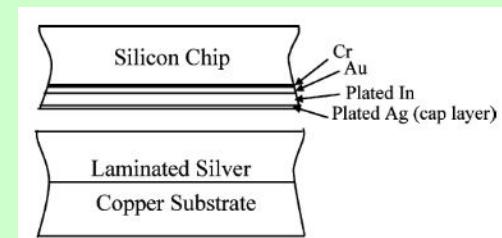
How far can we push solders?

Challenges with scaling Cu pillar technology to < 20 µm pitch

Controlled reaction with reduced solder volume



Void-free manufacturable SLID* bonding technology

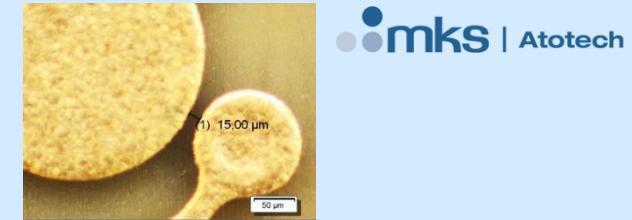


Complex bumping process

Our solutions:

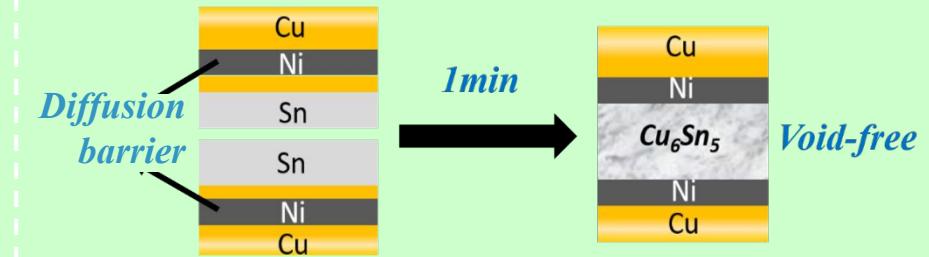
Surface finish & barrier layer designs

PallaBond® surface finish



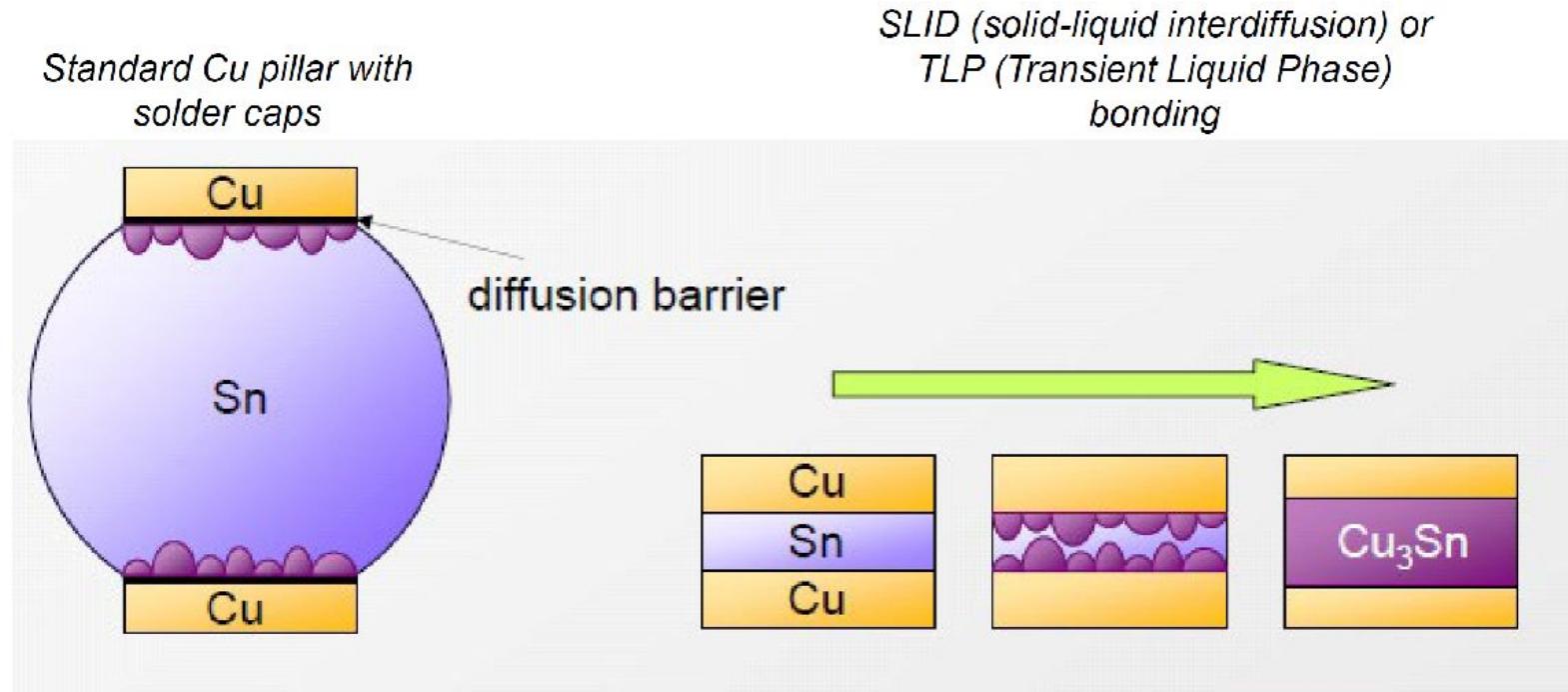
Scalable to high-density RDL:
no extraneous plating with < 10µm spacings

Metastable Cu_6Sn_5 SLID bonding



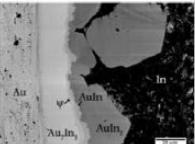
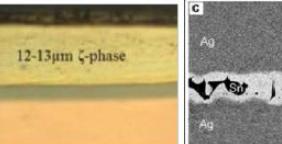
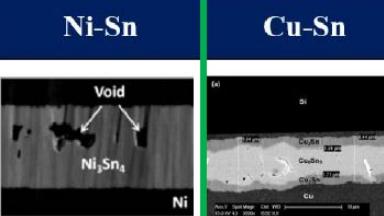
Void-free SLID with 20X shorter assembly time

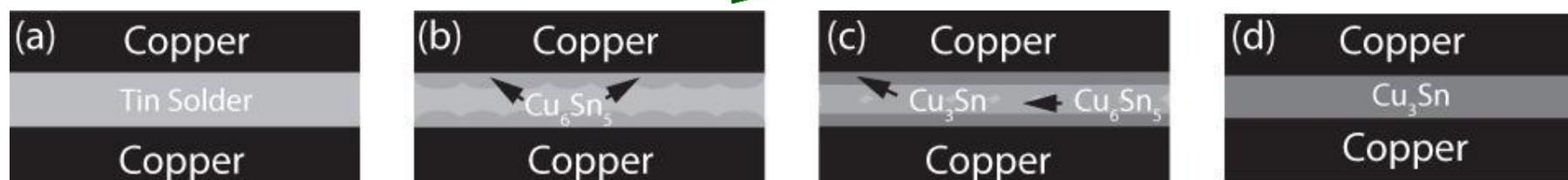
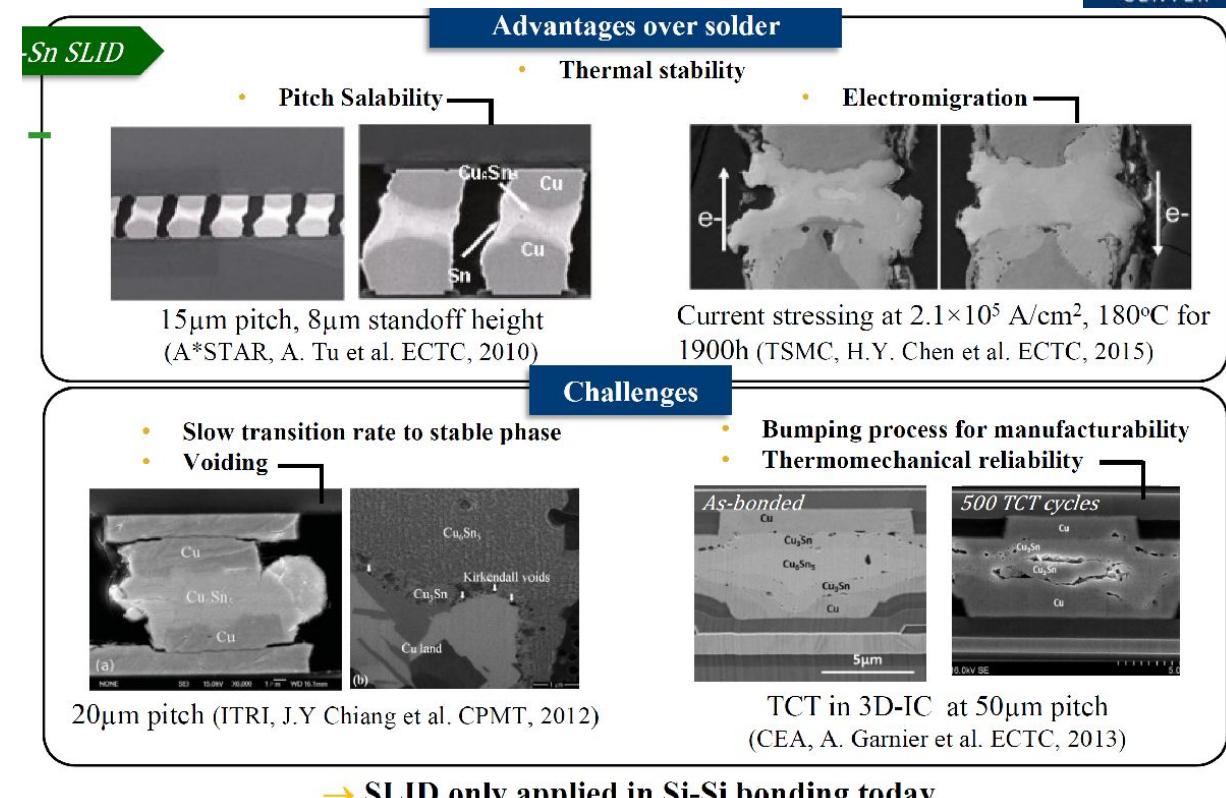
Solid-Liquid Interdiffusion (SLID) Bonding Concept



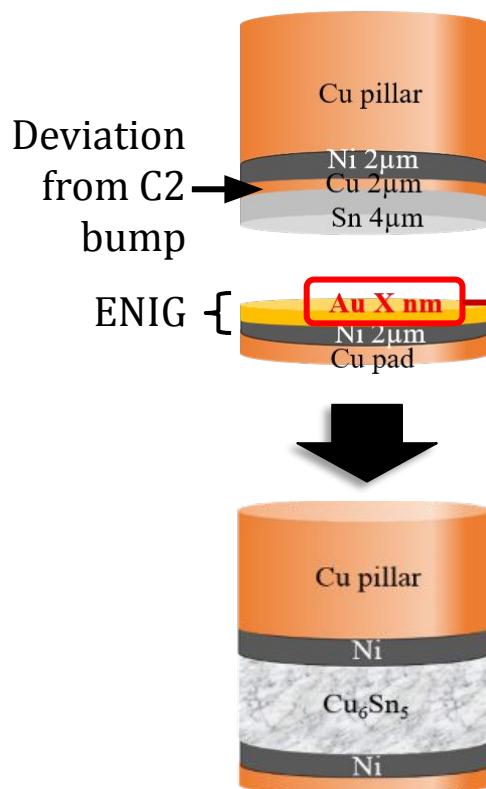
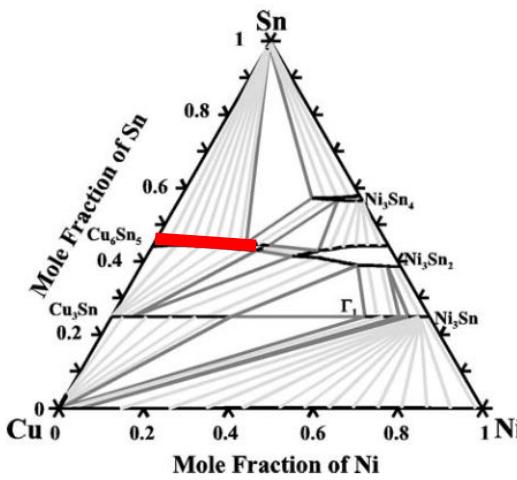
- Large solder volume
- Phase growth controlled by:
 - Diffusion barrier (Ni/Au)
 - Low-temperature budget
- Solidification by cooling
- Very thin reactive layer (low melting point)
- Full conversion to IMCs / an alloy with higher melting point than assembly temp.
- Solidification isothermally

Examples of SLID systems

System	Ag-In	Au-Sn	Ag-Sn	Ni-Sn	Cu-Sn
Snapshot					
Bonding temperature	180-190°C	350-360°C	260°C	260°C	260°C
Bumping	E-beam	E-beam	Ag foil / Electroplating	Electroplating	Electroplating
Bonding time	15 min (under vacuum)	15min for 12μm	2min for 5μm	15-30min	15-30min
Pressure	3 MPa	4.7 MPa	2-5 MPa	2-5 MPa	< 3 MPa
Melting point	450-540 °C	450 °C	480°C	794.5 °C	638.4 °C
Volume shrinkage	-	AuSn: -12%	Ag ₃ Sn: -9.14%	Ni ₃ Sn ₄ : -11.3%	Cu ₃ Sn: -27.3% Cu ₆ Sn ₅ : -3.9%
Main Challenges	<ul style="list-style-type: none"> Multiple phases Indium oxidation Delamination 	<ul style="list-style-type: none"> Cost High bonding temp 	<ul style="list-style-type: none"> Cost Deposition Brittleness 	<ul style="list-style-type: none"> Low transition rate Voids Volume shrinkage 	



Metastable CuSn SLID Stack-Up Design



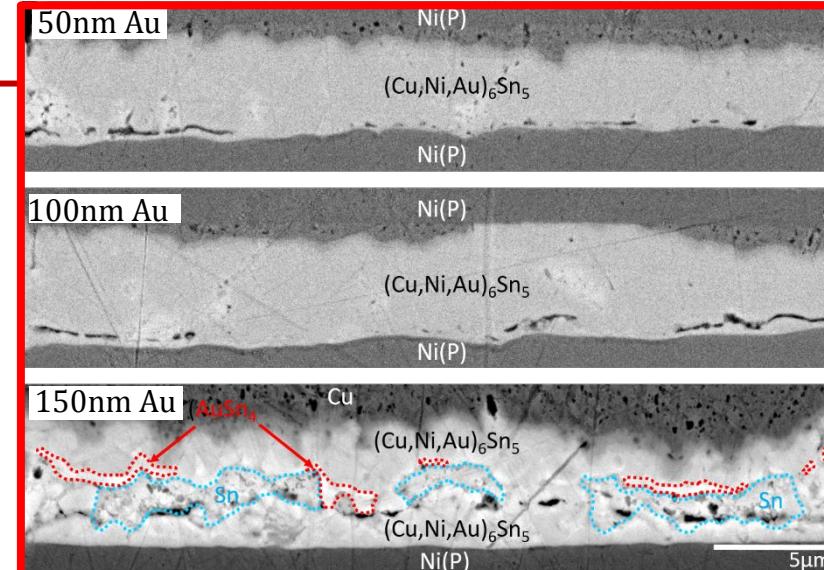
- Superior bumping manufacturability from Ni substitution:
1.2 μ m variation in Cu thickness acceptable from designed 2 μ m

- < 100 nm Au thickness in ENIG

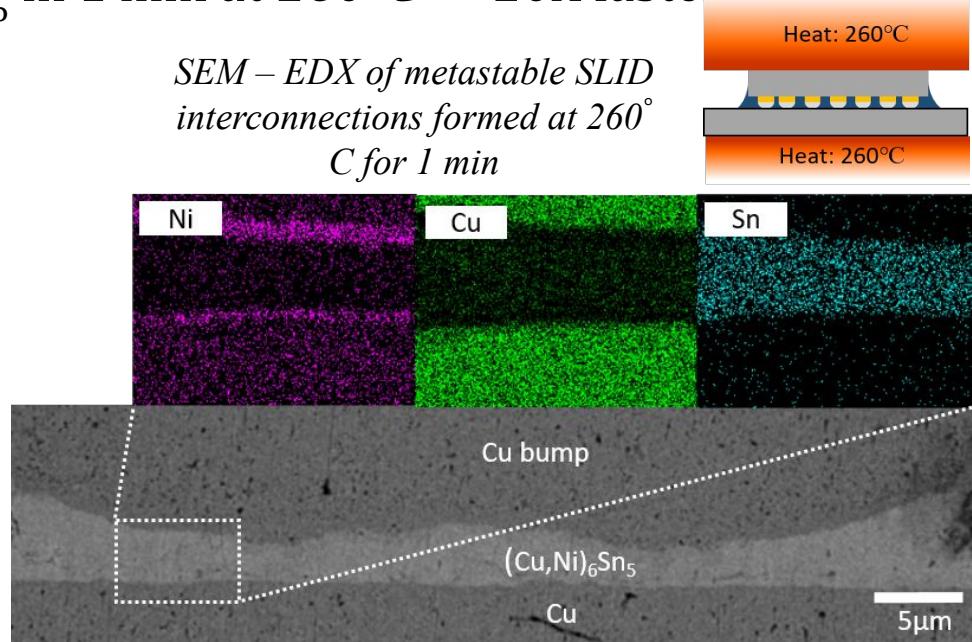
- Ni barrier thickness imposed by current stressing: $\sim 4 \mu\text{m}$ for 10^5 A/cm^2

- Full transition to $(\text{Cu},\text{Ni},\text{Au})_6\text{Sn}_5$ in 1 min at 260°C → 20X faster

Study of Au embrittlement in metastable SLID



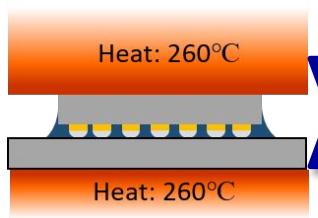
SEM – EDX of metastable SLID interconnections formed at 260°C for 1 min



Enhancing Assembly Throughput

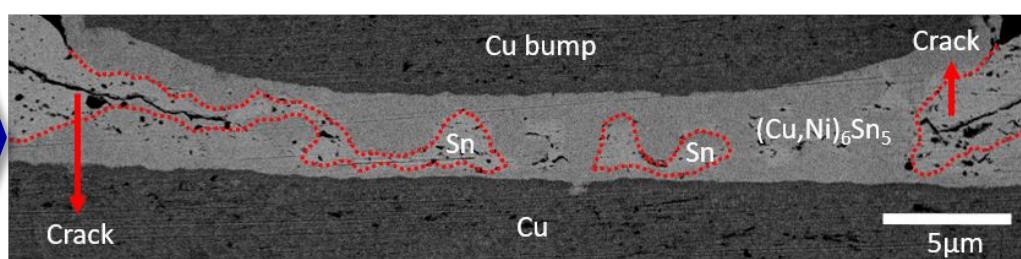
- What we want: shortest time under compression...

1min at 260°C



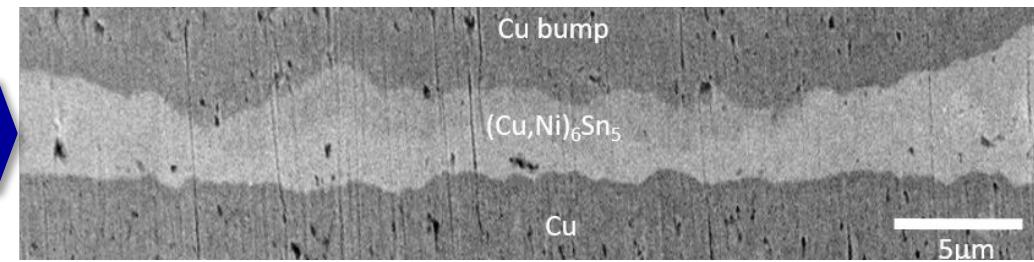
Too long for C2S

30s at 260°C



Insufficient residual solder

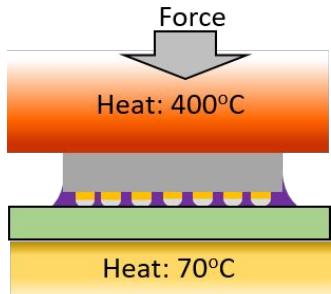
3s TC-NCP process + 1 reflow cycle at 260°C



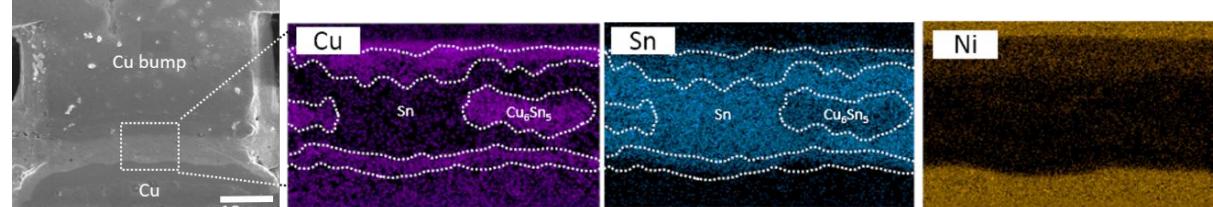
2-step process leveraging board-level reflow

- ... but it's not that simple with thin glass cores (100 μm thick)

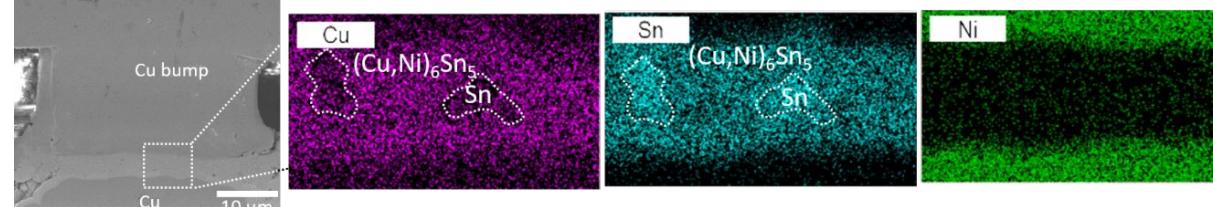
TC-NCP at a glance



1min dwell time



1min 30s dwell time



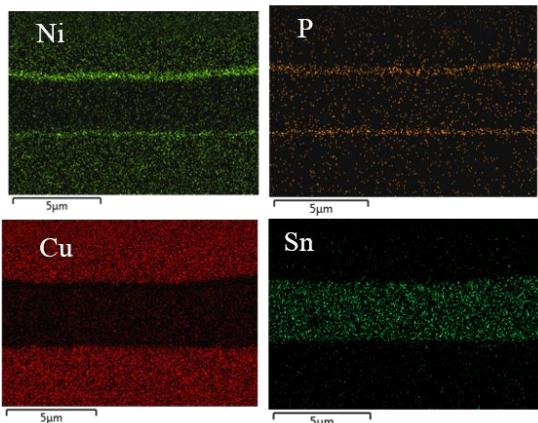
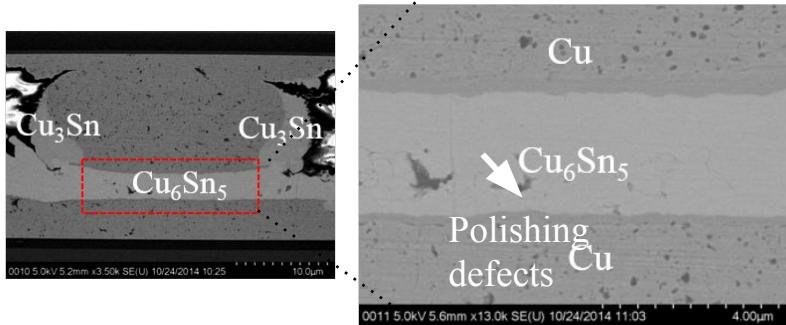
Max temperature in solder: 244 °C

Performance at a Glance

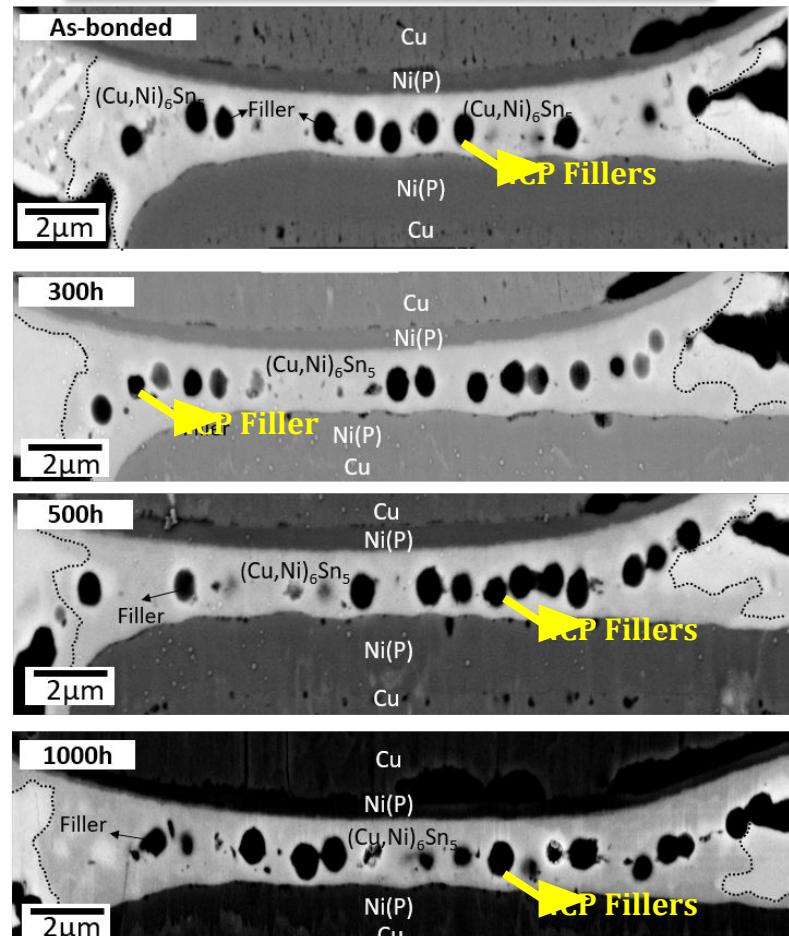
- Superior die shear strength: 88 ± 11 MPa vs. 40-65 MPa for Cu pillars / ~ 40 MPa for Cu_3Sn SLID

10X reflow

22 out of 24 daisy chains survived with stable resistance values in $2.4\text{-}5.3 \Omega$ range

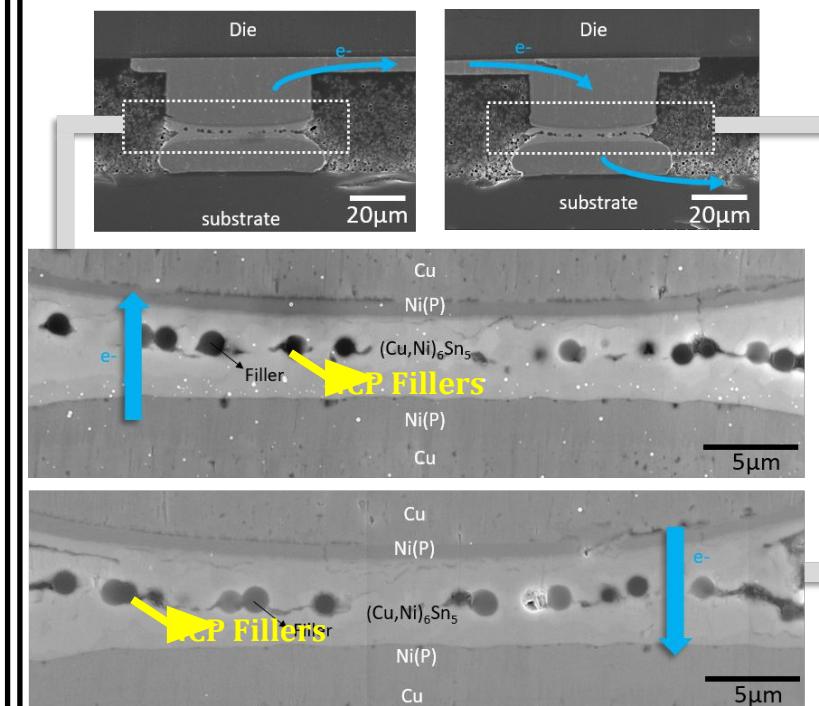


HTS at 200°C for 1000h



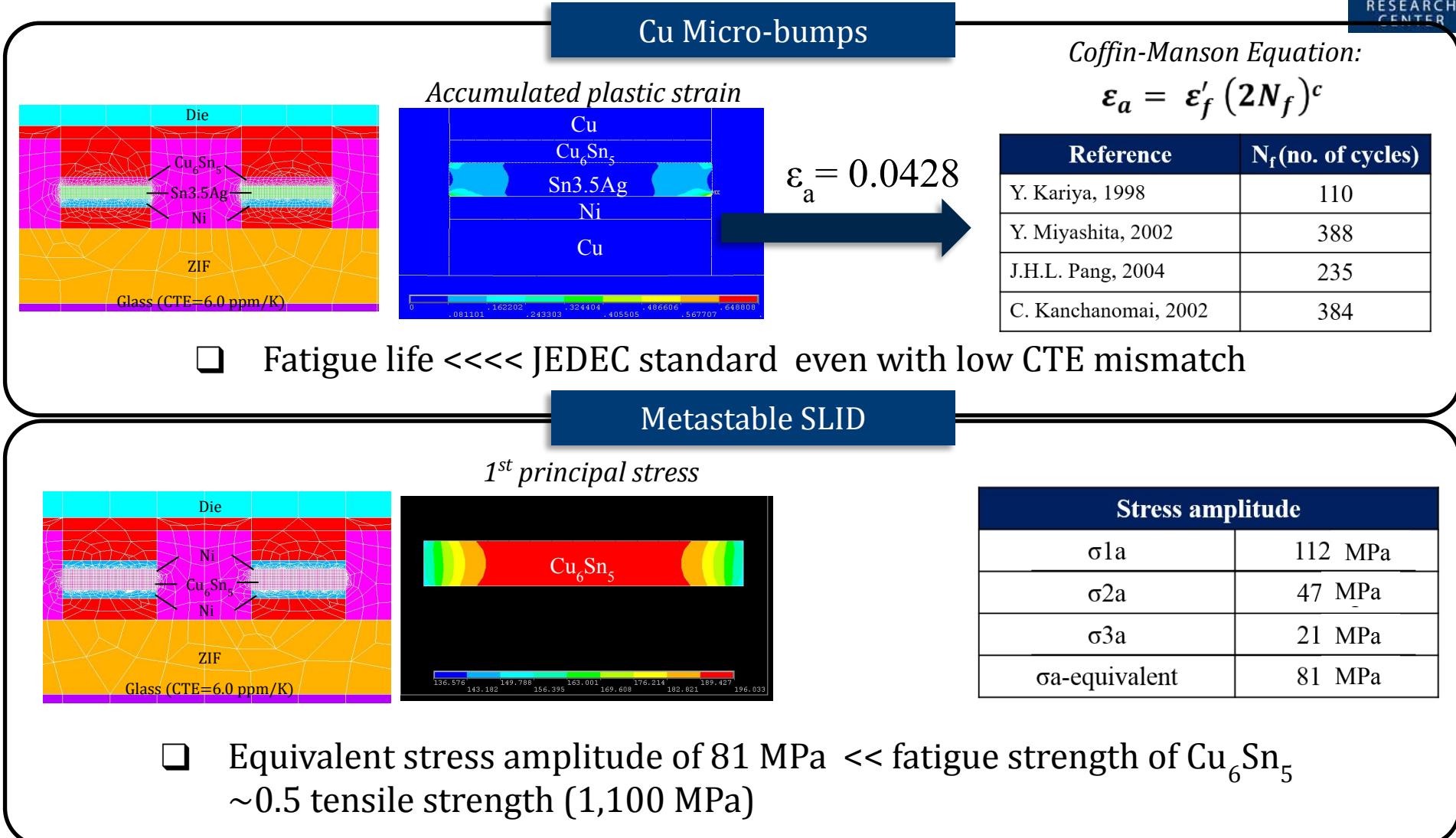
EM at 10^5 A/cm^2 , 150°C for 1000h

Stable microstructure, no change in measured daisy chain resistance

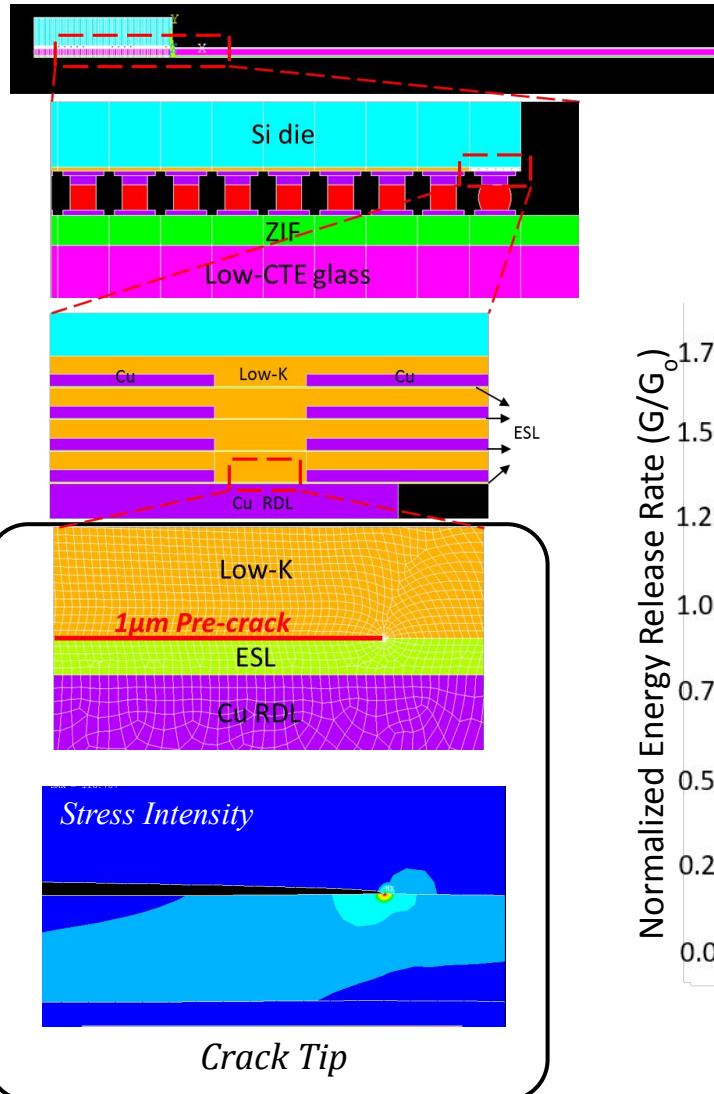


Rigid Interconnections: a Shift in How we Approach Reliability

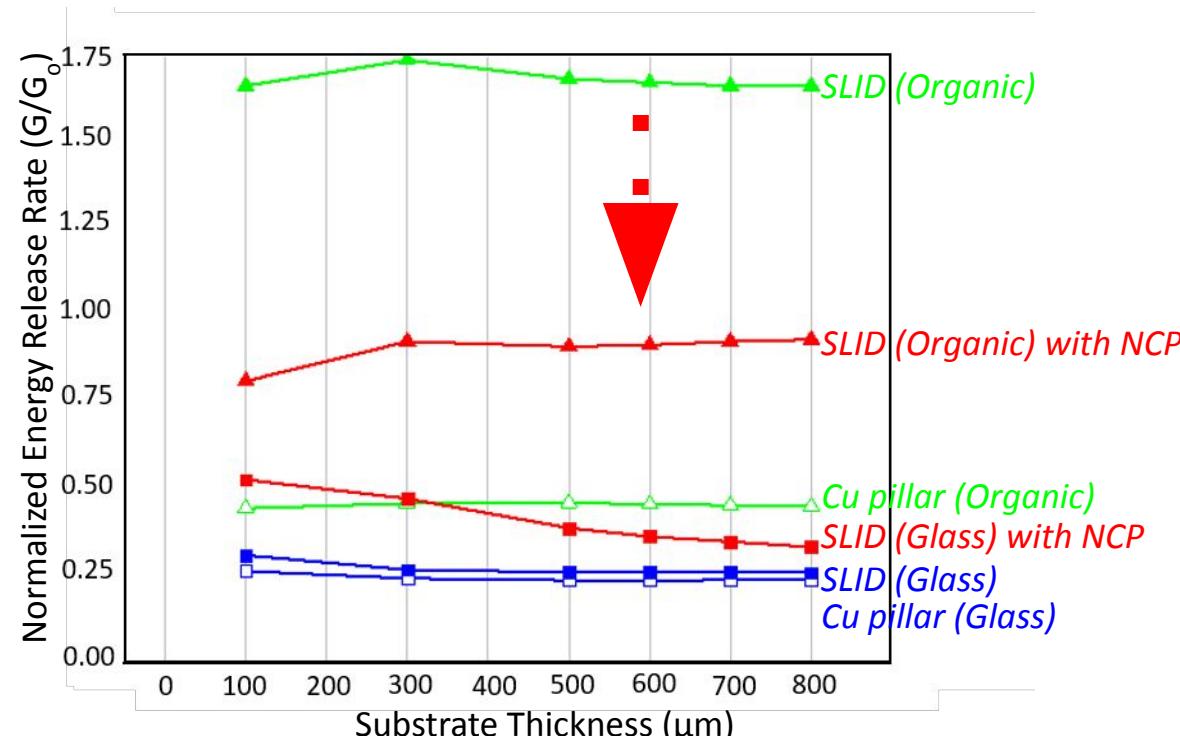
- Bump diameter: 15 μm
- Pitch : 30 μm
- 66 bumps per edge
- JEDEC TCT Standard - Condition B
 - 30min per cycle
 - 5min soak at top and bottom temp.
 - Ramp rate of 18°C/min



Perspective on ULK Dielectric Failures

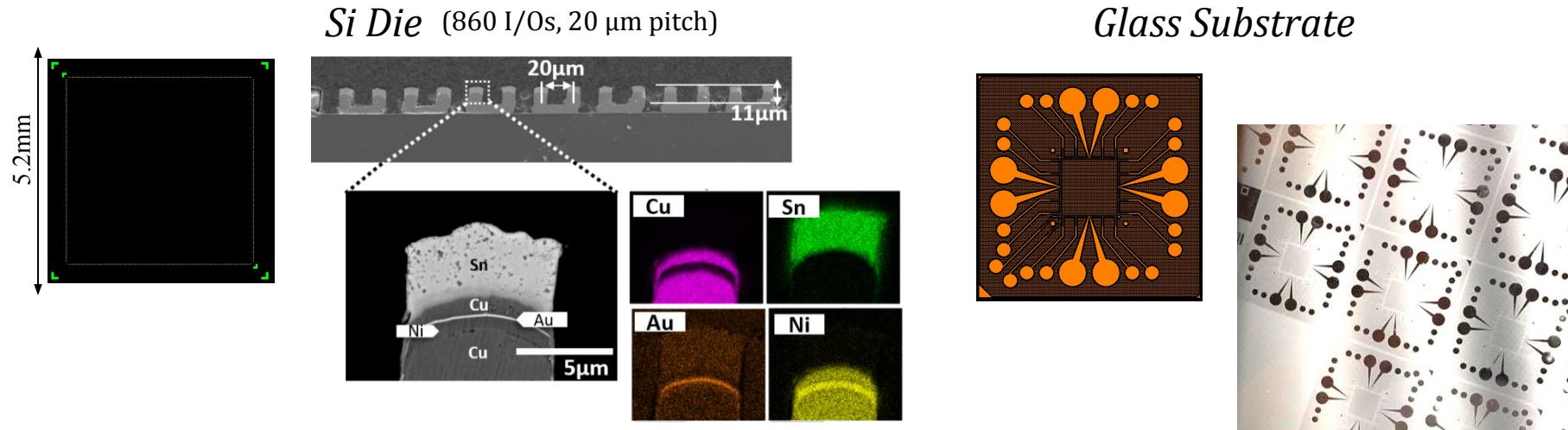


- Die thickness: 400 μm
- Substrate core material: glass / organic E679FGS
- Core thickness: 100 – 800 μm
- 5mm \times 5mm die on 2cm \times 2cm substrate
- Bump diameter: 15 μm
- I/O pitch: 30 μm
- $G_0 = 5 \text{ J/m}^2$

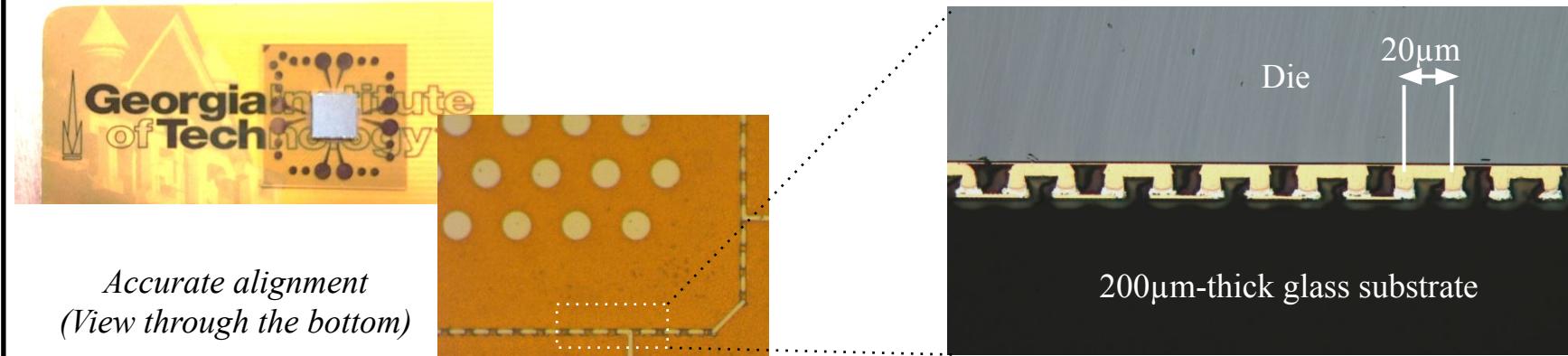


- High-CTE substrates show high risk of crack propagation with SLID
- Some CTE mismatch can be accommodated through polymer hybrid bonding... but just how much?

Metastable SLID at 20 μm Pitch on Low-CTE Glass

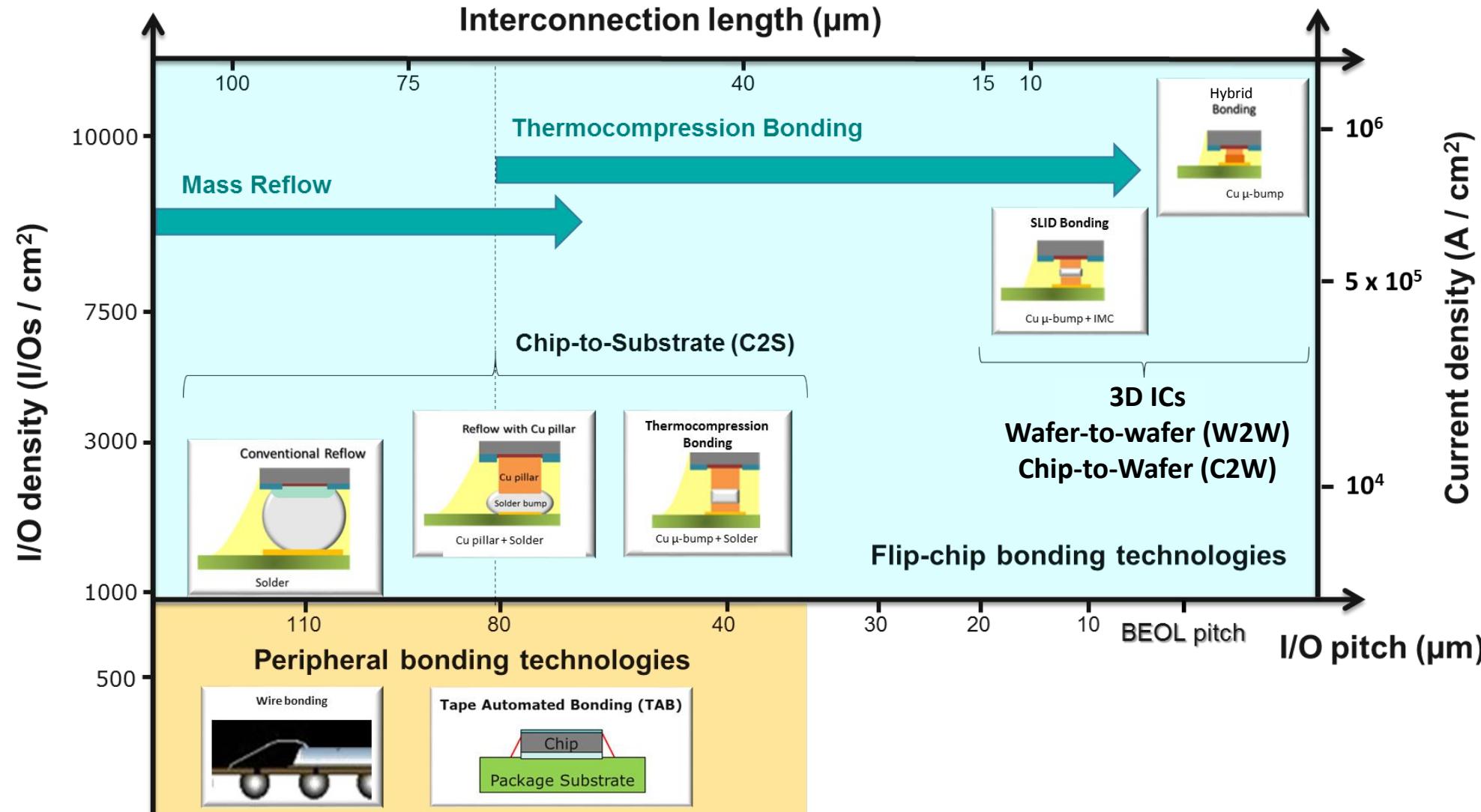


Assembly on 200 μm -thick glass package with ENIG finish



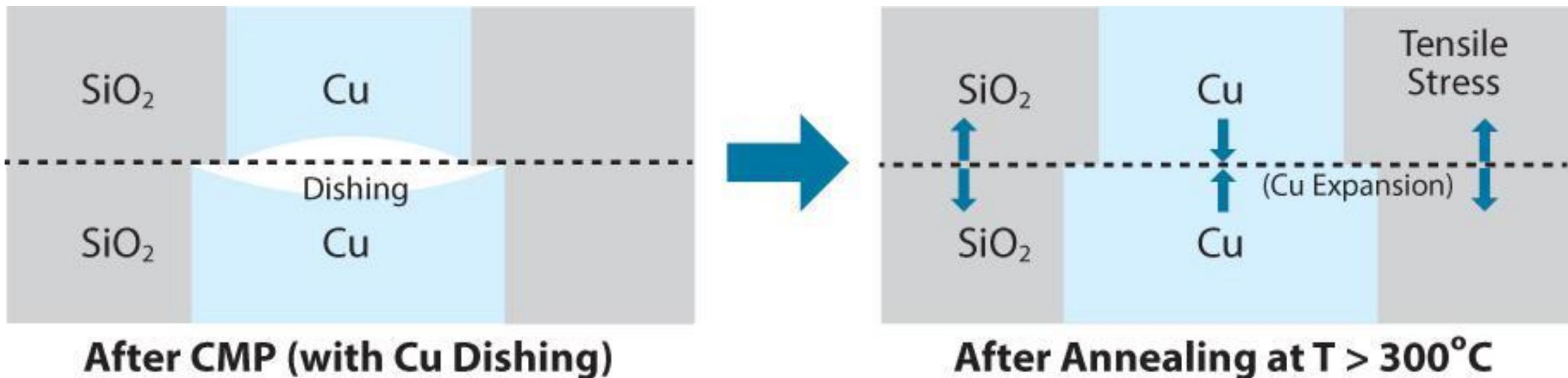
- In-house wafer bumping and substrate fabrication, full daisy-chain yield

The future is unsurprisingly solderless



Foundry-based solution: Cu/SiO₂ hybrid bonding

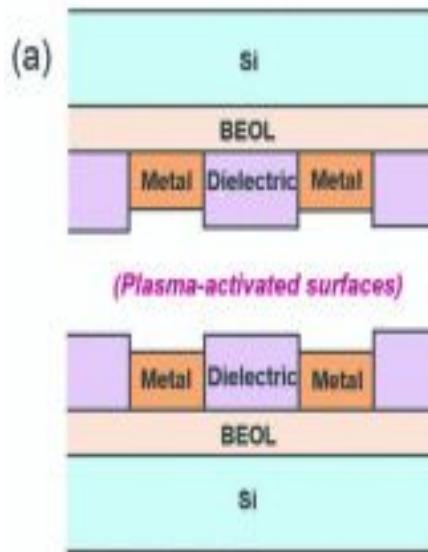
- Scalable to sub-micrometer pitches
- Applicable to wafer-to-wafer (W2W), chip-to-wafer (C2W) and chip-to-chip (3D ICs) assembly



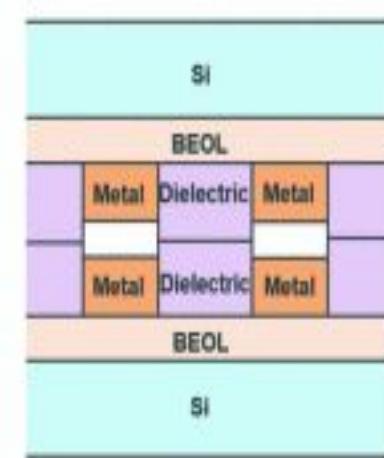
Why hybrid bonding will not work at package level

Overview of hybrid bonding process

CMP yields ultra-flat surfaces with controlled Cu recess



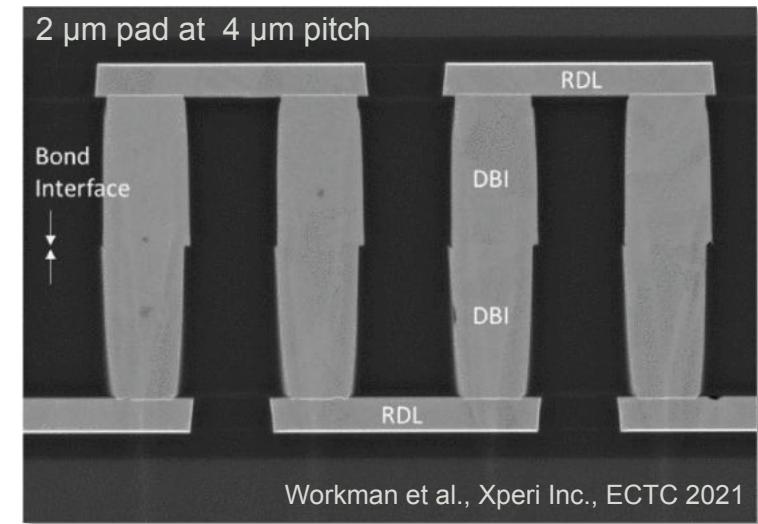
Spontaneous oxide bonding at room temperature



Annealing at elevated temperature → CTE-mismatch-induced metallurgical bonding



Unmatched scalability in pitch and performance



Si-Si only – W2W, C2W, C2C
First demo of chip on Si interposer in May 2023!

Incompatible with package-level materials and processes

What do we need?

Requirements of C2S Cu-Cu bonding:

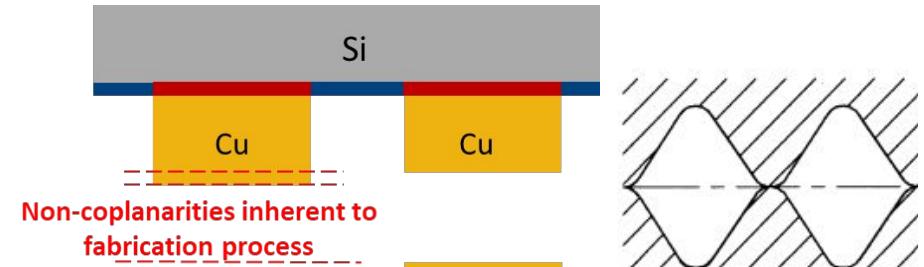
- Low bonding temperatures (< 250°C)
- Short bonding times
- Materials and processes compatible with current infrastructures for bumping and assembly

Enabled by:

- High diffusivity at bonding interface
- Design of interconnection material
- Clean, oxide-free surfaces

Remaining challenge:

- Surface topography tolerance at panel scale



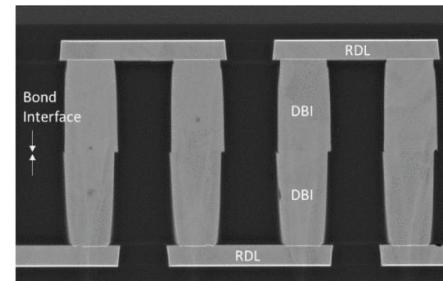
Uniformity tolerances in industry-plated Cu pillars			
Within Die	Within Feature	Global	
50 µm pillar On 300 mm Si wafer	90 nm / 1.7%	1.77 µm / 3.5%	3 µm / 7% (Inoue et al. 2022)
10 µm RDL On 500 mm panel	--	--	1 µm / 10% (Hübner et al. 2018)

How to handle non-coplanarities?

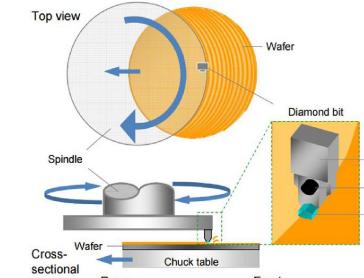
□ Cut them off

- CMP / fly cut
- Process / material incompatibilities

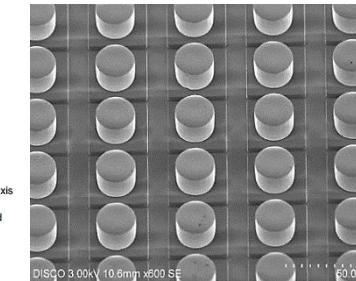
Hybrid bonding



Workman et al., Xperi Inc., ECTC 2021



Fly-cut planarization

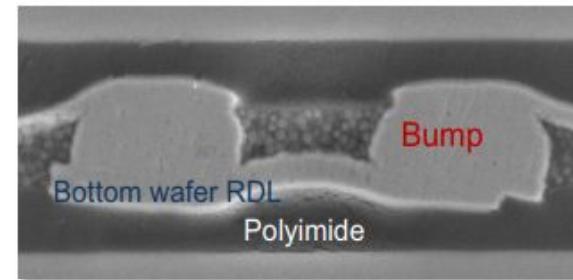


Courtesy of Disco

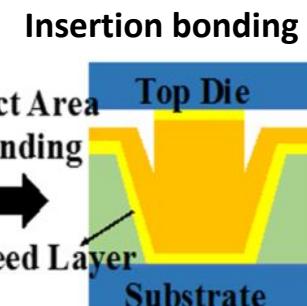
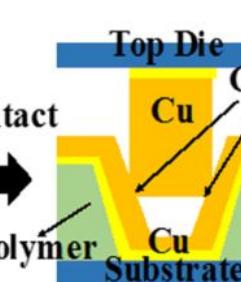
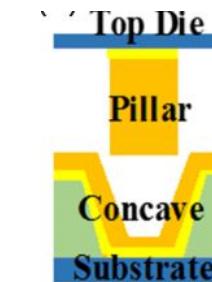
□ Confront them

- Relatively high temperature and pressure requirements
- Possible damage to underlying structures

Thermocompression bonding



L Xie et al, ECTC 2016

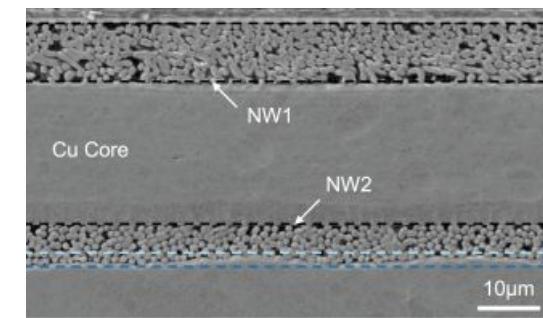


Panigrahy, ASME, 2018

□ Entertain them

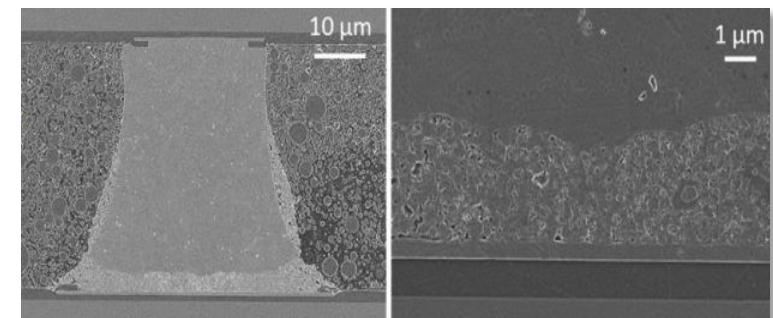
- ‘Solder-like’ behavior in assembly
- Expensive / difficult to manufacture
- Can you really get ‘bulk’ properties?

Cu-nanowire array sintering



Yu, NanoWired GmbH, IEEE EPTC 2021

Cu-nanoparticle ink and paste sintering



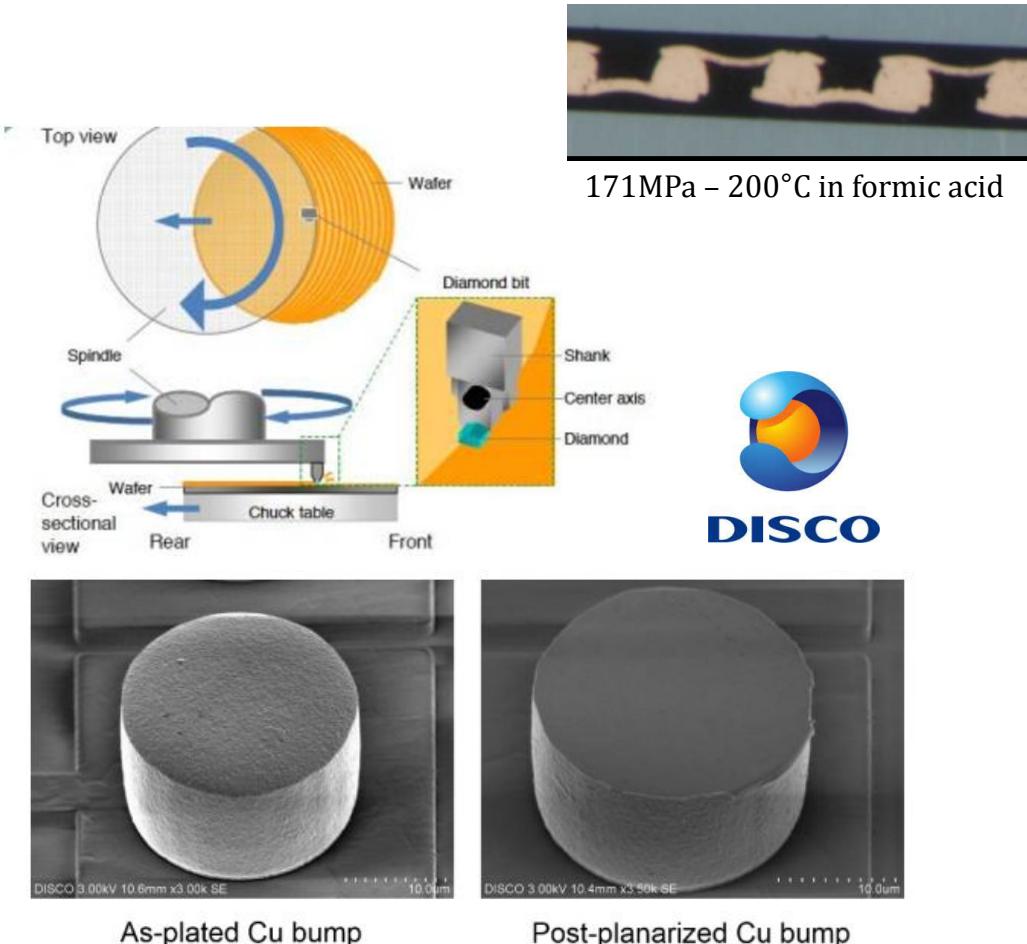
Del Carro et al, IEEE CPMT 2019

Accommodation of non-coplanarities through planarization

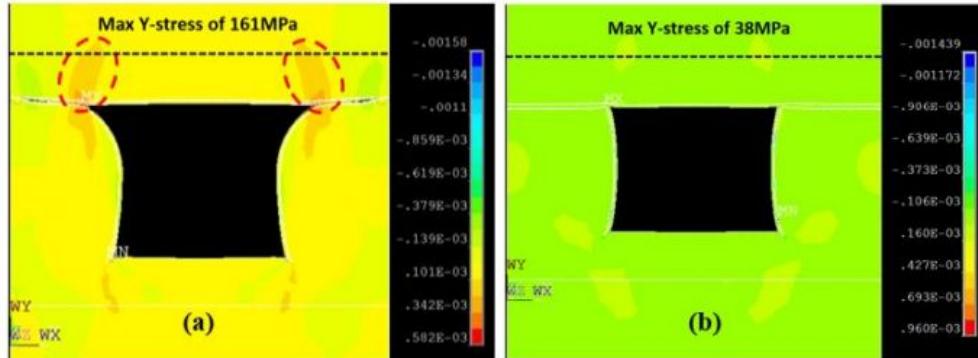


Flatness control through fly-cut and passivation of Cu surfaces with PallaBond®

- ☐ Evidence of RDL delamination in TC bonding

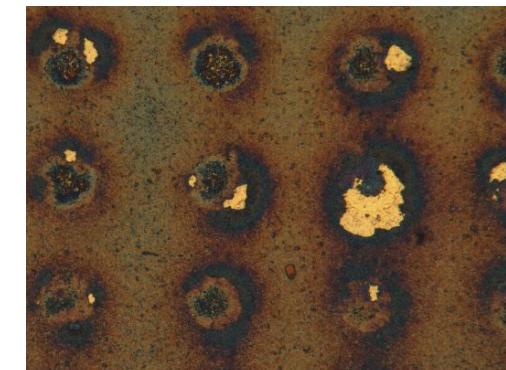


- ☐ Reduction in bonding pressure from 365 MPa to 120 MPa & lessened risk of RDL delamination

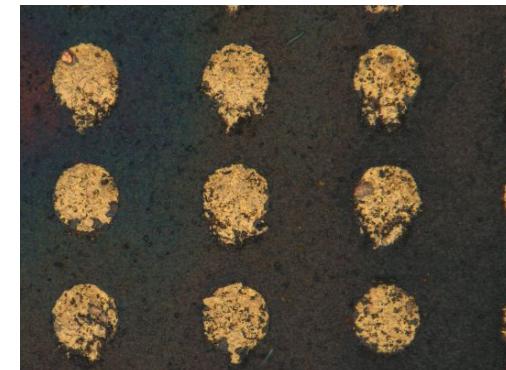


- ☐ Substrate-side die-shear fracture analysis: full-area contact only achieved with planarization

Non-planarized Cu bumps

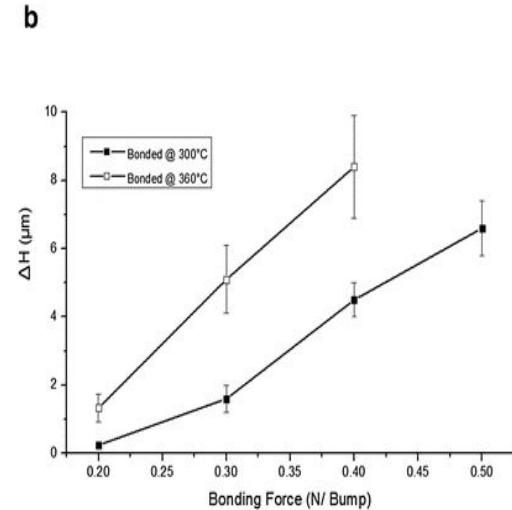
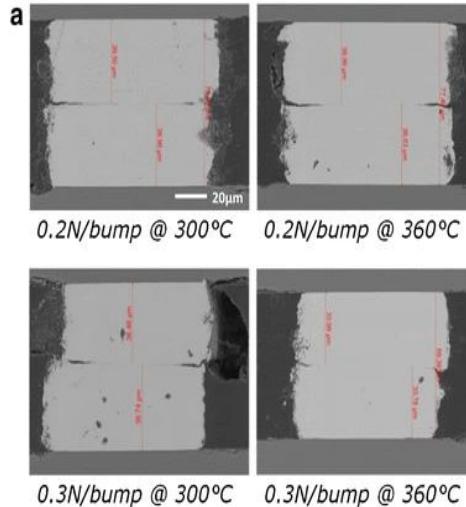


Planarized Cu bumps

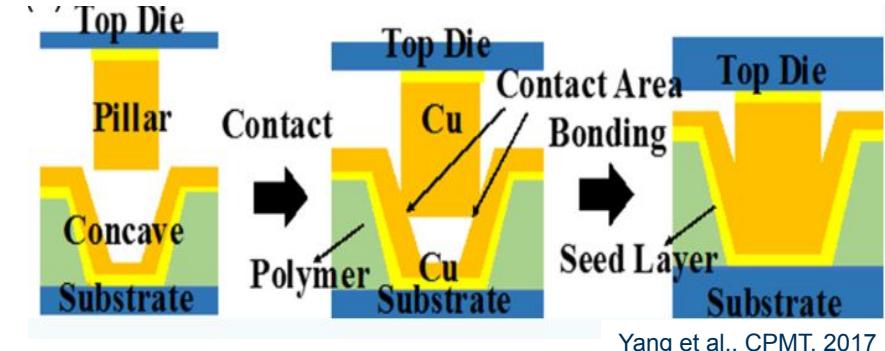


Accommodation of non-coplanarities through plastic strain

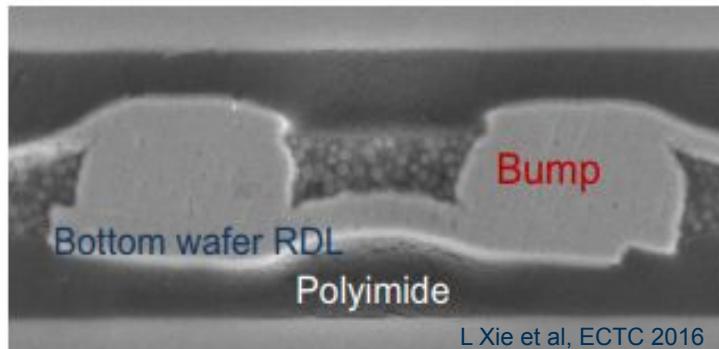
Cu-Cu thermocompression bonding



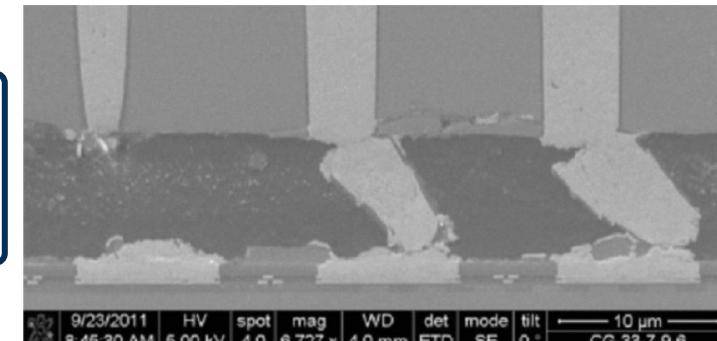
Insertion bonding



Design of geometry for highly localized plastic deformation



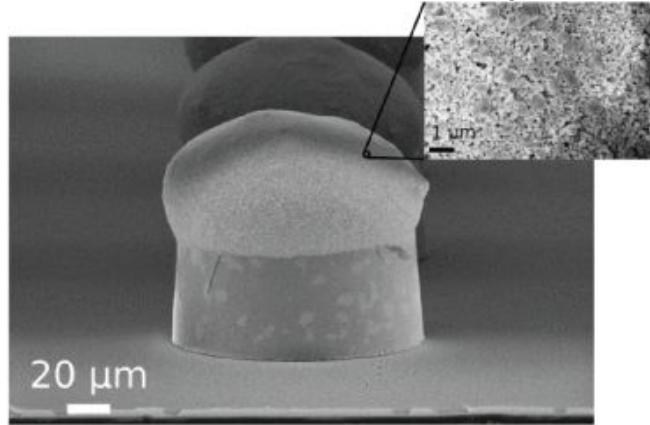
Severe reliability concerns



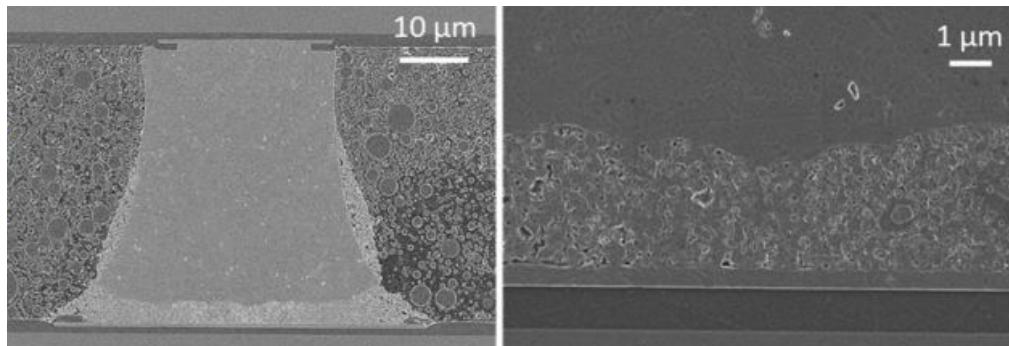
Accommodation of non-coplanarities through low-modulus interface

Nanoparticle sintering

Nano-Cu ink cap on Cu pillar by dip transfer



Cross-section of sintered interconnection

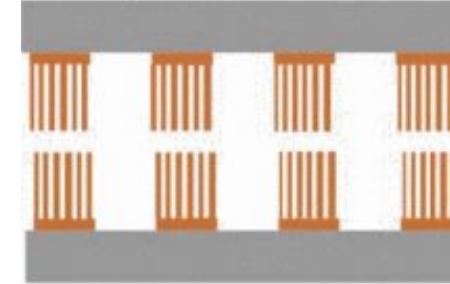


Del Carro et al, IEEE CPMT 2019

Nanowire array sintering

Fabrication of nanowire array by electrodeposition through porous template

a)



KlettWelding
 $T = 21 \text{ }^{\circ}\text{C}$
 $P = 1 \text{ MPa} - 15 \text{ MPa}$
 Time = 60 ms



Mechanical interweaving and sintering of nanowire arrays

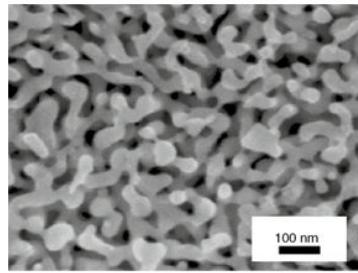


Our solution: nanoporous copper

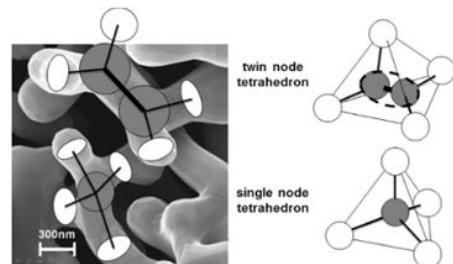
Structure of nanoporous-Cu



Guo et al., 2016

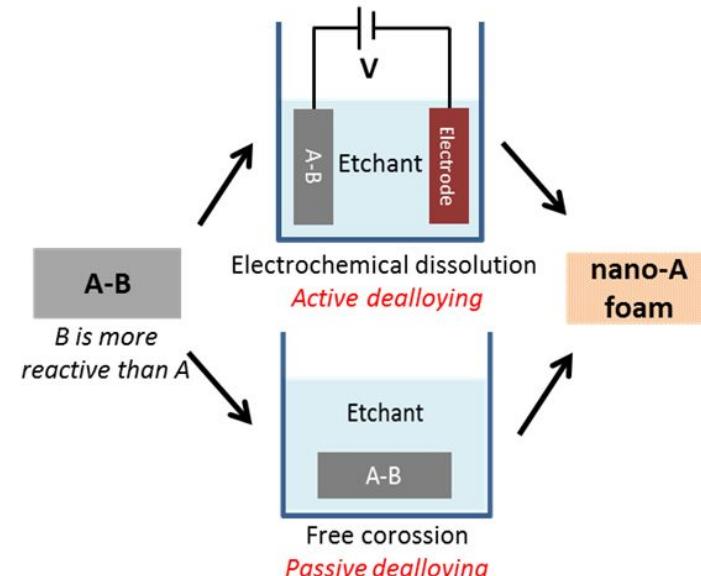


Hou et al, Sci. Rep. 2013



Huber et al., 2014

Synthesis of nanoporous-Cu



NP-Cu: 3D interconnected network of nanosized ligaments

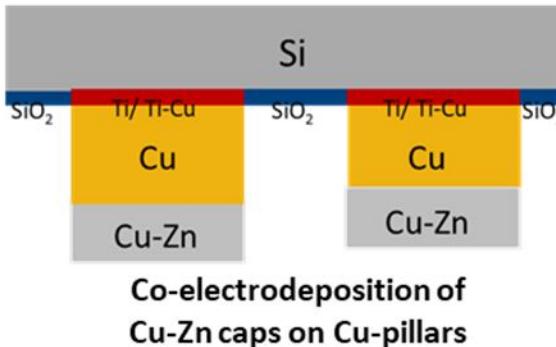
- Low-modulus compared to bulk-Cu: 6-20 GPa
- High initial relative density (>50%)
- Large surface area
- Metastable non-discrete solid-state system

Synthesis by (electro)chemical dealloying of Cu-Zn precursor alloy

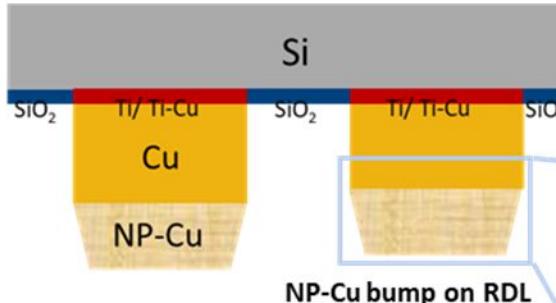
- Compatible with semi-additive build-up
- High control over material properties through fabrication process parameters

Manufacturability is key to technology adoption!

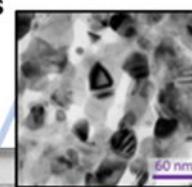
NP-Cu cap fabrication



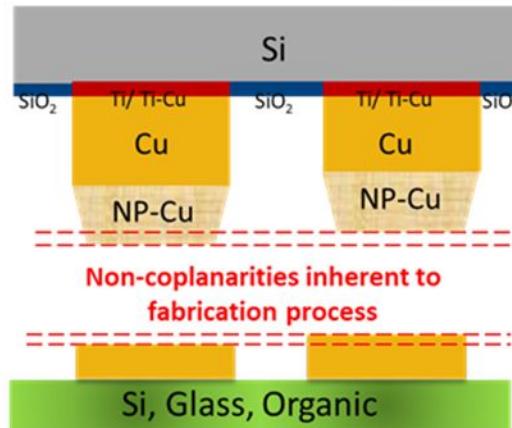
Controlled dealloying to remove Zn



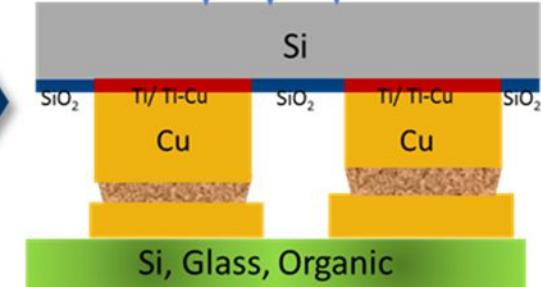
3D interconnected network of nanoscale ligaments



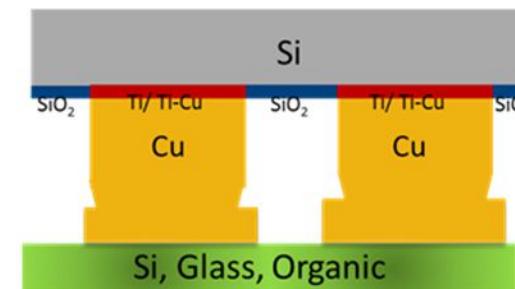
NP-Cu to Cu bonding



Initial placement pressure deforms NP-Cu



Pressureless sintering



Highly reactive NP-Cu then densifies due to sintering, yielding all-Cu interconnections with void-free bonded interfaces

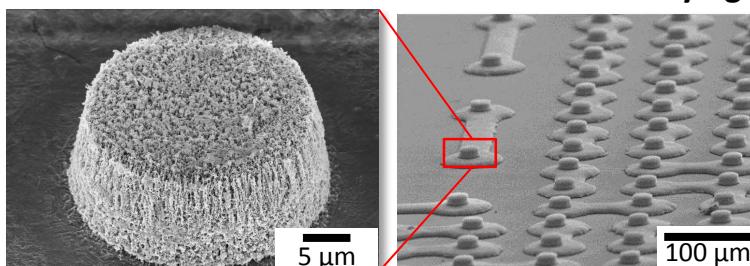
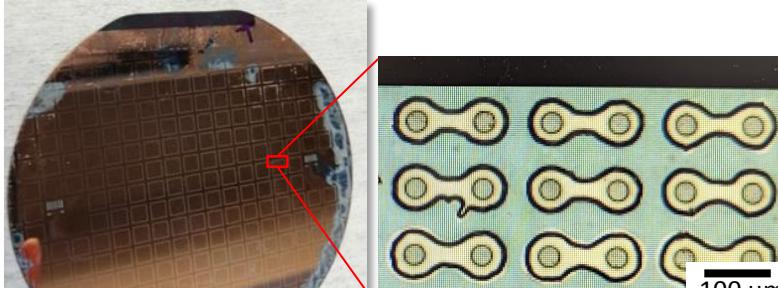
Technology overview at a glance

□ It's soft

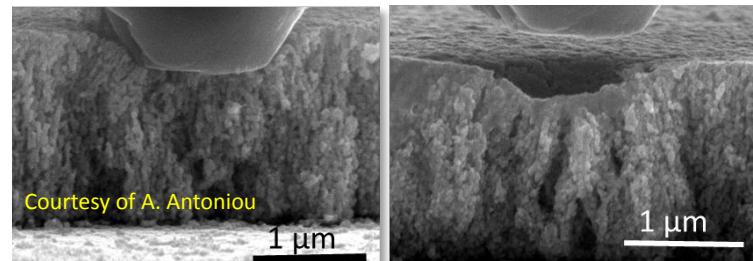
- Elastic modulus < 20 GPa,
but relative density > 50%

□ It's patternable

30 μm \varnothing Cu-Zn bumps on Cu RDL patterned on
4" Si-wafer at 100 μm pitch



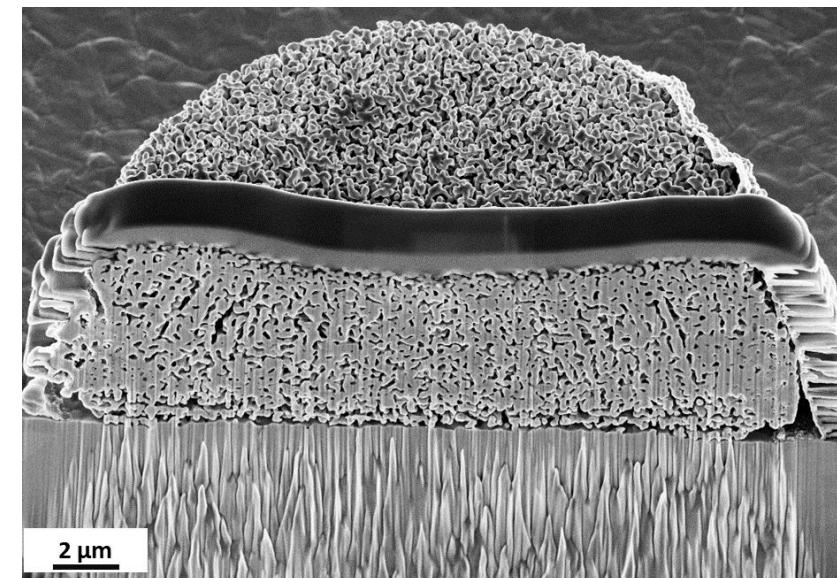
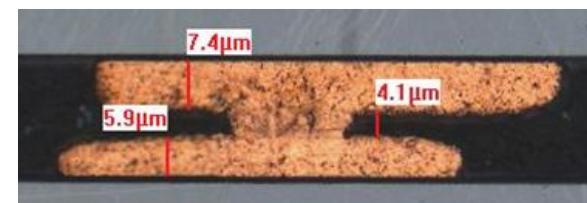
In-situ indentation with the frustum indenter on 2 μm -thick NP-Cu films



Collaboration with A. Antoniou

□ It sinters

Cross-section and FIB-SEM of NP-Cu joints
sintered at 300°C for 5min, 50MPa
placement pressure only

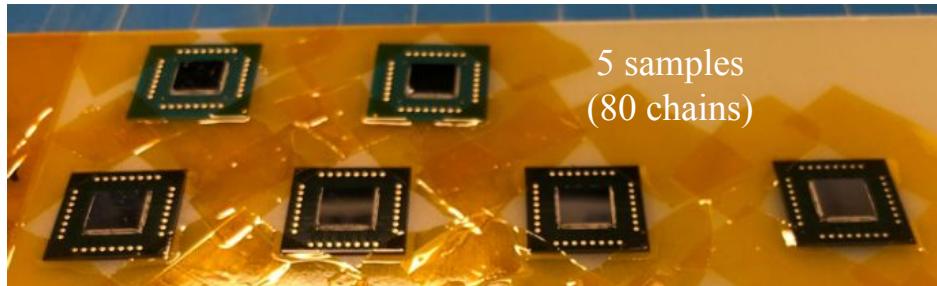


□ It performs

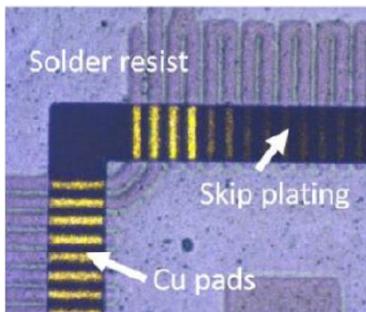
- Density > 95% (*before* process optimization)
- Die shear strength: 80–150 MPa
- Passed 1000h HTS at 150 °C
- Passed 1000h EM at 10^5 A/cm^2 – 90 °C
- TCT JESD22-A104F Cond. M – ongoing, passed 250 cycles

What's left: chip-package interactions in non-CTE matched package architectures

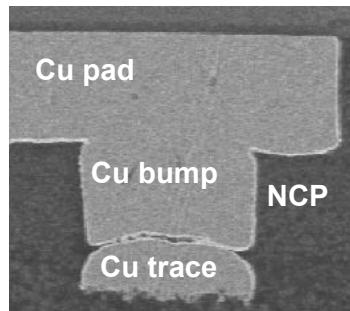
Daisy-chain TV: low-CTE glass at 50 μm pitch



- Failure criterion: 20% increase in as-bonded Ω
- Pre-conditioning (JESD22-A113F)
- Thermal shock test at $-55^\circ\text{C}/125^\circ\text{C}$, 2 cycles per h

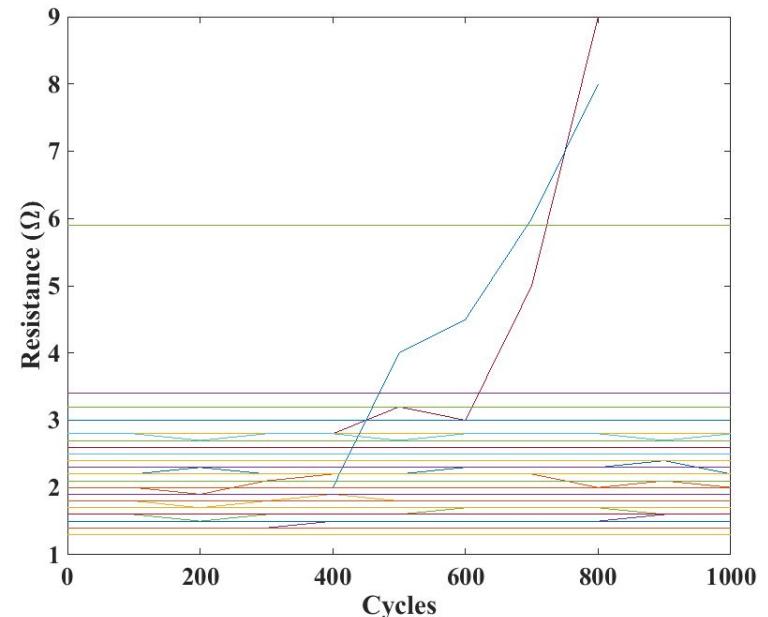


As-bonded yield issues



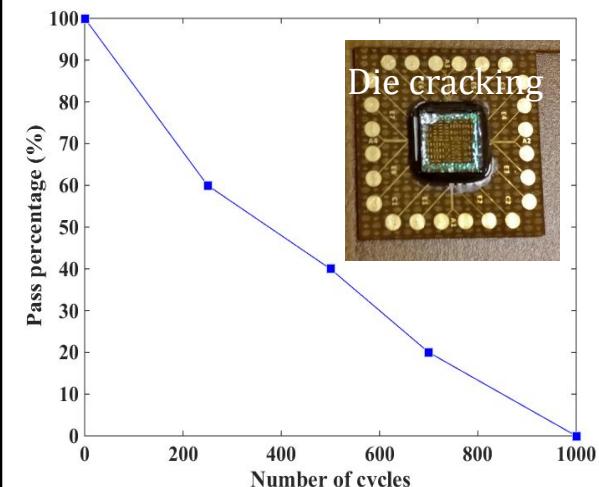
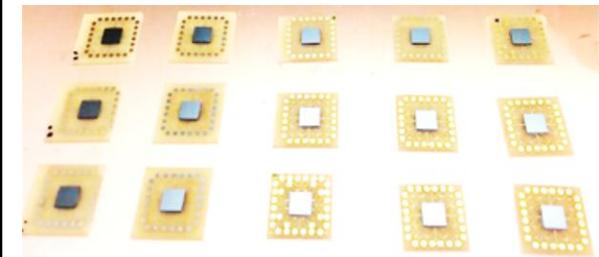
Filler entrapment

TCT failure distribution



- 70% as-bonded yield
- Two daisy chains failed > 500 cycles
- All other daisy chains passed the test
- Successfully validated reliability model

With FR-4



- Matching modeling predictions

Examples of application-specific requirements

HPC & AI

6G

Flexible & wearable

High-power Electronics

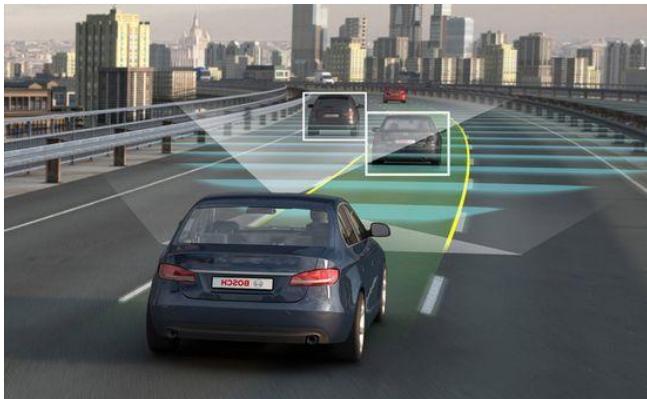
Sensing

High-temp. Electronics

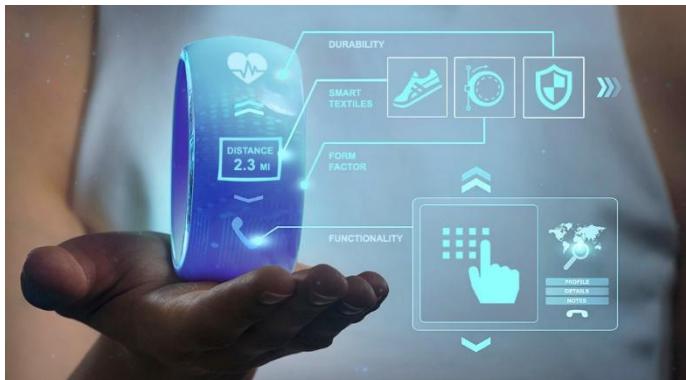
Pitch?



Power handling?



Thermal stability?



Compliance?

Length?



Reliability?

Assembly process?

A few examples

HPC & AI

- <10 µm pitch off-chip interconnections
- Board- to system-level reliability in 2-level hierarchy

Sensors

- Low-stress, low-temp. assembly
< 150°C, fluxless

High-temp. Electronics

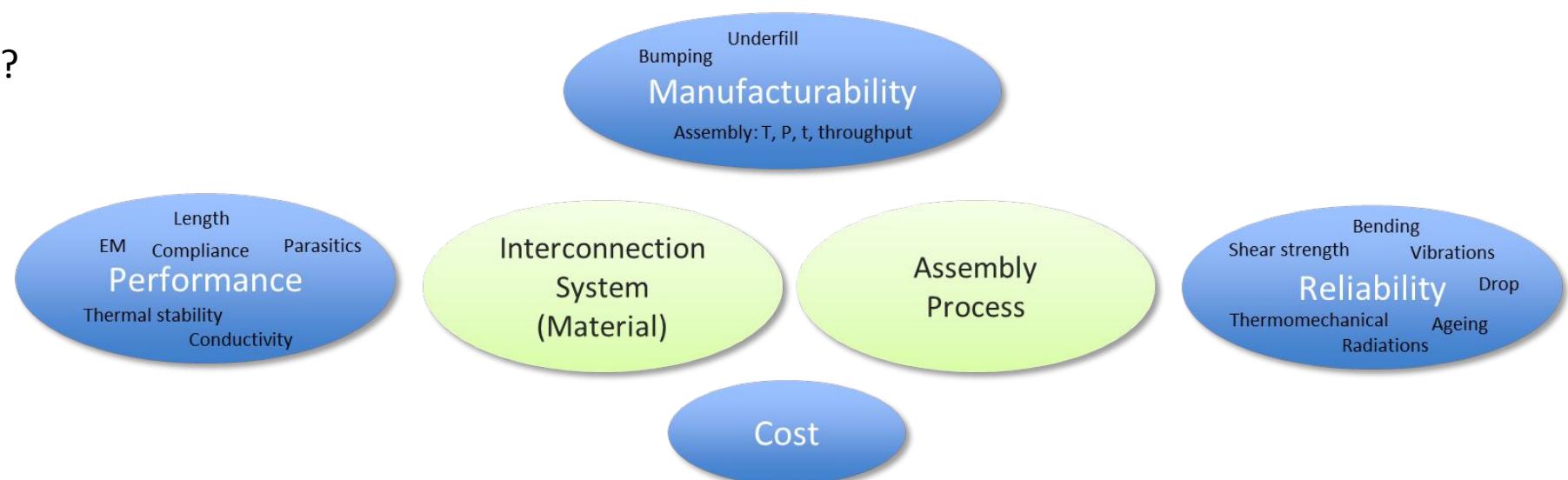
- Low-temp. assembly
- Thermal stability > 250°C

High-power Electronics

- Electrical & thermal >> solders
- Thermal stability > 250°C
- Stress management
- Low-temp. assembly

How to select an interconnection technology / assembly process for a given application?

- Understand (1) the needs of the application, (2) the application constraints (design box for innovation) – domain knowledge is key
- Interconnection system:
 - ❖ Materials, geometry, stack-up – reacting interfaces (surface finish, UBM, ...)
 - ❖ Multi-physics modeling: diffusion models, FEM
- Assembly: bonding mechanism – metallurgical, adhesive, ...
 - ❖ Metallurgical bonding: how do you (1) create contact, (2) bring energy for diffusion, (3) create a joint with the targeted properties
 - ❖ What kind of energy?
 - Heat: local / global
 - Pressure
 - Ultrasonic



Key questions to help select a solution

- What are the processing constraints imposed by my application:
 - ❖ Max admissible temp. (and for how long), pressure
 - ❖ Chemical sensitivity (e.g. no chloride- or fluoride-based etchants)
 - ❖ Accuracy of placement: sub-micron in photonics vs tens of microns in BGAs
 - ❖ Cost
- What is the performance / reliability needed:
 - ❖ Electrical: length, parasitics, current density
 - ❖ Thermal: temperature of use, mission profile (use thermal profile)
 - ❖ Mechanical: strength, compliance, etc
 - ❖ Reliability: what are the standards for the application / expected failure modes

Thank

You