



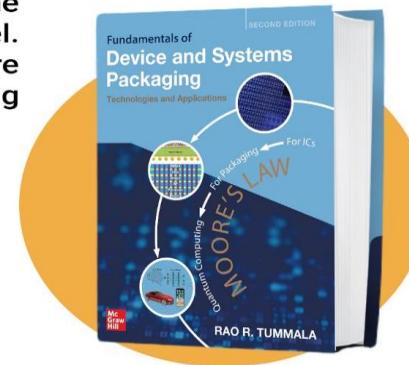
# INTRODUCTION TO DEVICE AND SYSTEMS PACKAGING

► September 21st – November 24th 2024 ◀

As India begins its long-awaited journey in semiconductors and packaging, India needs to acquire the state-of-the-art knowledge to bring itself to global level. Integrated systems packaging is becoming more valuable than either semiconductors or packaging as Moore's Law benefits slow down.

This course is based on integrated semiconductors and packaging R&D and the textbook by Prof. Rao Tummala and his Georgia Tech Team in the USA - **Fundamentals of Device and Systems Packaging** (McGraw-Hill, 2019).

It covers 17 core semiconductor, packaging and system technologies



- For Industry Engineers, Academic Faculty, and Postgraduate Students.
- Taught by Global Experts. Participation certificate will be issued to each student for the courses taken.
- Book and course content same.
- Each student can order a low cost Indian edition from amazon.
- 36 Hours of teaching over three months.
- Each student completing the course will get a certificate.

## Class Duration:

**Each class is about 2 hours followed by 30 min. Q&A discussion**

## Class Timing:

**Classes start at 7.30PM IST on Saturdays and Sundays  
(A total of 18 classes over three months)**

## Course Topics and Faculty List

- Introduction to Device and Systems Packaging  
Prof. Rao R. Tummala, Georgia Tech
- Introduction to Devices  
Prof. Abhishek Dixit, IIT Delhi
- Fundamentals of Electrical Design  
Prof. Rohit Sharma, IIT Ropar
- Fundamentals of Thermal Technologies  
Prof. Anandaroop Bhattacharya, IIT Kharagpur
- Fundamentals of Thermo-mechanical Reliability  
Prof. Ganesh Subbarayan, Purdue University
- Fundamentals of Package Materials  
Dr. Ravi Bhatkal, MacDermid Alpha India
- Fundamentals of Package Substrates  
Dr. Venky Sundaram, 3D System Scaling LLC
- Fundamentals of Passive Components and Their Integration  
Prof. Raj Pulugurtha, Florida International University
- Fundamentals of Chip-to-Package Interconnect. & Assembly  
Prof. Vanessa Smet, Georgia Tech
- Fundamentals of Embedded & Fan Out Packaging  
Dr. Beth Keser, Zero ASIC
- Fundamentals of 3D Packaging With and without TSV  
Dr. Siddharth Ravichandran, Chipletz
- Fundamentals of RF and Millimeter-wave Packaging  
Prof. Emmanouil M Tentzeris, Georgia Tech
- Fundamentals of Opto-electronics packaging  
Dr. Ajey Jacobs, USC
- Fundamentals of MEMS and Sensors packaging  
Prof. Venkatesh KP Rao, BITS Pilani
- Fundamentals of Encapsulation, Molding & Sealing  
Dr. Jack Moon, Georgia Tech
- Fundamentals of Printed Wiring Boards  
Dr. Sundar Kamath, Sammina
- Fundamentals of Board Assembly  
Prof. Nilesh Badwe, IIT Kanpur
- Power Electronics  
Prof. Shiladri Chakraborty, IIT Bombay



# Introduction to Device and Systems Packaging

Prof Rao R Tummala

- Advisor to Government of India
- Founding Director & Emeritus Professor
- 3D Electronic Systems Packaging Research Center(PRC)
- Georgia Institute of Technology, Atlanta, GA, USA
- Former IBM Fellow & Director of Adv. Pkg. Tech. Lab @ IBM

**[rtummala@ece.gatech.edu](mailto:rtummala@ece.gatech.edu)**

# **Greetings from Indian DSPS Team**

A vision for India to be a Global System Foundry Hub

With Advances in Design, Semiconductor, Packaging and System Technologies and Their Integration.

**Prof. Rao R. Tummala**

Advisor to Ministry of Electronics and IT (MeitY)

**Emeritus Professor and Founding Director, Georgia Tech**

**IBM Fellow & Director of Packaging, IBM**



इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी मंत्रालय  
MINISTRY OF  
ELECTRONICS AND  
INFORMATION TECHNOLOGY  
सर्वदा जरूरी



इंडिया सेमीकंडक्टर मिशन  
India Semiconductor Mission  
Catalyzing India's Semiconductor Ecosystem

Indian DSPS R&D Team. Together, We Can.

Competitive Factor	Strengths/Weaknesses
Market Size	Strong
Educated Workforce in Basic Sciences & Engineering	Strong
Design Expertise & Resources	Strong
R&D Infrastructure, Expertise & Resources	Weak
Manufacturing Infrastructure, Expertise & Resources	Weak
Investment Opportunities in R&D	Strong
Investment Opportunities in Manufacturing	Strong



Strong



Fair



Weak

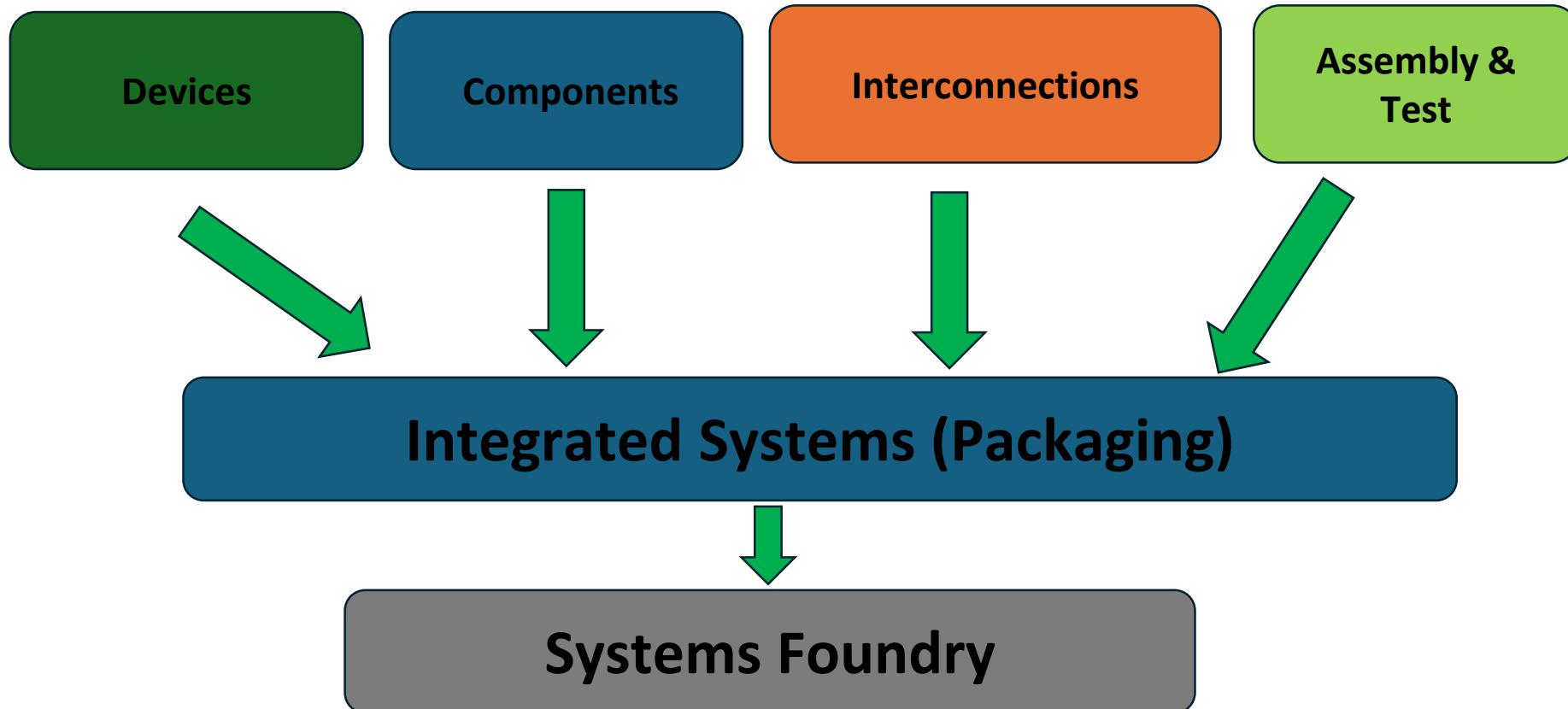


इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी मंत्रालय  
MINISTRY OF  
ELECTRONICS AND  
INFORMATION TECHNOLOGY  
सरकार द्वारा



इंडिया सेमीकंडक्टर मिशन  
India Semiconductor Mission  
Catalyzing India's Semiconductor Ecosystem

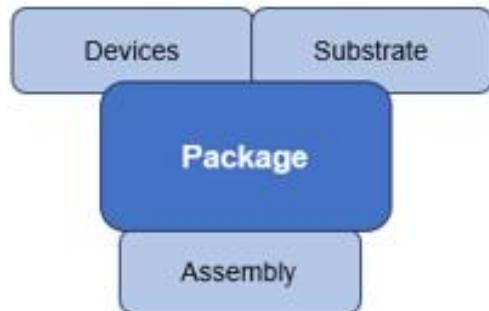
Indian DSPS R&D Team. Together, We Can.



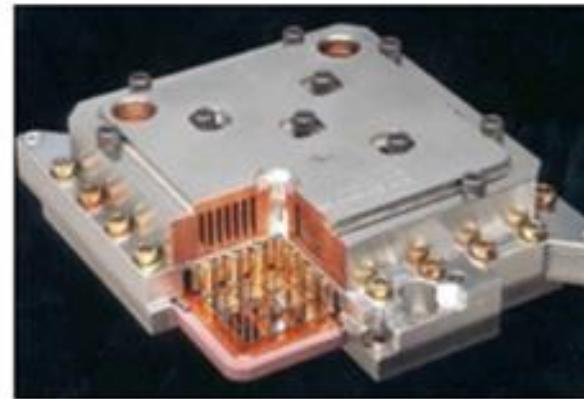
**Past**



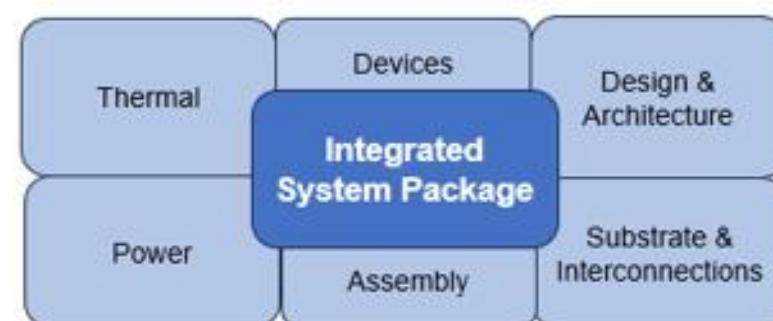
IC Assembled on a Package Substrate



**Future**



Interconnected Module



# Introduction to Device and Systems Packaging

- Why the course and why now in India?
- What is Packaging and Why?
  - Device level & System Level
- Anatomy of a Packaged- system
- Devices and Moore's law
- Four Technology Waves Since 1960s
- Moore's Law for ICs and Tummala's Law for Packaging
- Evolution of Packaging Technologies
- Future Outlook
- How the Course is Organized?
- Introducing PDC Expert Tutors
- What can you expect from the course?

# Semiconductors , Packaging and Systems in Our Lives

## Mobile/Wearable

[Galaxy S22 Ultra ]



[ iPad Pro ]



[ Galaxy Watch ]



Source : ko.ifixit.com/News/57567/galaxy-s22-teardowns-apple-is-making-samsung-sweat  
ryueyes11.tistory.com/6335  
gigglehd.com/gg/mobile/4400521

## Data Center for AI/Deep Learning

[ ChatGPT]

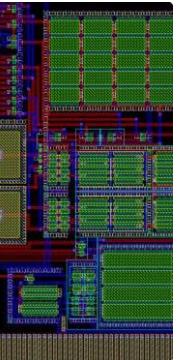
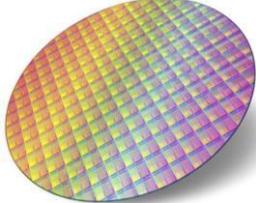
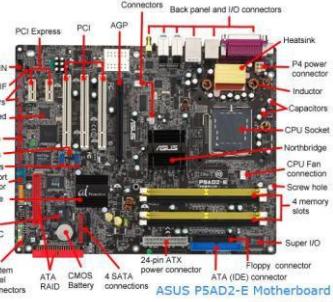
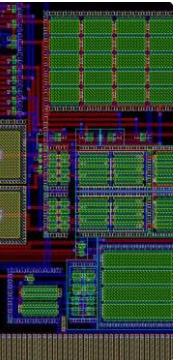
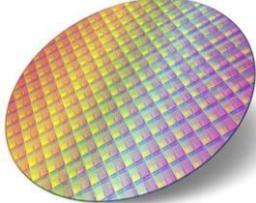
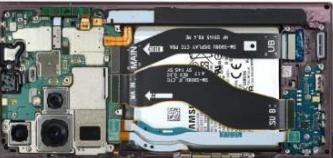
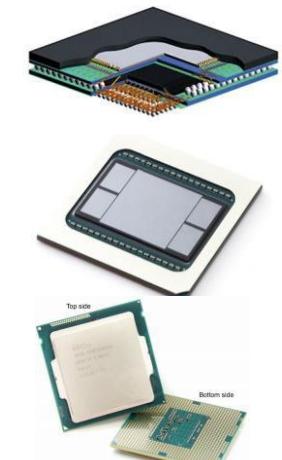


- CPU
- GPU
- NPU
- Server DRAM/NAND



Source : [www.tomshardware.com/news/google-cloud-socs-uri-frank](http://www.tomshardware.com/news/google-cloud-socs-uri-frank)

# What Are Semiconductors, Packaging and Systems?

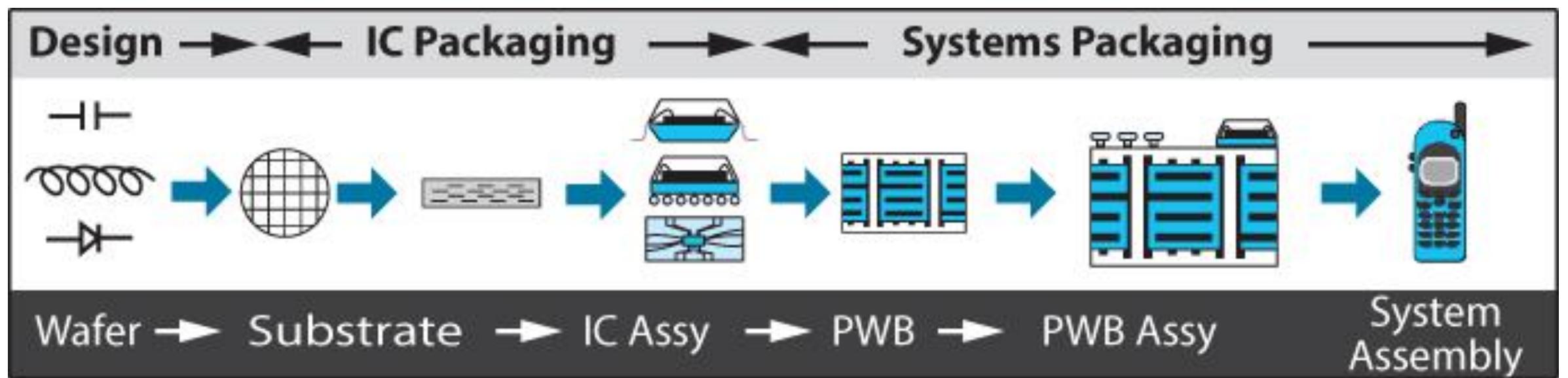
Semiconductor		System Board	Electronics
Design	Wafer		
		 <p>ASUS P5AD2-E Motherboard <a href="http://www.computerhope.com/argon/m/mothboar.htm">www.computerhope.com/argon/m/mothboar.htm</a></p> <p>Labels on diagram:</p> <ul style="list-style-type: none"><li>3-pin fan Connectors</li><li>Back panel and I/O connectors</li><li>Heatsink</li><li>P4 power connector</li><li>Inductor</li><li>Capacitors</li><li>CPU Socket</li><li>Northbridge</li><li>CPU Fan connection</li><li>Screw hole</li><li>4 memory slots</li><li>Super I/O</li><li>Floppy connector</li><li>ATA (IDE) connector</li><li>24-pin ATX power connector</li><li>4 SATA connections</li><li>ATA RAID CMOS Battery</li><li>System panel connectors</li><li>PCI Express PCI AGP</li><li>CD-IN SPDIF</li><li>1394 Headers integrated circuit</li><li>SATA RAID</li><li>Jumpers</li><li>USB headers Serial port connector</li><li>Southbridge</li><li>FWH in PLCC</li></ul>	 
			 
<b>Package</b>			
			

**Source:** <https://any silicon.com/ic-design/>

**Source:**  
[https://www.itwissen.info/en/package\\_118544.html#gsc.tab=0](https://www.itwissen.info/en/package_118544.html#gsc.tab=0)  
[http://aseglobal.com/en/technology/advanced\\_25dic](http://aseglobal.com/en/technology/advanced_25dic)  
<https://superuser.com/questions/324284/what-is-meant-by-the-terms-cpu-core-die-and-package>

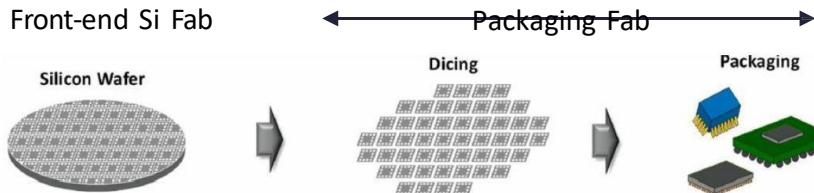
[ko.ifixit.com/News/57567/galaxy-s22-teardowns-apple-is-making-samsung-sweat](http://ko.ifixit.com/News/57567/galaxy-s22-teardowns-apple-is-making-samsung-sweat)

System Starts with Design to Wafers to ICs to Packages to Boards and to systems



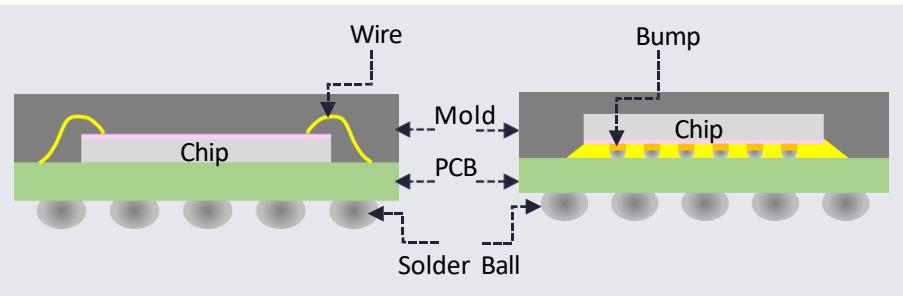
# Traditional Package Assembly

## Traditional Packaging



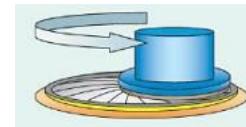
In traditional package, package technology has been separated from front-end Si technology

## Example



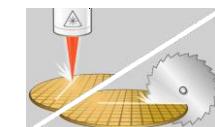
## Key Technologies

### Back grinding



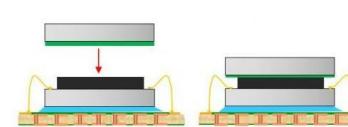
Source :Disco website

### Dicing



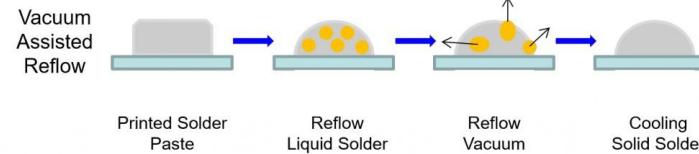
Source :Accretech website

### Die attach



<https://polymerinnovationblog.com/polymers-electronics-part-thirteen-die-attach-adhesives-part-6/>

### Solder Paste Reflow



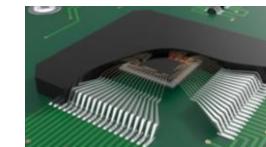
<https://hellerindustries.com/void-free-soldering/>

### Underfill



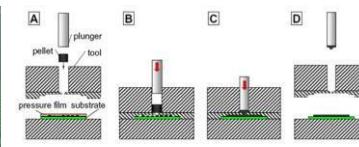
<https://www.tctech.co.kr>

### Wire-bonding



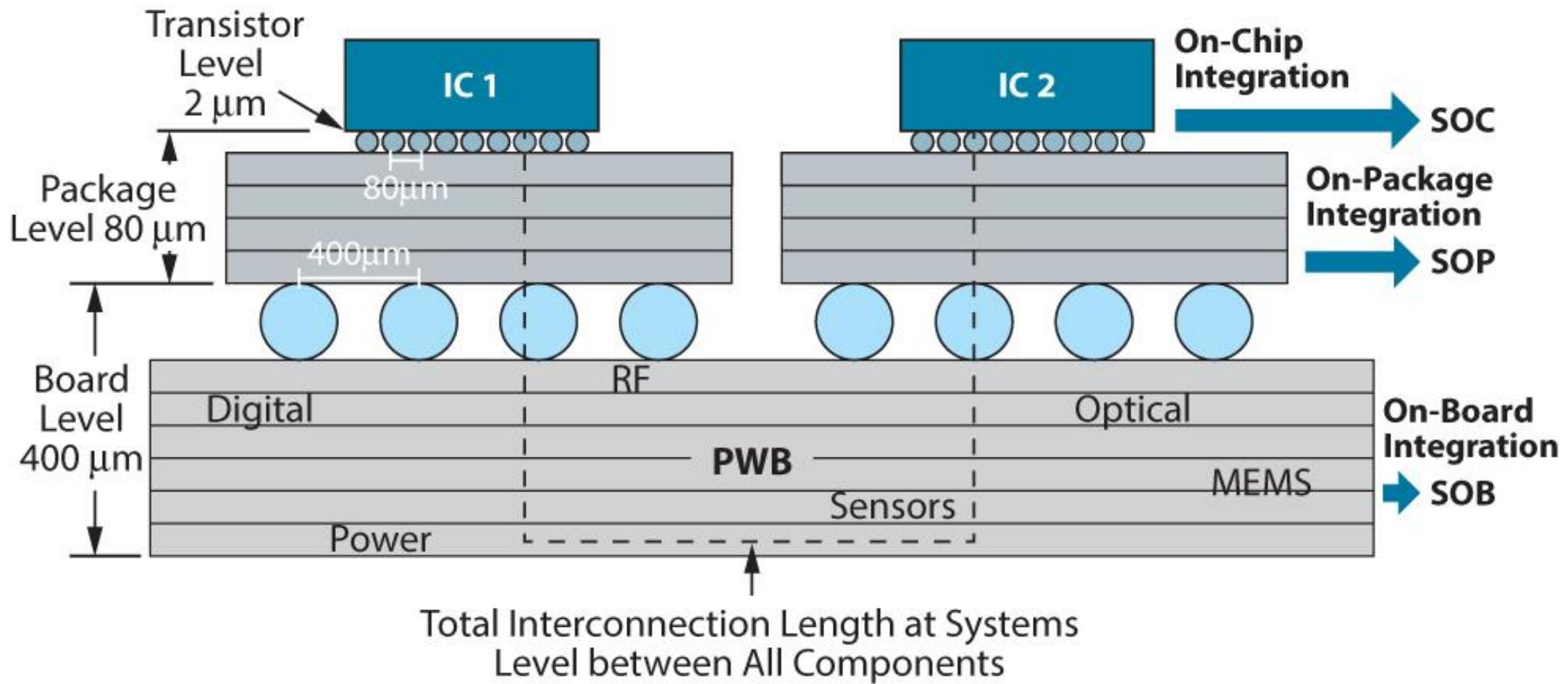
<https://www.henkel-adhesives.com/kr/ko/industries/electronics/semiconductor-packaging/wirebond-semiconductor-packaging.html>

### Molding



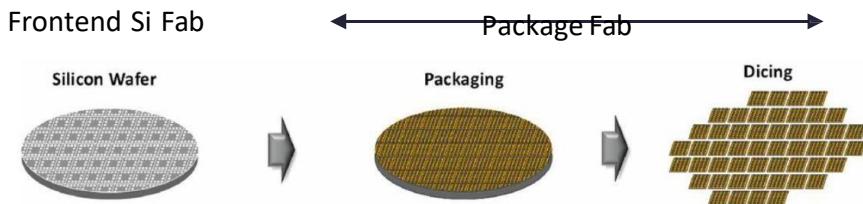
<https://www.sensorprod.com/glossary/prescale/prescale.php>

# Traditional Packaging: Bulky & Low Performance



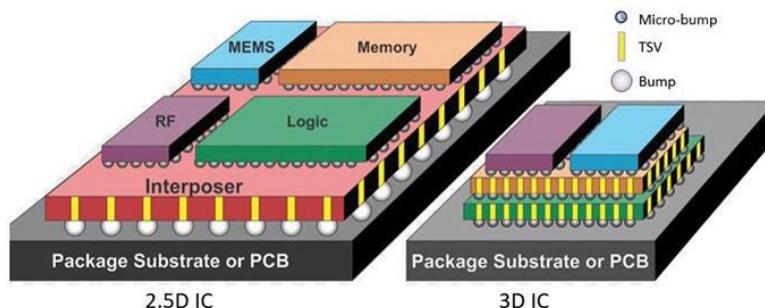
# Advanced Package (Wafer Level Package)

# Advanced Packaging



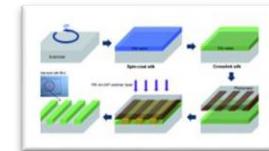
Use of Si front end technology (RDL, TSV, microbump) allows very fine pitch connection for high I/O counts and multiple chips which are stacked side by side or vertically (3D) in a package.

## Example



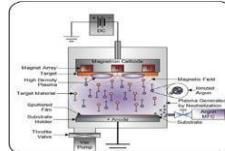
## Key Technologies

## 1 Lithography.



<https://pubs.rsc.org/en/content/articlelanding/2016/ra/c6ra04516b>

2 PVD, Sputter.



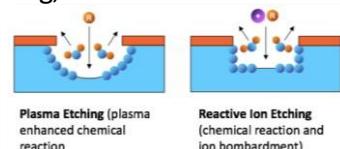
<https://www.semico.com/news/94-what-is-dc-sputtering>

### 3. Electroplating



<https://byjus.com/chemistry/electroplating-process/>

#### 4. Etching, Plasma etch & Wet etch



<https://materean.com/dpn-etching/>

**Reduction in noncompliance**

<https://materean.com/dry-etching/>

[https://scienceon.kisti.re.kr/srch/selectPORsRchReport  
do?cn=TRKO201400028228](https://scienceon.kisti.re.kr/srch/selectPORsRchReport.do?cn=TRKO201400028228)

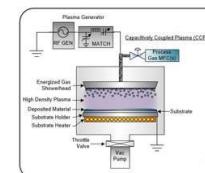
[https://scienceon.kisti.re.kr/srch/selectPORsRchReport  
.do?cn=TRKO201400028228](https://scienceon.kisti.re.kr/srch/selectPORsRchReport.do?cn=TRKO201400028228)

6 Bonding



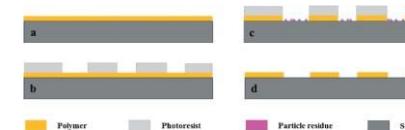
<https://www.3dincites.com/2018/04/hybrid-bonding-from-concept-to-commercialization/>

7. CVD



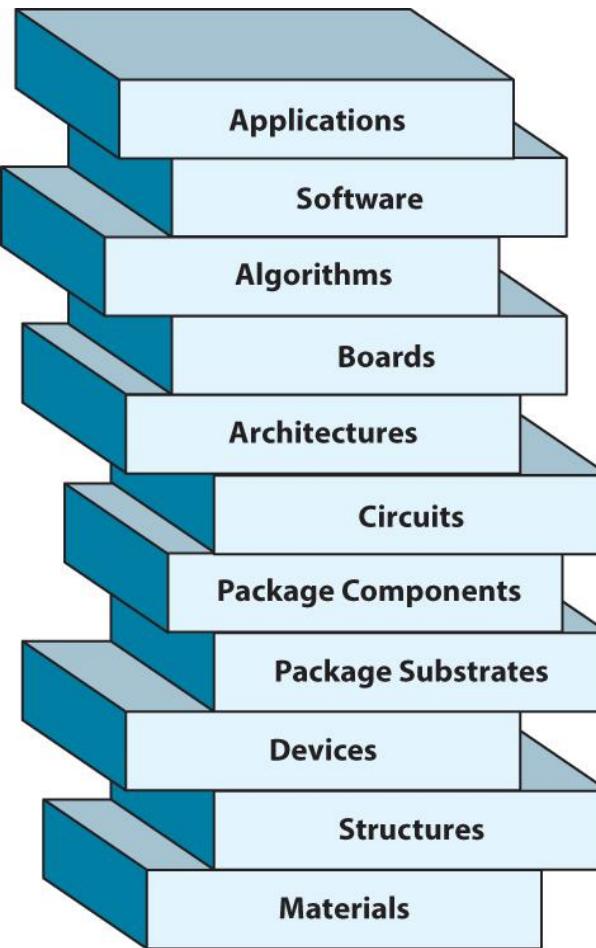
<https://www.semore.com/news/111-what-is-plasma-enhanced-chemical-vapor-deposition-pecv>

## 8 Striping Wet/Dry

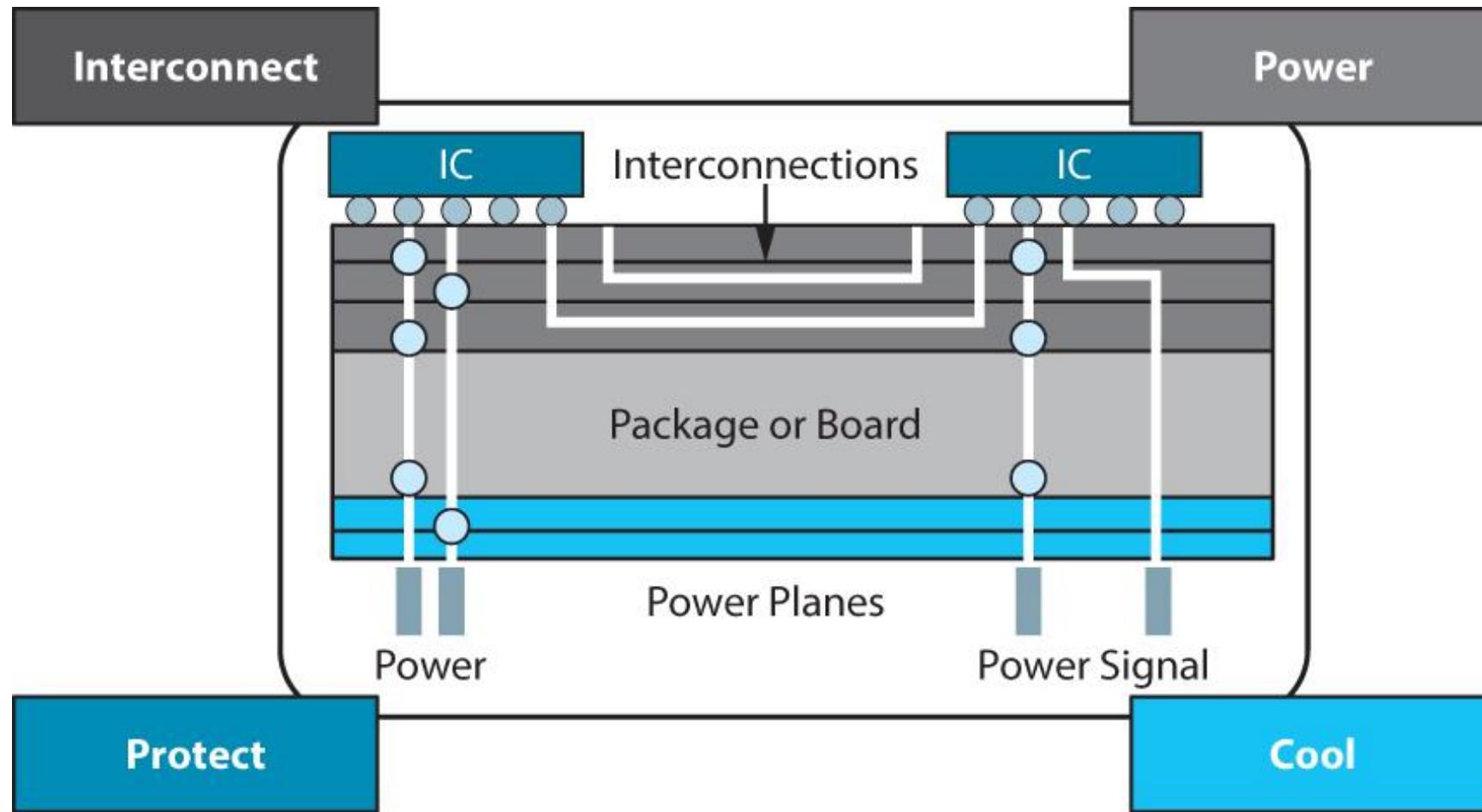


[https://www.researchgate.net/figure/Fabrication-process-of-polymer-etching-by-ICP-a-polymer-deposition-b\\_fig1\\_301705258](https://www.researchgate.net/figure/Fabrication-process-of-polymer-etching-by-ICP-a-polymer-deposition-b_fig1_301705258) dry

# Electronic Systems Require Many Technologies



# What is Packaging? Package serves four functions

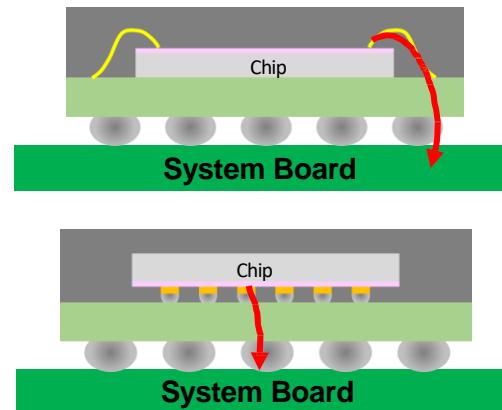


# Basic Functions of Package

## Interconnection

### Electric interconnection between chip and system board

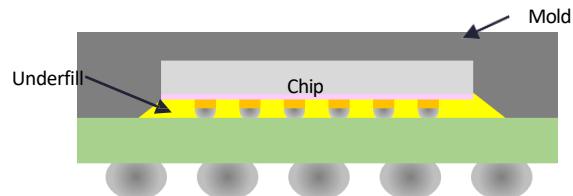
- Scaling down dimension from chip (nm) to PCB (mm) interconnect
- Input/output (I/O) signal & power connect



## Protection

### Mechanical & electrical protection

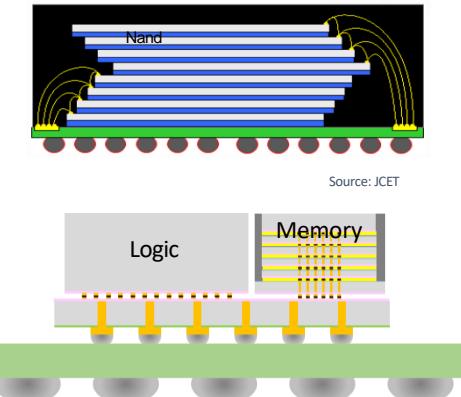
- Mold, or underfill for protection
- Enhance long-term reliability
  - . Mechanical reliability :Humidity, Temperature, Damage (Drop, vibration, etc)
  - . Electrical Reliability :Electrostatic, etc.



## Integration

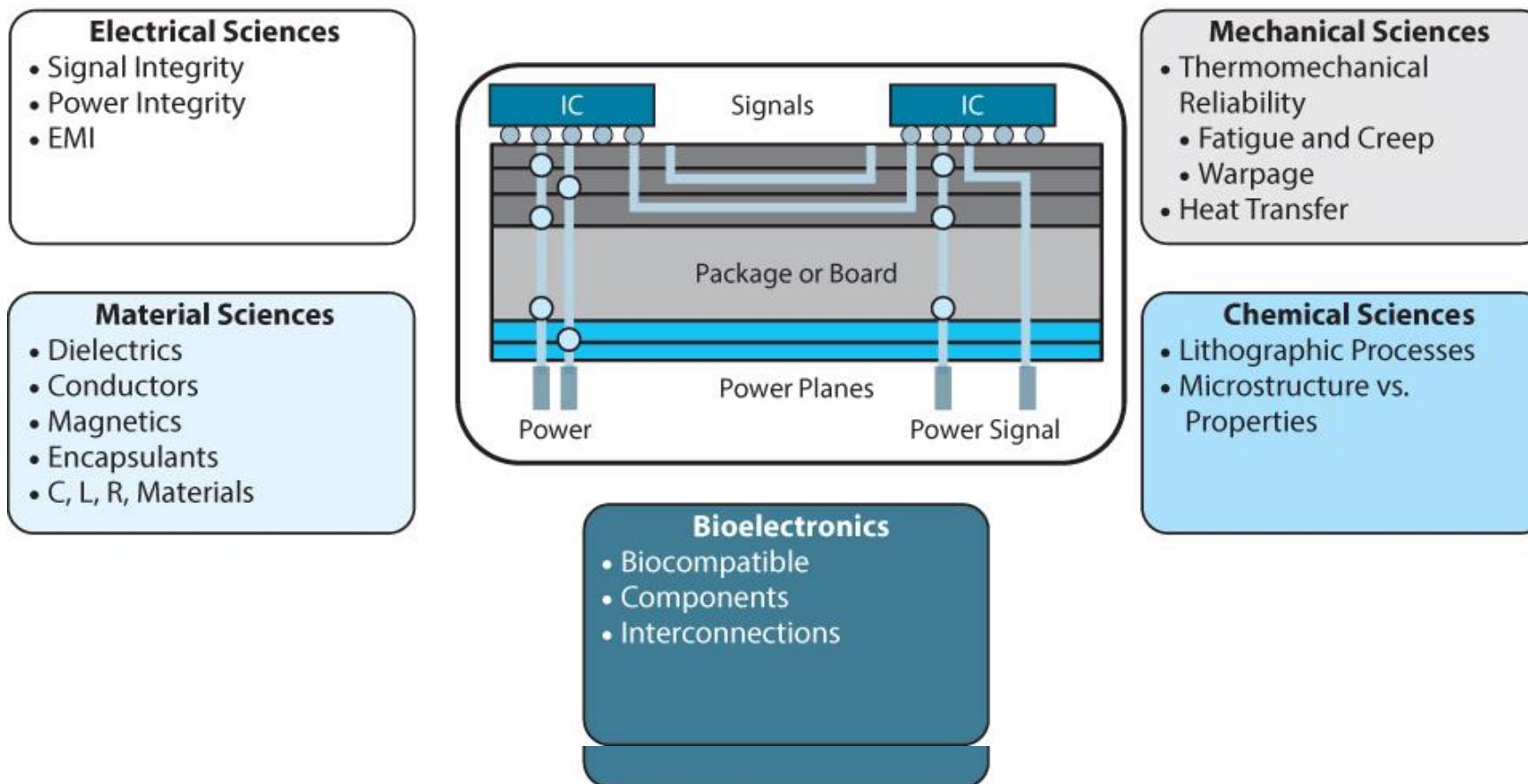
### Homo/Heterogenous integration

- Increase the density of the same device
  - . DRAM, NAND
- Increase the performance of devices
  - . Integration of Logic and Memory



# Interdisciplinarity of Electronic systems

## Interdisciplinarity of Electronics Systems



# Why Package Any Device? Two Reasons

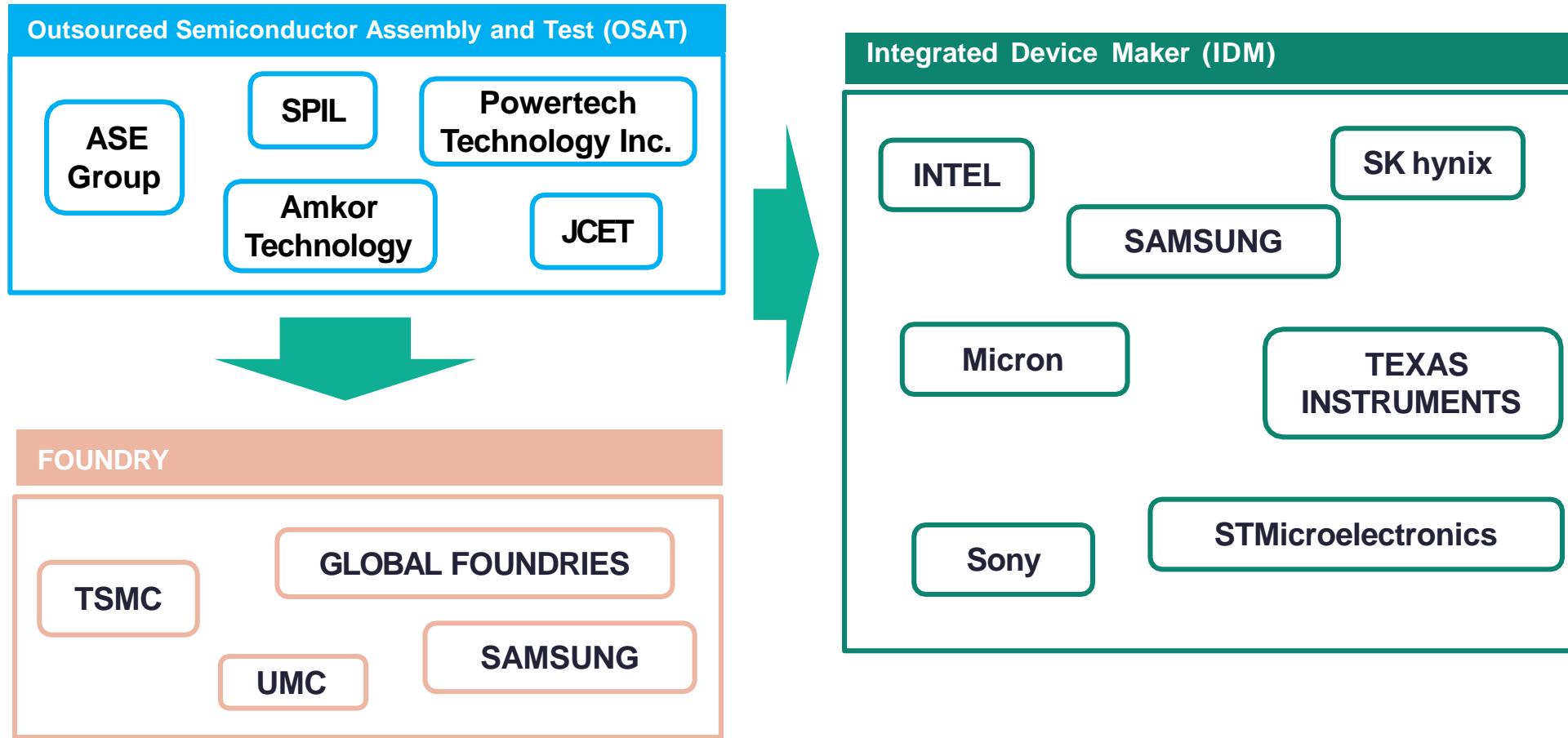
## Two Reasons for IC Packaging

- 
- ```
graph TD; A[Two Reasons for IC Packaging] --> B[1. Guarantee or Certify Goodness of Die]; A --> C[2. SMT to Board]
```
1. Guarantee or Certify Goodness of Die
  2. SMT to Board

## Challenges

- 
- ```
graph TD; A[Challenges] --- B[ ]
```
- High Cost-sensitive
  - Size-sensitive for Mobile
  - Reliability Challenges Due to Huge CTE-Mismatch
  - Unaffordable Advances in Materials, Thermal, etc.

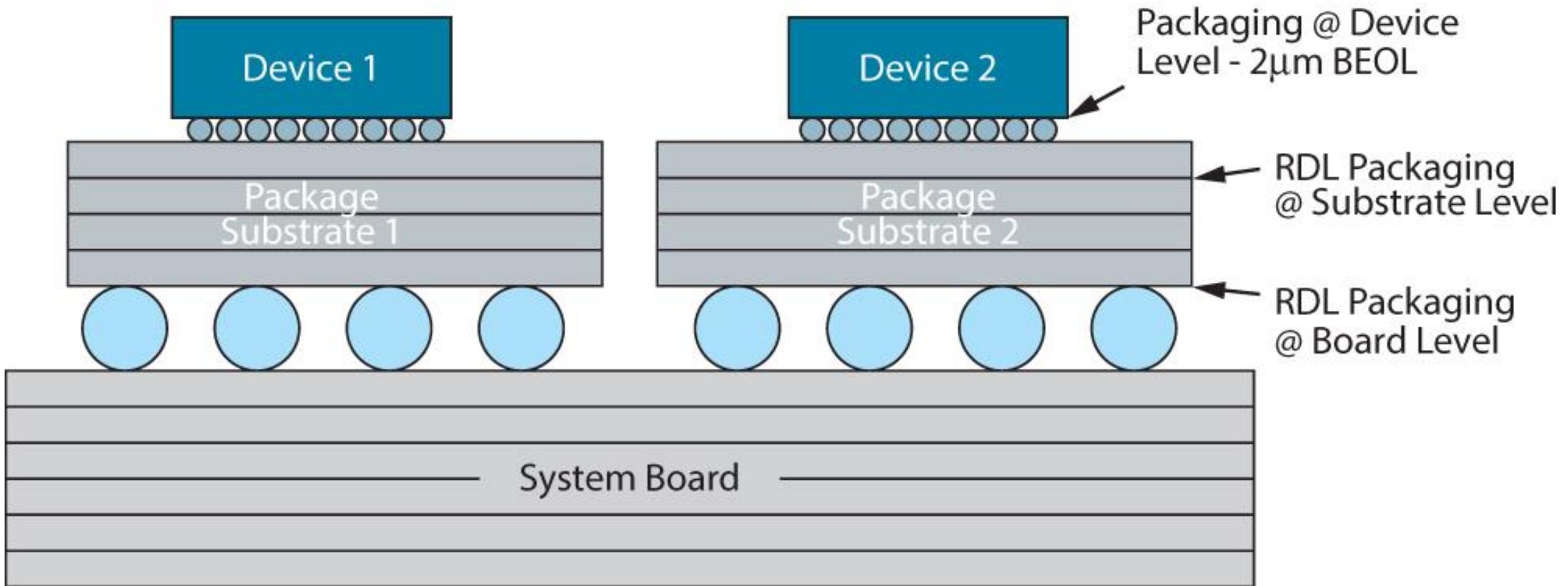
# Some Major Players in Advanced Packaging Market



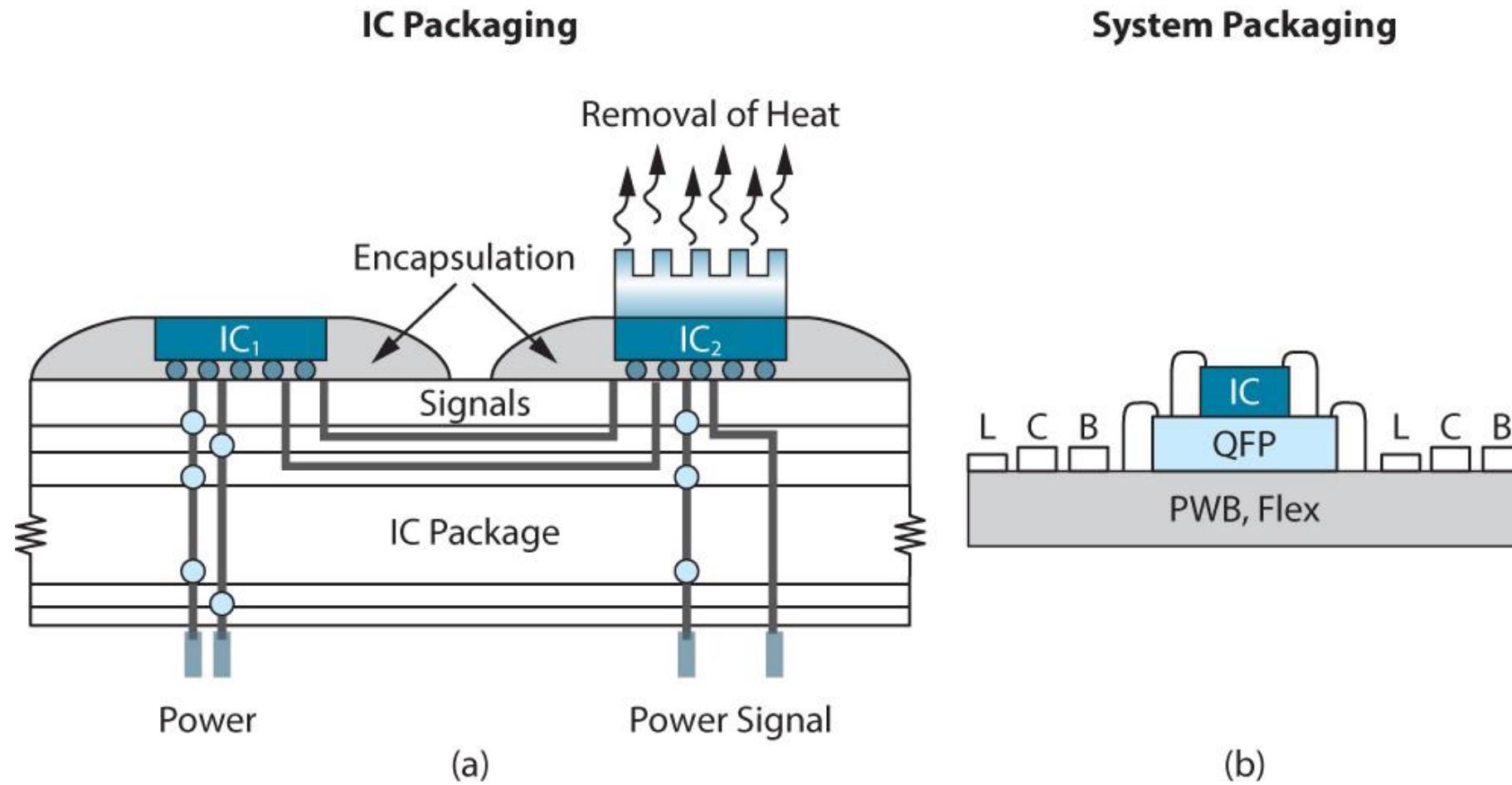
# Introduction to Device and Systems Packaging

- Why the course and why now in India?
- What is Packaging and Why?
  - Device level & System Level
- **Anatomy of a Packaged- system**
- Devices and Moore's law
- Four Technology Waves
- Moore's Law for ICs and Tummala's Law for Packaging
- Evolution of Packaging Technologies
- Future Outlook
- How the Course is Organized?
- Introducing PDC Expert Tutors
- What can you expect from the course?

# Anatomy of a Packaged- electronic System



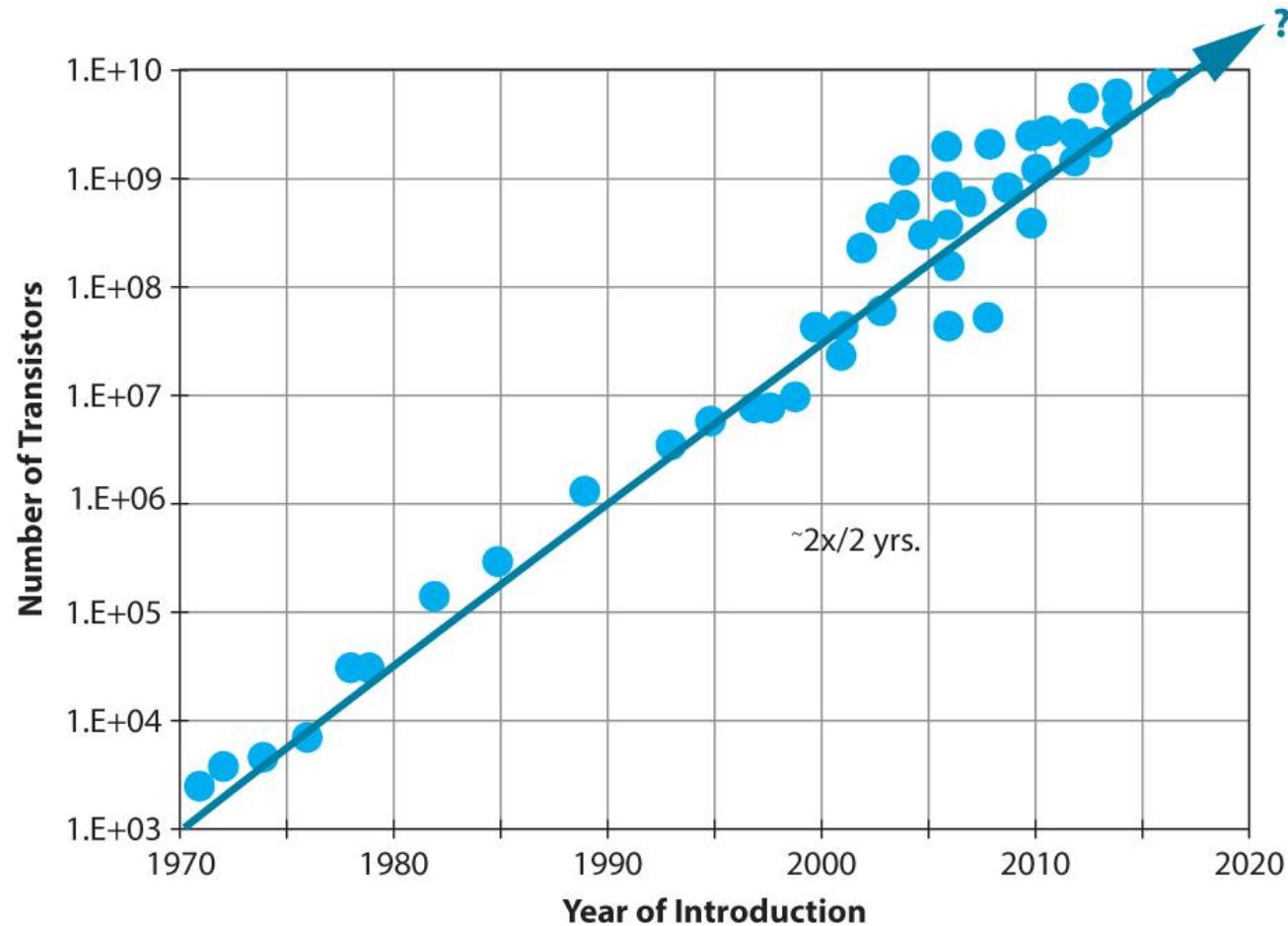
# Device Packaging Vs. Systems Packaging



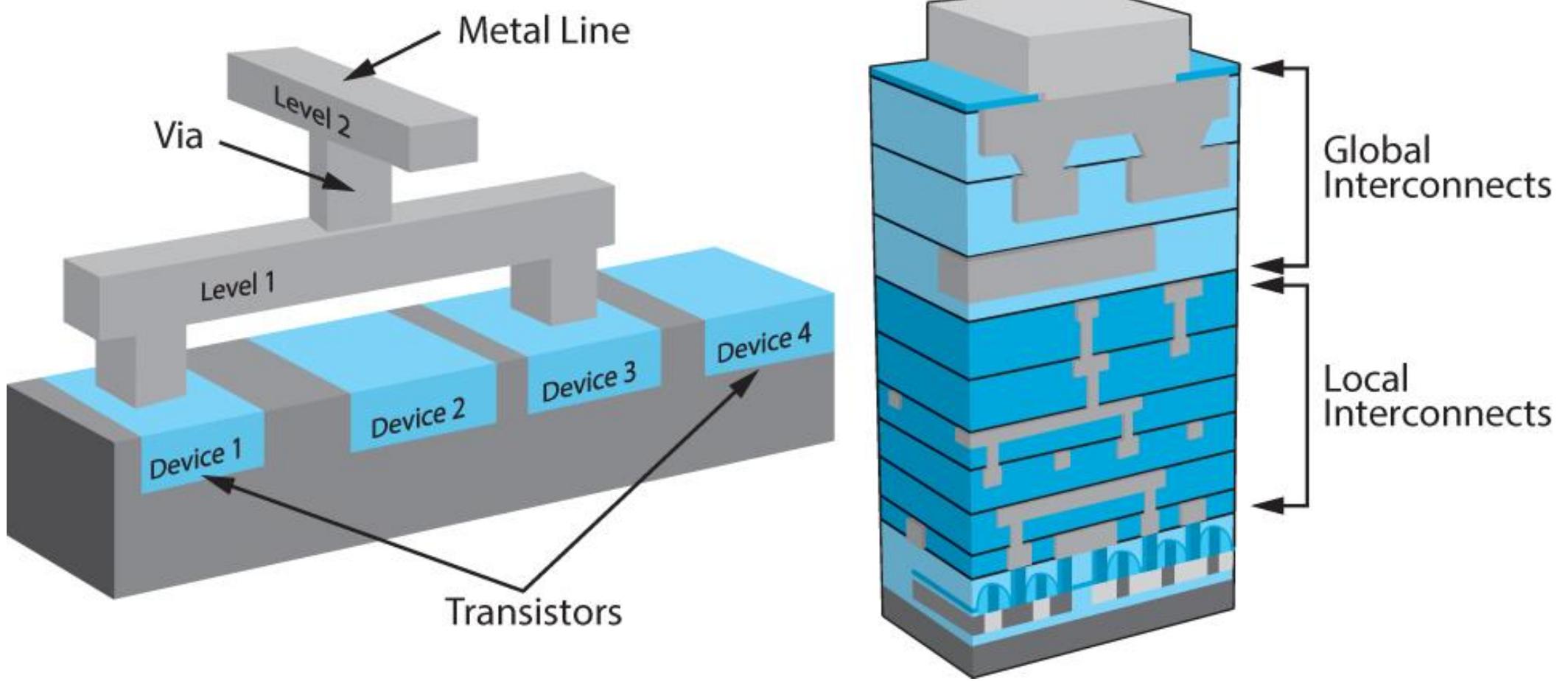
# Introduction to Device and Systems Packaging

- Why the course and why now in India?
- What is Packaging and Why?
  - Device level & System Level
- Anatomy of a Packaged- system
- **Devices and Moore's law**
- Four Technology Waves
- Moore's Law for ICs and Tummala's Law for Packaging
- Evolution of Packaging Technologies
- Future Outlook
- How the Course is Organized?
- Introducing PDC Expert Tutors
- What can you expect from the course?

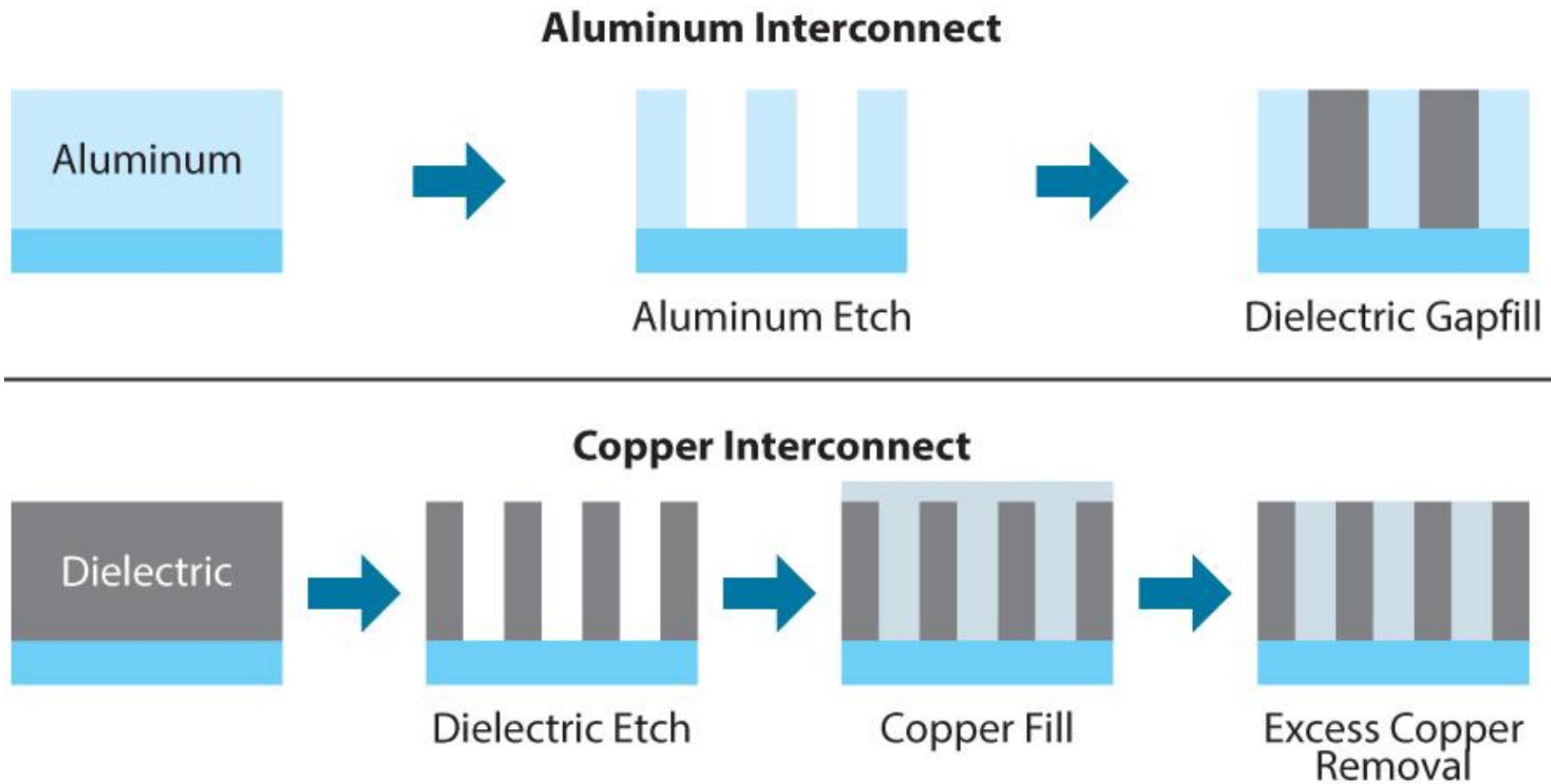
# Moore's Law is About Doubling Transistors Every 18-24 Months



# On-Chip or BEOL Interconnections

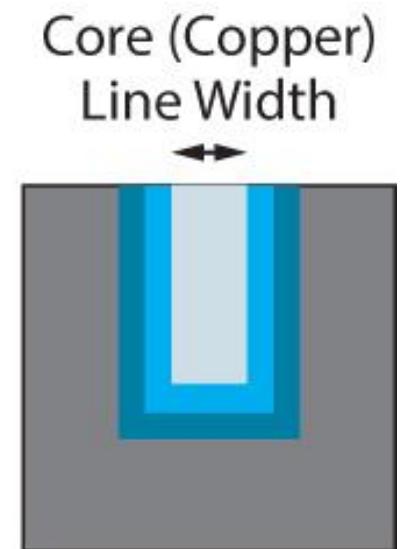
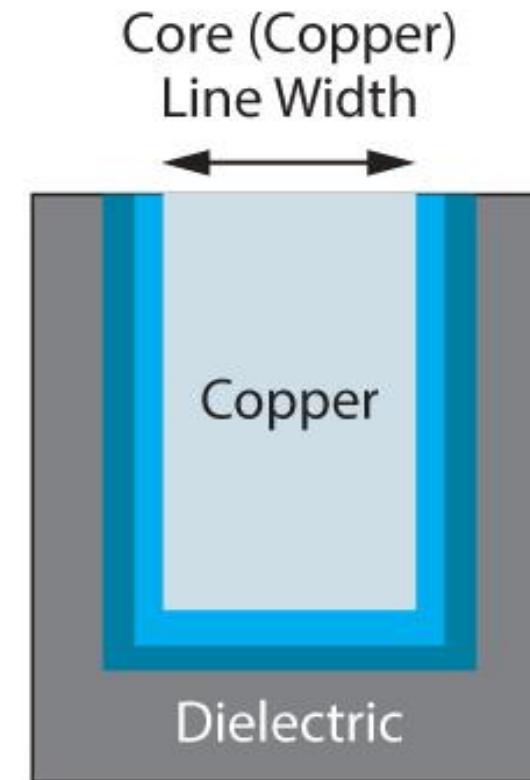
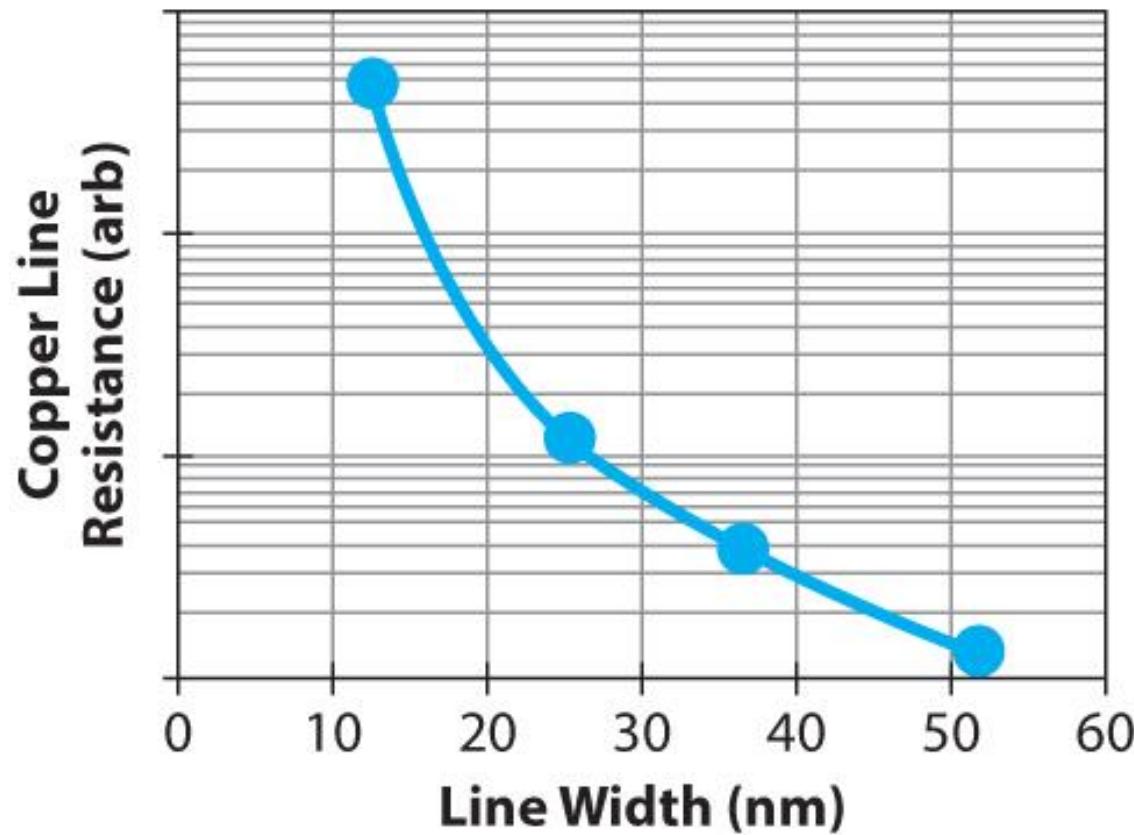


# On-Chip or BEOL Wiring Fabrication

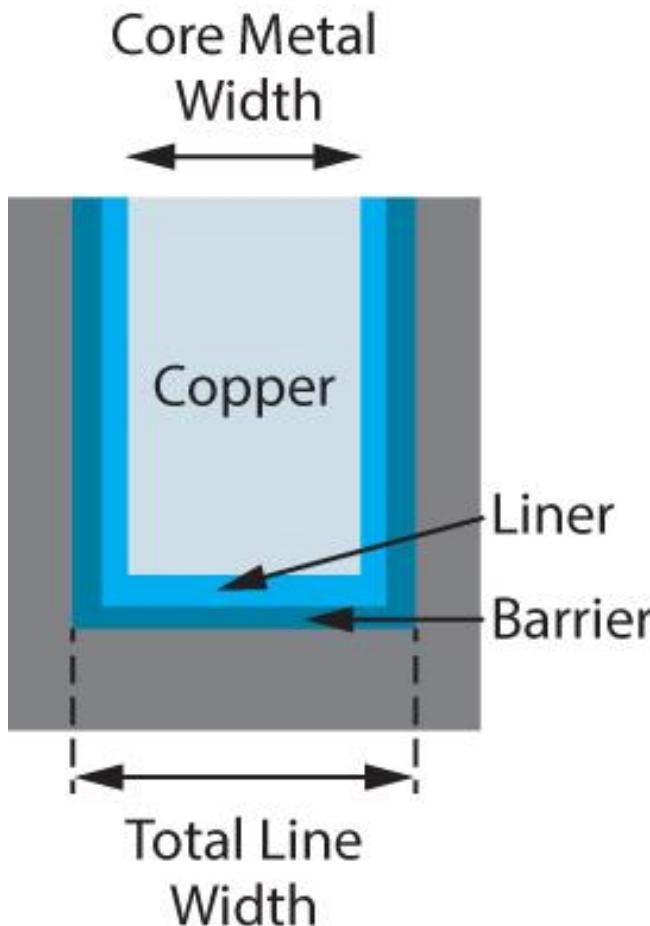


# Resistance of BEOL Wiring as Function Line Width

**Higher Resistance with Smaller Line Width**

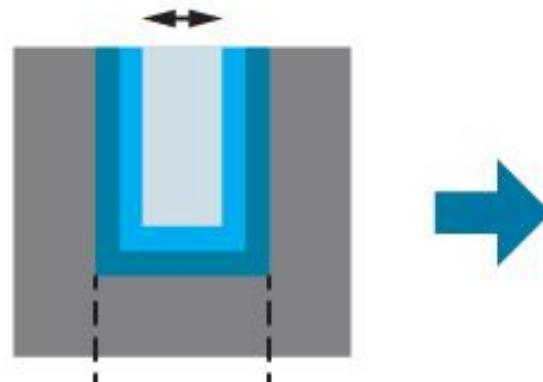


# Copper Interconnections or TSV Require Liner, Barrier and Seed Layer



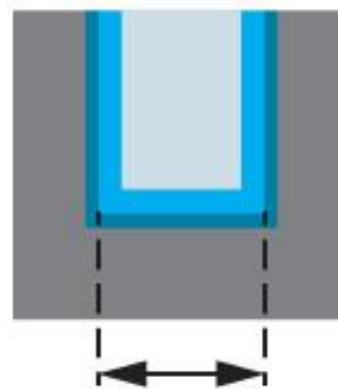
## Simple Shrink Leads to Line Resistance Issues

Not Enough Room  
for Core Metal

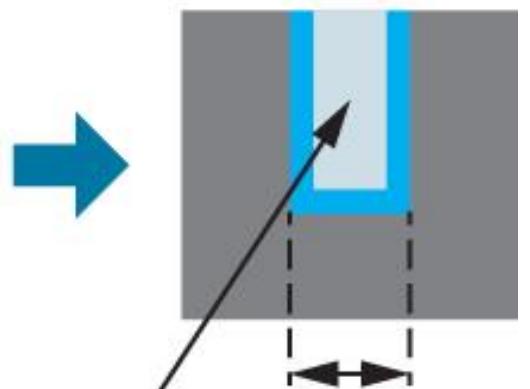


## Lower Line Resistance Options

Alternate  
Barrier



No  
Barrier



Alternate  
Metal

# Introduction to Device and Systems Packaging

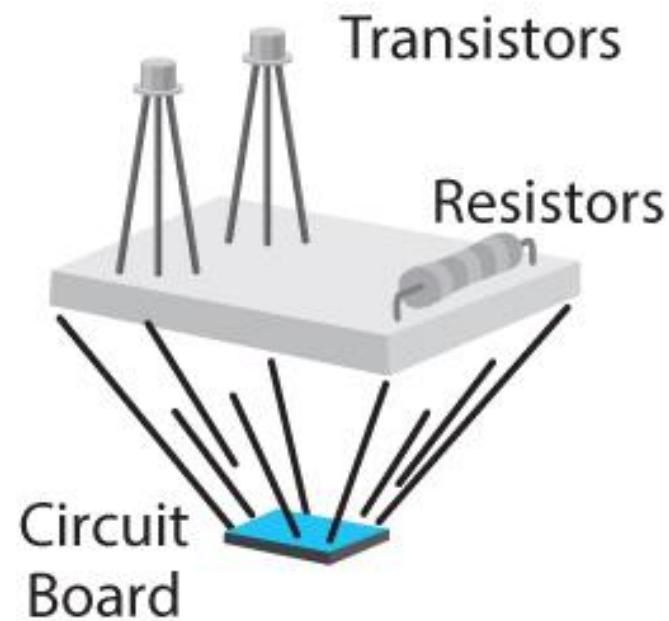
- Why the course and why now in India?
- What is Packaging and Why?
  - Device level & System Level
- Anatomy of a Packaged- system
- Devices and Moore's law
- **Four Technology Waves**
- Moore's Law for ICs and Tummala's Law for Packaging
- Evolution of Packaging Technologies
- Future Outlook
- How the Course is Organized?
- Introducing PDC Expert Tutors
- What can you expect from the course?

# The Invention of the 1<sup>st</sup> Integrated Circuit

**Transistor**

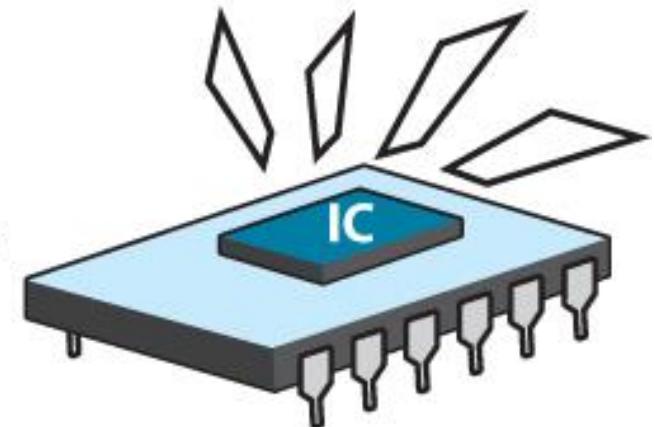


**Rudimentary IC**

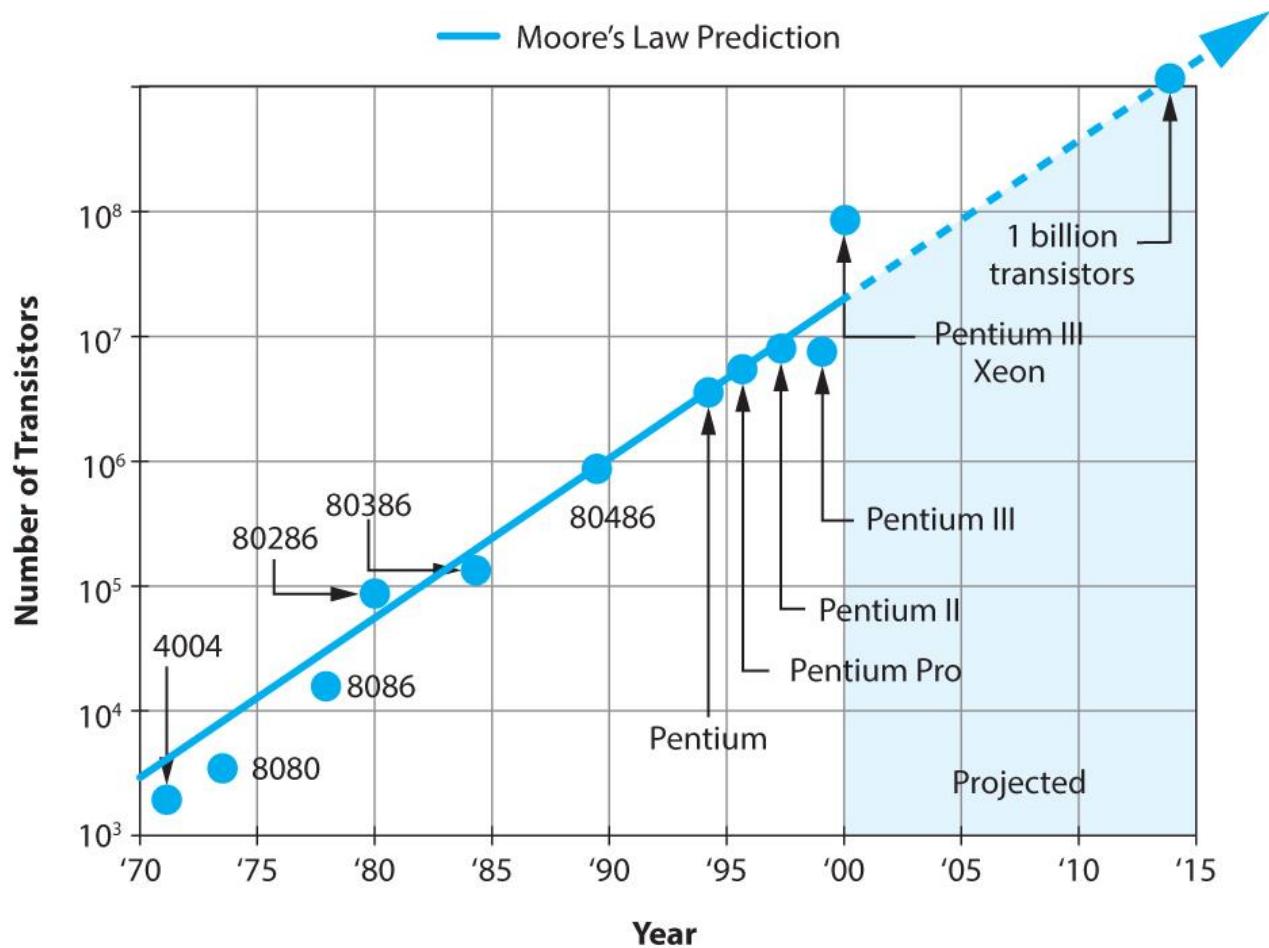


Integration  
of Transistors

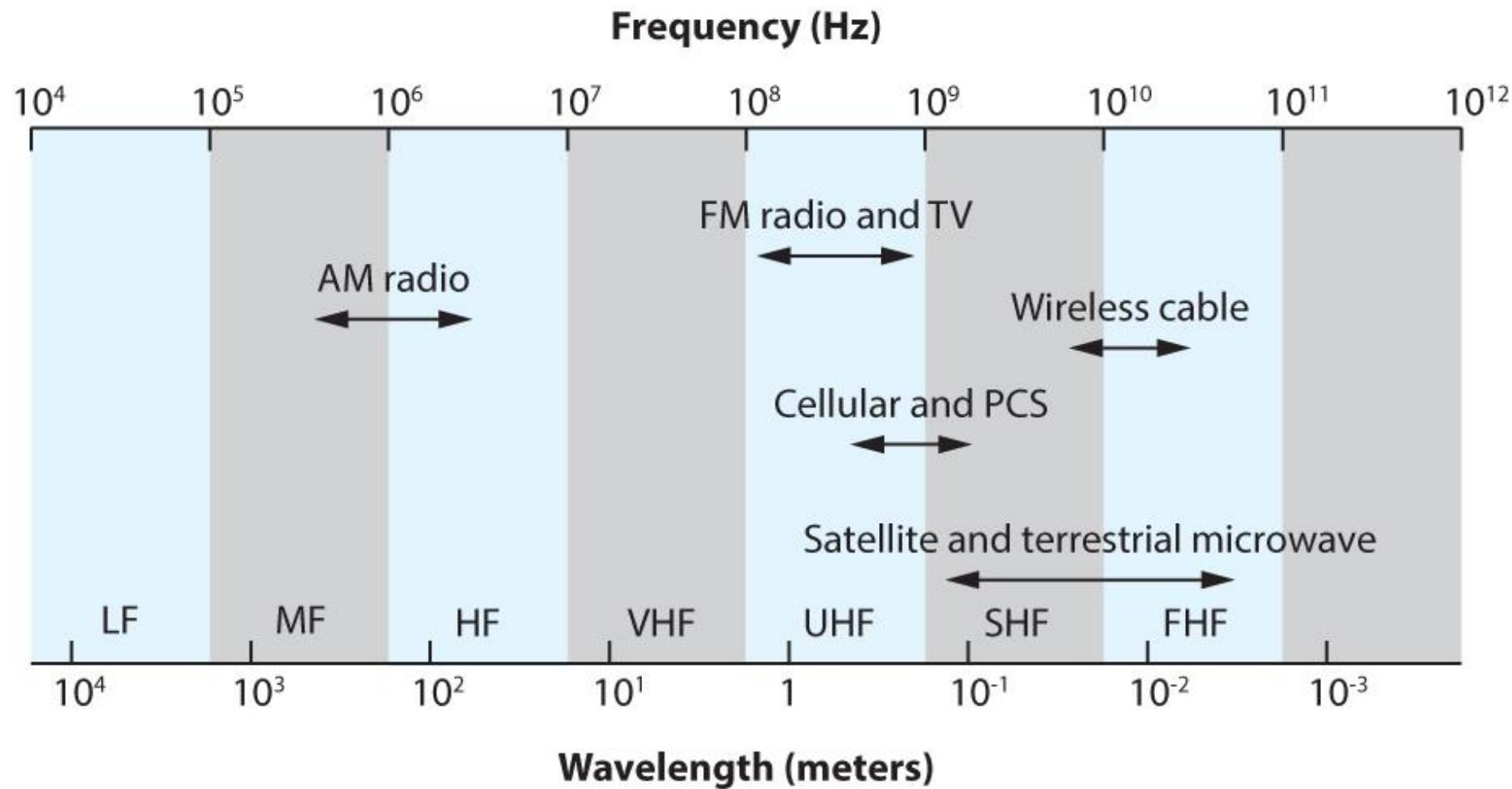
**Packaged IC**



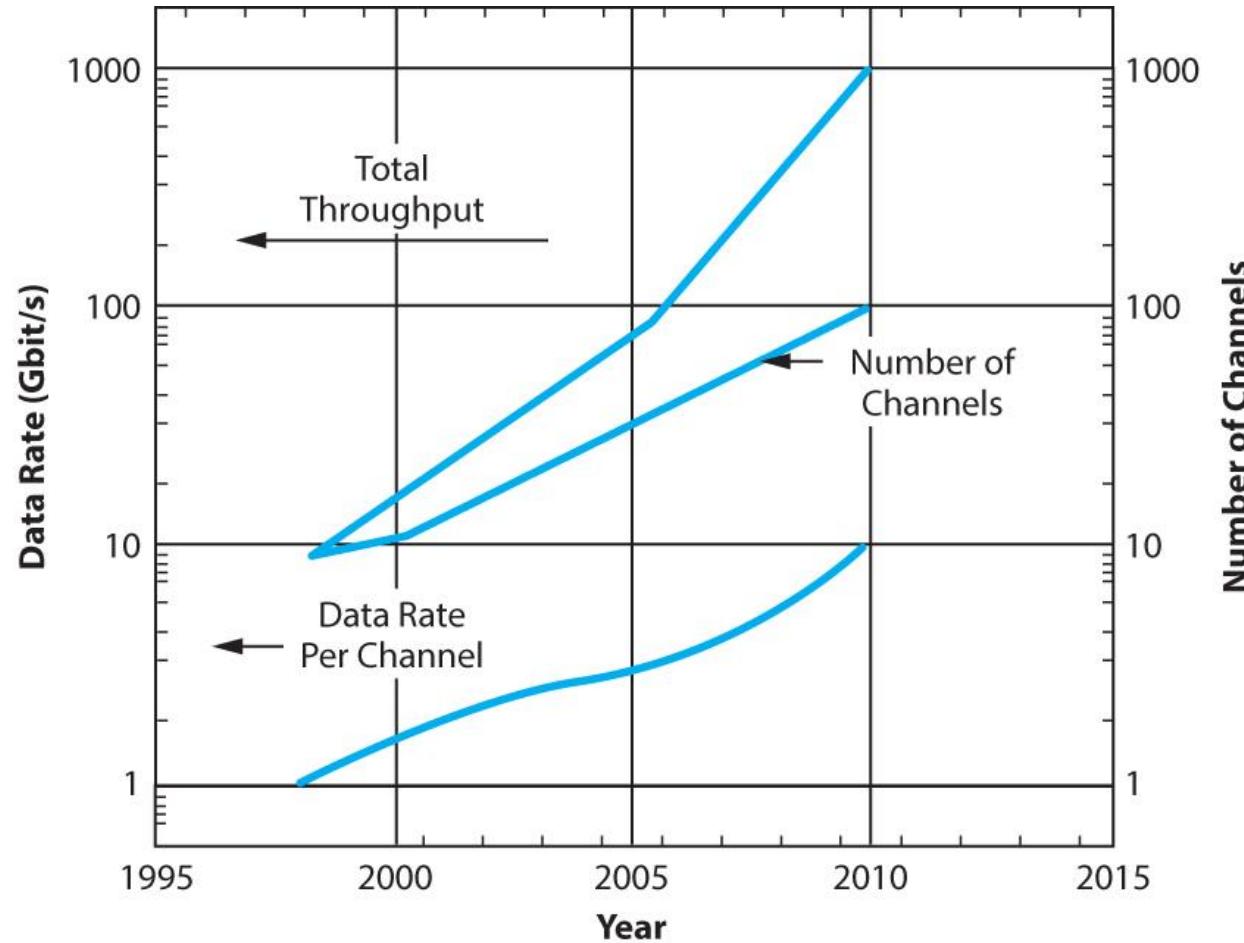
# Moore's Law Predicts The IC Integration to Double Every 18-24 months



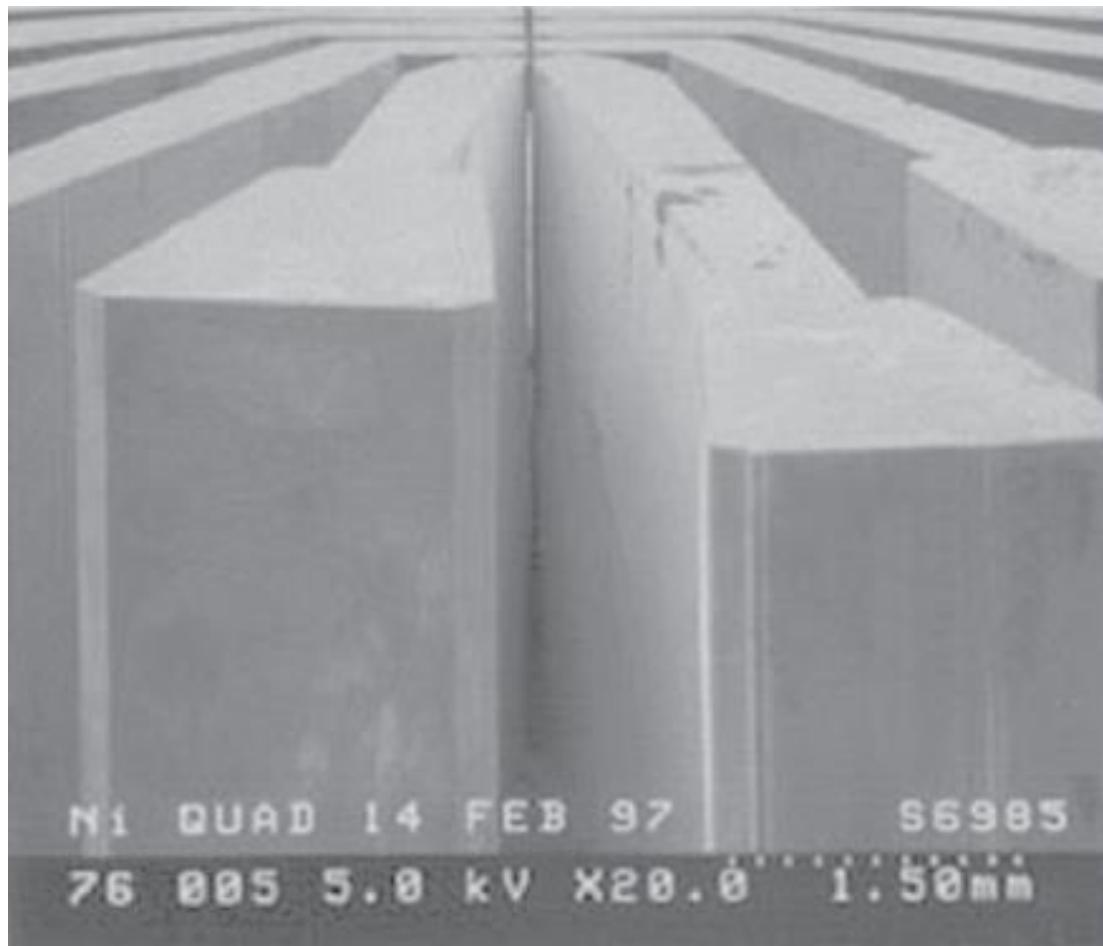
# RF and Wireless: Wavelength and Applications



# Potential of Optoelectronic Technology to Terabits Per Second



# Example of Mems Device

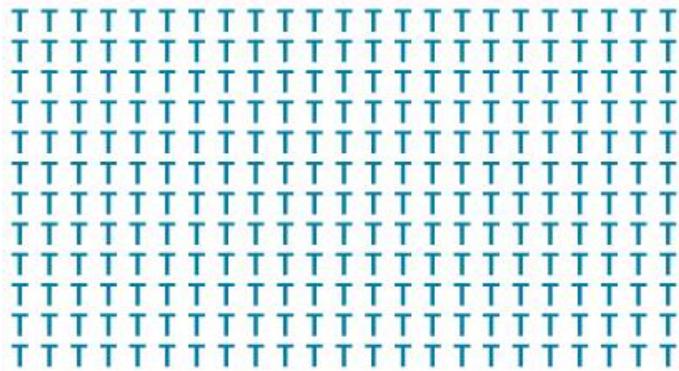


# Introduction to Device and Systems Packaging

- Why the course and why now in India?
- What is Packaging and Why?
  - Device level & System Level
- Anatomy of a Packaged- system
- Devices and Moore's law
- Four Technology Waves
- **Moore's Law for ICs and Tummala's Law for Packaging**
- Evolution of Packaging Technologies
- Future Outlook
- How the Course is Organized?
- Introducing PDC Expert Tutors
- What can you expect from the course?

# Concept of Moore's Law for Packaging. Tummala's Law Packaging

**Moore's Law for ICs**

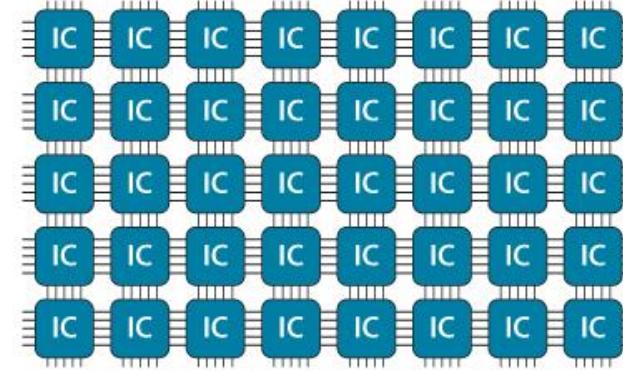


## **Large IC**

*Largest IC with smallest transistors at low performance and high cost*

- 5-30 Billion transistors
- 30-50 miles of wiring
- Low transistor performance
- High RC interconnect delays
- High design and manufacturing cost

**Moore's Law for Packaging**

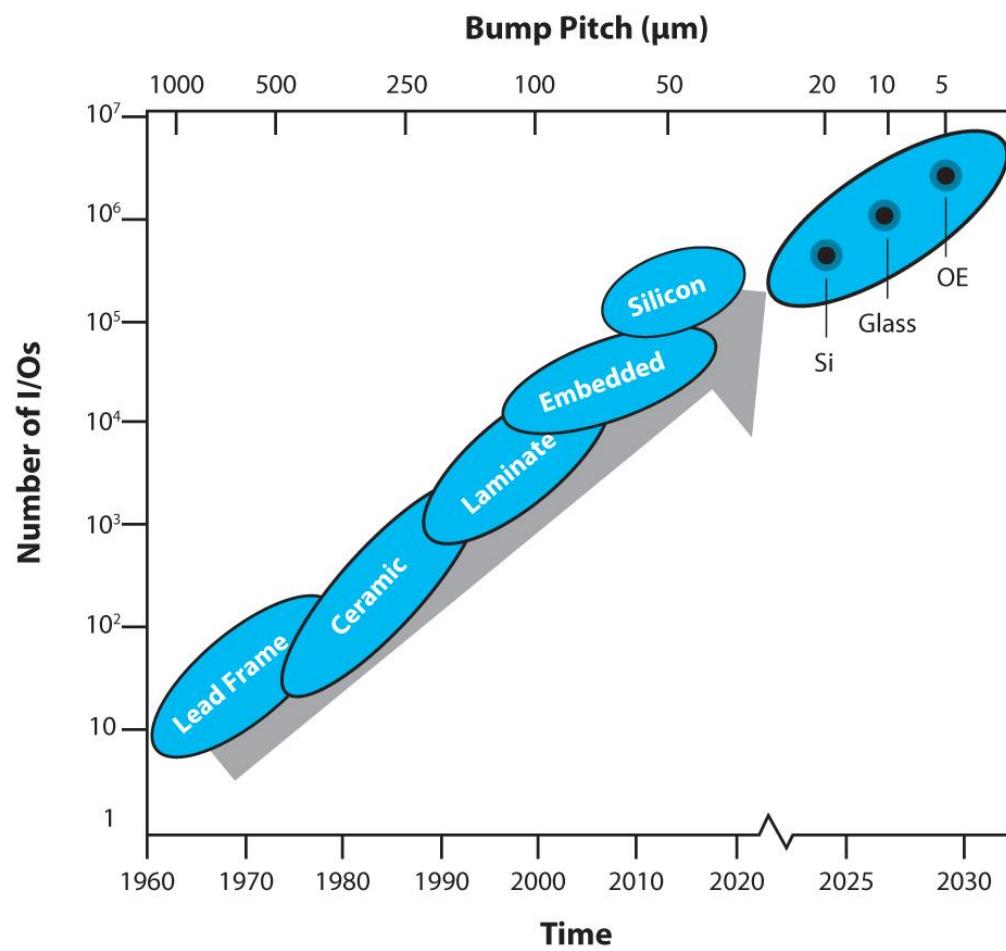


## **Large Package**

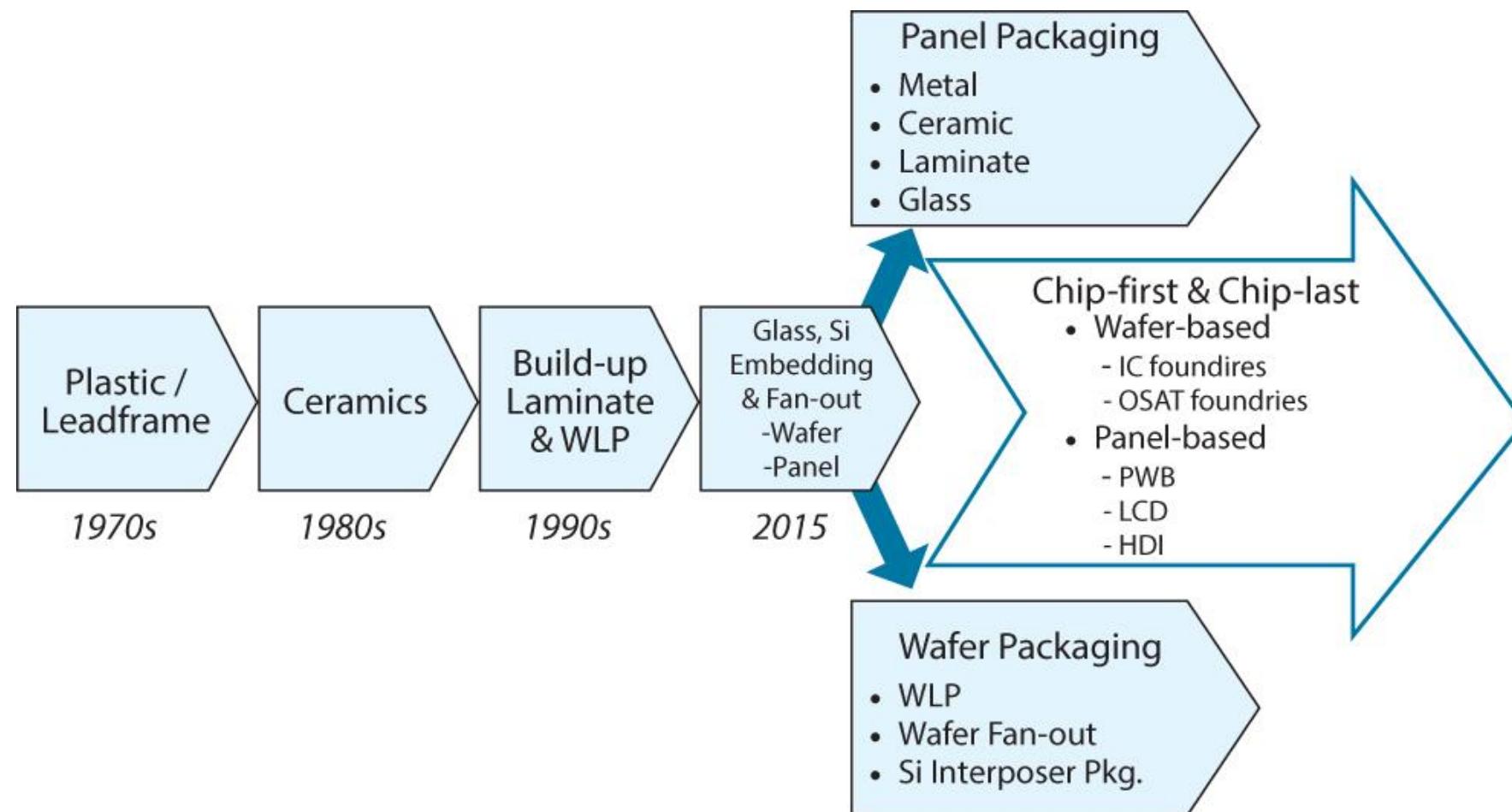
*Large package with small ICs with transistors and interconnects at high performance and low cost*

- 5-30 Billion transistors
- <30 miles of wiring
- High transistor performance
- Low RC interconnect delays
- Low design and manufacturing cost

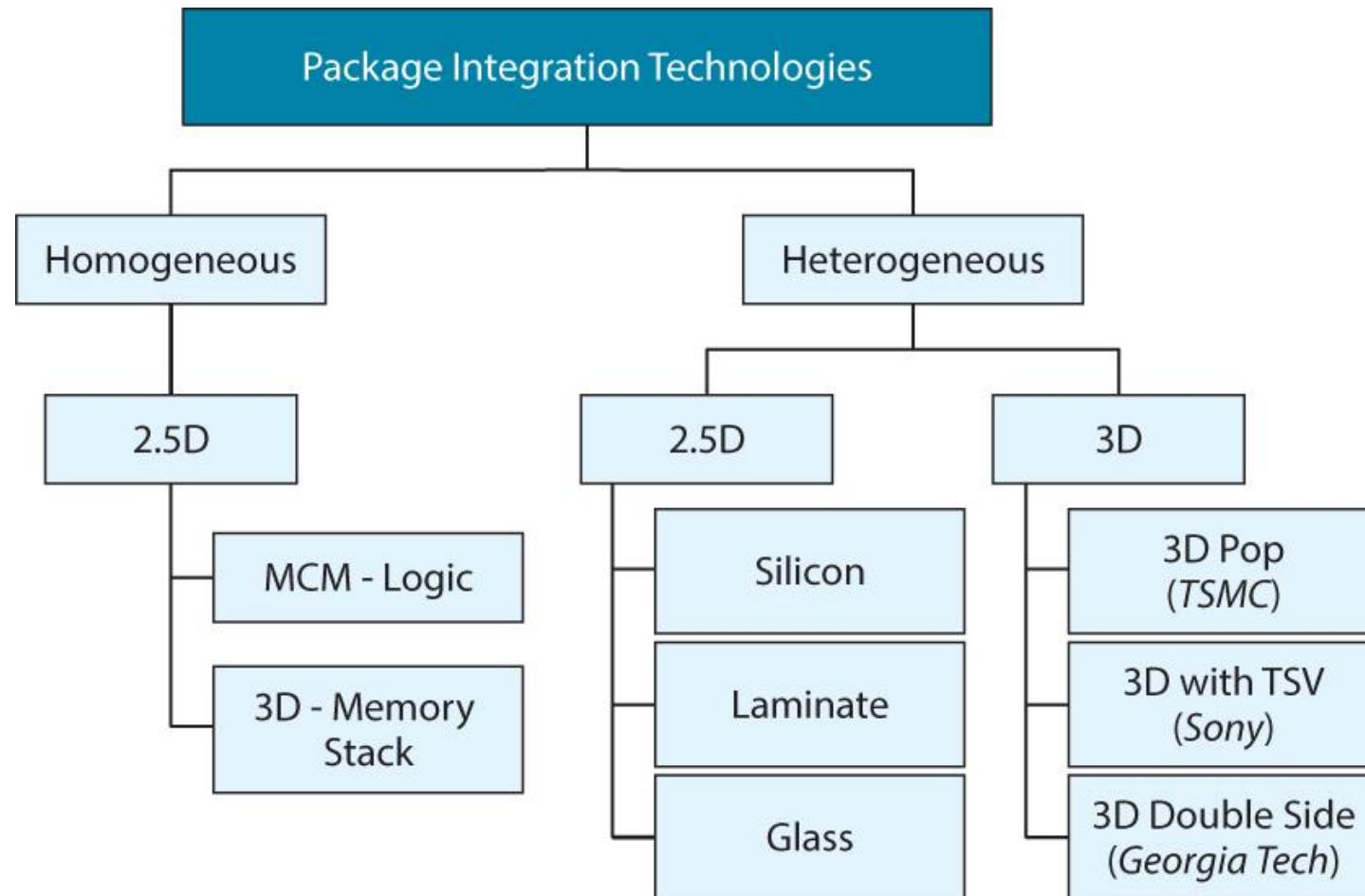
# Tummala's Law for Packaging: I/Os vs Transistors



# Evolution of Packaging Consistent with Tummala's Law for Packaging

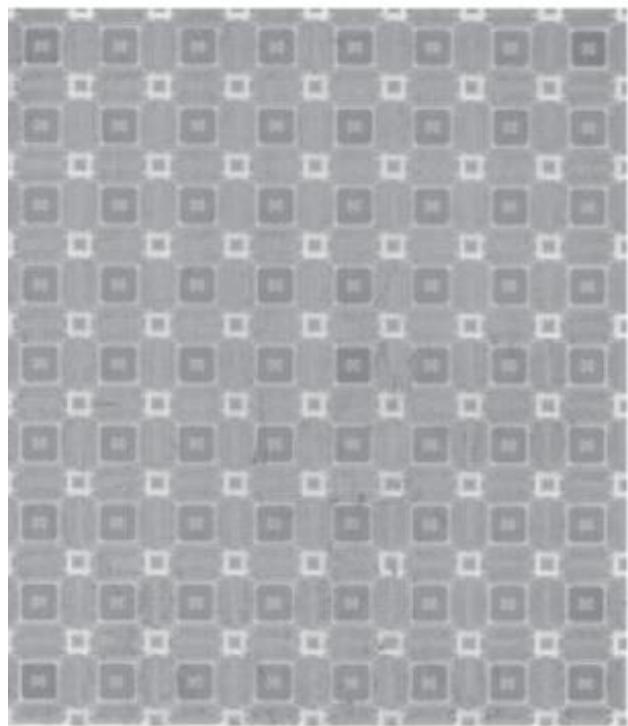


# Package Integration Technologies



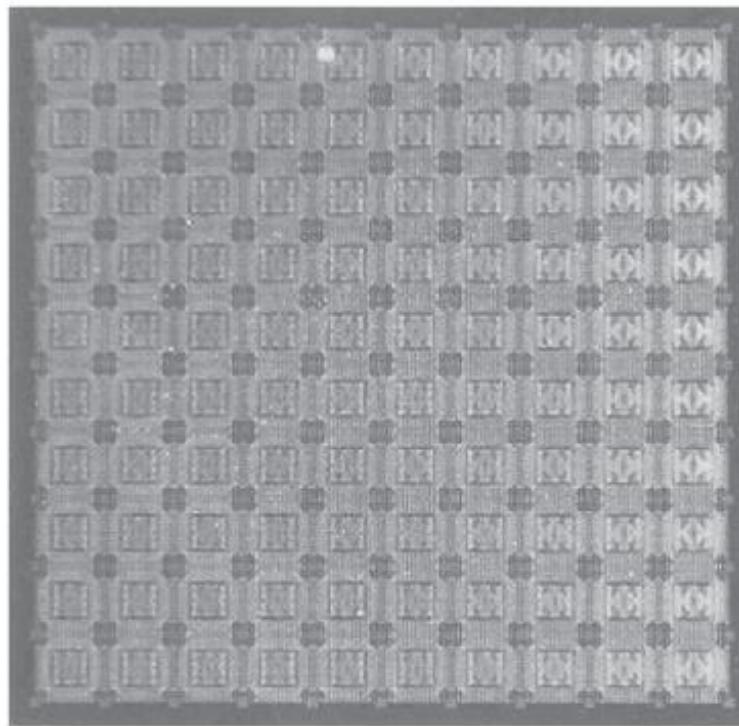
Industry' 1<sup>st</sup> LTCC Invention by Prof. Tummala, Now applied for all RF Applications. Invented for Computing Applications in 1980s

**MCM with HTCC  
(IBM, 1982)**



(a)

**61-Layer LTCC/Cu-MCM  
(IBM, 1992)**



(b)

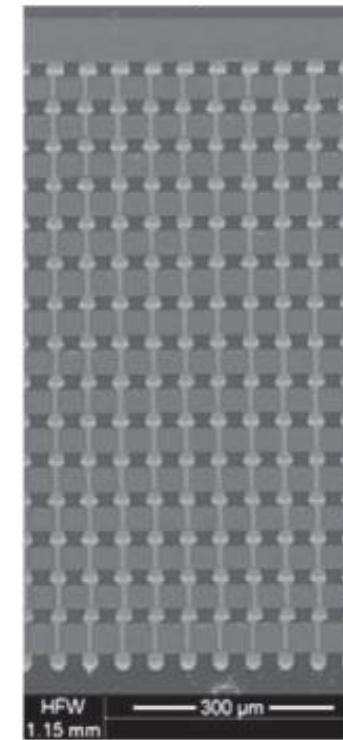
3D Packaging Started with Memory Stacking:  
Wire-bonded in 1990s , TSVs since 2015

**24-Layer 3D Stack with  
Wirebond (Amkor)**



(a)

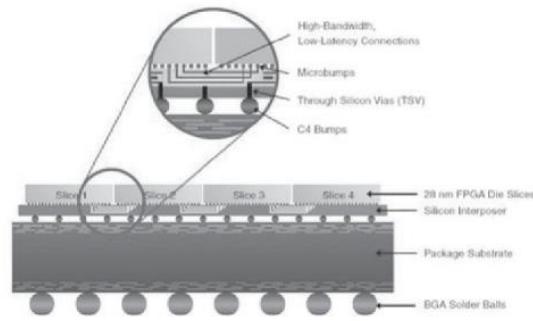
**16 DRAM Stack with  
TSV (Hynix)**



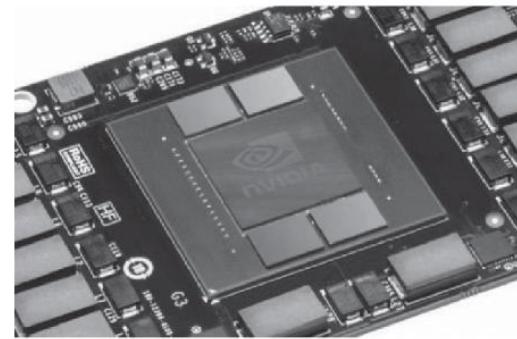
(b)

# 2.5 Silicon Interposers for Logic-memory

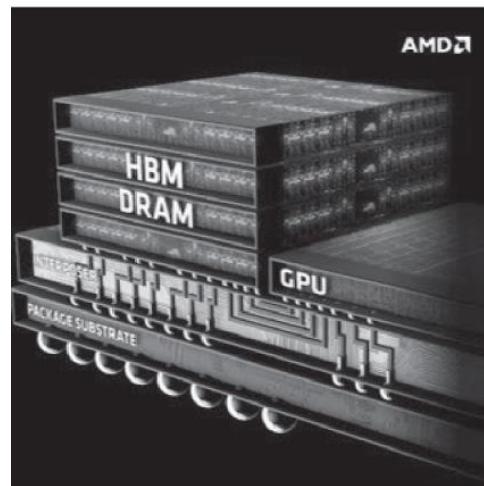
2.5D Interposer by XILINX



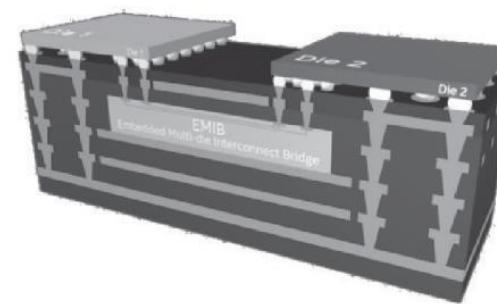
2.5D Interposer by NVIDIA



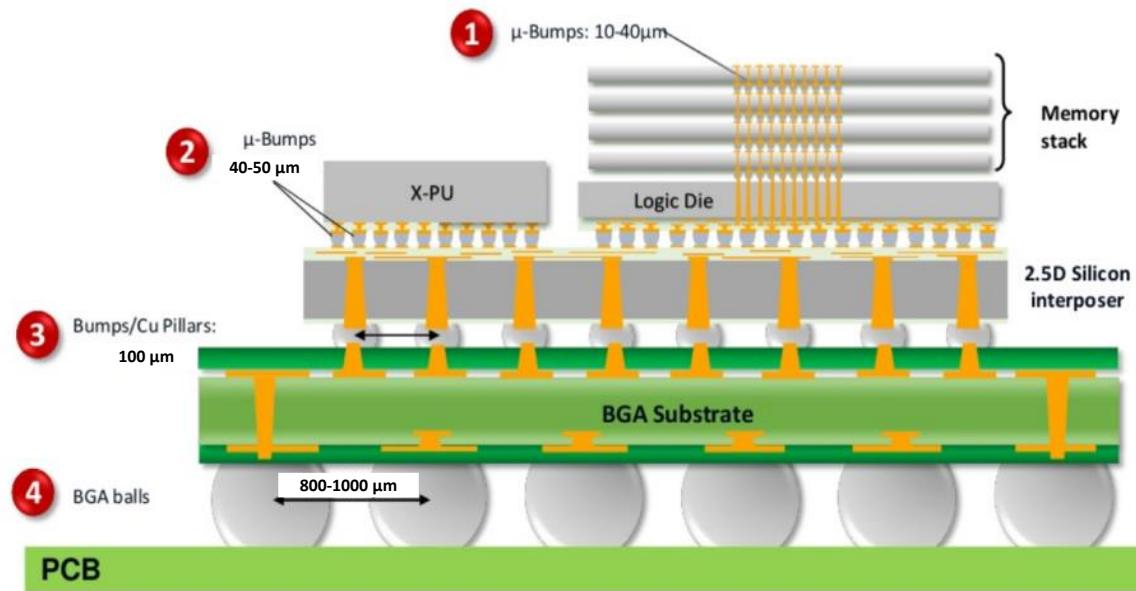
2.5D Interposer with HBM by AMD



Embedded Multi-Die  
Interconnect  
(EMIB) by Intel

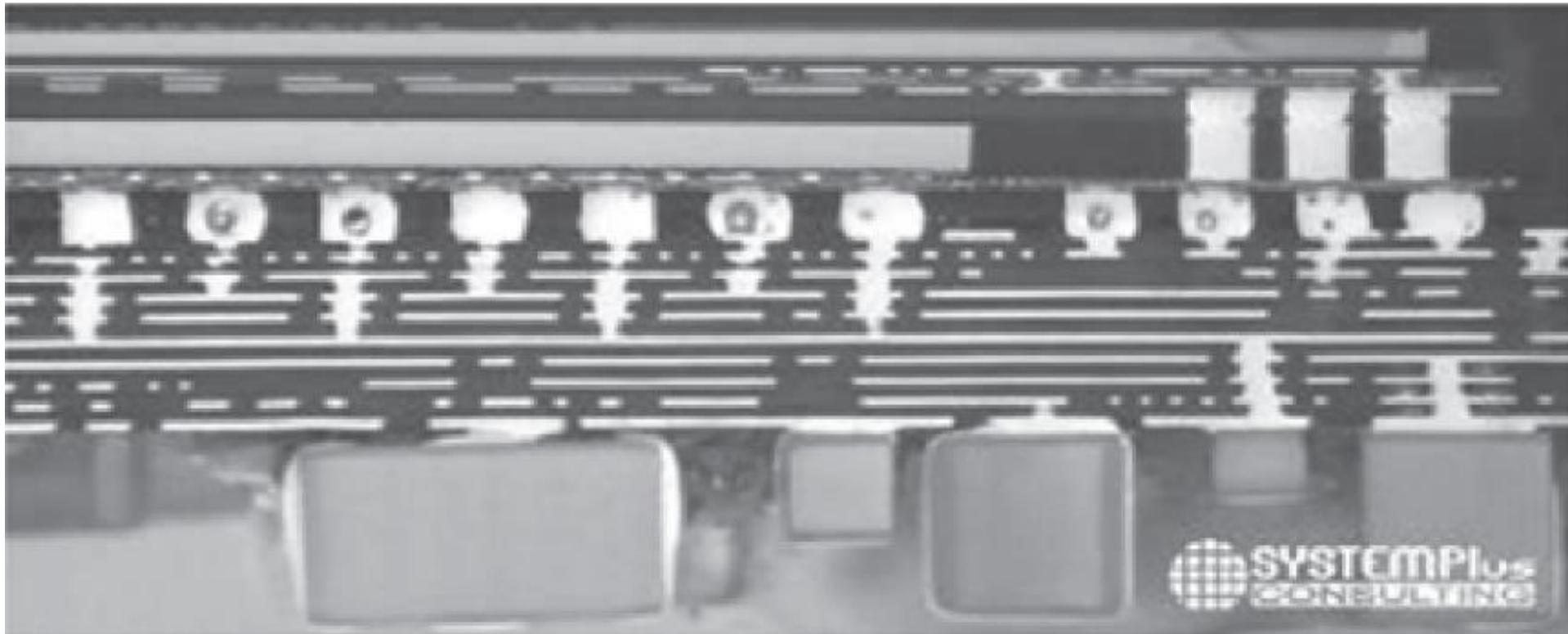


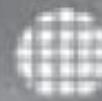
# Si Interposers & Bridges Require 4 Levels of Pkg.



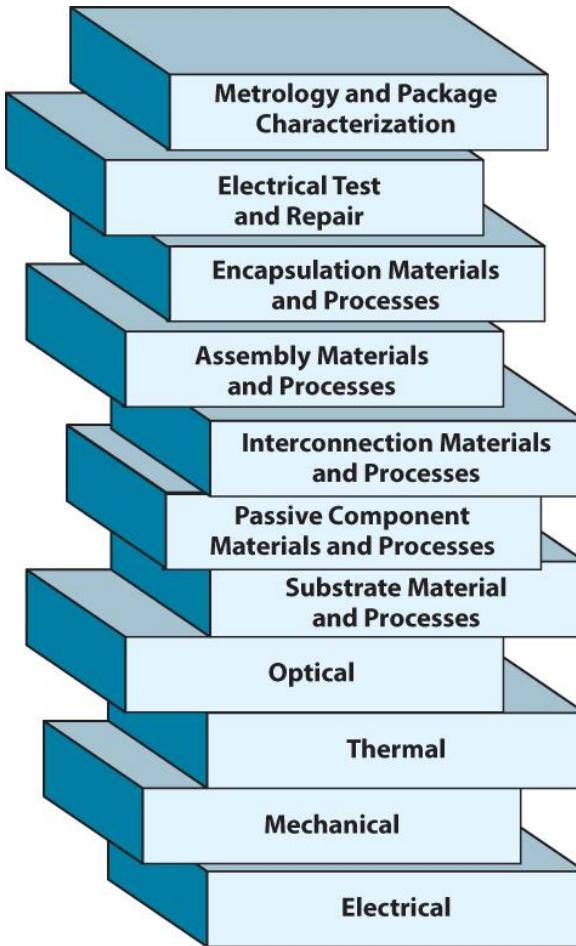
# Concept of Embedding. InFO Package by TSMC

**InFO-PoP  
Processor-memory Stacking**



 SYSTEMPlus  
CONSULTING

# Systems Require Many Technologies



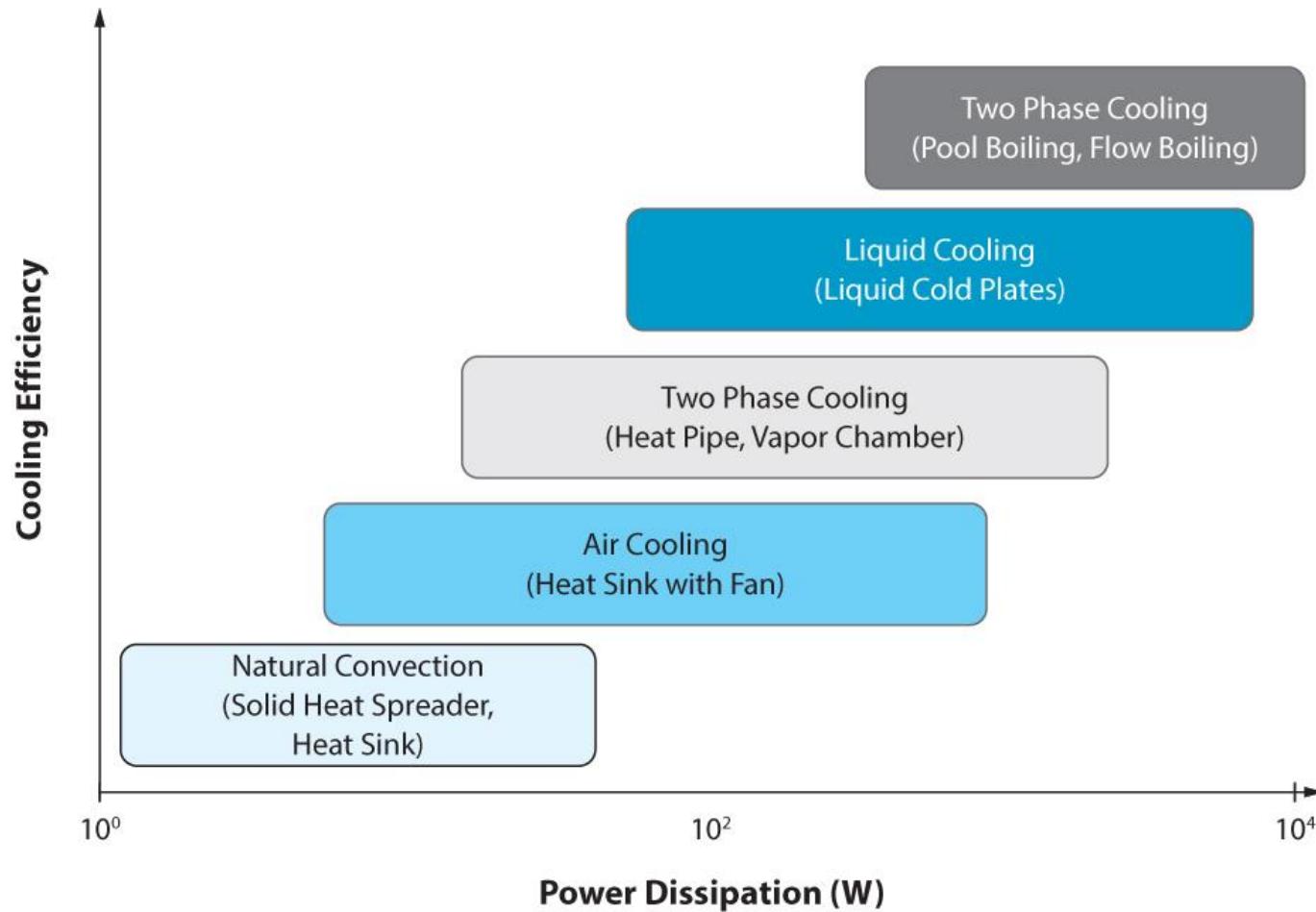
# Introduction to Device and Systems Packaging

- Why the course and why now in India?
- What is Packaging and Why?
  - Device level & System Level
- Anatomy of a Packaged- system
- Devices and Moore's law
- Four Technology Waves
- Moore's Law for ICs and Tummala's Law for Packaging
- **Evolution of Packaging Technologies**
- Future Outlook
- How the Course is Organized?
- Introducing PDC Expert Tutors
- What can you expect from the course?

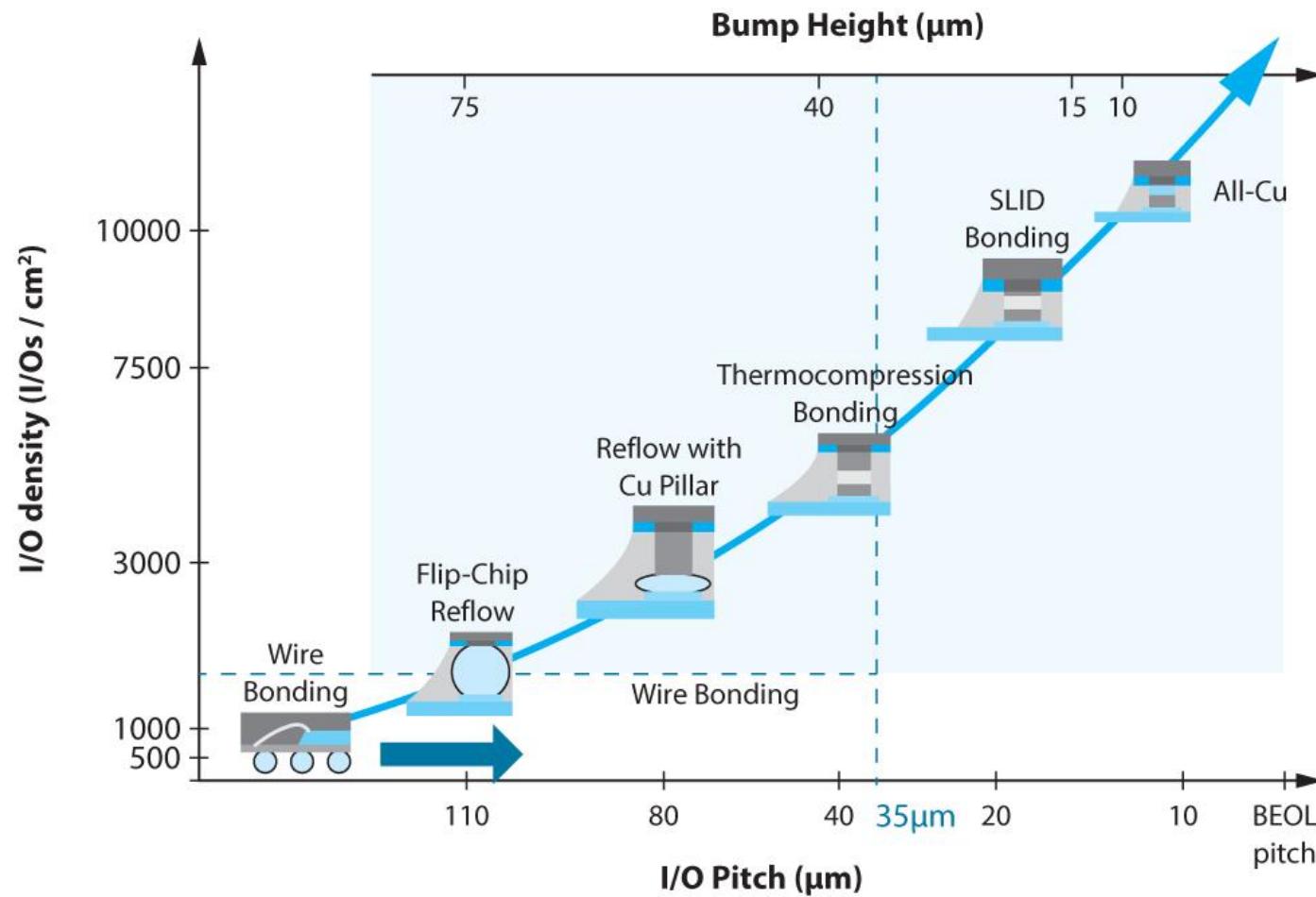
# Bio Break for 5 mins

- 20:45 to 20:50 IST

# Evolution of Thermal Technologies

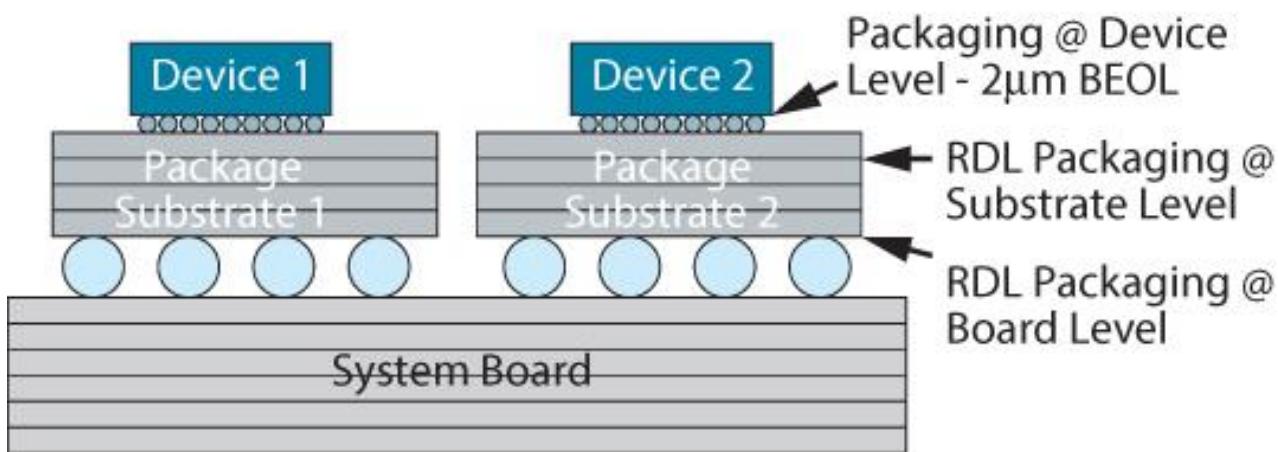


# Evolution of IC Assembly Technologies



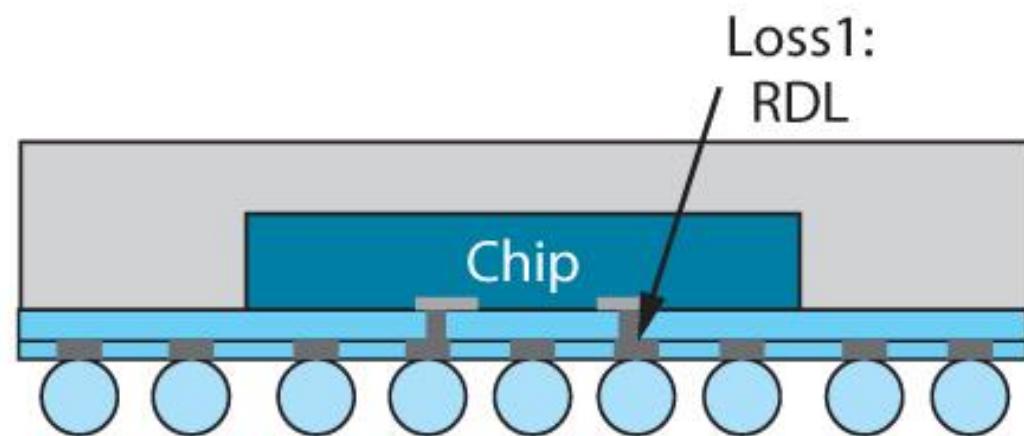
# Concept of Embedding for IC Assembly.

**Non-embedded Chip**



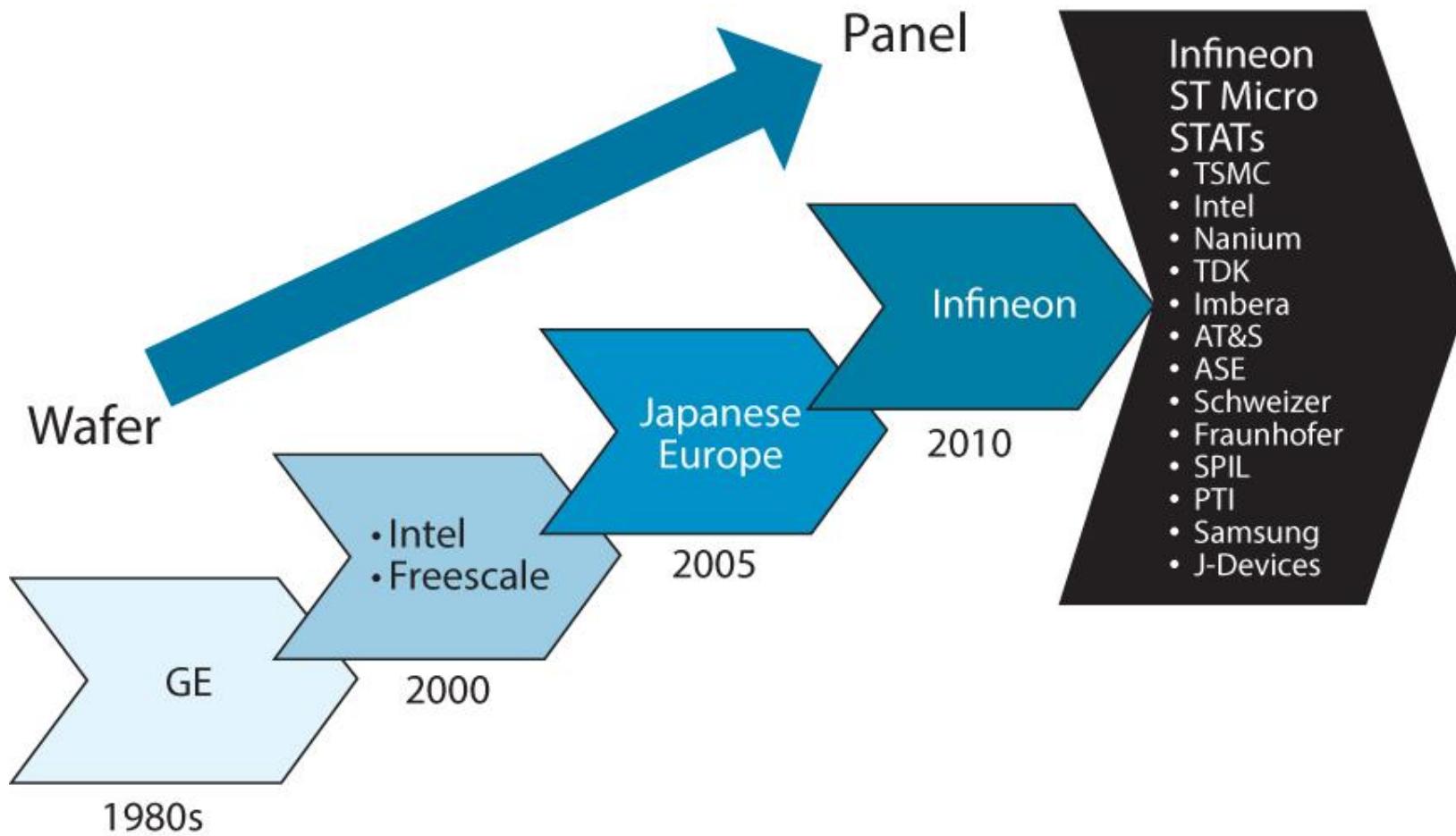
(a)

**Embedded Chip**

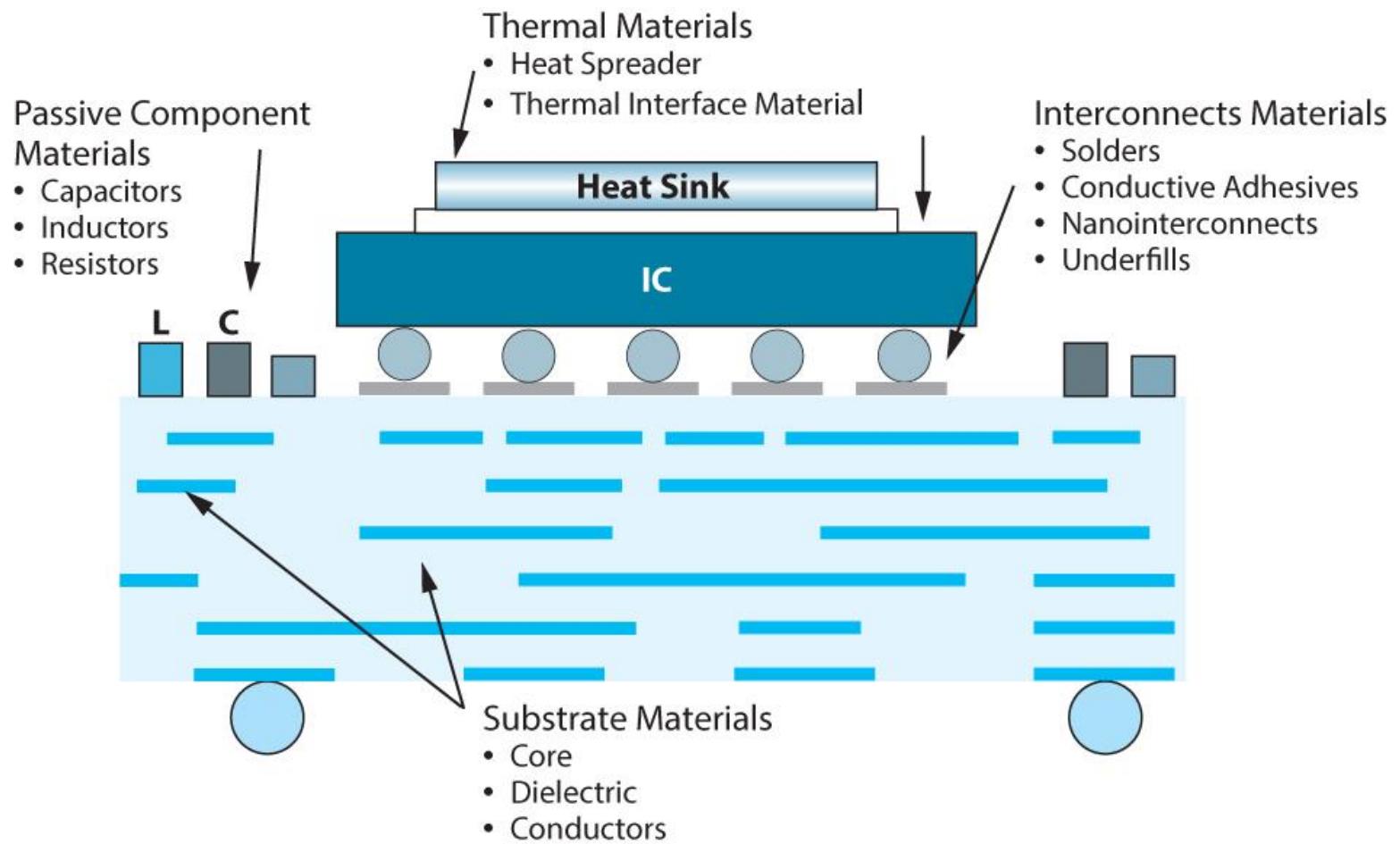


(b)

# Evolution of Wafer and Panel Embedding



# Materials in Packaging

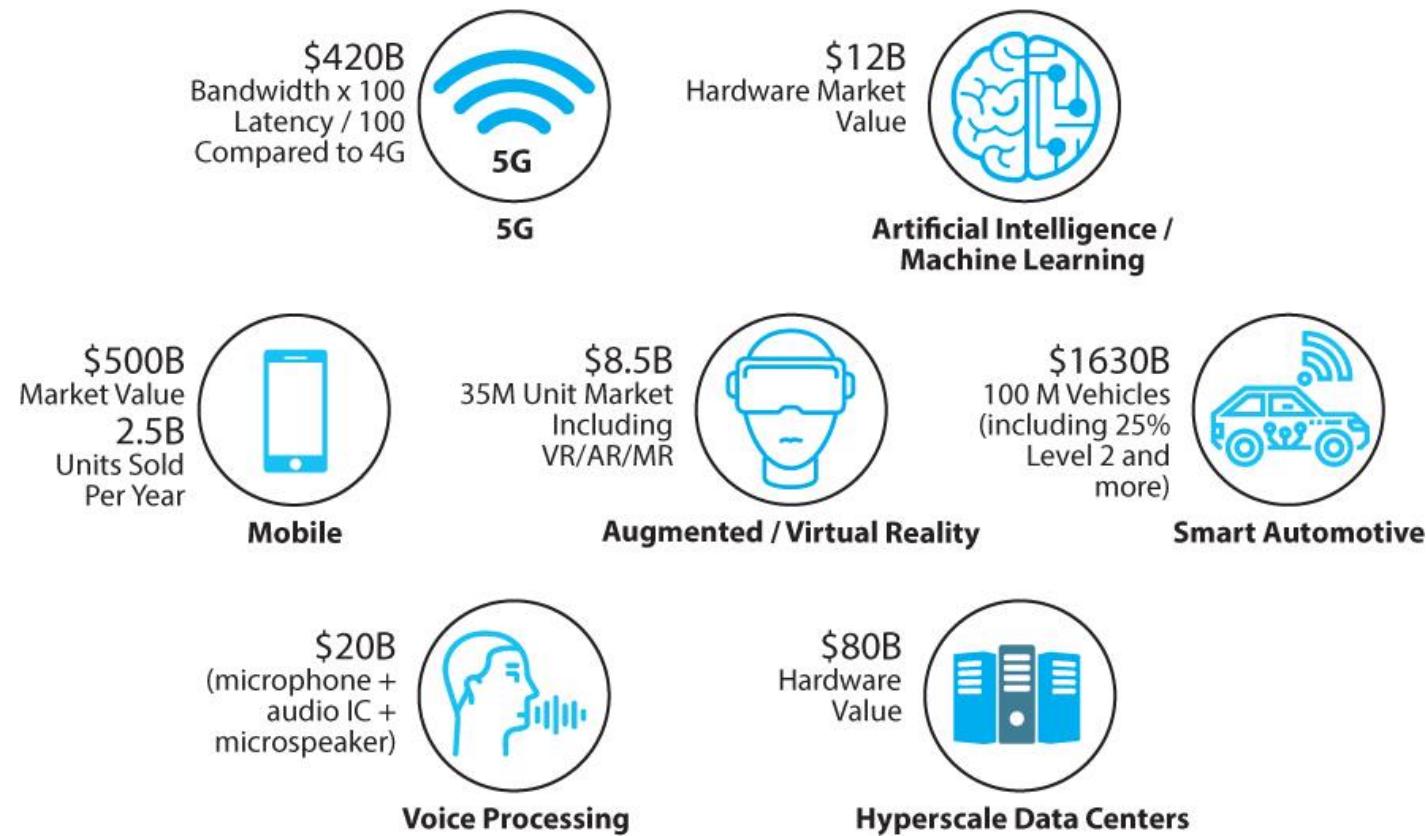


# Introduction to Device and Systems Packaging

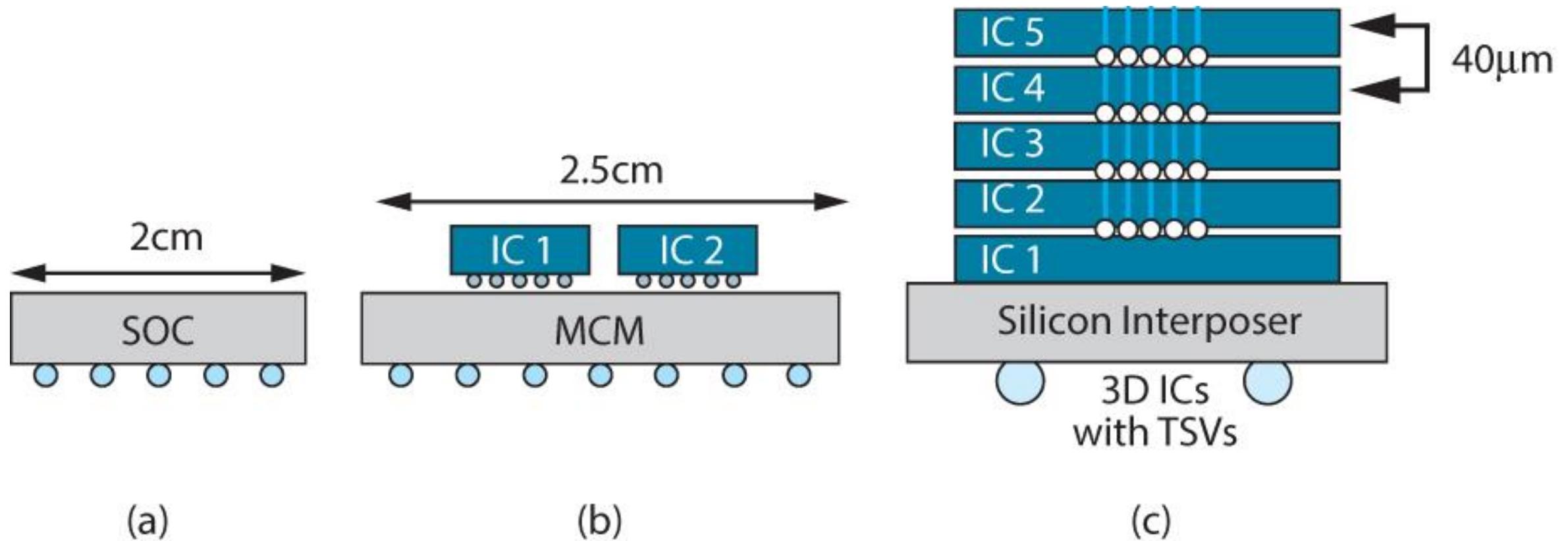
- Why the course and why now in India?
- What is Packaging and Why?
  - Device level & System Level
- Anatomy of a Packaged- system
- Devices and Moore's law
- Four Technology Waves
- Moore's Law for ICs and Tummala's Law for Packaging
- Evolution of Packaging Technologies
- **Future Outlook**
  - How the Course is Organized?
  - Introducing PDC Expert Tutors
  - What can you expect from the course?

# Mega Trends in Electronic Systems

## Electronic Megatrends (2021)

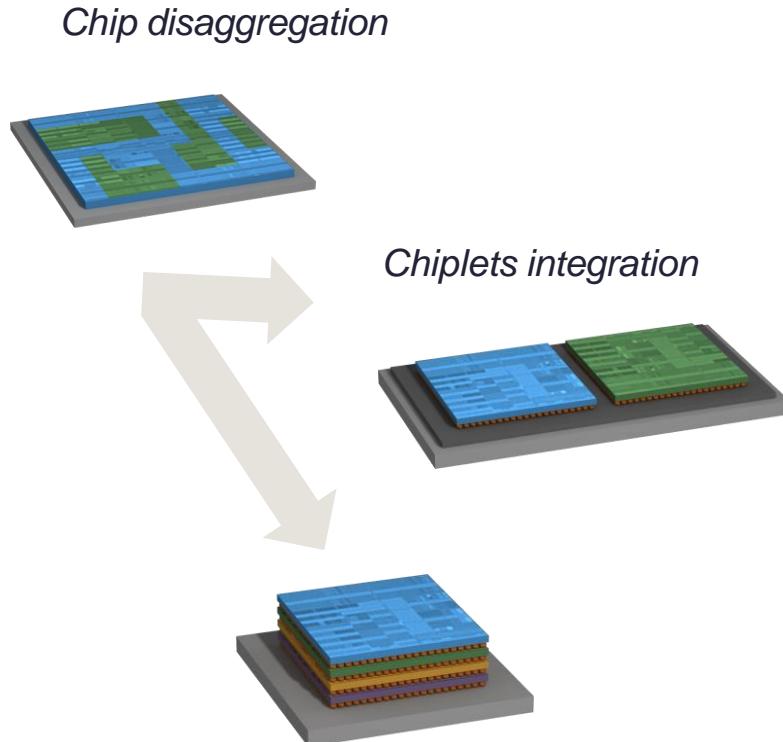


# Evolution to Chiplet and 3D Packaging



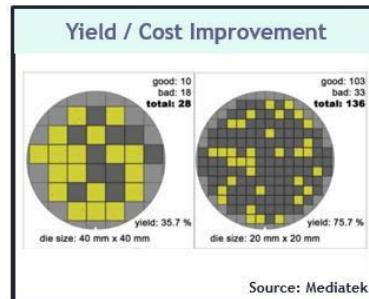
# Beyond Si Technology Limit : Chiplet solution

## Chiplets

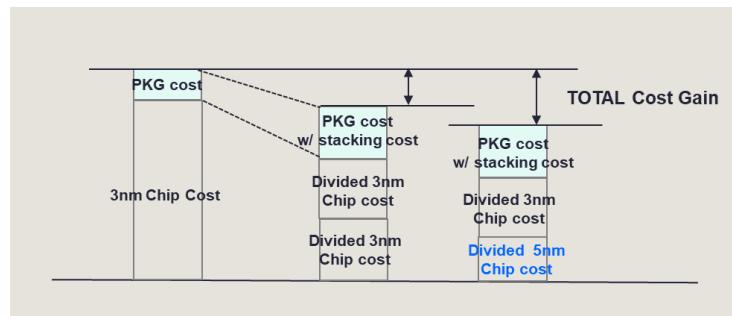


## Cost

Die Size ↓ → Yield ↑ → Die Cost ↓



Node mixing, IP re-use -> Cost optimization



## Many more...

### Performance

- Shorter interconnect distance
- Increased on chip memory / logic
- Increased functionality

### Form Factor

- 3D stacking saves 2D space

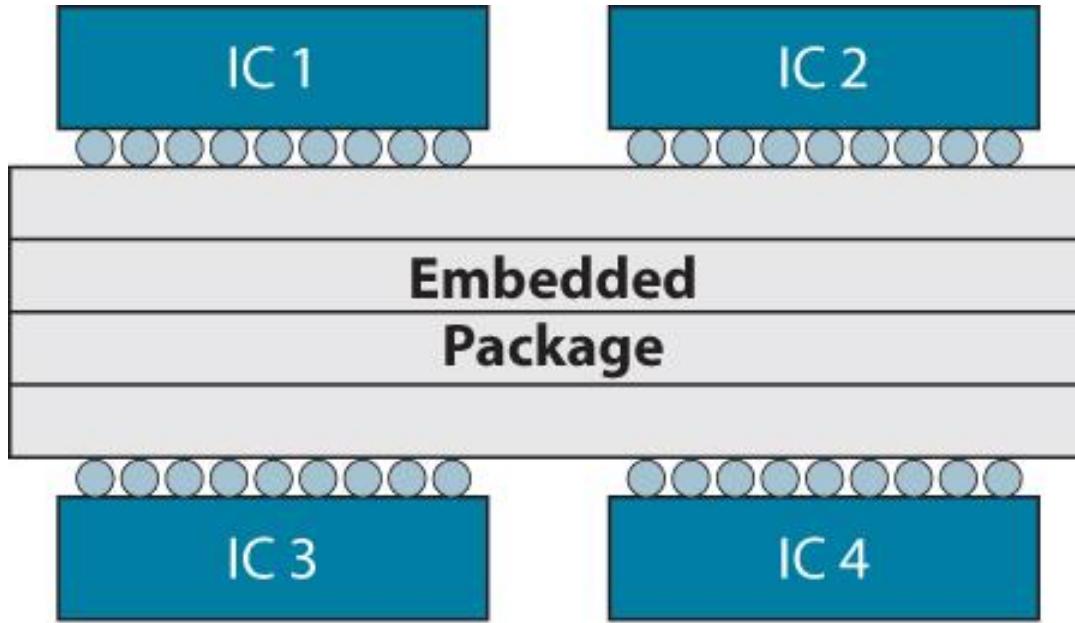
### Time to market

- Flexibility in design, R&D, MFG

### Power

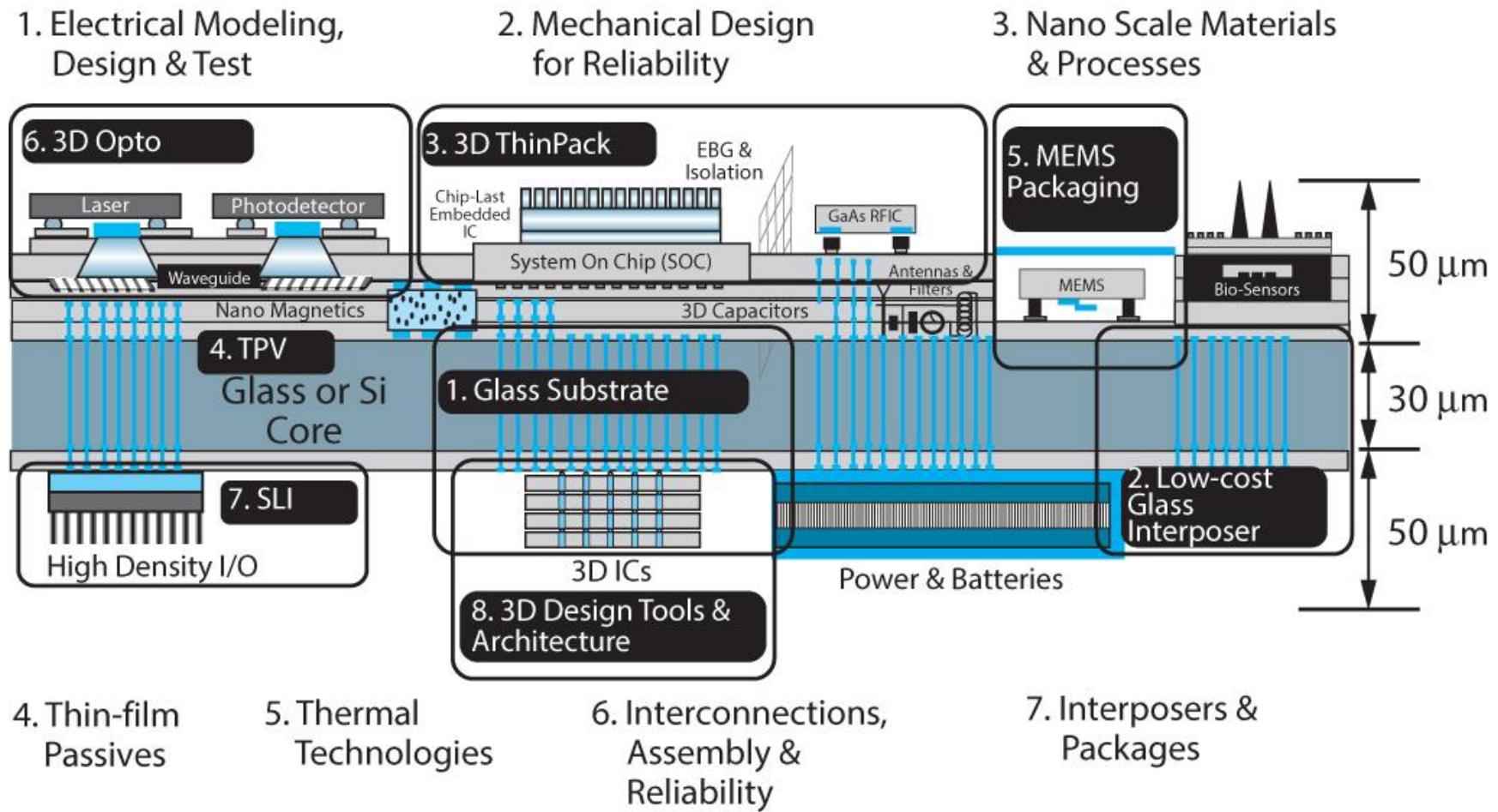
- Shorter interconnect

# Emerging SOP Concept



- Ultra-short TSV-like system interconnects  
in ultra-thin large panel substrate
  - Signal vias, power vias, photonic vias  
and large thermal vias

# An Example of A Future System in SOP Concept.



# Introduction to Device and Systems Packaging

- Why the Course and Why Now in India?
- What is Packaging and Why?
  - Device level & System Level
- Anatomy of a Packaged- system
- Devices and Moore's law
- Four Technology Waves
- Moore's Law for ICs and Tummala's Law for Packaging
- Evolution of Packaging Technologies
- Future Outlook
- **How the Course is Organized?**
- **Introducing PDC Expert Tutors**
- **What Can You Expect From the Course?**

# What Can you expect from the course?

- On-Chip Integration Era; Every IC must be packaged. While packaging is necessary , added no value to systems. This led to system on Board—Bulky & low performance.
- On-package Integration Era: Started in 1980s but exploding for AI. Examples: MCMs, 2.5D, 3D, Chiplet.
- Moore's Law + Tummala's Law Era:While transistor scaling continues, transistor performance dramatically slowed down. The new Moore's Law is enabled by packaging . Integrated systems packaging is the highest Value add and most appropriate for India.
- System level packaging requires knowledge of many , many technologies and is highly interdisciplinary.
- India needs to master this technology to grow its economy and for its national security.