

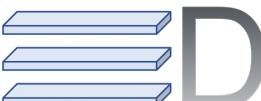
Fundamentals of Substrates

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Tutorial Series hosted by BITS Pilani

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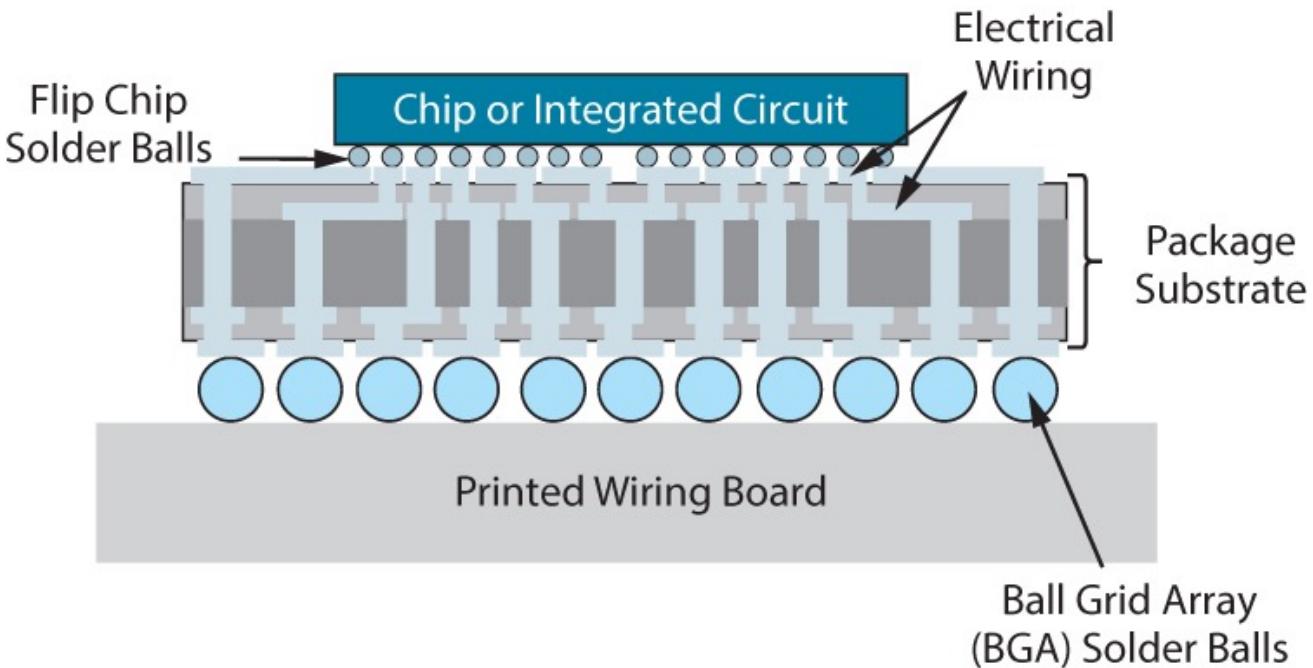


OUTLINE

- What is a Package Substrate?
- Anatomy of a Package Substrate
- Substrate Materials and Their Properties
- Substrate Technologies
 - Ceramic Substrates
 - Organic Build-up & Coreless Substrates
 - Glass Substrates
 - Silicon Interposers
- Summary and Future Trends

What is a Package Substrate?

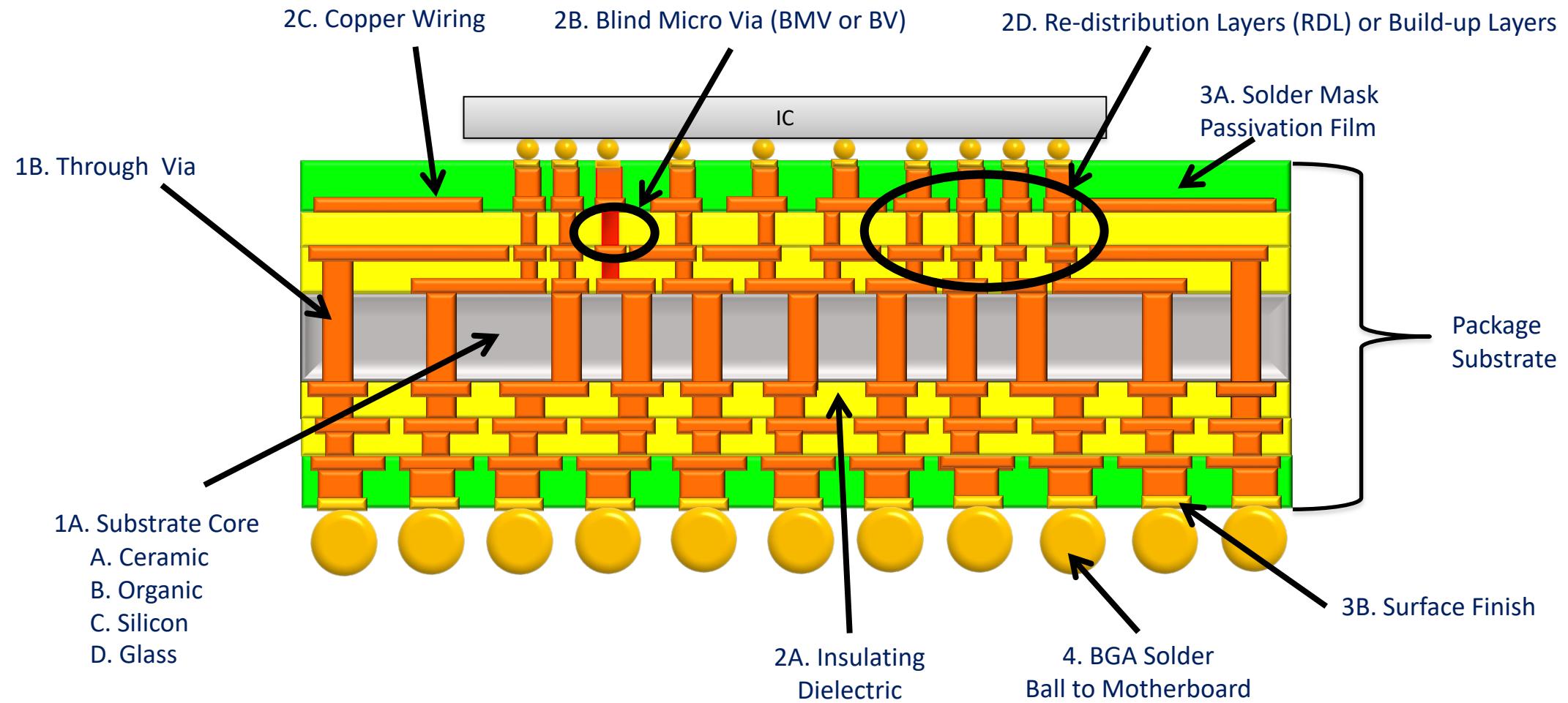
- A dimensionally stable carrier on which to build and integrate wiring & interconnects, connecting to fine-pitch chip I/Os on top side and coarse pitch board I/Os on the bottom side
- Ready to assemble 2D or 3D ICs & passive components
- Substrate Generations
 - Ceramic: 1960 –
 - Organic: 1990 –
 - Silicon and Glass: 2010 –



A typical package substrate showing interconnections to the IC on one side and to PWB on the other side

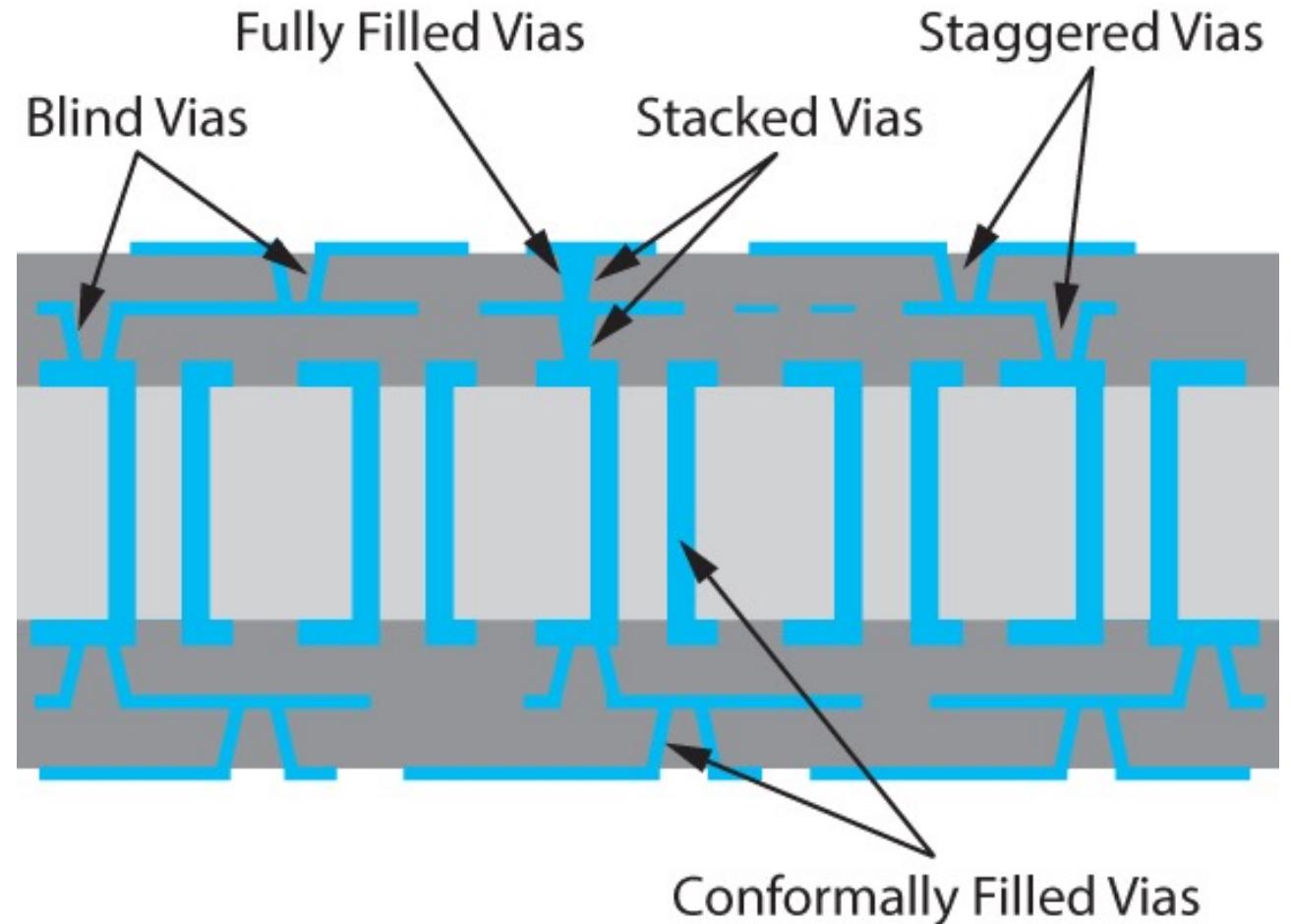
Anatomy of a Package Substrate

- Key Materials and Structures that constitute a typical package substrate



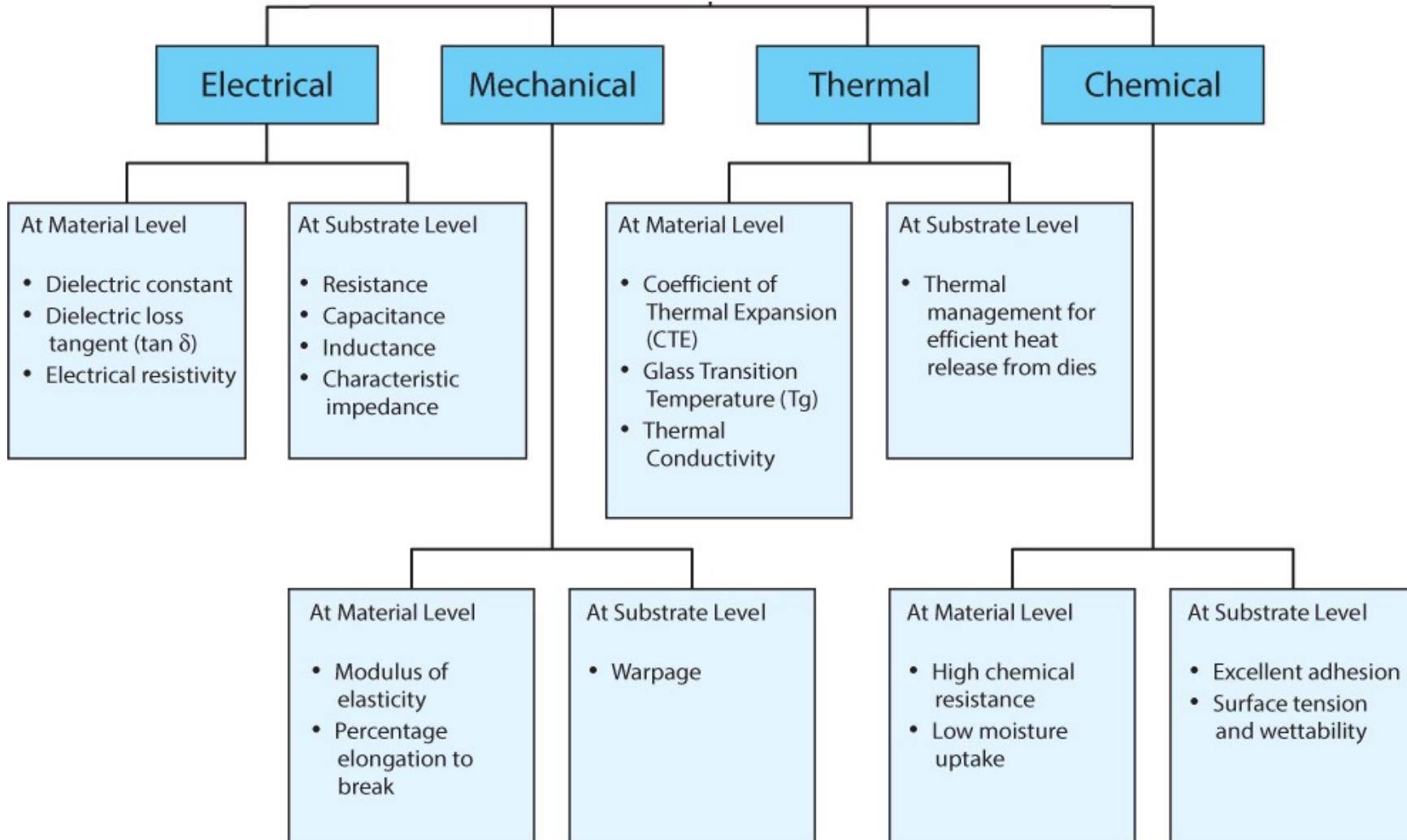
Different via configurations in multi-layer thin-film substrates

- **Through Via:** Extends from one surface to the opposite surface of a substrate core.
- **Blind Via:** Connects one metal layer to another metal layer on one side of the substrate (can pass through more than one layer of dielectric).
- **Conformal Via:** Copper is deposited only on the side wall of the via and does not fill the inner volume of the via.
- **Fully Filled Via:** Copper is deposited to fill the entire inner volume of the via, leading to lower via resistance and higher current carrying capacity.



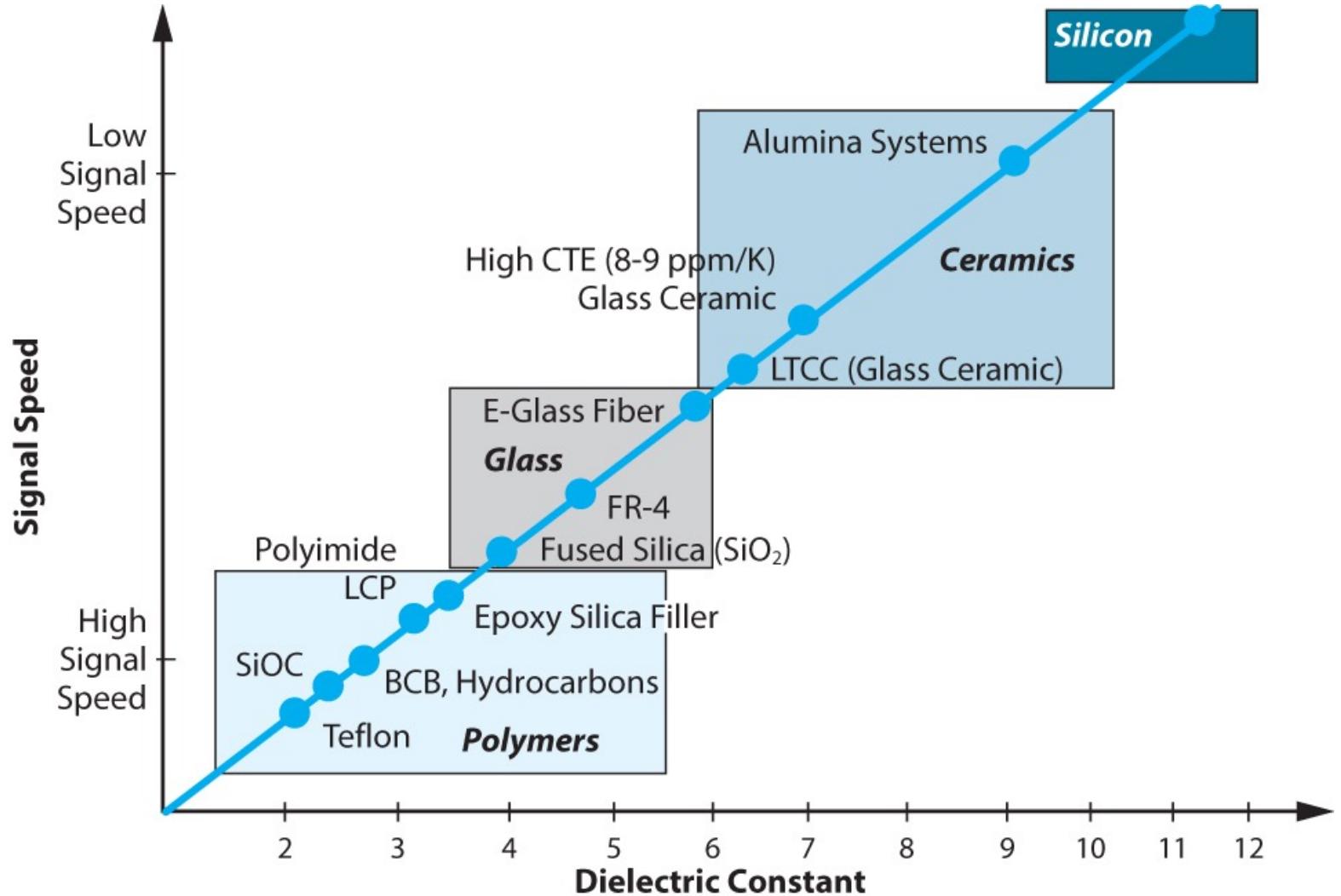
Package Substrate Material Properties

- Fundamental material properties translate directly to performance and reliability metrics at substrate level.



Signal speed as a function of dielectric constant of substrate materials

- Lower dielectric constant results in lower signal capacitance and reduces RC delay → higher signal speeds
- Higher dielectric constants are useful in certain RF circuit designs for miniaturization
- Higher dielectric constant materials are used as embedded capacitors for improving power delivery efficiency in the package



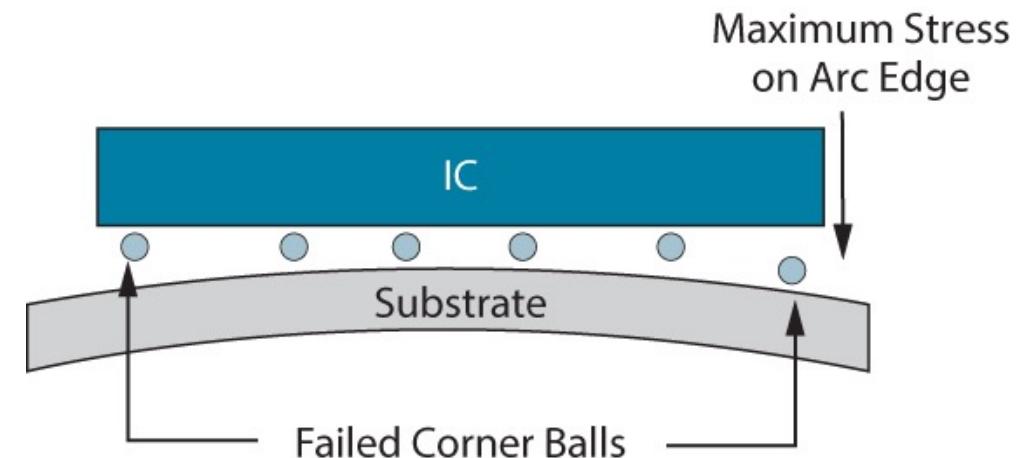
Thermo-mechanical Properties Control Substrate Warpage

- High Elastic Modulus to resist warpage

$$\rho \propto E_s \Rightarrow \text{Warpage} \propto \frac{1}{E_s}$$

ρ is the radius of curvature of the substrate

E_s is the elastic modulus of the substrate



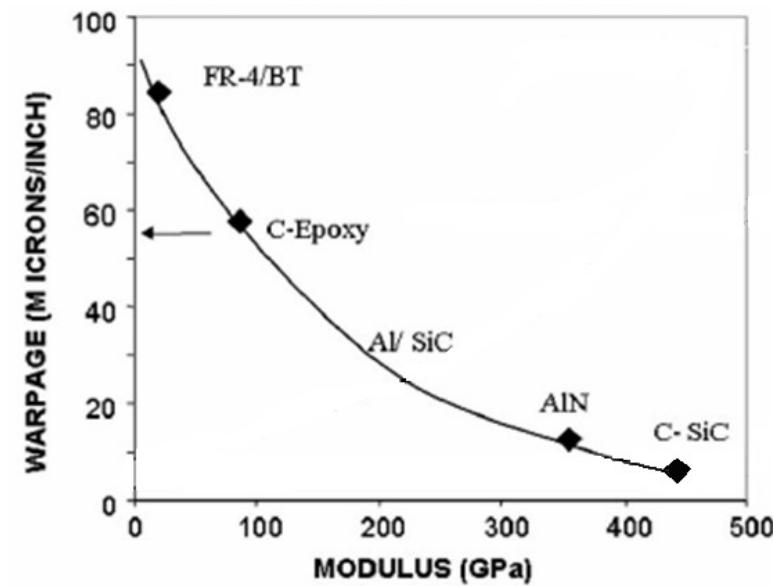
- Low CTE (Coefficient of Thermal Expansion)

$$\alpha \text{ proportional to } \Delta l / \Delta T$$

α is the CTE or TCE

Δl is the change in length or x-y-z dimension

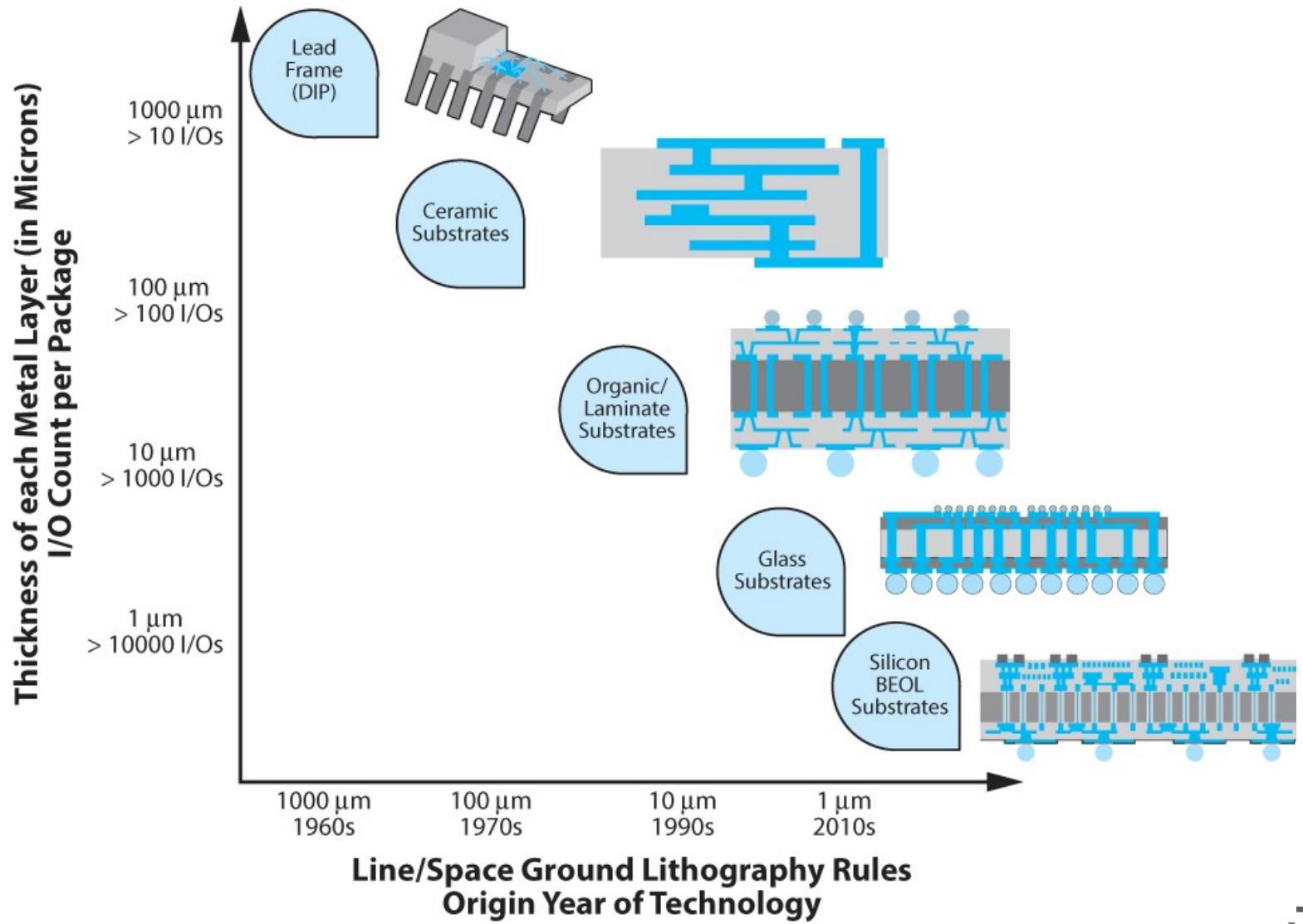
ΔT is the change in temperature



Warpage for 0.65mm Thick Substrate

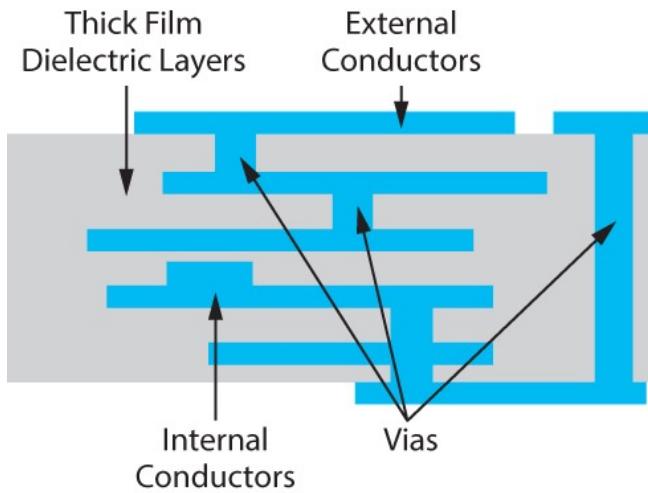
Evolution of package substrates as a function of I/O need

- Substrates transitioned from small ceramic panels to large organic panels, simultaneously reducing wiring and interconnect pitch
- Glass substrates enable finer wiring pitch than organic substrates, while maintaining the large panel size.
- As RDL pitch on substrates trends towards sub-micron dimensions, silicon wafers are the only viable substrates, but the smaller wafer size increases substrate cost.



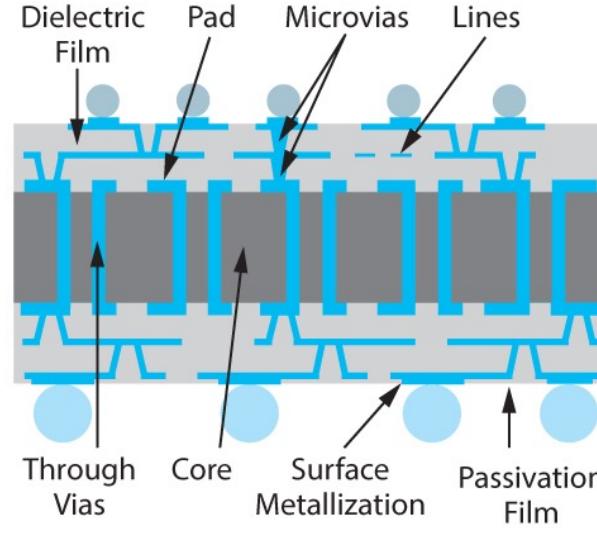
Anatomy of Ceramic (Thick Film), Thin Film (Organic) and Ultra-Thin Film (Glass & Silicon) Substrates

Thick Film (50-100 μm) Since 1960



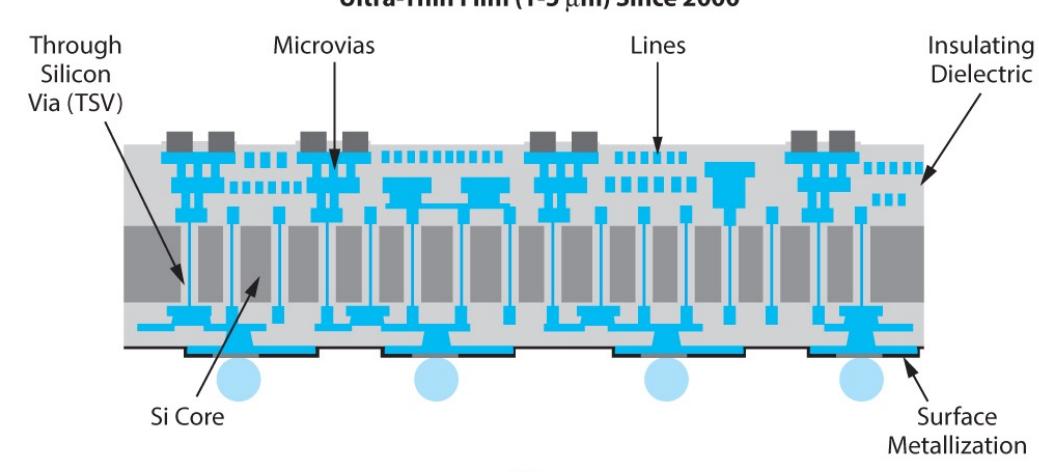
(a)

Thin Film (5-50 μm) Since 1990



(b)

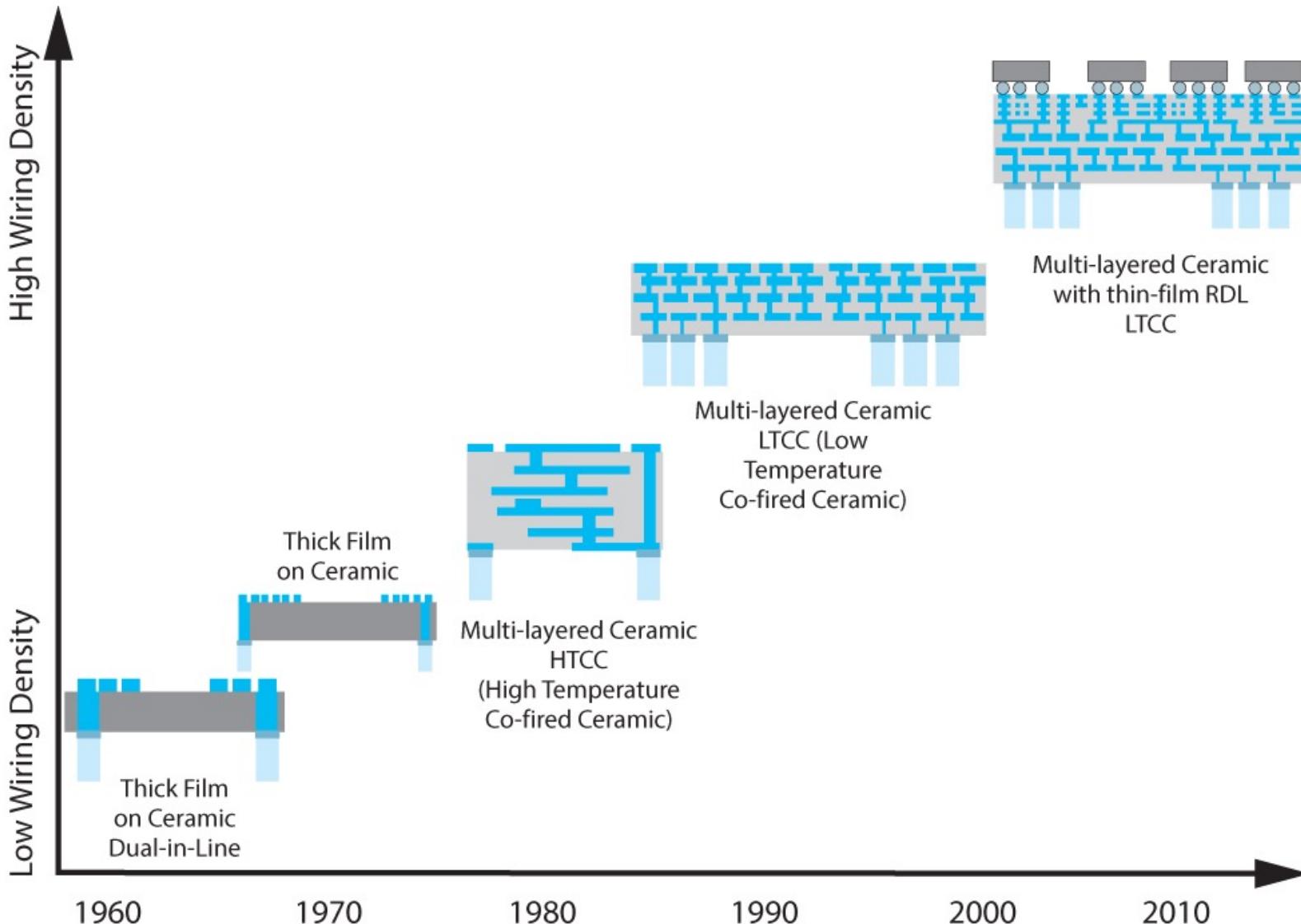
Ultra-Thin Film (1-5 μm) Since 2000



(c)

Finer Pitch Chip-to-Substrate Interconnections

Evolution of Ceramic Substrates



Low-temperature co-fired ceramic substrate (LTCC): Materials, Properties and Manufacturing process

- Key Property Advantages of LTCC
 - Low CTE close to Silicon
 - Low dielectric loss, high dielectric constant
 - High temperature stability

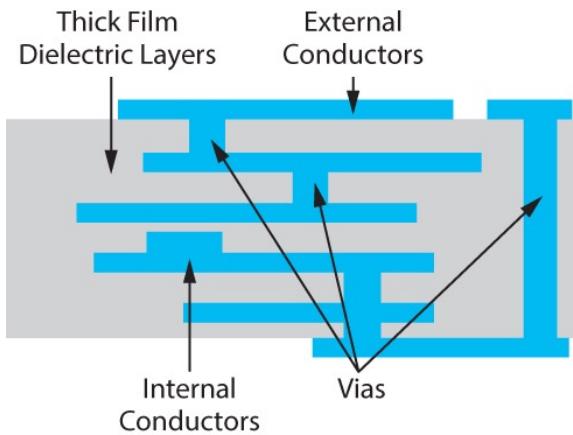
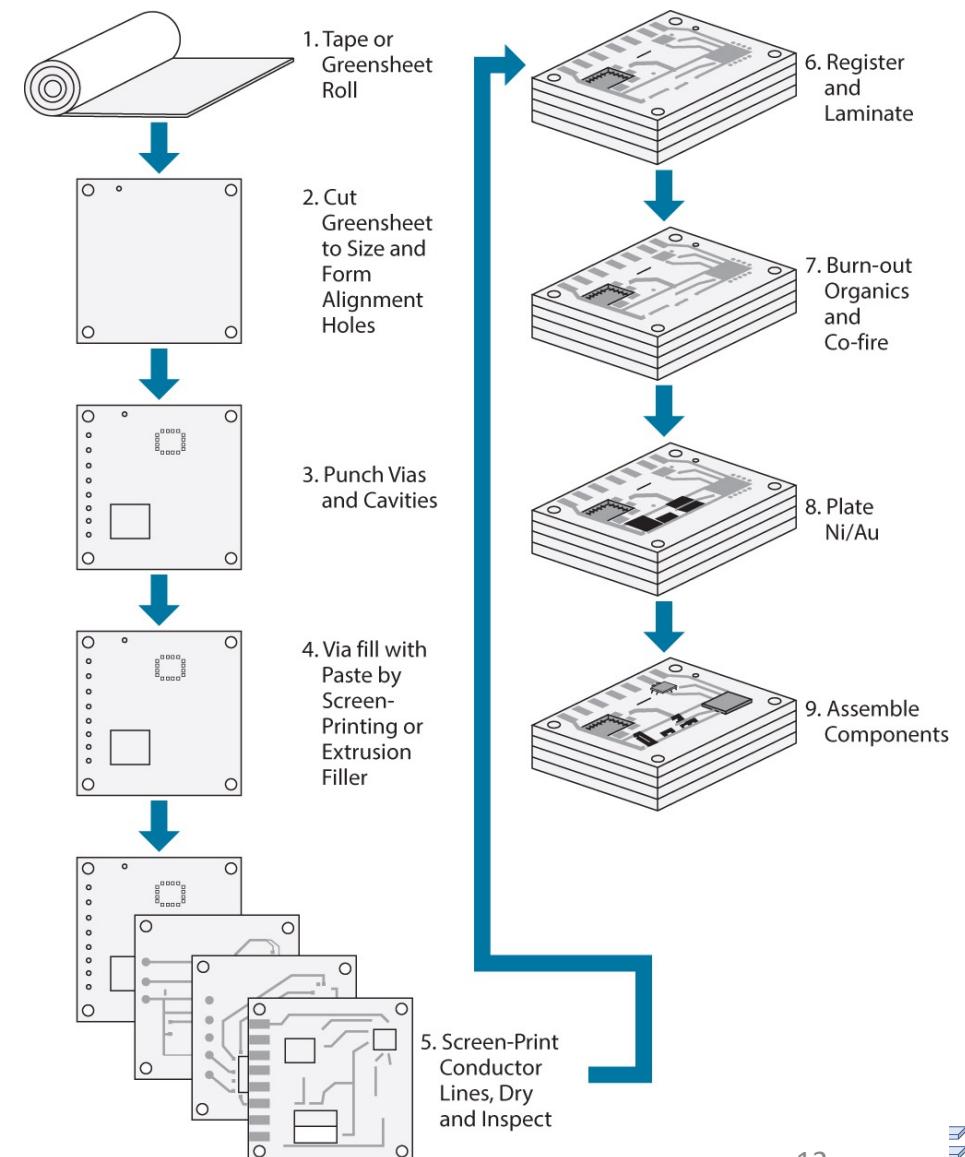


TABLE 6.4 Properties of Ceramic Substrate Materials

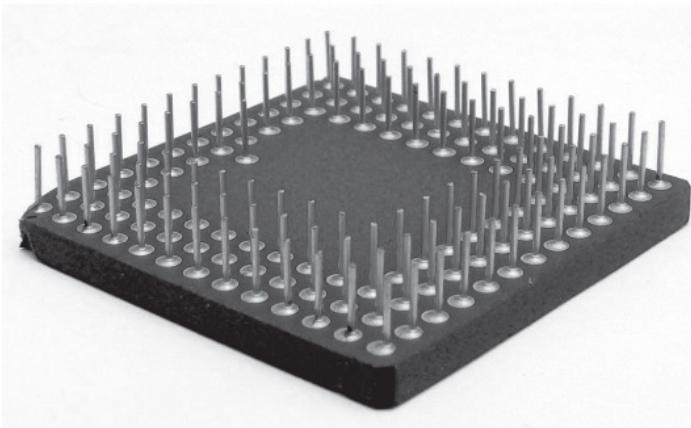
Material	Relative Permittivity @1 MHz	Thermal Conductivity (W/m·K)	Thermal Exp. Coeff. (ppm/K)	Loss Tangent $\tan \delta (10^{-4})$	Elastic Modulus (GPa)
Al_2O_3	9.8	20	7	2	350
AlN	9	230	4.1	3–10	380
SiC	40	270	3.7	500	380
BeO	6.8	260	5.4	4–7	345
LTCC	5	5	3–5	2	150



LTCC Applications Benefit from Key Properties

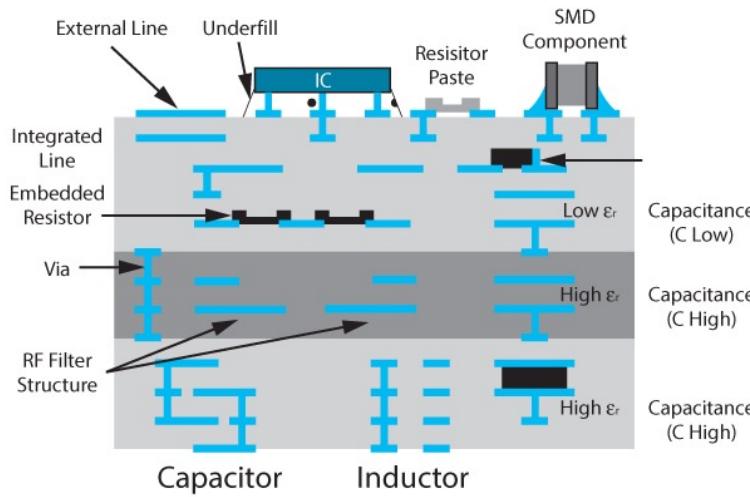
High Performance Computing

- Low CTE enables highly reliable packages



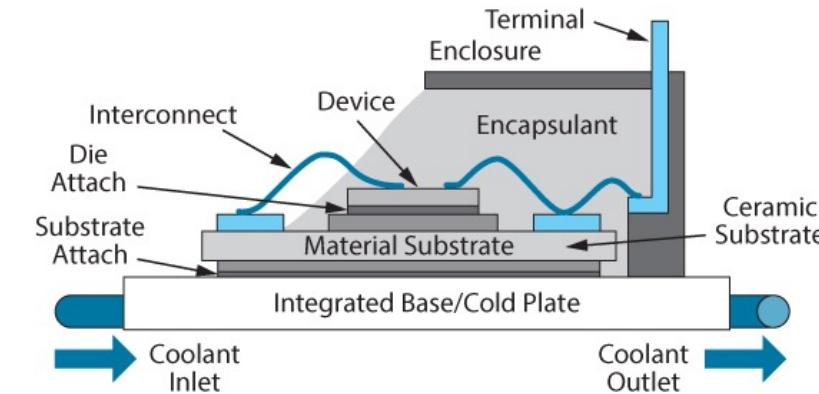
RF and mm-wave (5G, 6G)

- Low dielectric loss and high precision circuitry enables RF interconnects
- High dielectric constant for low loss RF capacitors



Automotive and High Power

- High temperature stability enables high power packages with high reliability

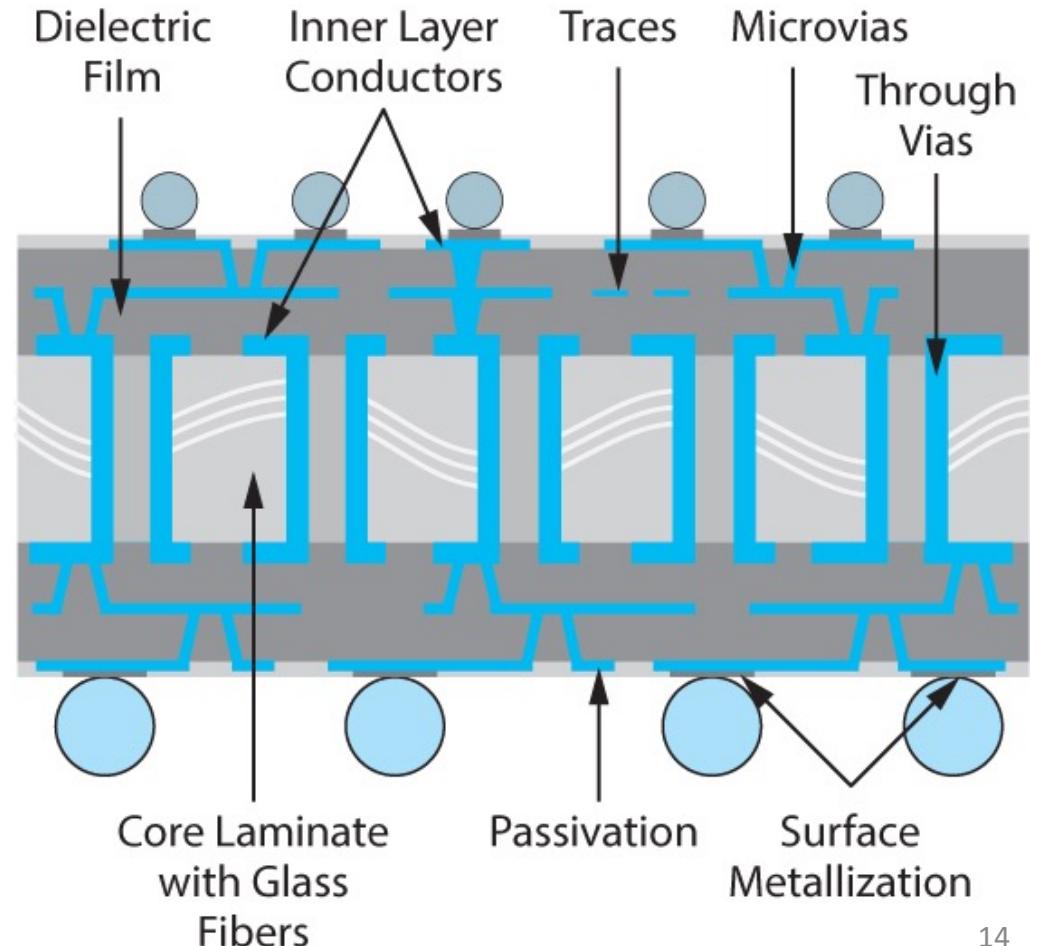


Organic Substrates - Primary Platform for the Past 30 Years

Why Organic Substrates?

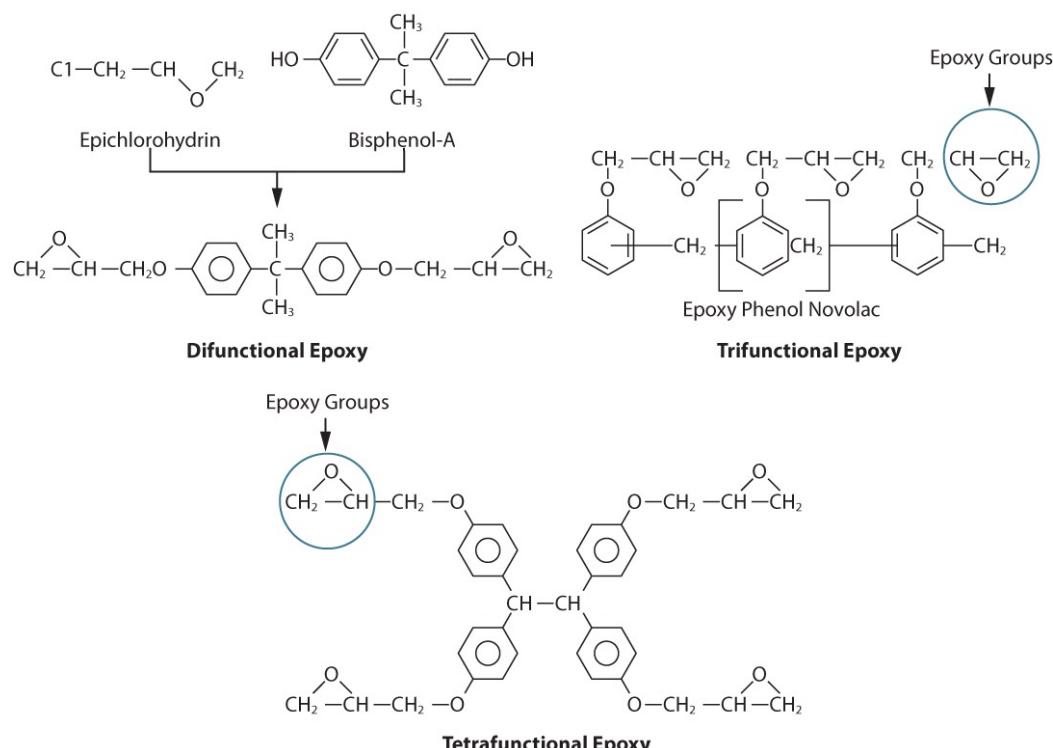
- Low-Cost Processes
 - Large panel manufacturing
 - Low temperature processes (<200 C)
- Low dielectric constant materials
- Matched expansion to mother board (PWB)
- Flexible materials for ultra-thin packages

Anatomy of an Organic Substrate

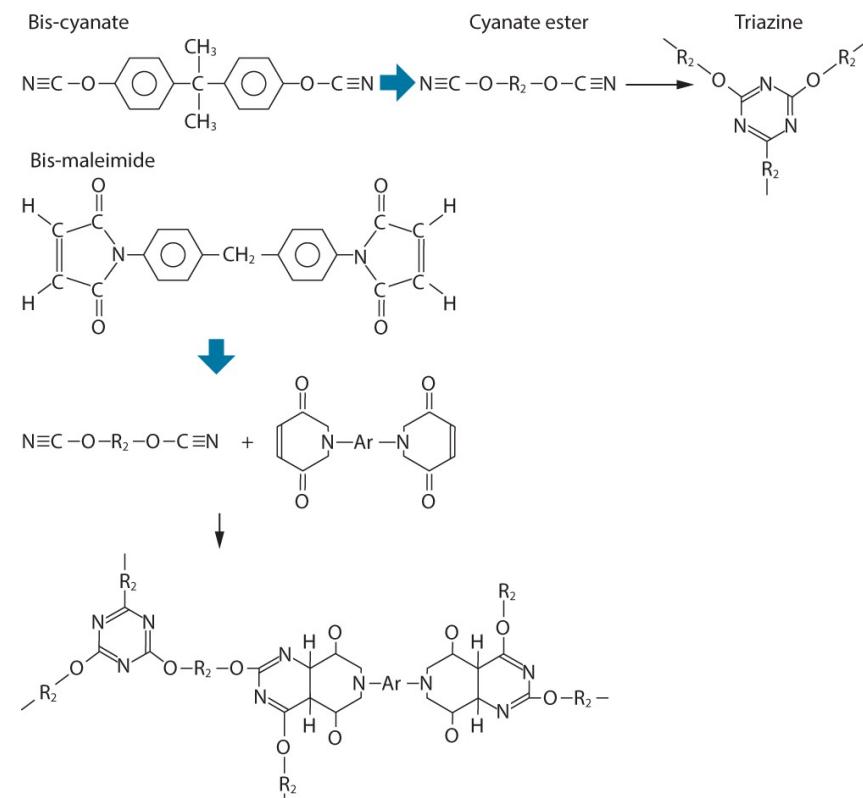


Organic Laminate Core Materials - Commonly Used Resins

➤ FR-4/FR-5: Most common series of organic laminate core materials. Comprised of one of several functional types of epoxy resins for a range of T_g (Glass Transition Temperature)

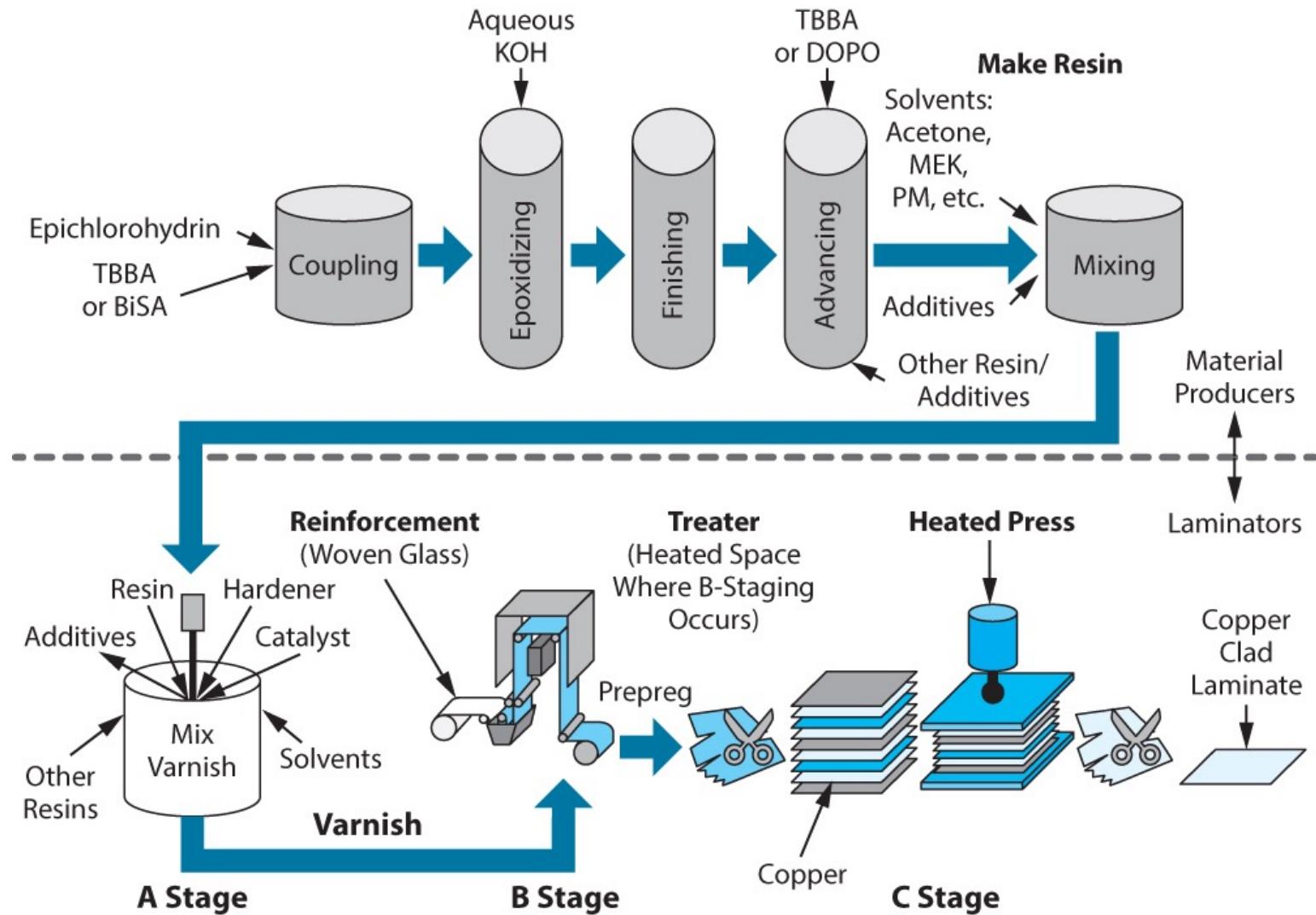


➤ BT - Bismaleimide-Triazine: A series of higher T_g laminate core materials with improved thermo-mechanical properties used in high performance package substrates

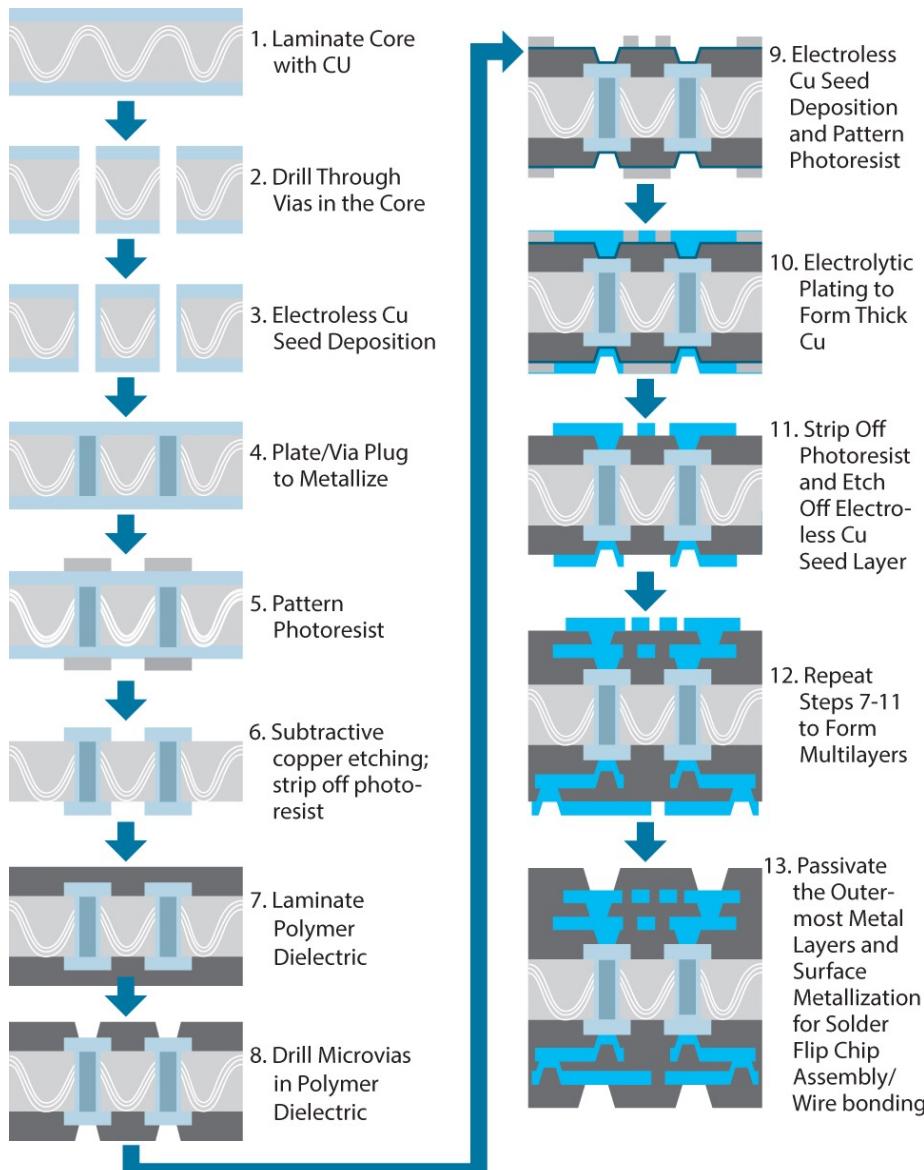


Organic Laminate Core Materials - Manufacturing Process

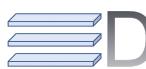
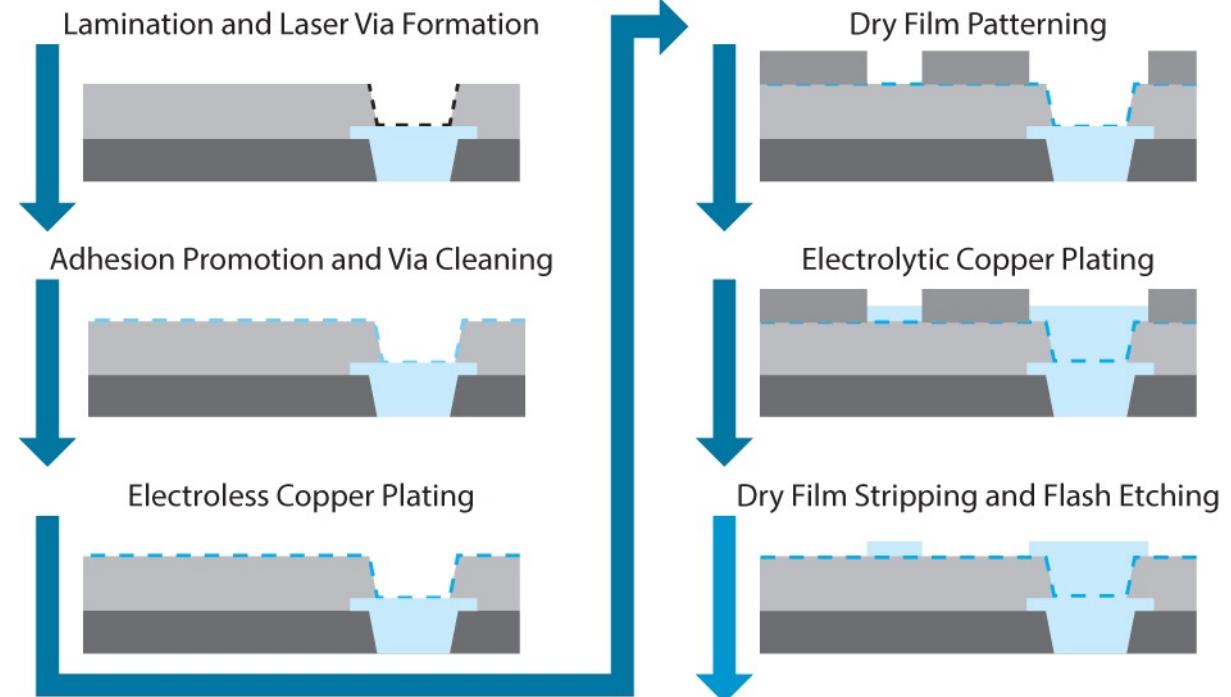
- **Prepreg:** Polymer resin impregnated into woven glass fabrics and partially cured to enable handling, while retaining adhesive properties
- **Laminate:** Final organic core material fabricated by hot pressing several prepgs (to achieve final thickness) with copper foils on both surfaces, a fully cured material ready for through via fabrication



Organic Substrate Process Flow

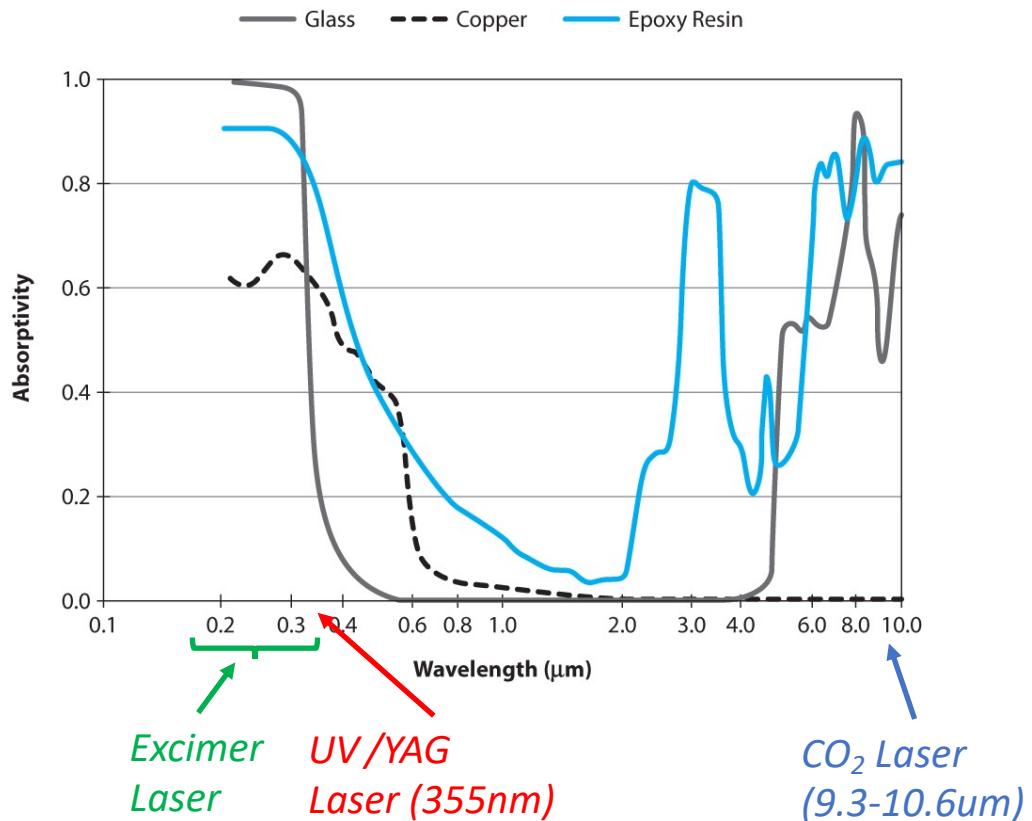


➤ **Semi-additive Process (SAP) is the most common build-up process flow used in current organic substrates**

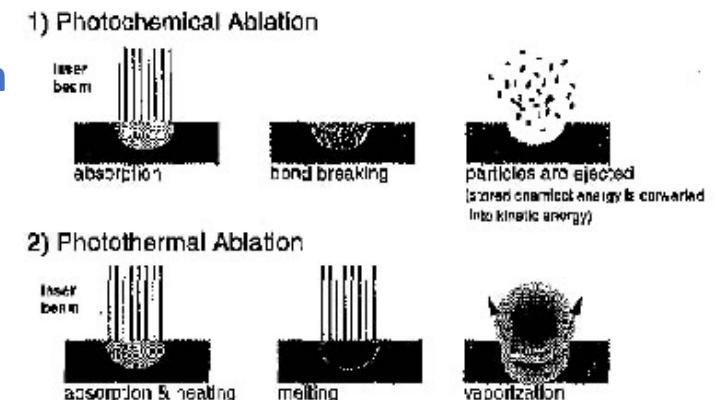


Laser Via Process Technologies

- Fundamental mechanism of laser-material interaction is governed by the absorption of the incident laser wavelength by the specific material (e.g. epoxy build-up films such as ABF)

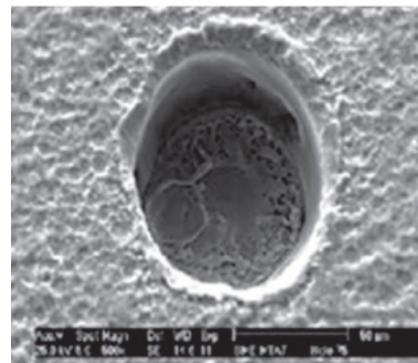


Laser Ablation Mechanisms



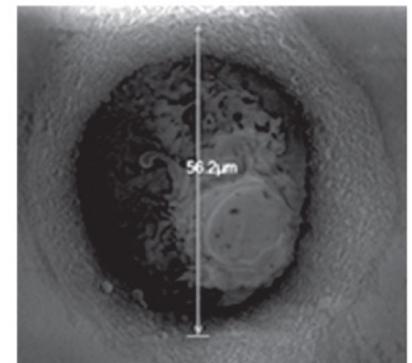
CO₂ Laser

- Thermal process
- Point-to-point drilling
- High throughput, inexpensive



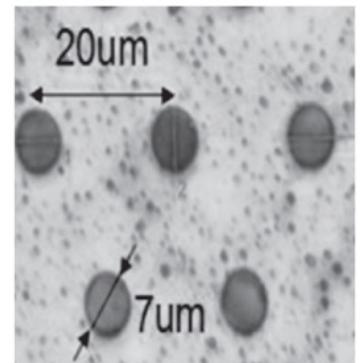
UV, Yag Laser

- Chemical/Thermal process
- Point-to-point drilling
- Medium throughput, high cost



Excimer Laser

- Mostly chemical process
- Mass via generation-projection lithography
- Potential for very high throughput, high cost

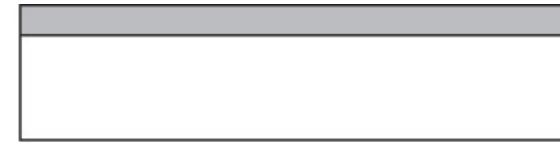


Copper Seed Layers on Polymer Dielectric Surface & Blind Vias

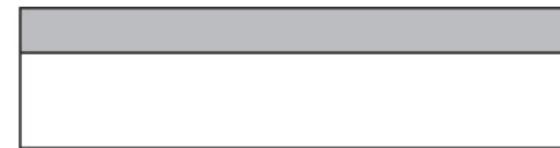
- Electroless copper plating is the most used manufacturing process
 - Wet process scalable to large batches of panels for high throughput
 - Polymer surface needs to be roughened to achieve sufficient copper adhesion
- Alternate process options such as Physical Vapor Deposition (PVD) and Plasma treatment of polymer dielectrics prior to electroless copper plating are being introduced to reduce Cu-polymer interfacial roughness

➤ Electroless Copper Plating Process Flow

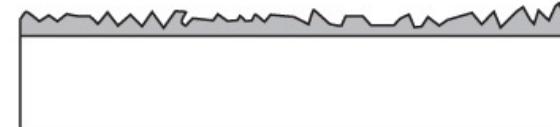
Untreated Sample



Swell Swelling Agent Prepares the Polymer for the Subsequent Etch Step

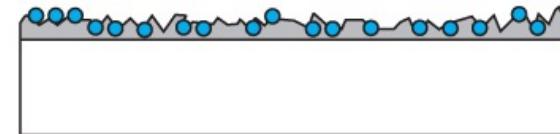


Etch Roughness is Created on Polymer Surface



Catalyst

● Pd Particle



Electroless Copper

□ Copper

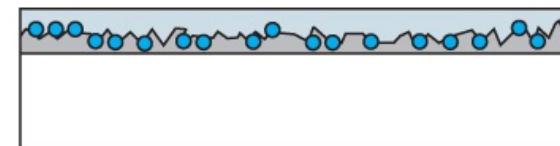
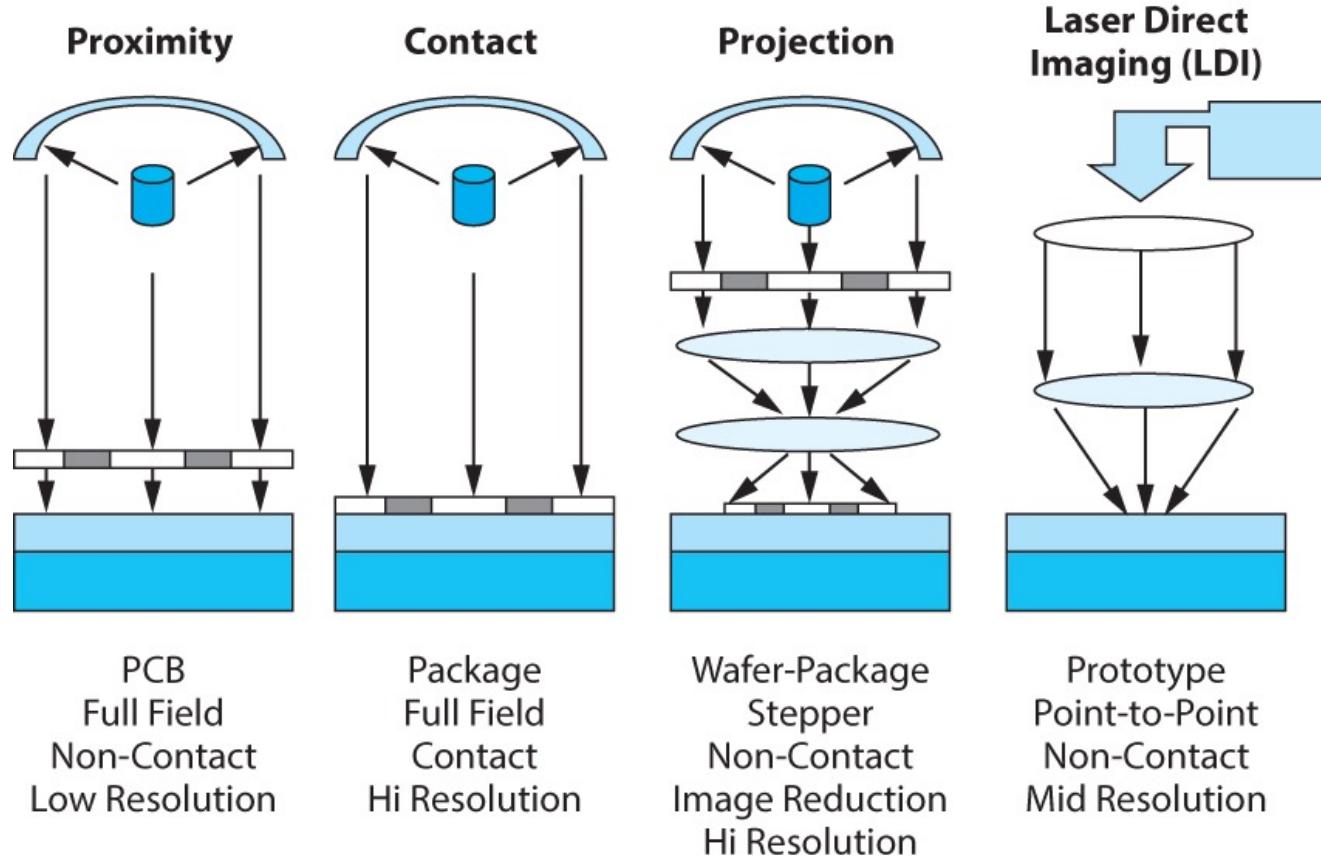
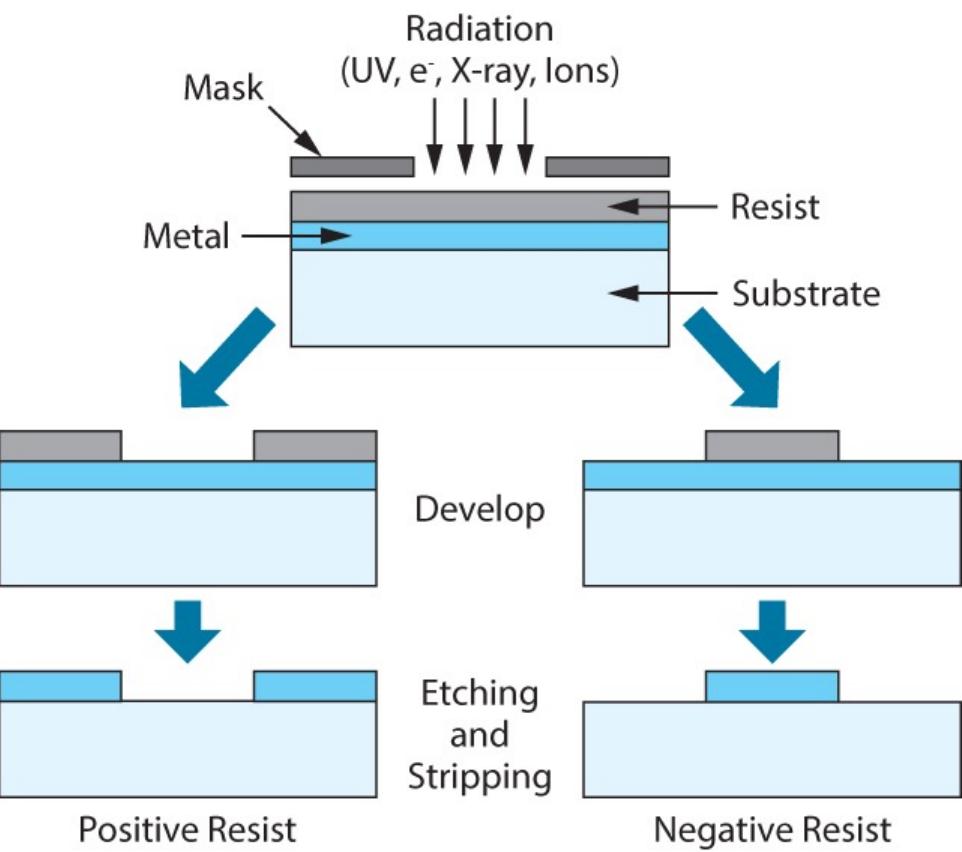


Photo-Lithography: A Critical Process Step in Scaling Wiring Pitch

➤ Four Main Types of Lithographic Processes



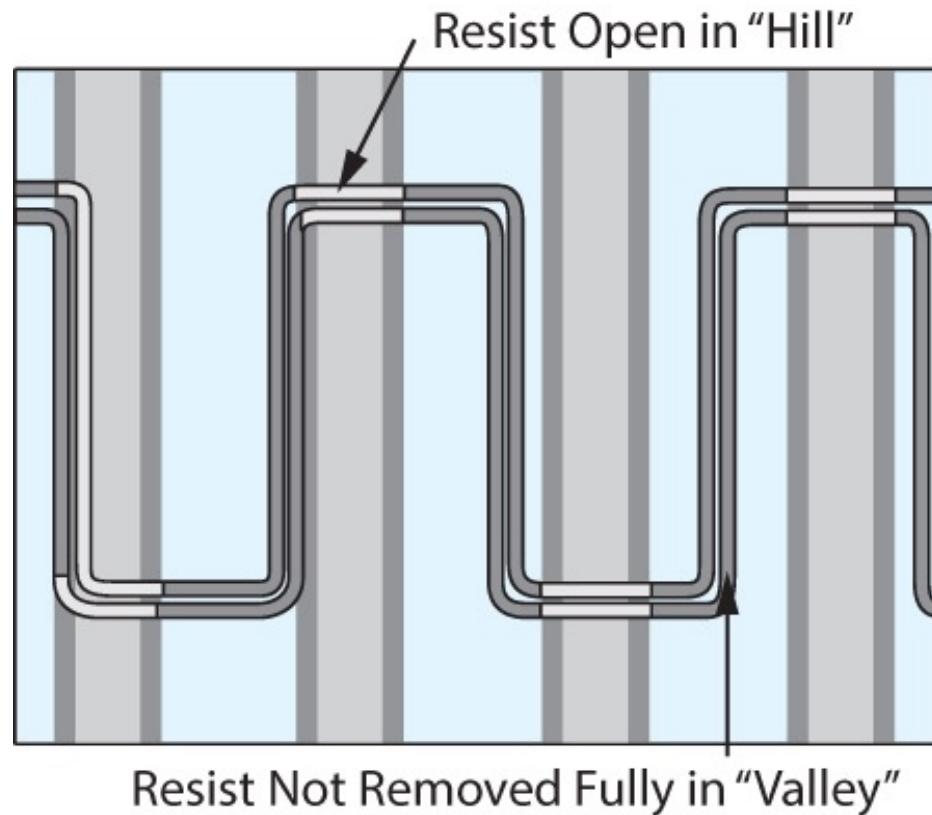
➤ Positive and Negative Photoresists



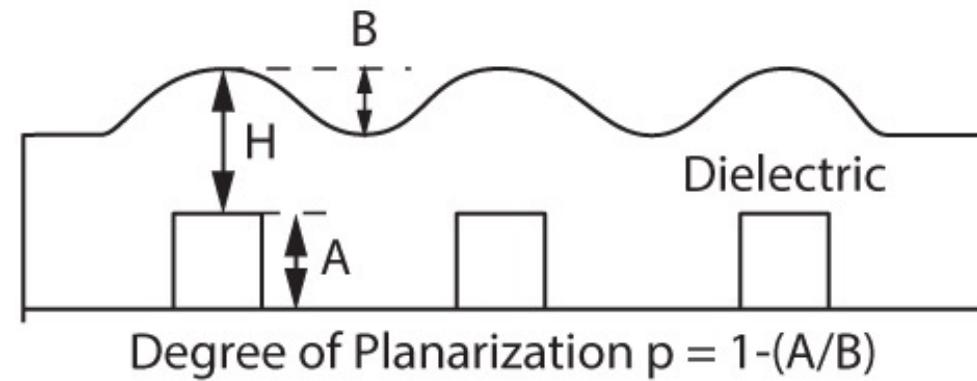
Depth of Focus (DoF) of the Lithography Tool and Surface Flatness/Smoothness of the Substrate Surface determine the smallest feature size that can be resolved.

Substrate Planarization and Degree of Planarity (DoP)

- Planarization of every build-up or RDL layer is becoming a critical requirement in the process flow to continue scaling the copper line widths and spaces from 10 microns to 1-2 microns and below.



(a)

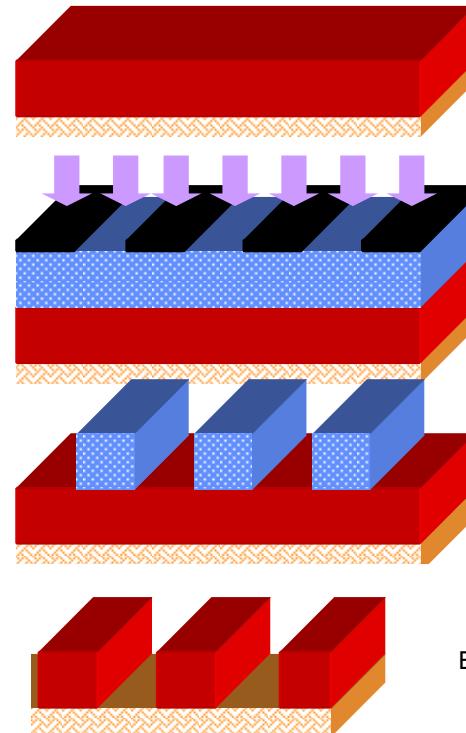


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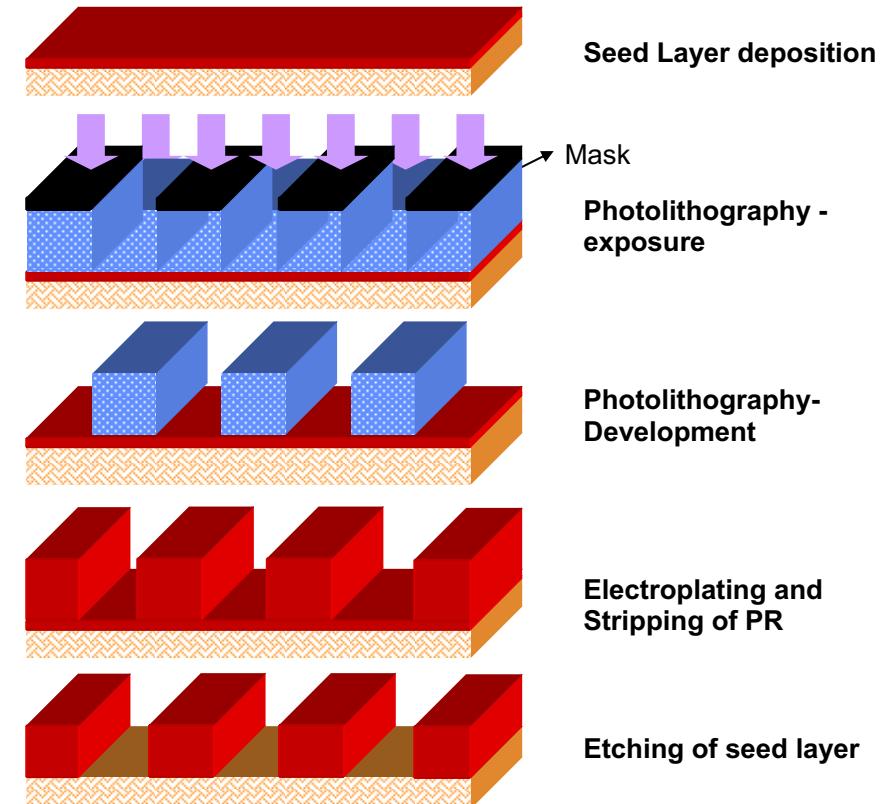
Copper Conductor Patterning: Subtractive vs. Semi-additive Process

- Subtractive patterning is used on the core layers (Copper Foil) of the organic laminate substrate
- SAP patterning is used on the build-up layers

Subtractive Patterning

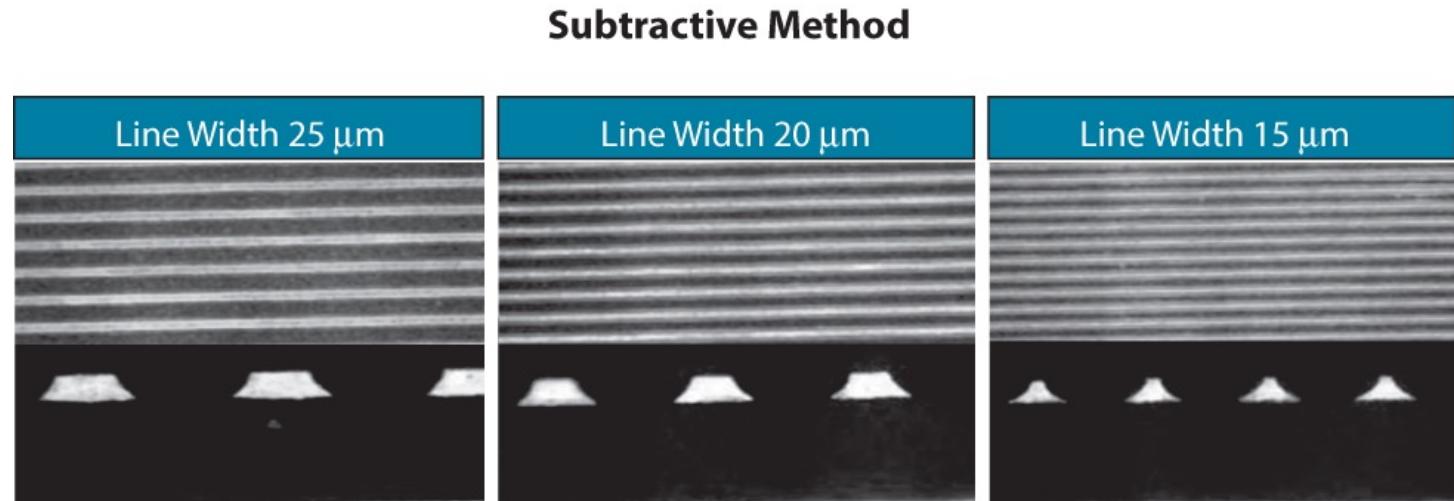


Semi-Additive Process (SAP)

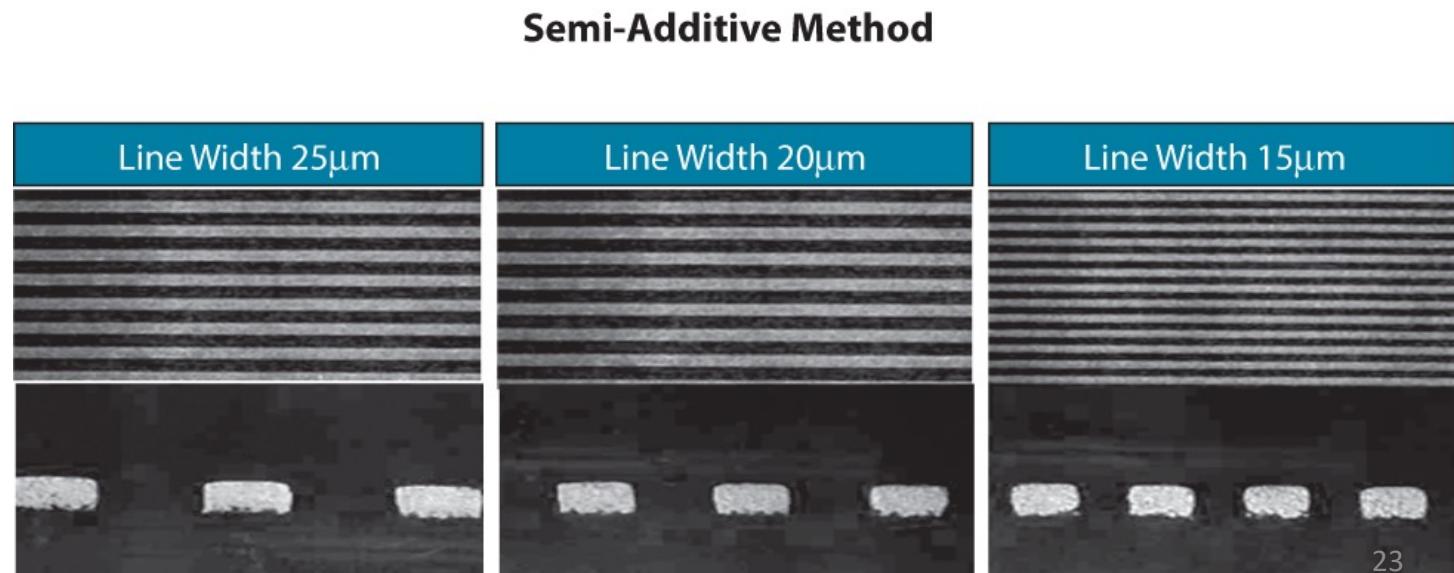


Comparison of Subtractive and Semi-additive Processes

- Concerns in achieving $<20\text{ }\mu\text{m}$ Cu traces using subtractive etching process with 12- μm thick Cu foil

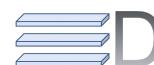
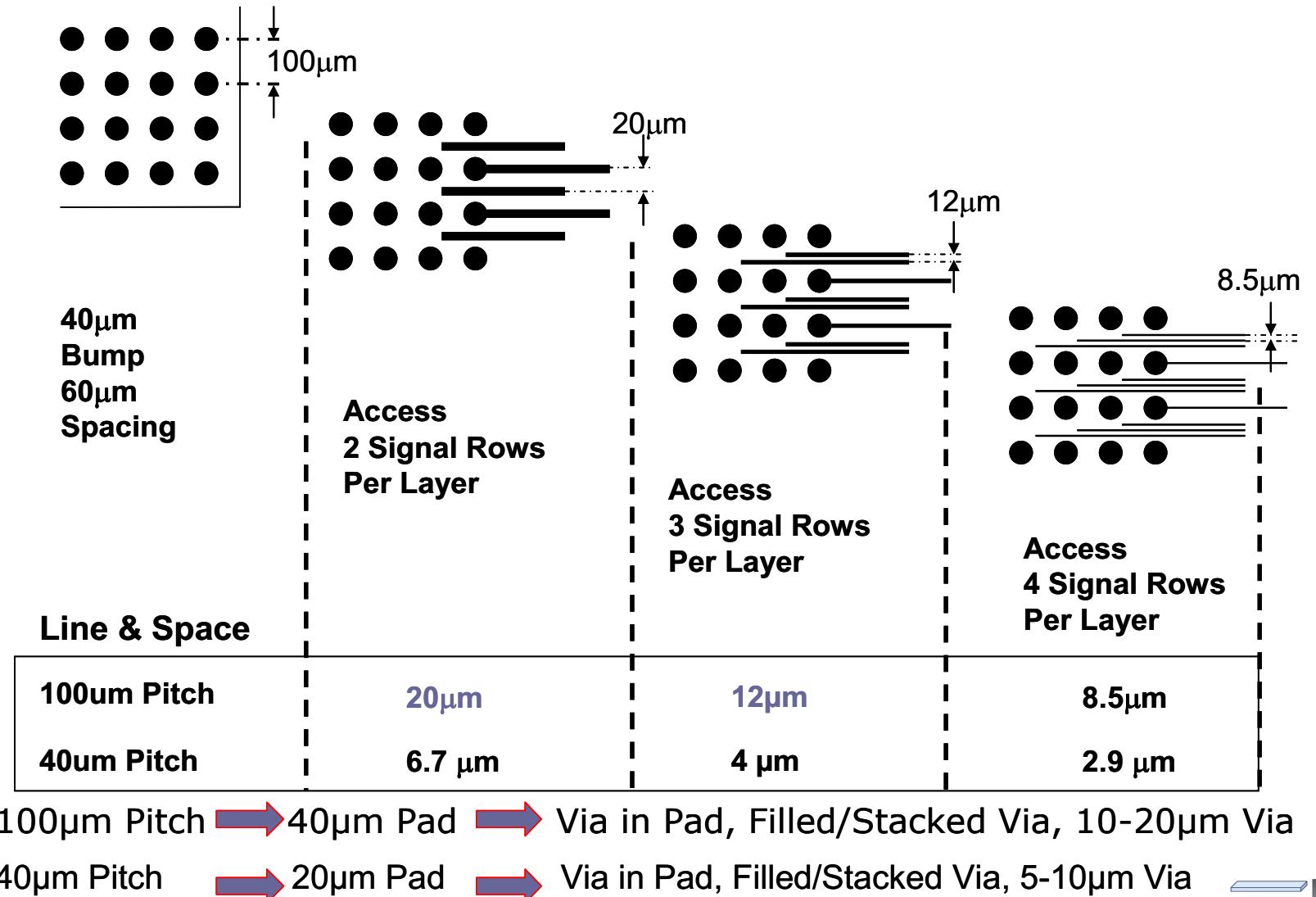


- Fabrication of 15 μm Cu trace using semi-additive process - scalable to less than 10 μm dimensions

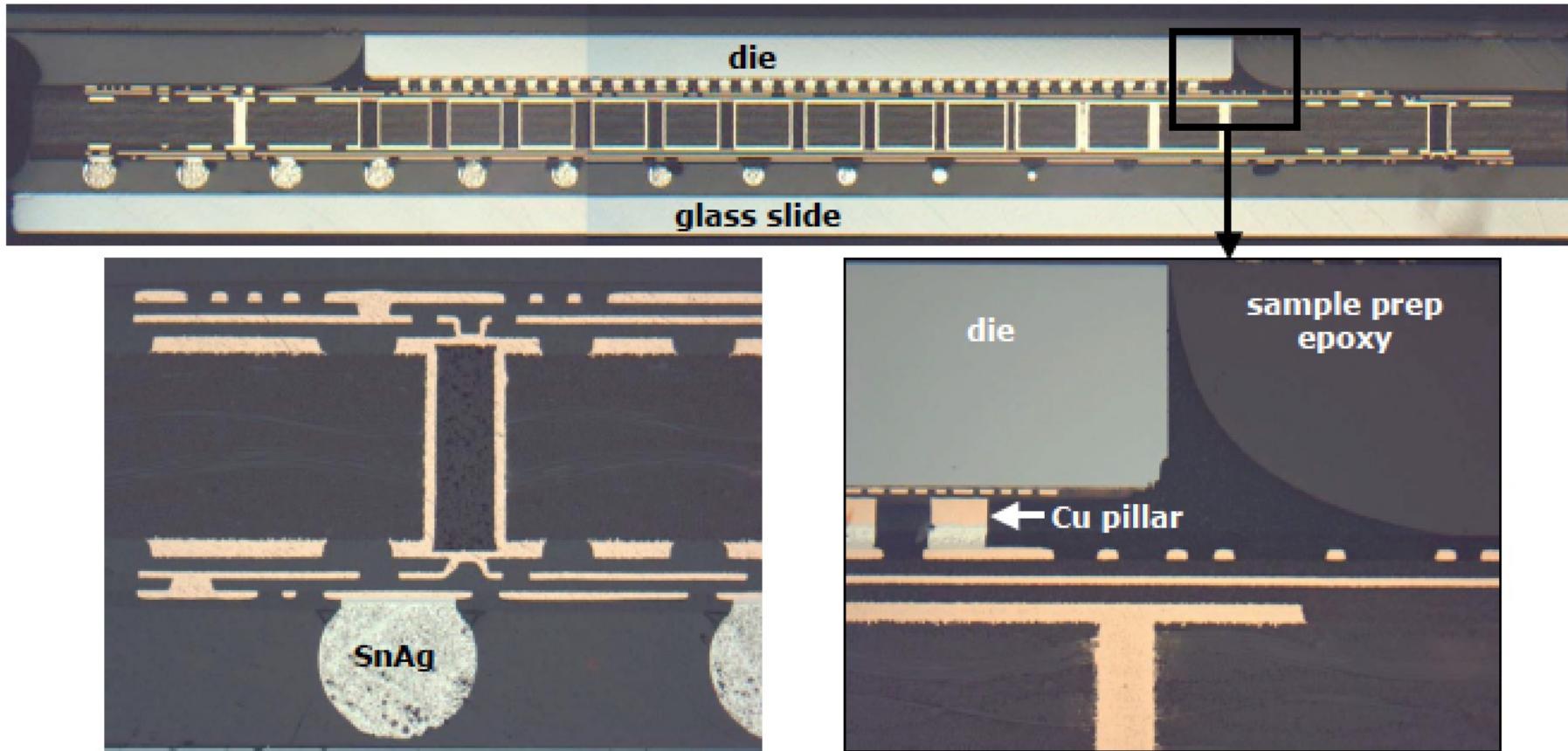


Routing Example for Multi-layer Build-up or RDL

- Any copper wiring layer consists of copper traces (or lines), spaces between lines, and blind via capture or landing pads.
- Wiring density of a substrate is a combination of dimensions - line widths and spaces, blind via and pad diameters.
- Smaller dimensions lead to lower layer counts for the same chip bump pitch



High Volume Application of Organic Substrates in CPU Packaging

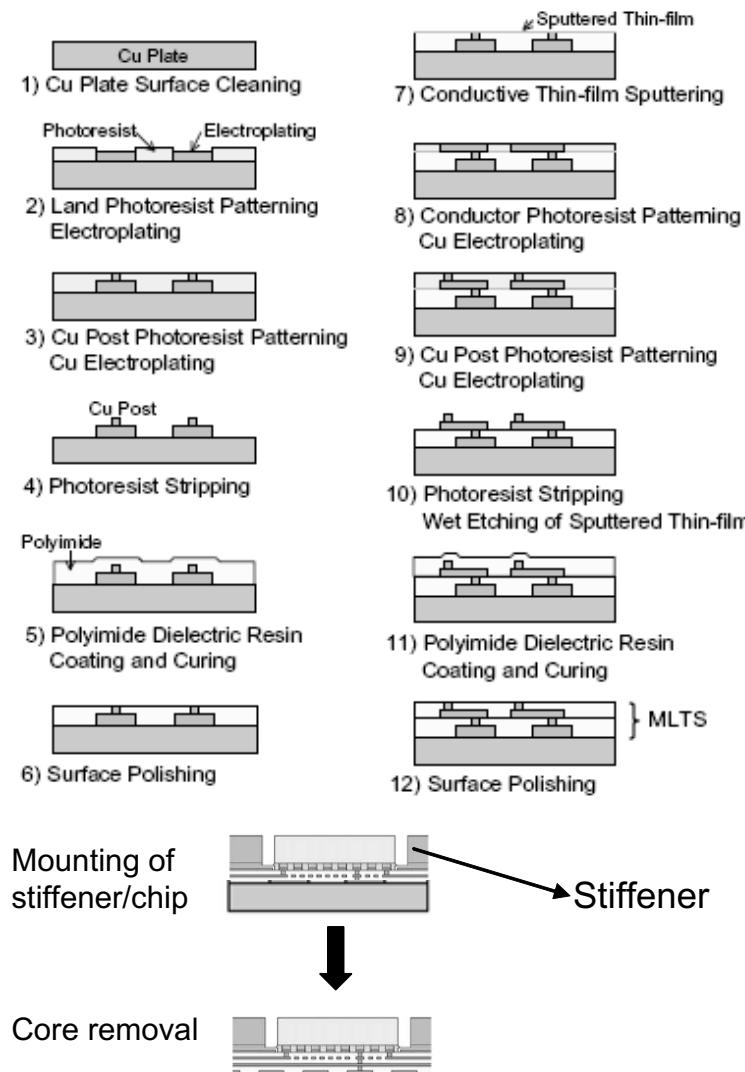


- Intel 45-nm Atom processor with copper pillar
- Six-layer substrate, double-sided core, four RCC layers
- Completely Pb-free for all Intel flip chip products

Source: Chipworks

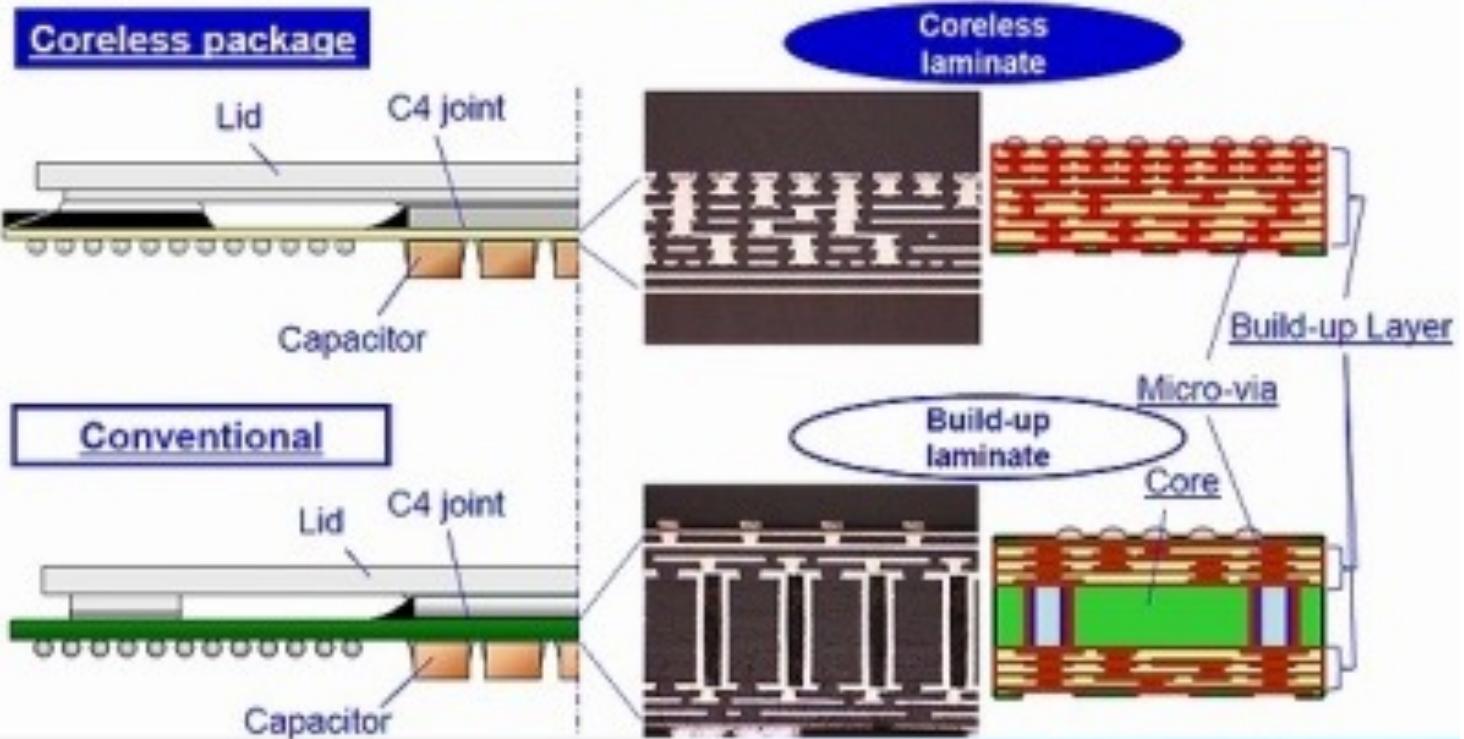
Coreless Organic Substrates - Thinner, Higher Performance

➤ Typical Process Flow



Package with high density wiring laminate by using only build-up process

Coreless package

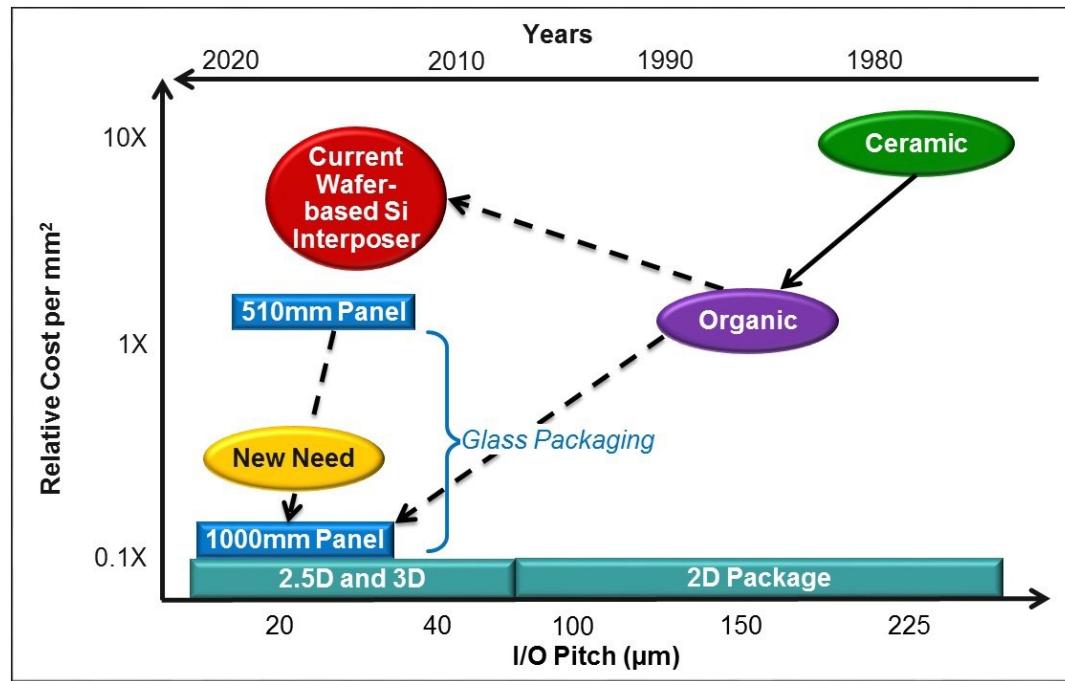


Source: Sony Semiconductor, 2011

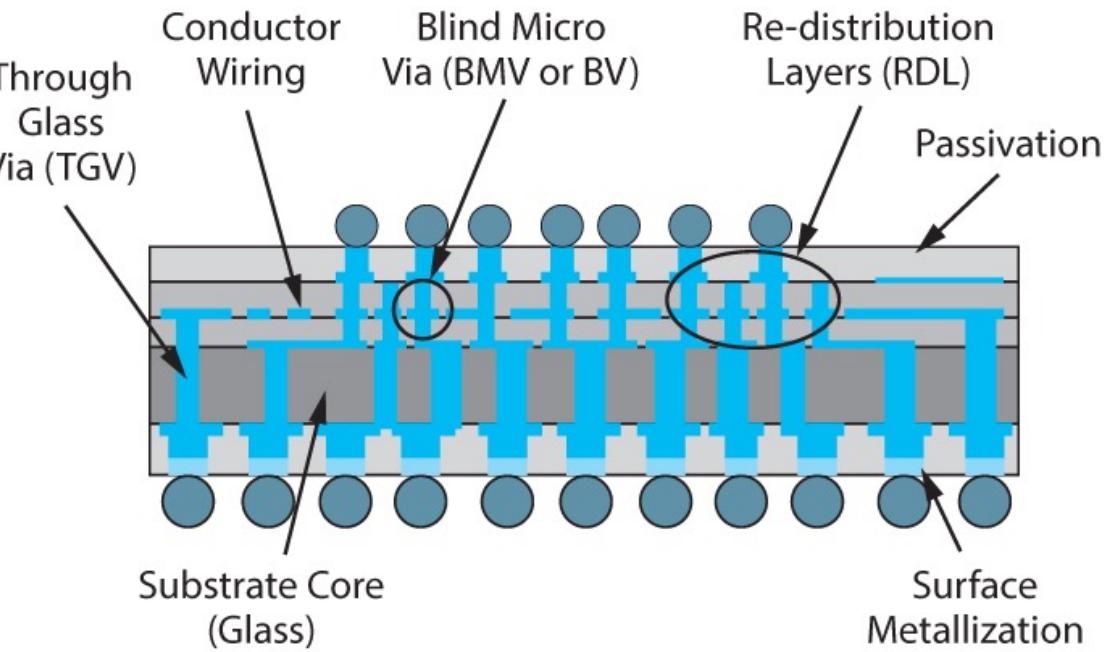
Glass Substrates - Emerging Technology to Continue Scaling

Why Glass Substrates?

- In R&D since the late 2000s, expected to enter manufacturing volumes in the next 3-5 years



Anatomy of a Glass Substrate



Typical Process Flow for Fabrication of Glass Substrates

1. Glass with TGV Drilled



2. Core Polymer Lamination to fill TGV



3. TPB Drilling through Polymer



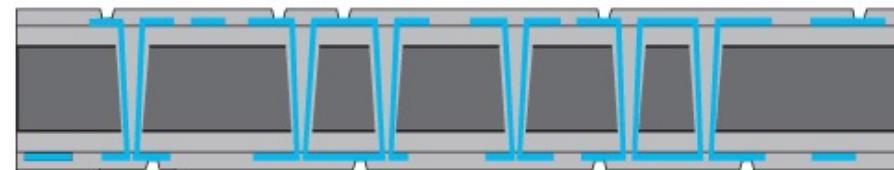
4. E-less Plating for TPV Coating



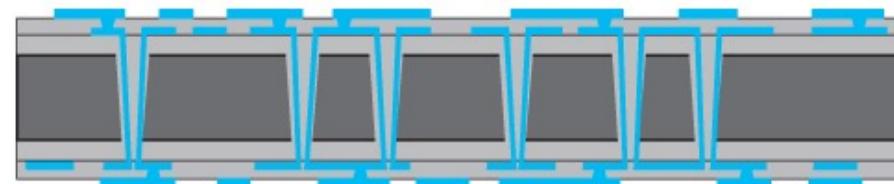
5. Metallization of Inner Layer



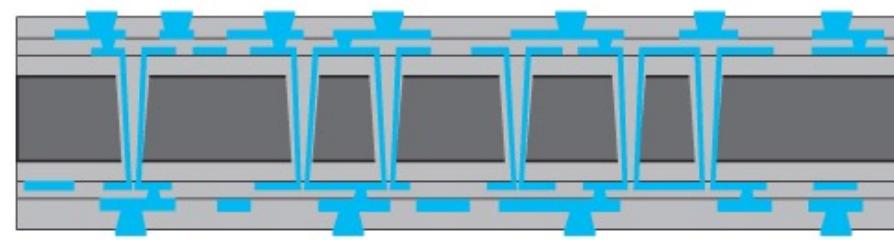
6. Polymer Lamination and Blind Via Drilling



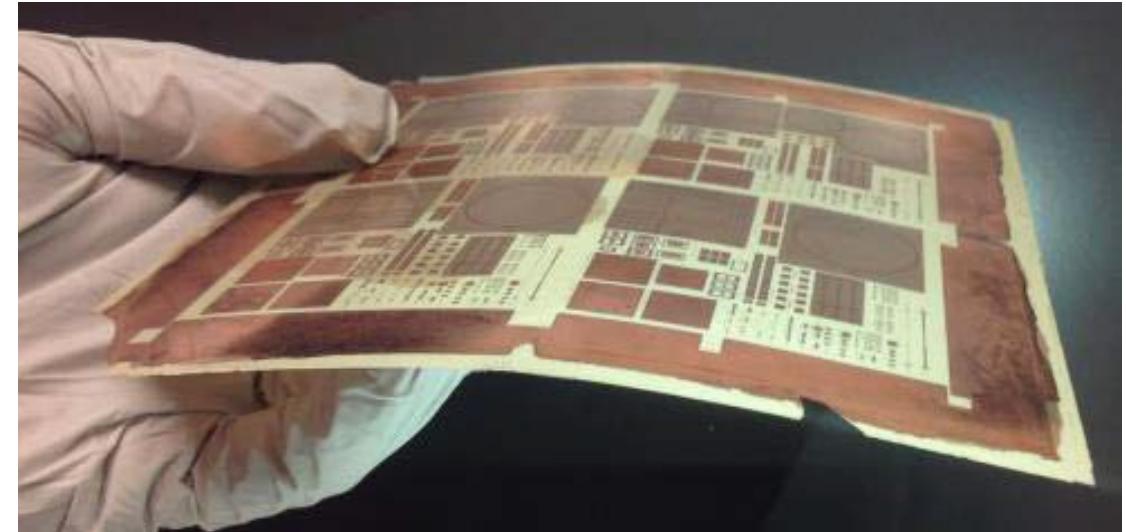
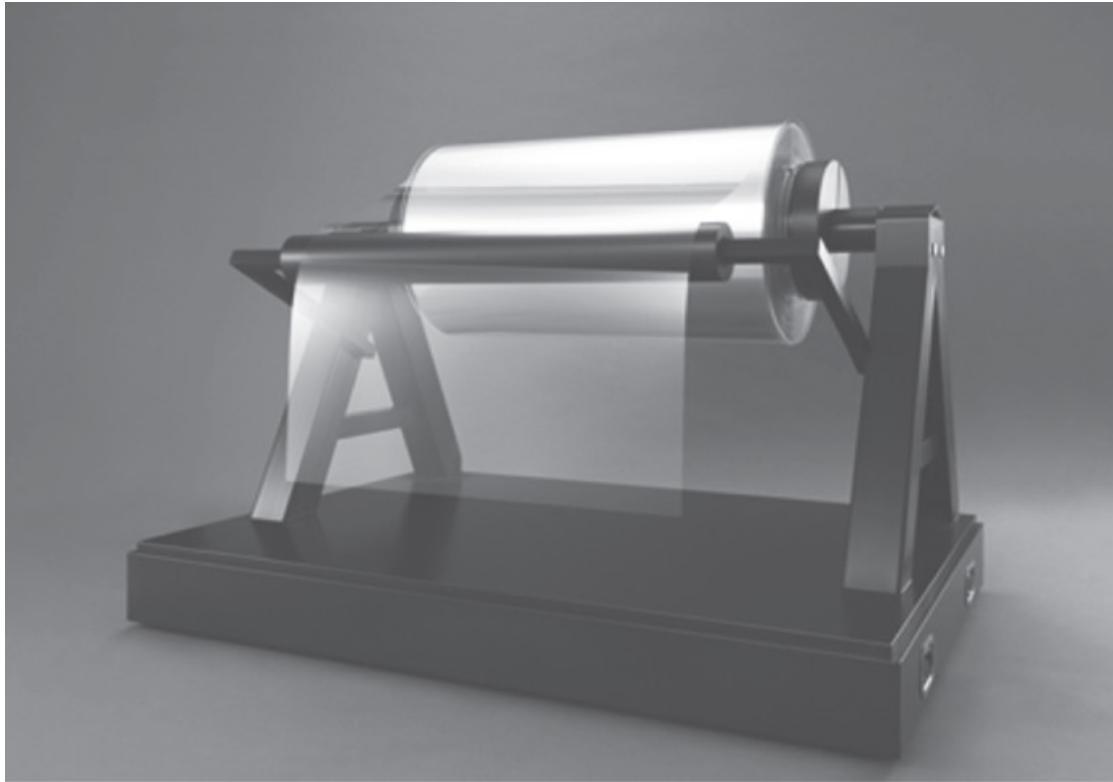
7. Metallization of Outer Layer



8. Passivation and Surface Metalization



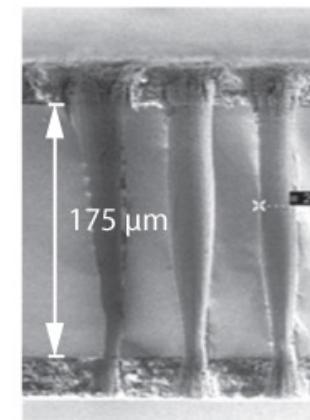
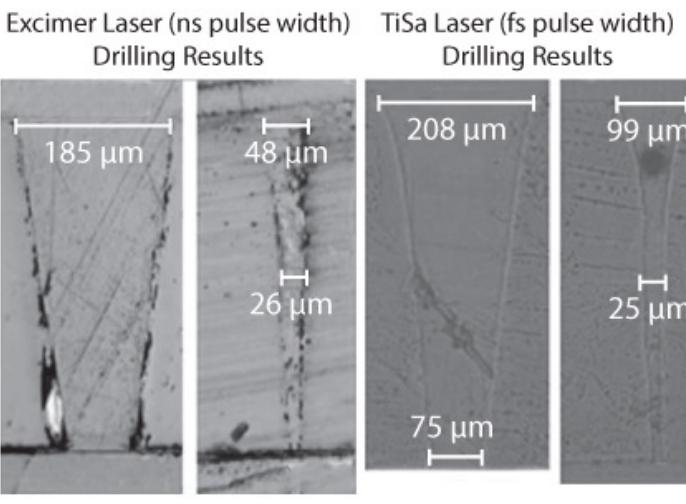
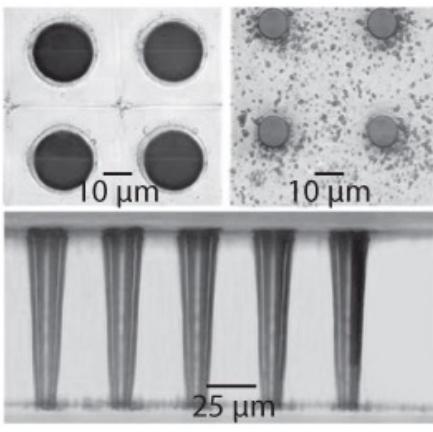
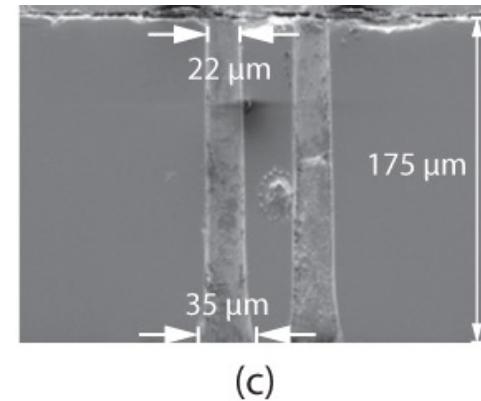
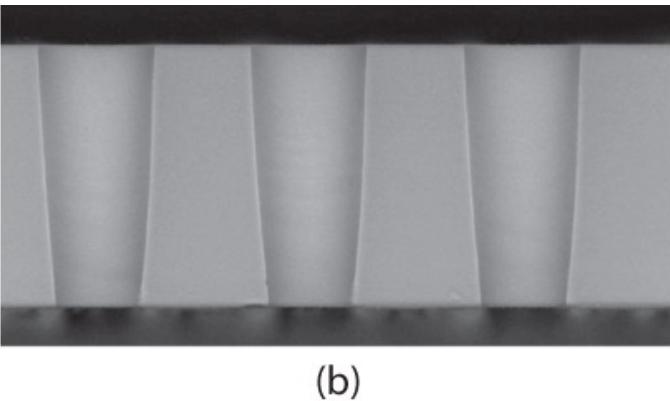
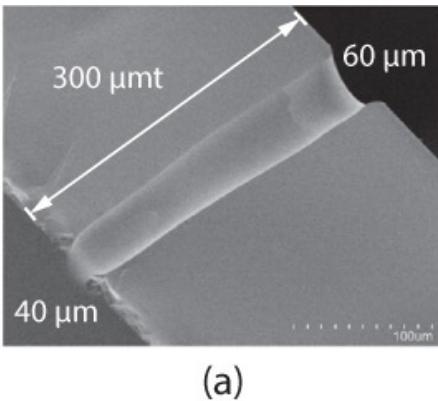
Thin-glass (30-100 μm) in Roll Form Ready for Substrates



30 micron Glass Core Substrate

Courtesy: Vijay Sukumaran, PhD Thesis

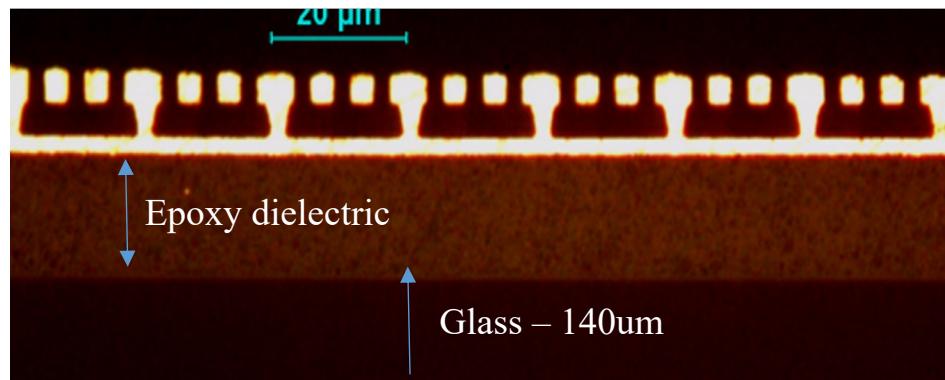
Through Vias in Glass Core: Key Enabler for Glass Substrates



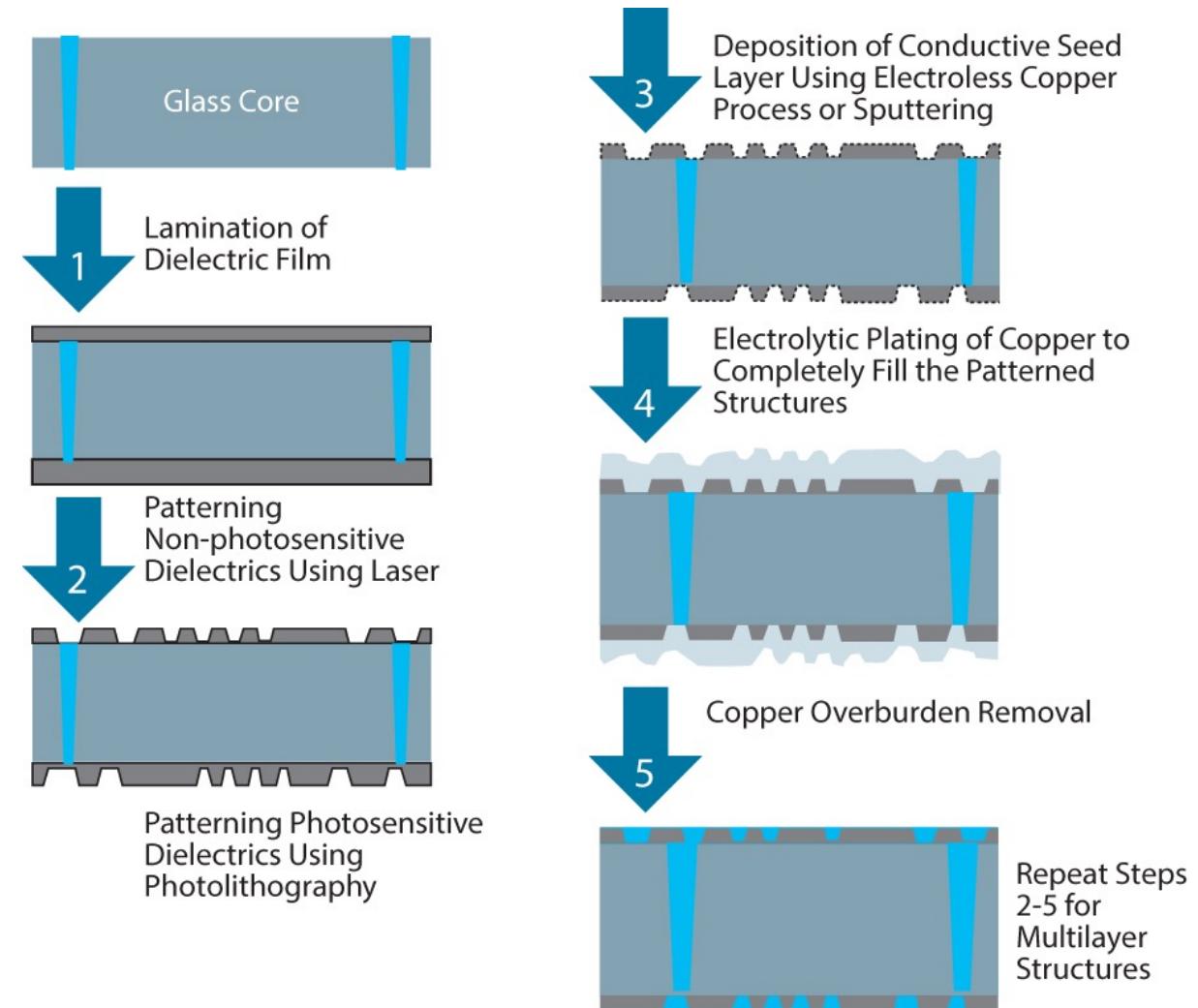
Through Glass Vias using several methods: (a) Electrical discharge (*Courtesy of AGC*), (b) Laser + Wet etch (*Courtesy of Corning*), (c) Excimer laser ablation (*Courtesy of Georgia Tech PRC*), (d) 193 nm excimer laser ablation (*Courtesy of Coherent*), (e) Laser ablation (*Courtesy of Fraunhofer IZM*), and (f) Excimer laser-ablation on polymer-laminated glass (*Courtesy of Georgia Tech PRC*)

Embedded Trench RDL Process for less than 5 μm Lines and Spaces

- Laser Ablation or photo-definition of Trenches
- Seed layer deposition in trenches, vias and surface
- Filling of Line Trenches with Electroplated Copper
- Polishing to remove copper overburden and form a planar surface
- Repeat above steps for multiple RDL layers

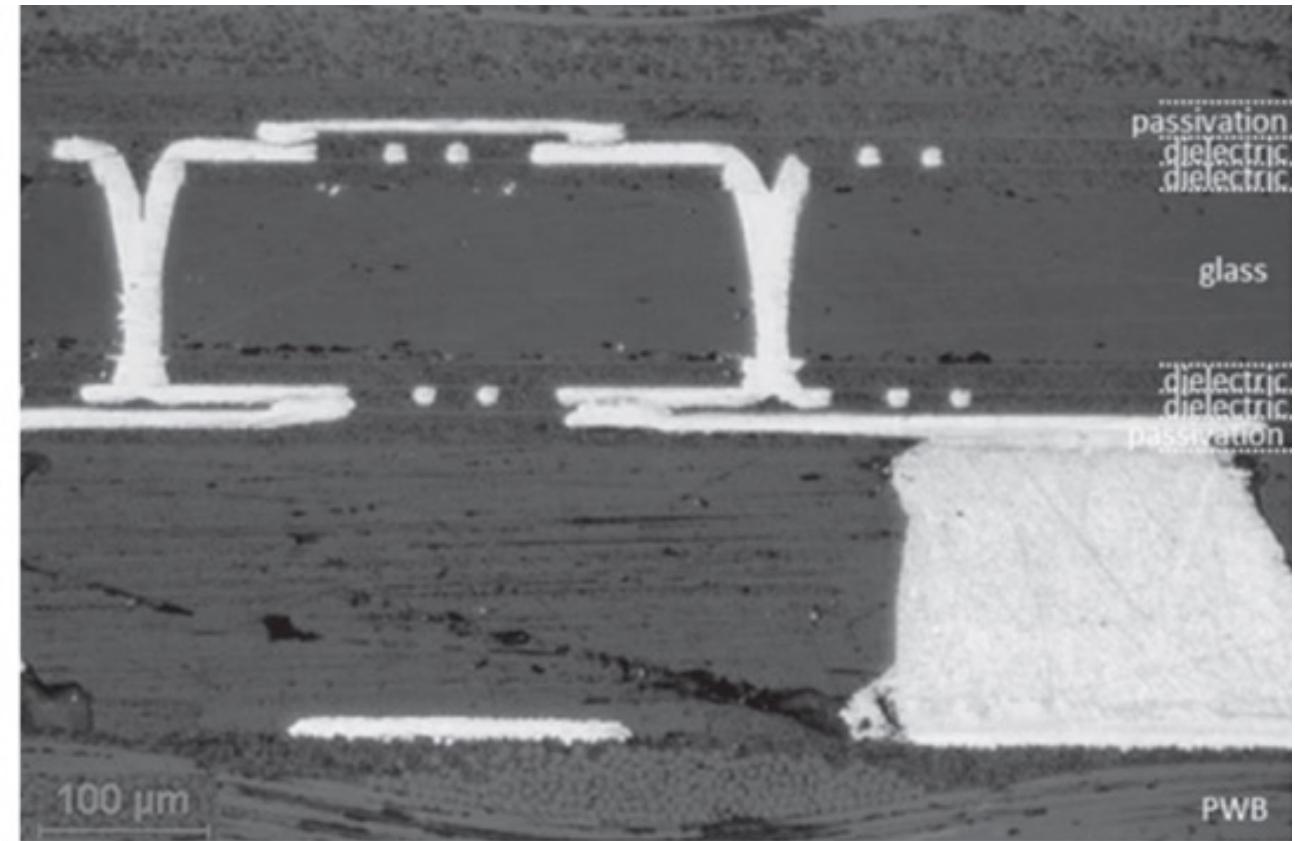
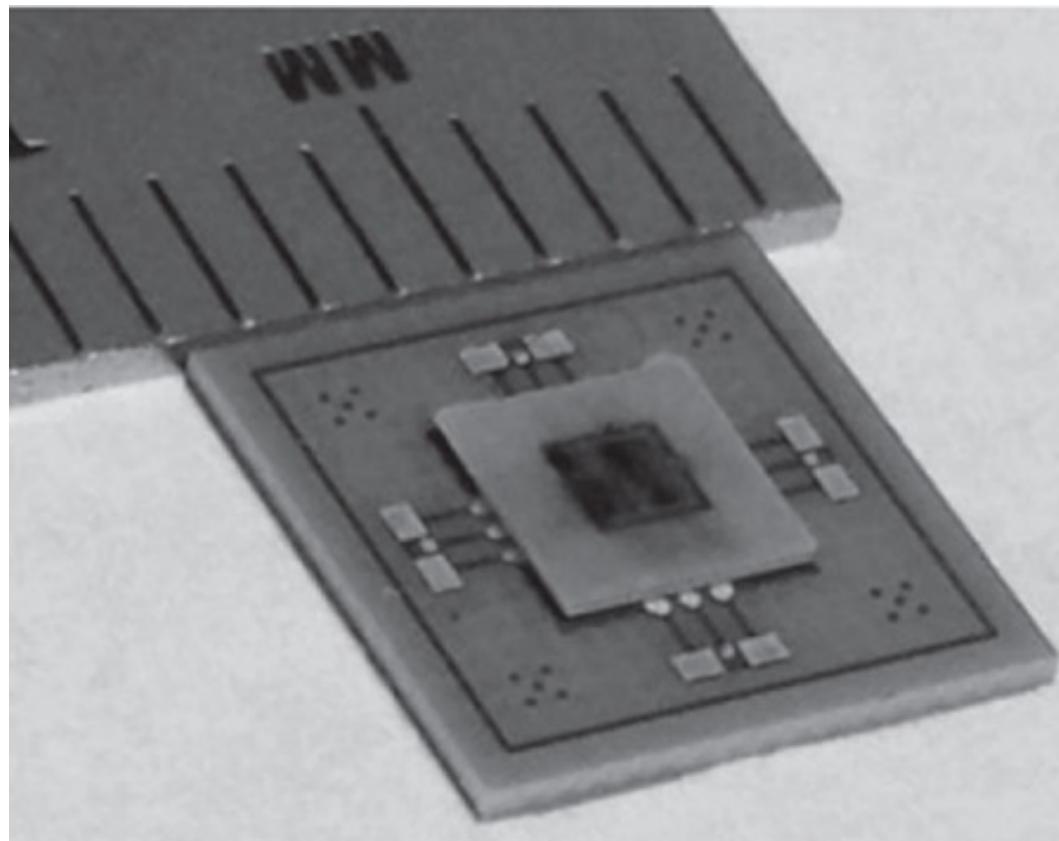


Silicon-like RDL on Glass Panels (Courtesy of GT PRC)



Application Example of Glass Substrates with Embedded Passives

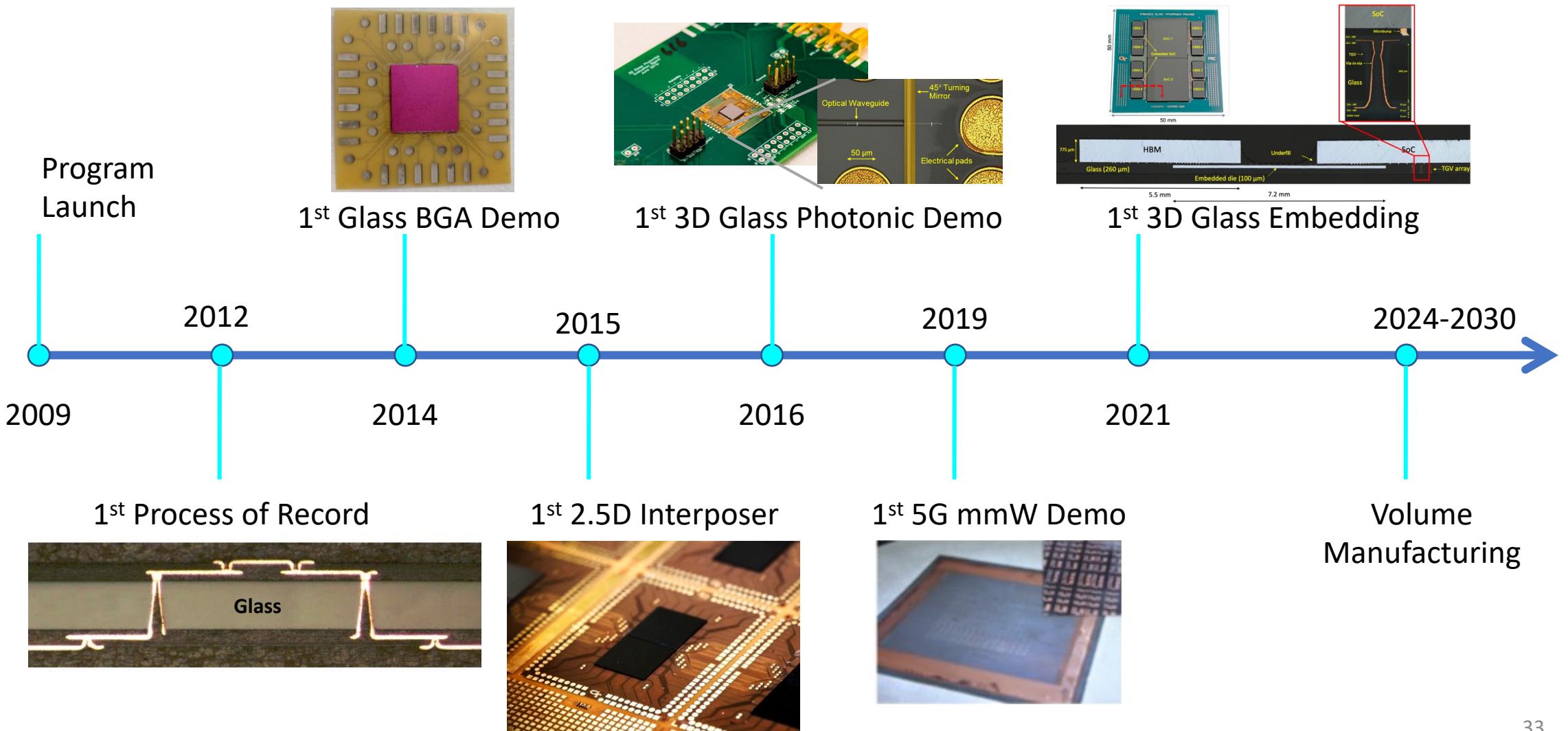
- High Precision RF Capacitors and Inductors fabricated in the RDL copper layers on both sides of the glass core.



RF module on glass substrate assembled onto PWB (Courtesy of Georgia Tech PRC)

Glass Panel Substrates by Industry Partners & Georgia Tech

R&D Investments exceed \$100M; Multiple Companies Investing in Manufacturing in Recent Years



Ultimate Potential of Glass for Low Cost

**Roll-to-Roll Glass For
Ultra-Smart System Substrate**



**System Substrate
*10X Cost Reduction***

>1000mm

**System Substrate
*5X Cost Reduction***

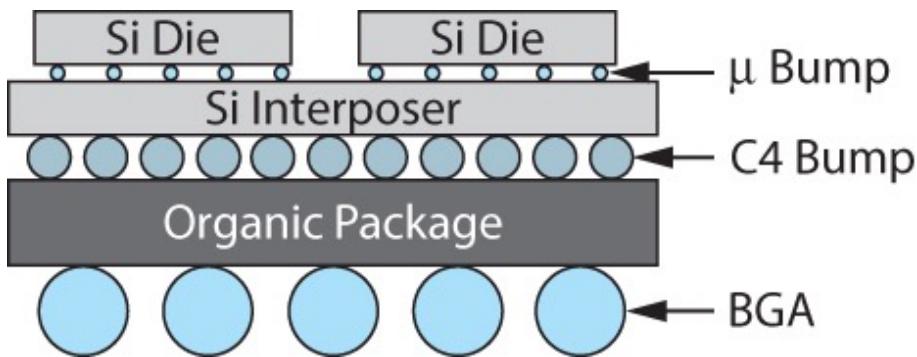
510mm

**Silicon
Substrate**

**Silicon
Wafer
300mm**

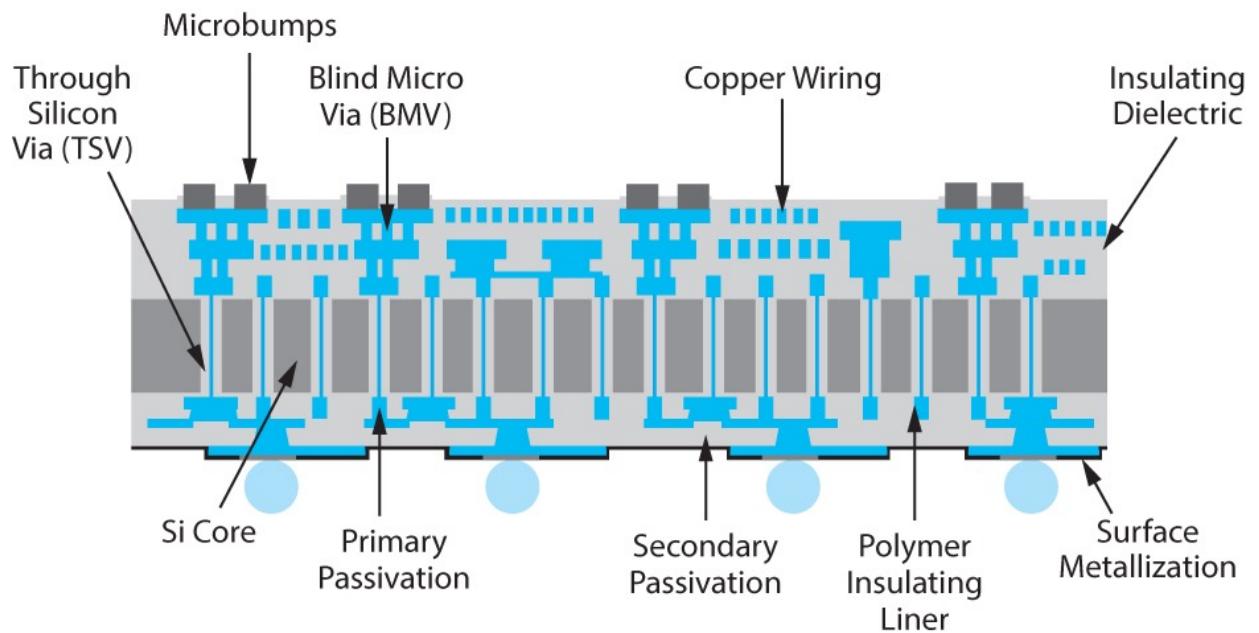
Silicon Interposers: Wafer Back-End of Line (BEOL) RDL and TSVs

- Packaging with Silicon interposers with an additional organic BGA package



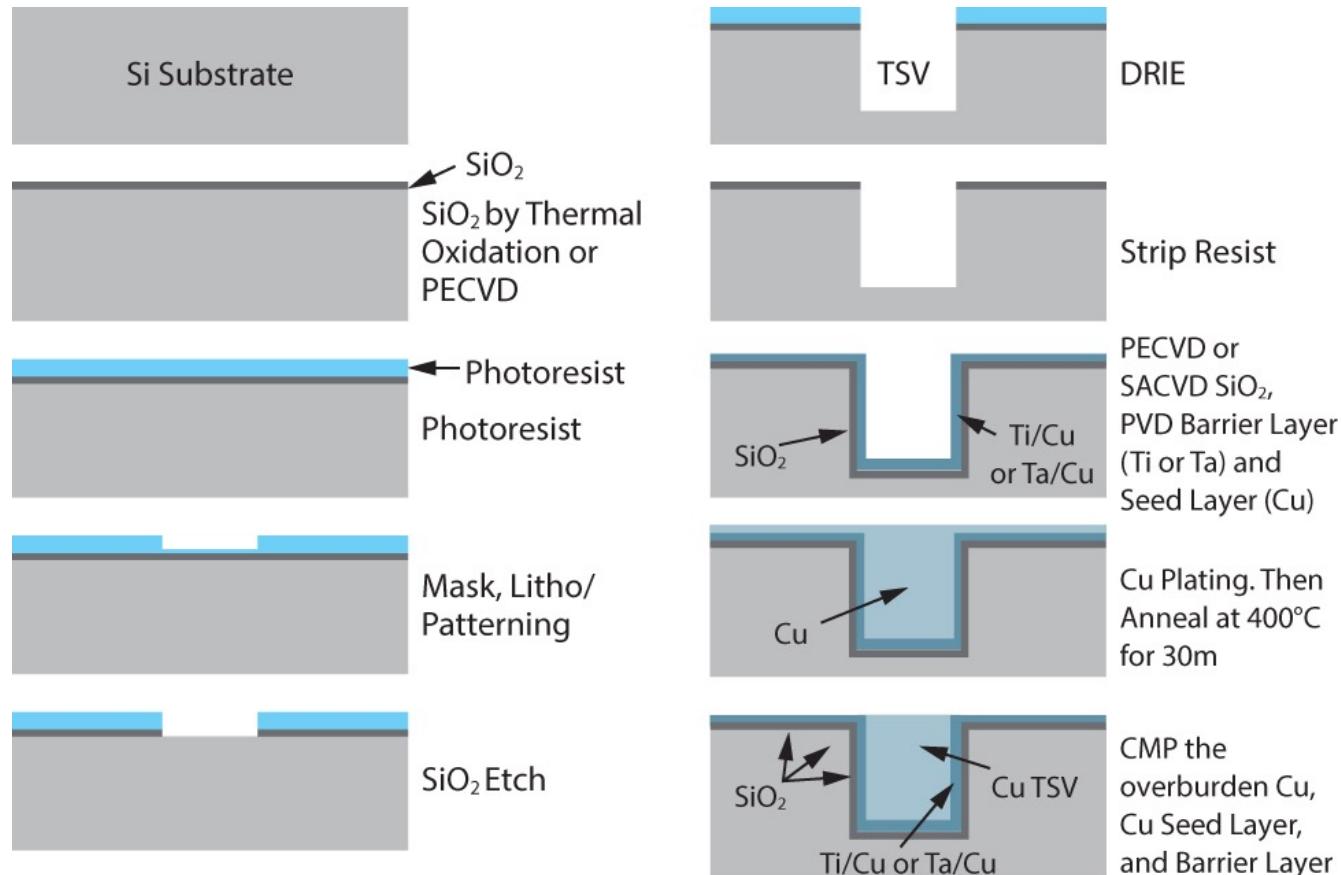
- Silicon ICs are mounted on Silicon Interposers using “microbumps”, whereas Silicon Interposers are assembled to organic substrates using flip-chip “C4” bumps

- Anatomy of a Silicon Interposer

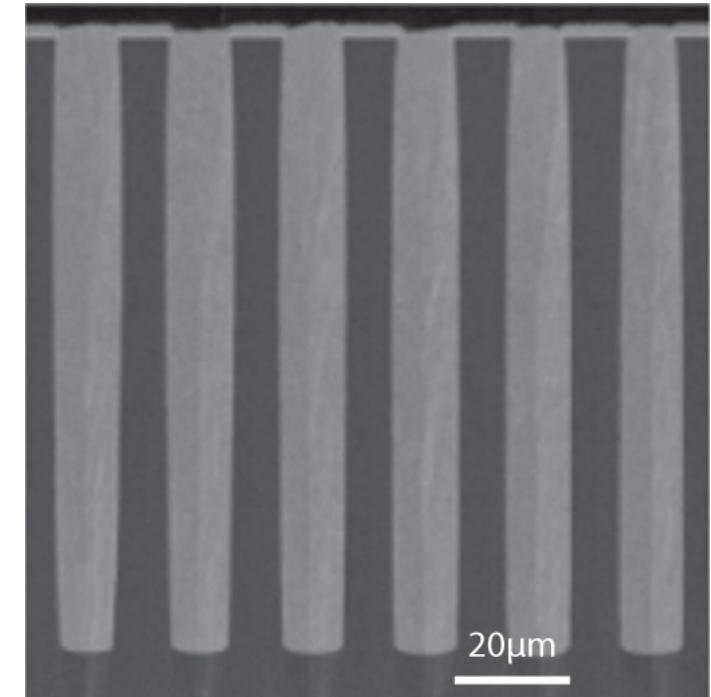


Through Silicon Via (TSV) Process Flow

➤ Typical Process Flow for TSVs



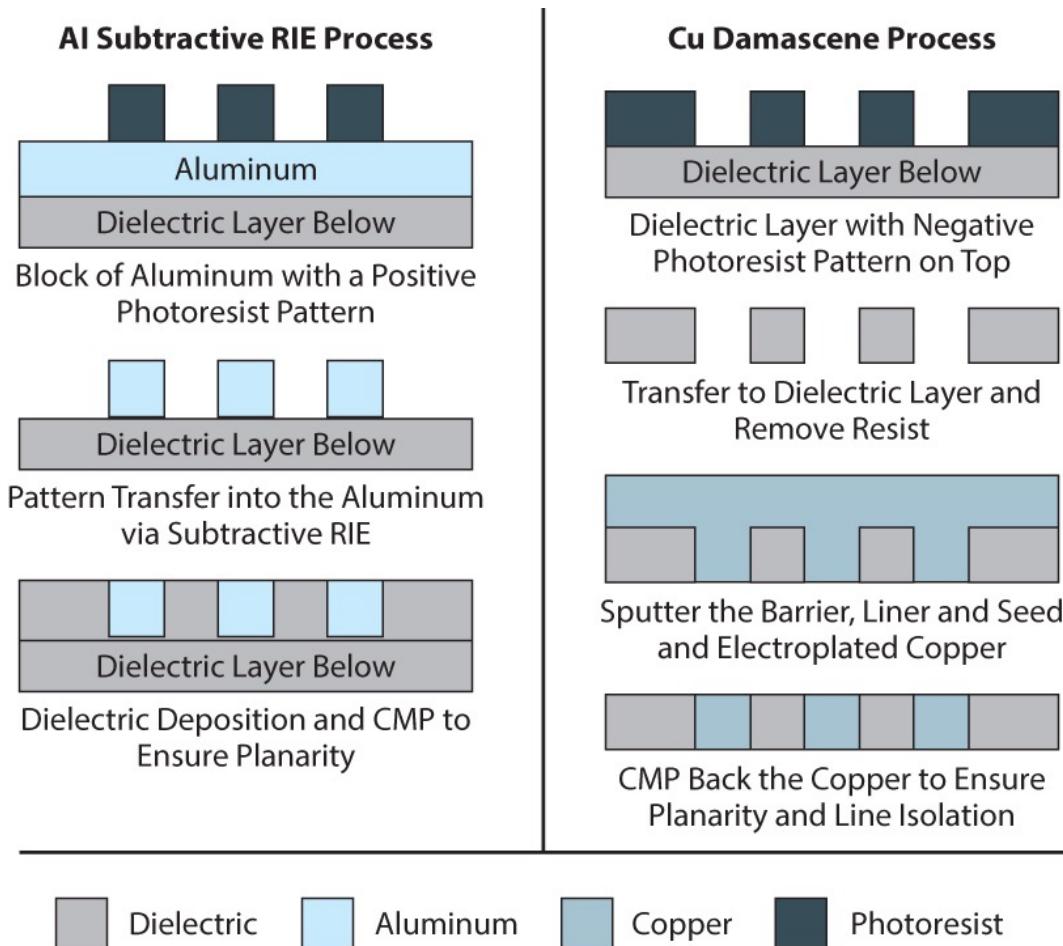
➤ Cross-section image of Cu-filled TSVs



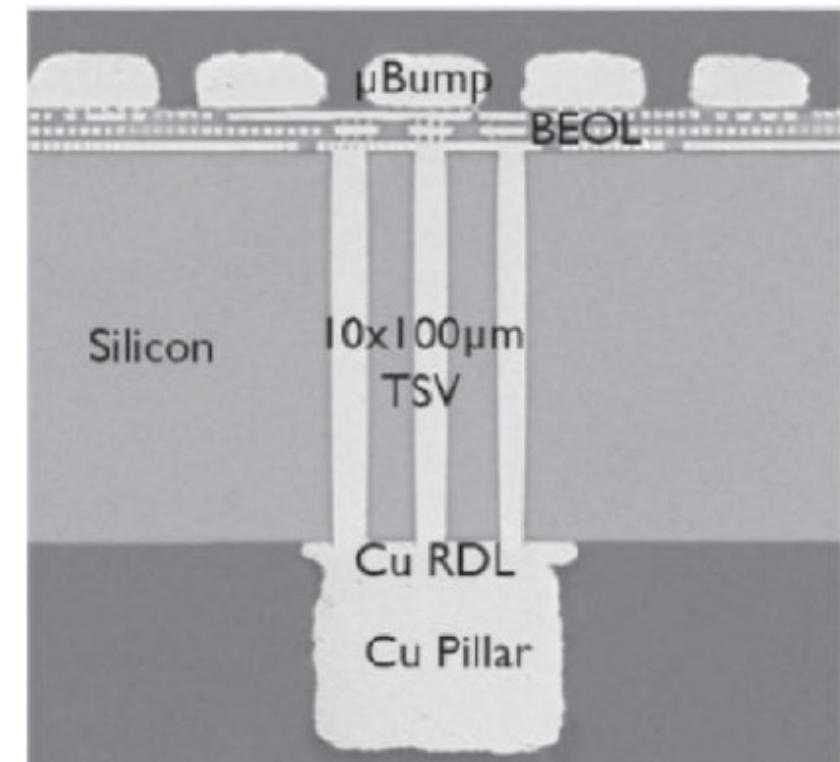
(Courtesy of ADEKA Corporation)

Wafer Back End of Line (BEOL) RDL

➤ Typical Process Flow for BEOL RDL



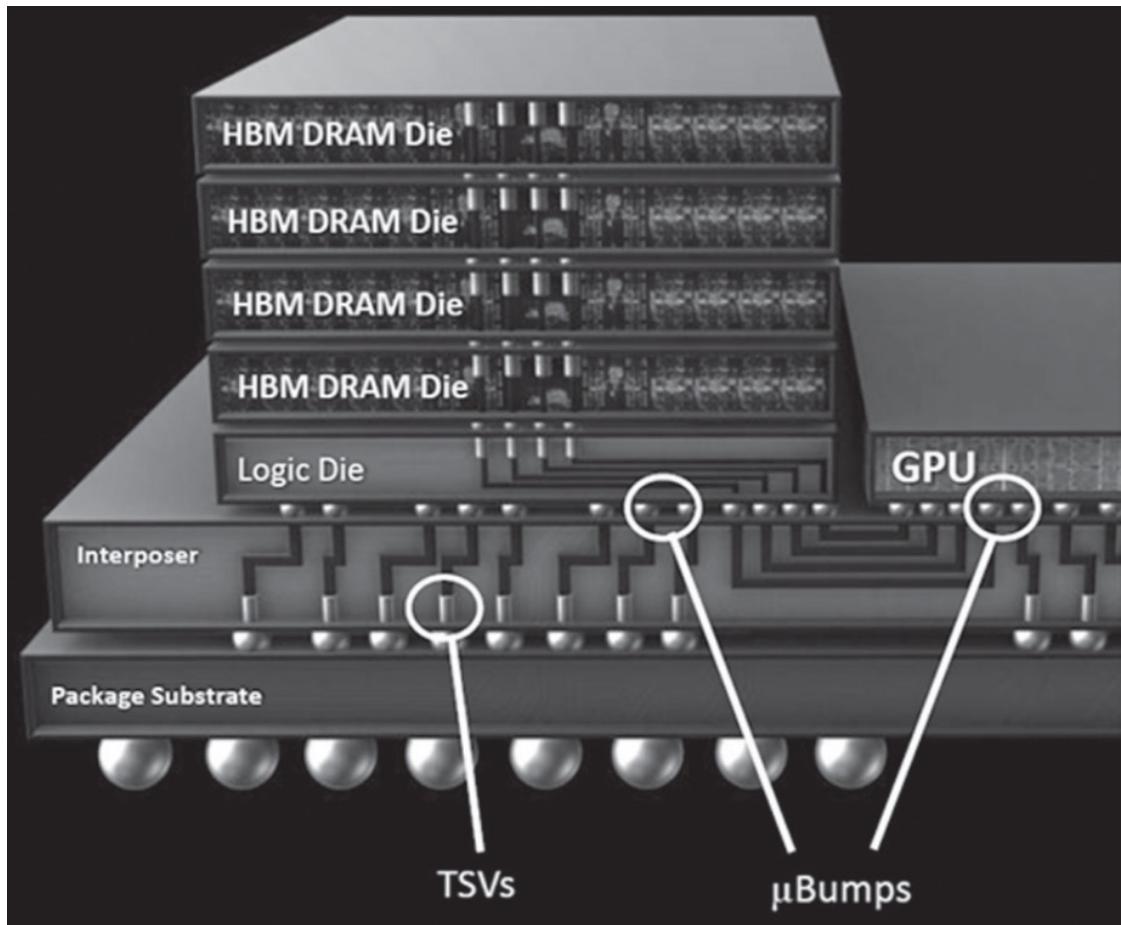
➤ Silicon substrate with complete back-end-of-line (BEOL) RDL and TSVs



Application of Silicon Interposer Substrates

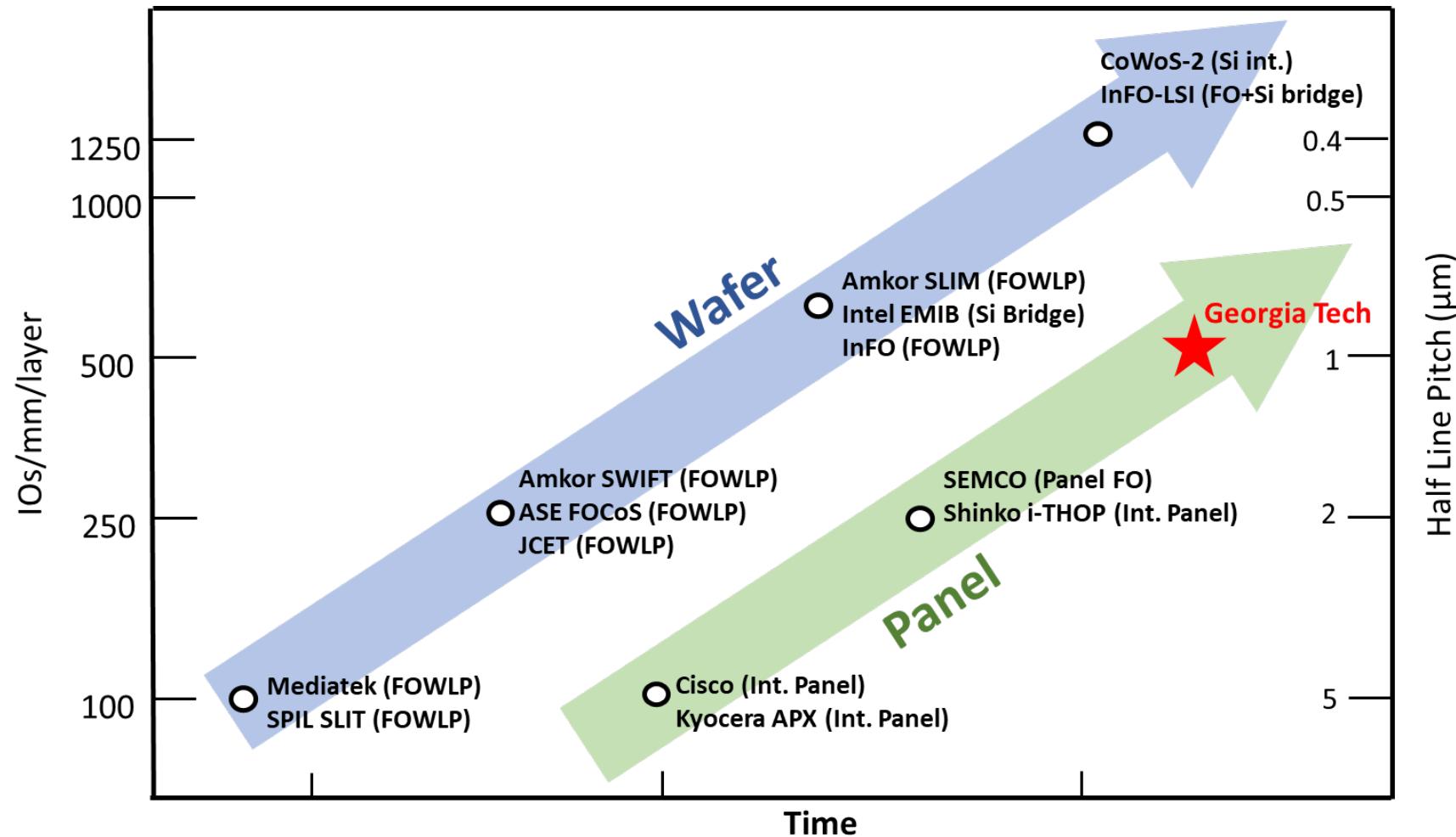
- Has enabled several die-to-die interconnect architectures
- First commercial use of silicon interposers was demonstrated by Xilinx in 2011 by breaking up a large FPGA die into four tiles (1st use of Chiplet concept)
- Heterogenous integration of logic (CPU, GPU) and high bandwidth memory (HBM) drove silicon interposers to high volume production (e.g. AMD Fury)

AMD's Radeon R9 Fury X GPU



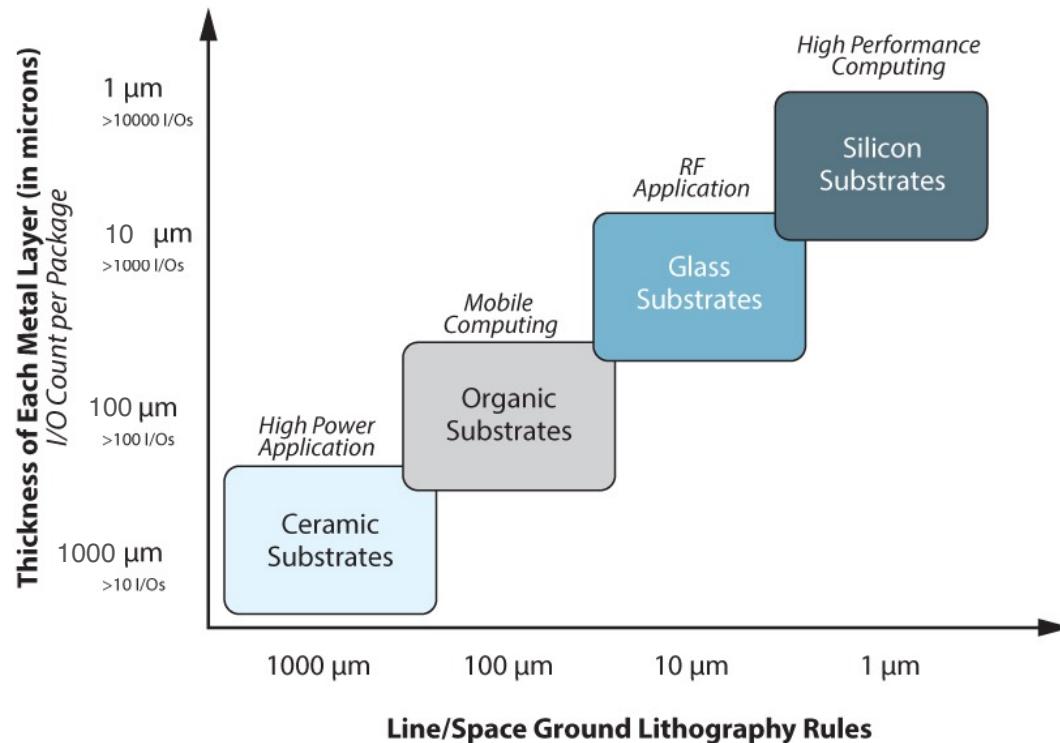
Summary of RDL Scaling on Substrates for Die-to-Die Interconnect

Bandwidth optimizes for RDL pitch (I/O per mm) and Bump Pitch (I/O per mm²)

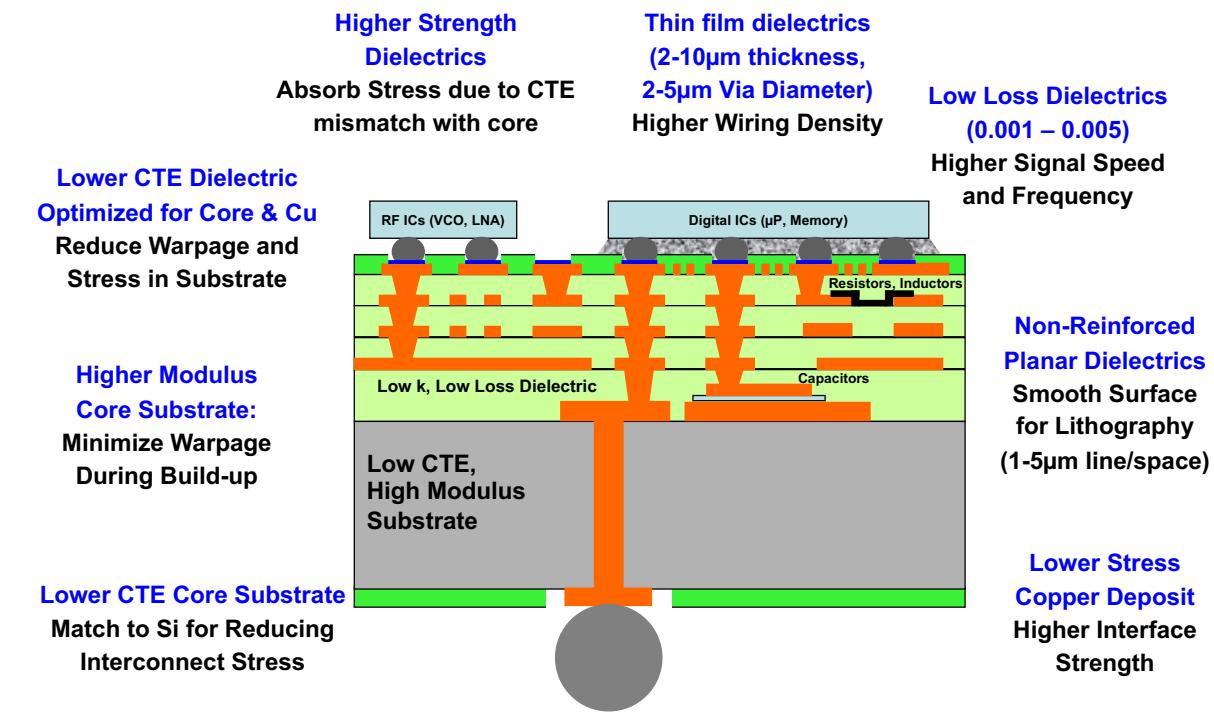


SUMMARY

Current Ceramic, Organic, Glass & Silicon Substrates



Future Needs for Package Substrates



And Lower Cost per mm² for Ultra-Large Package Sizes

Open for Q&A