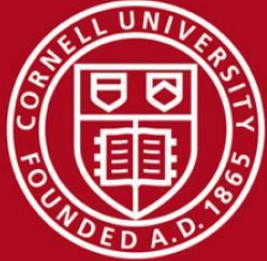


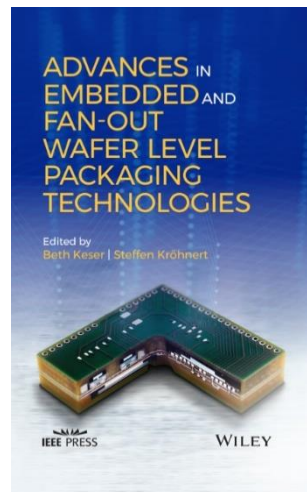
Fundamentals of Embedded and Fan-Out Packaging

Beth Keser, Ph.D.

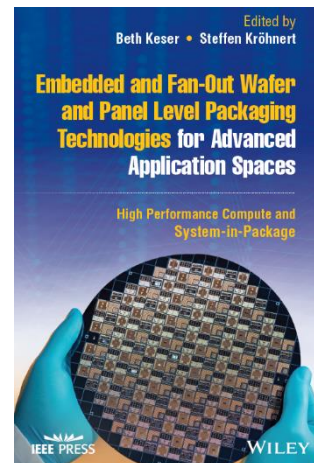
- **BETH KESER, Ph.D.**, a recognized global leader in the semiconductor packaging industry with over 27 years of experience, received her B.S. degree in Materials Science and Engineering from Cornell University and her Ph.D. from the University of Illinois at Urbana-Champaign.
- Beth has developed packaging technology at Motorola, Freescale (NXP), Qualcomm, & Intel.
- Beth's excellence in developing revolutionary electronic packages for semiconductor devices has resulted in 49 patents and patents pending and over 50 publications in the semiconductor industry.
- Beth is an IEEE Fellow & IEEE EPS Distinguished Lecturer
- Beth is currently the Past President of the International Microelectronics Assembly and Packaging Society (IMAPS), North America.



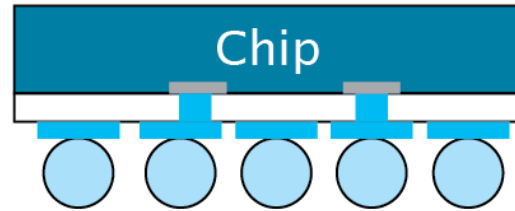
Published Feb 2019



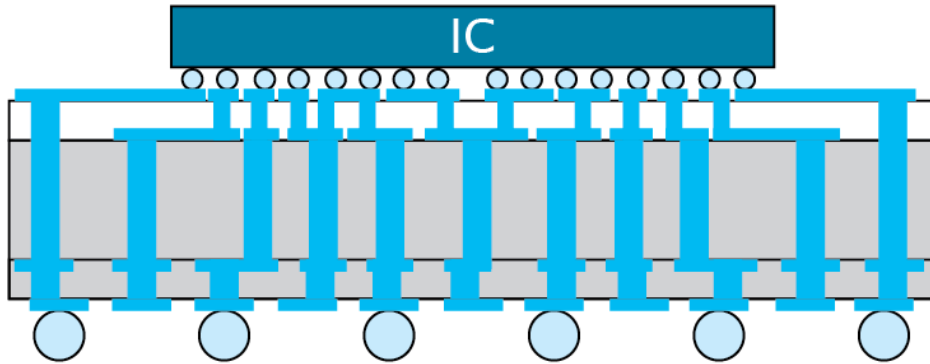
Published Dec 2021



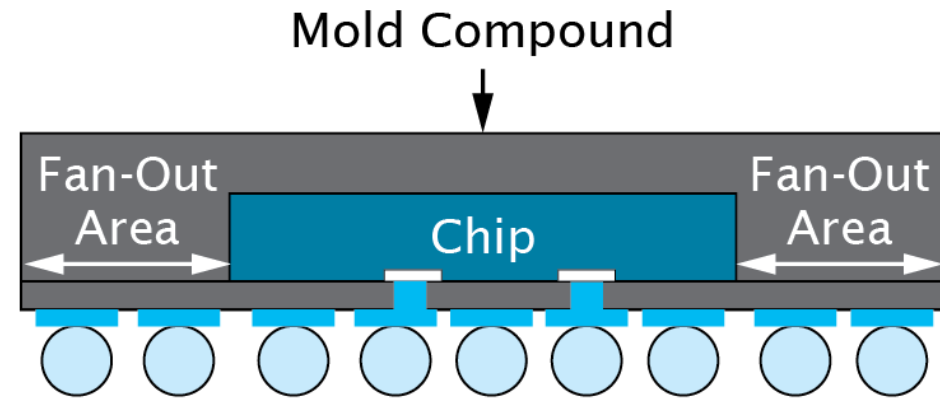
Wafer Level Package

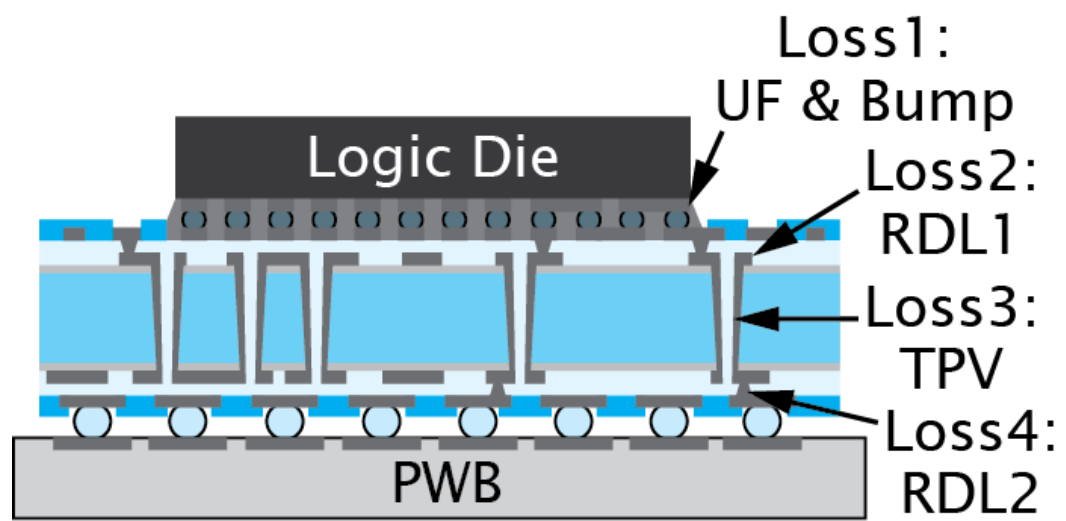


Fan-Out Package

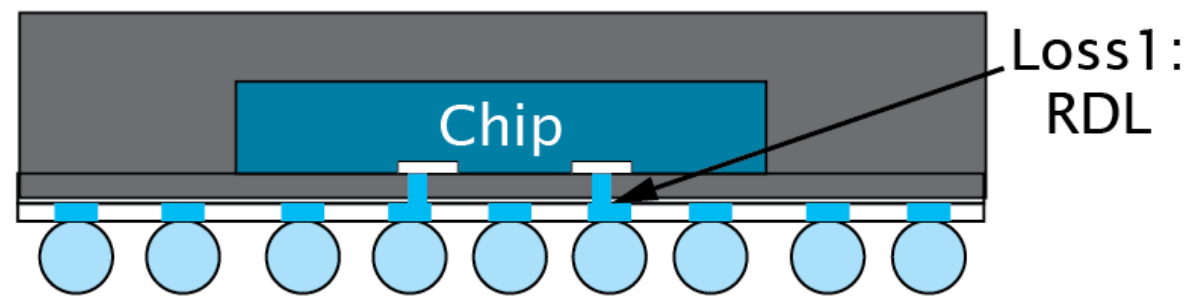


Embedded and Fan-Out Package

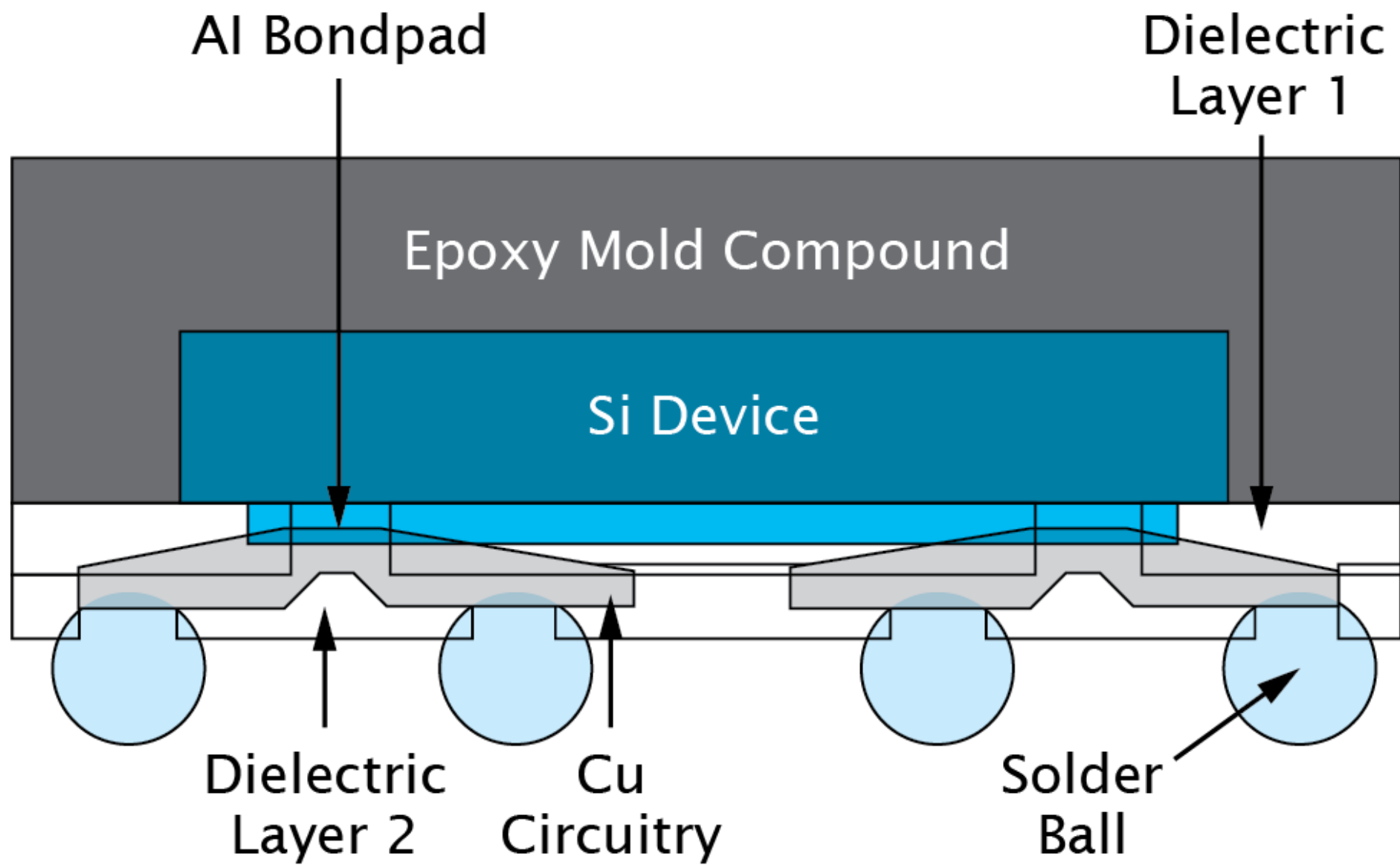




(a)

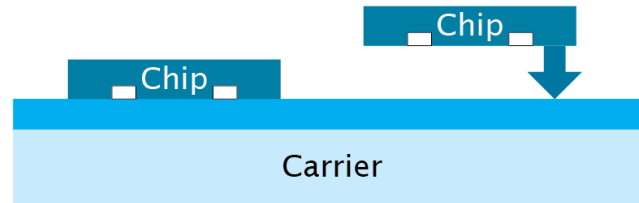


(b)

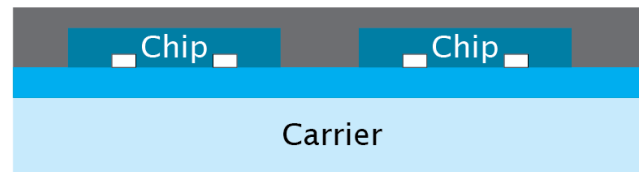




Adhesive Tape



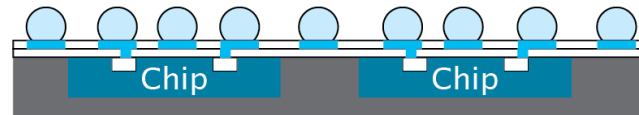
Placement of Dies on
the Tape Carrier



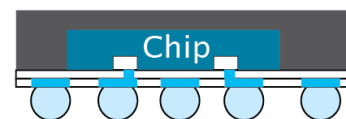
Mold Compound



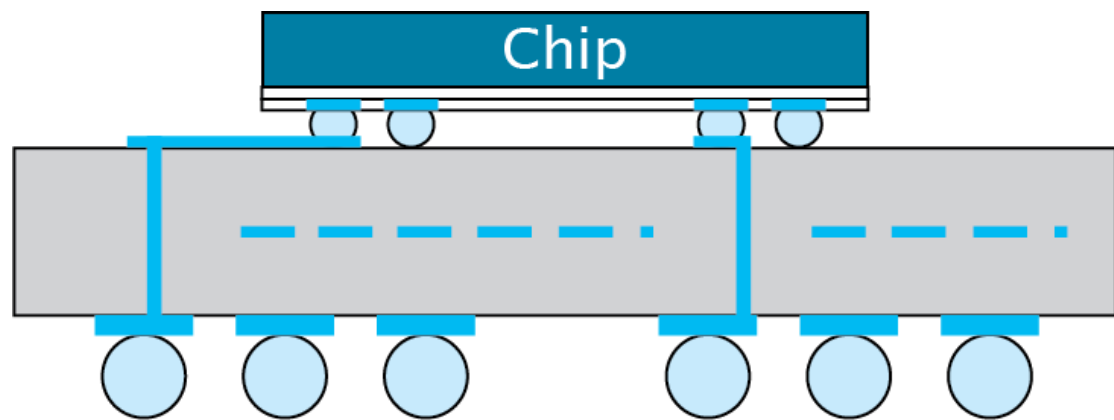
Carrier and Tape
Removal



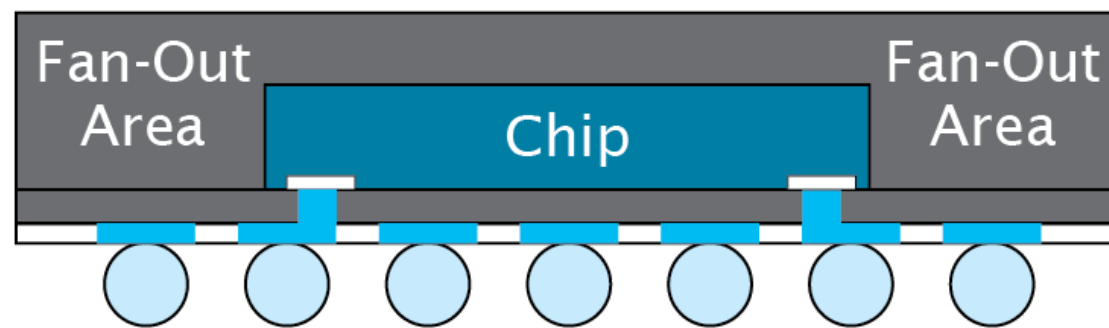
Flip and RDL
Formation



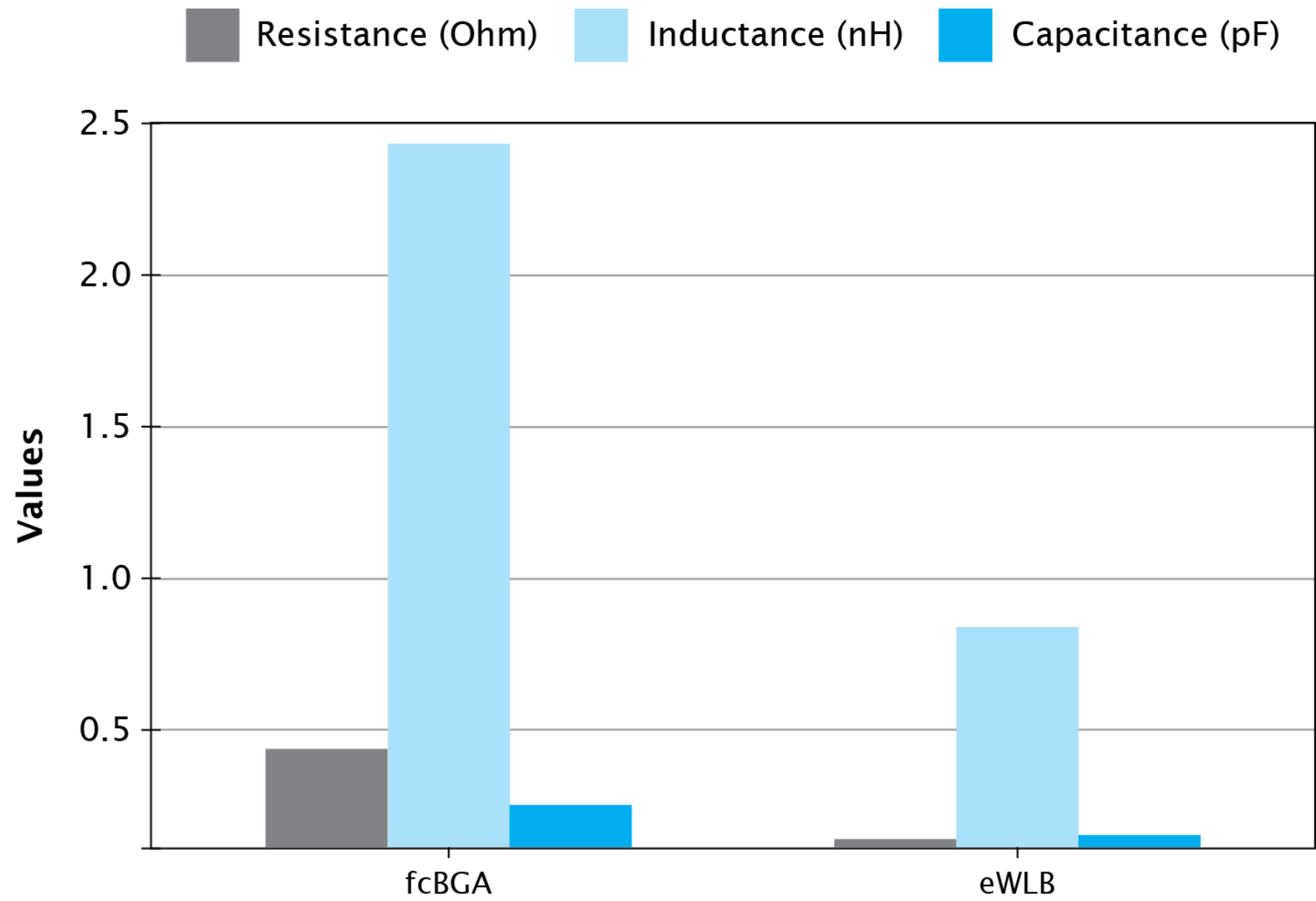
Package Singulation



(a)



(b)



Embedded Wafer Fan-Out

```
graph TD; A[Embedded Wafer Fan-Out] --> B[Direction of the Device]; A --> C[RDL Cu Circuitry]; B --> D[Face-Up]; B --> E[Face-Down]; C --> F[Chip First]; C --> G[Chip Last];
```

Direction of the Device

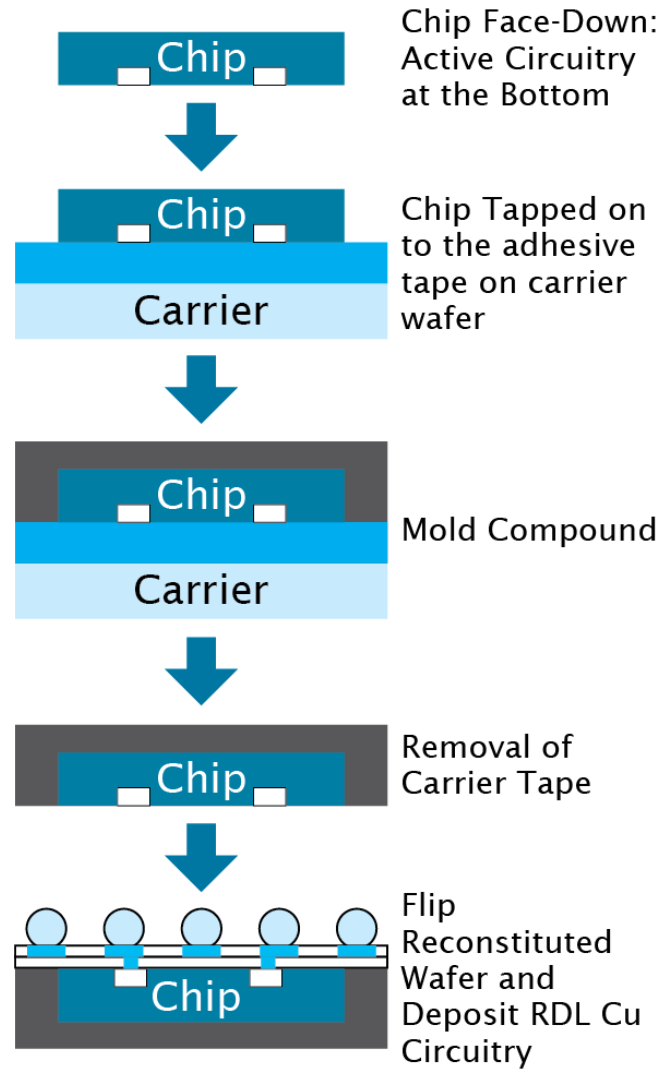
Face-Up

Face-Down

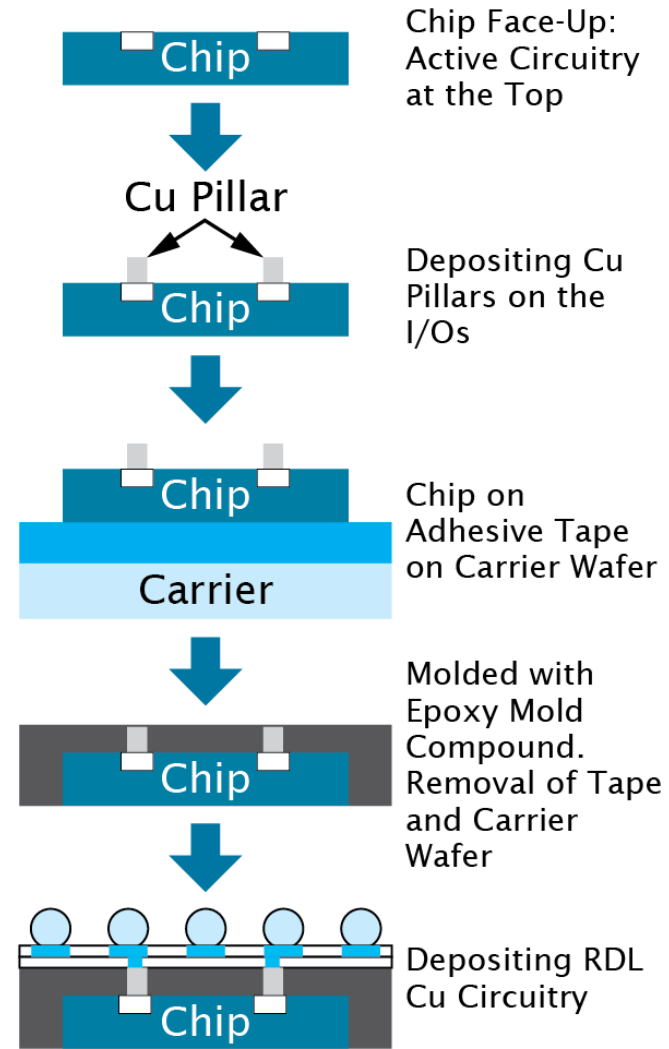
RDL Cu Circuitry

Chip First

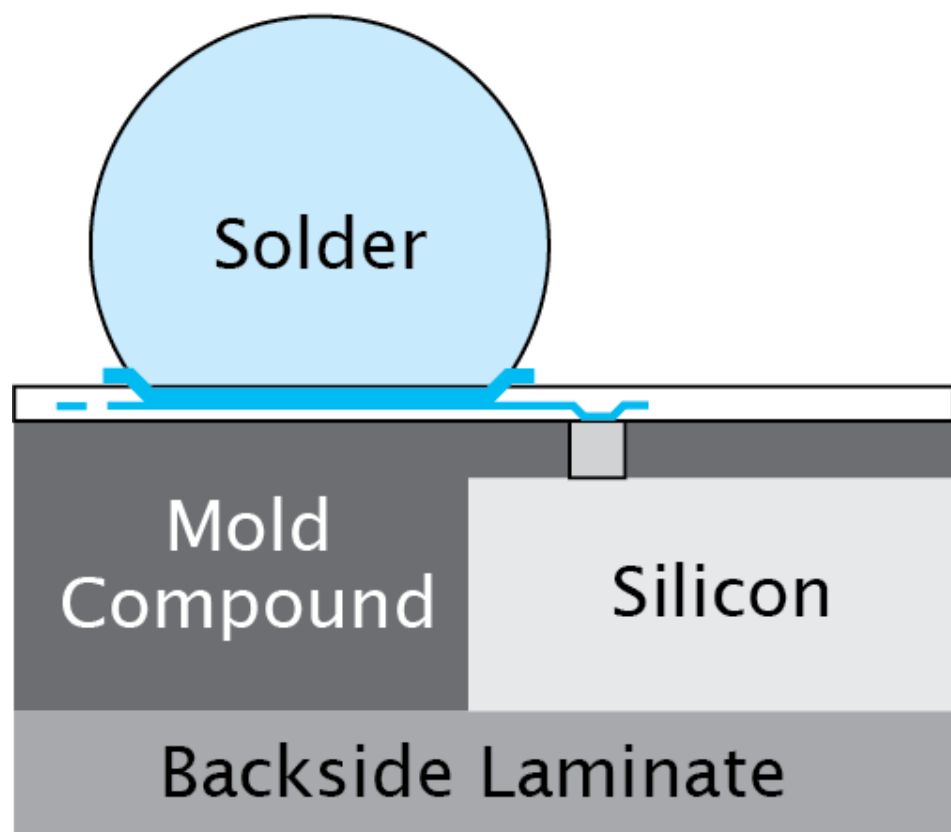
Chip Last



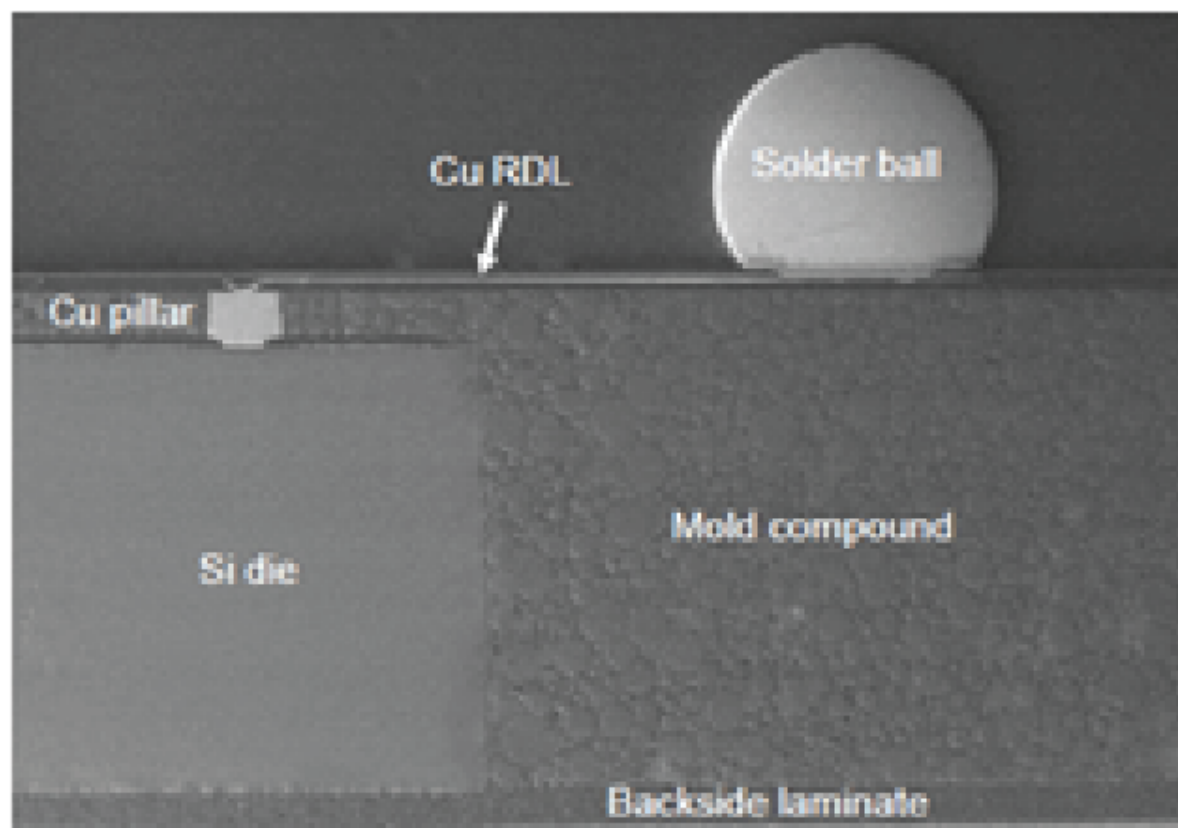
(a)



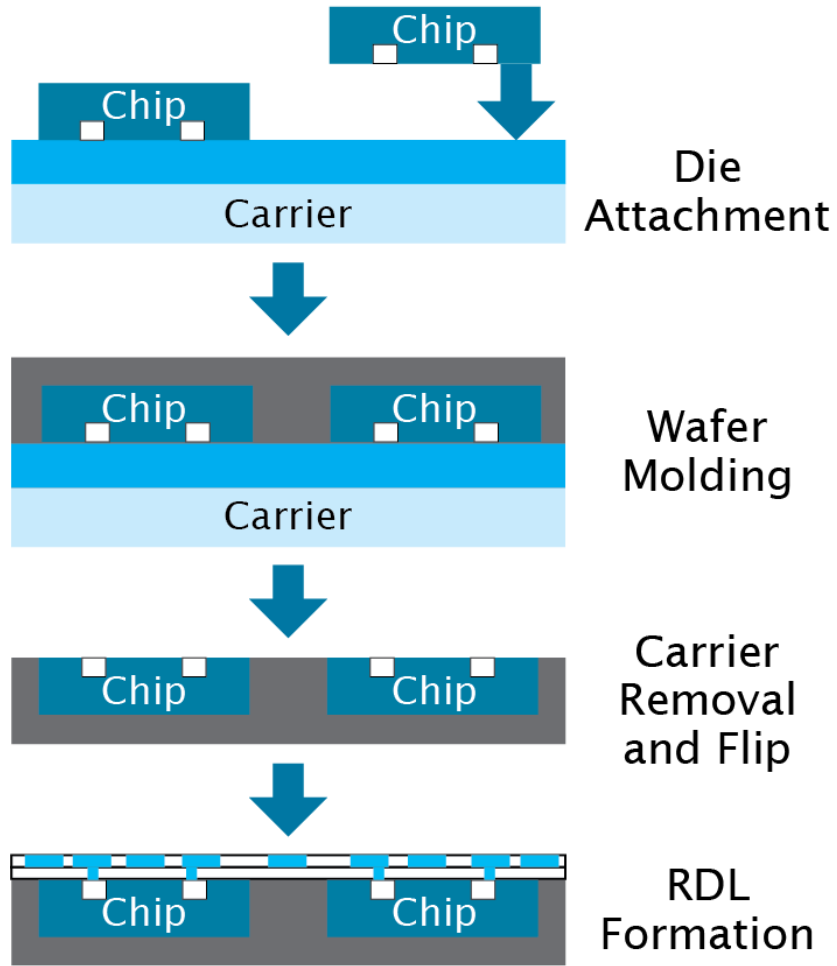
(b)



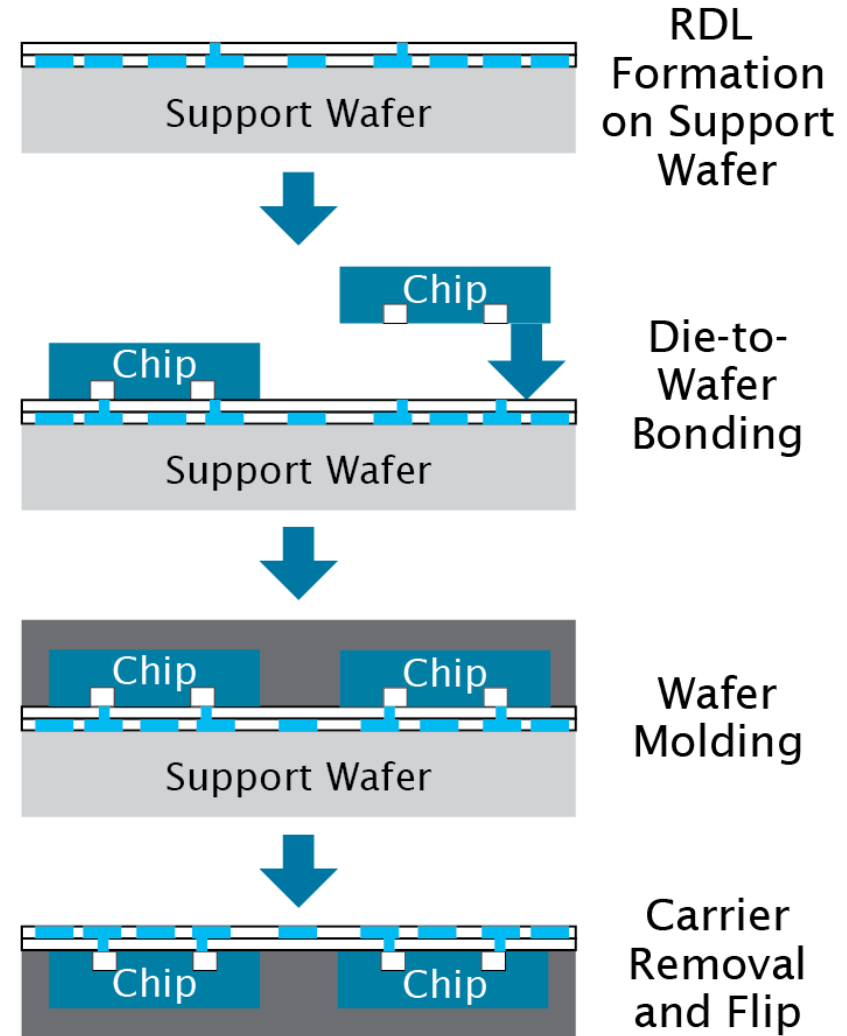
(a)



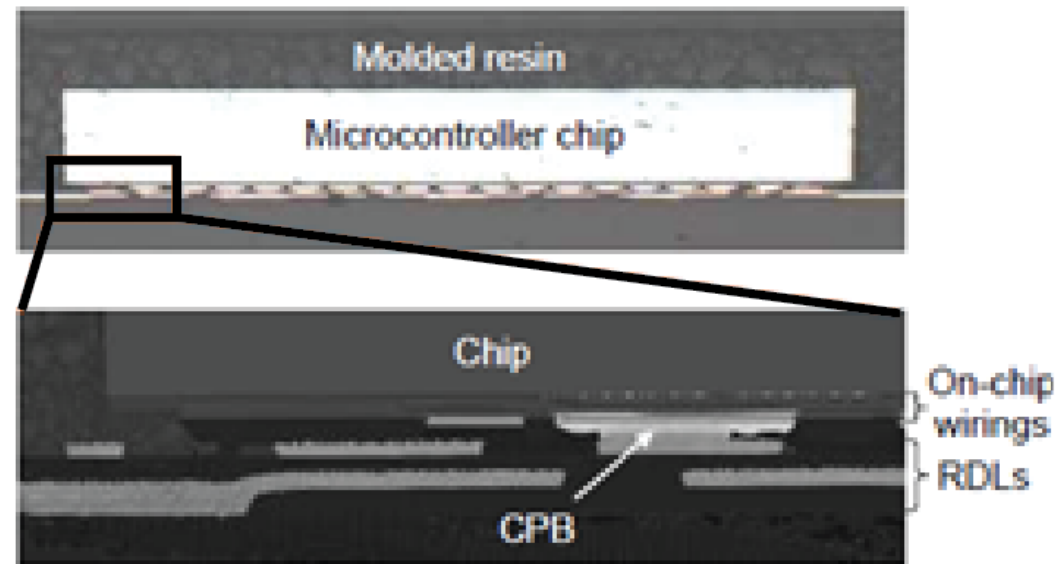
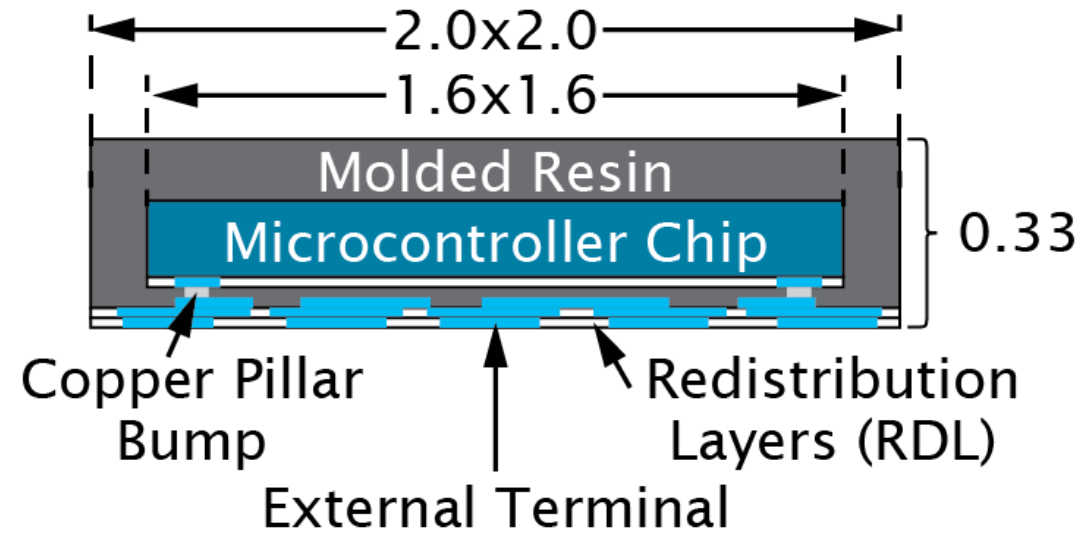
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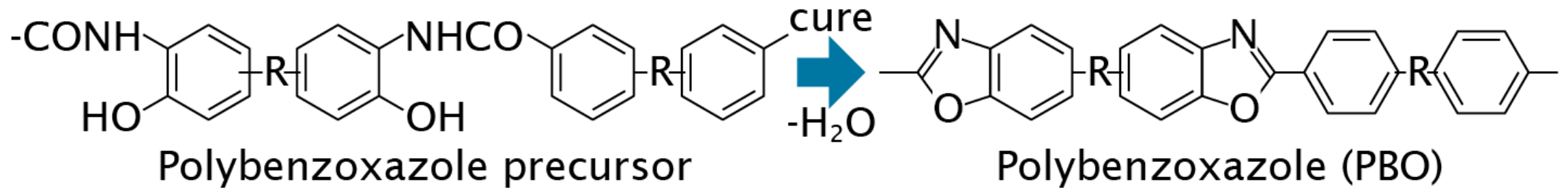
(a)



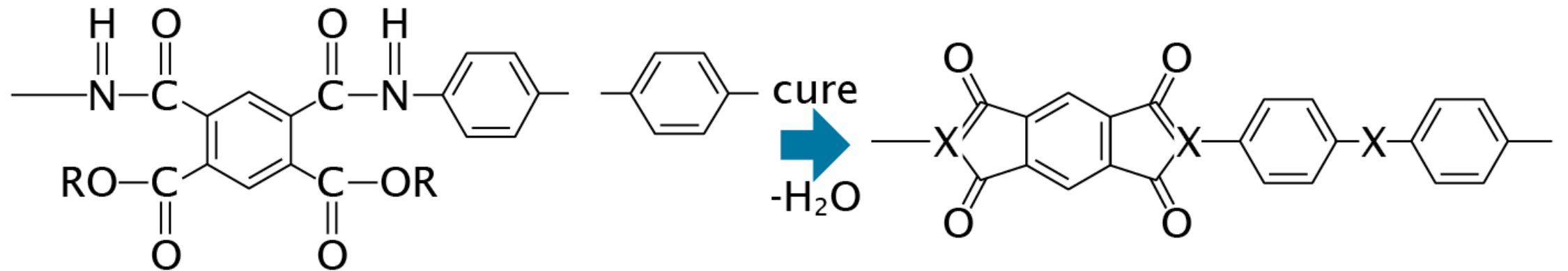
(b)

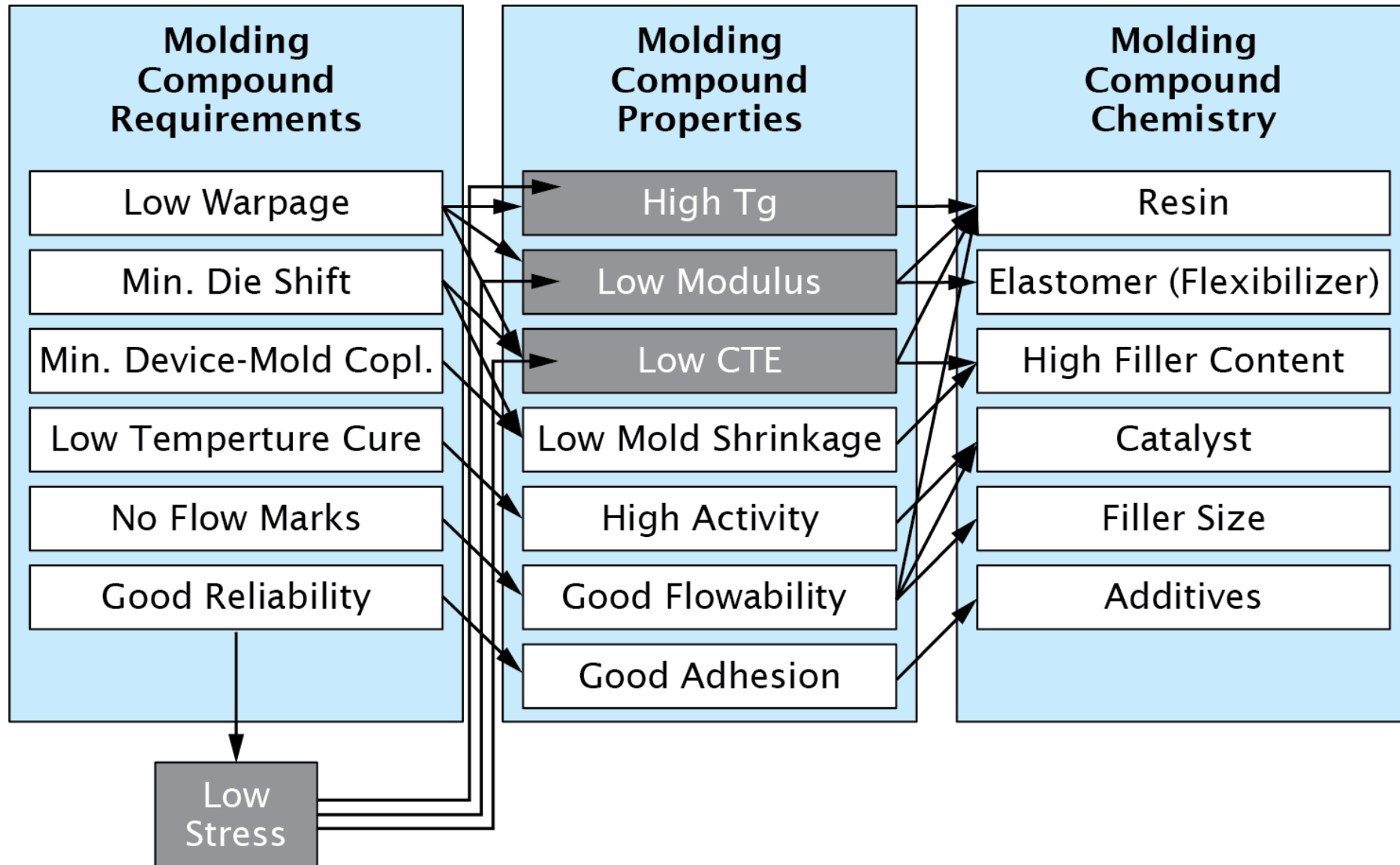


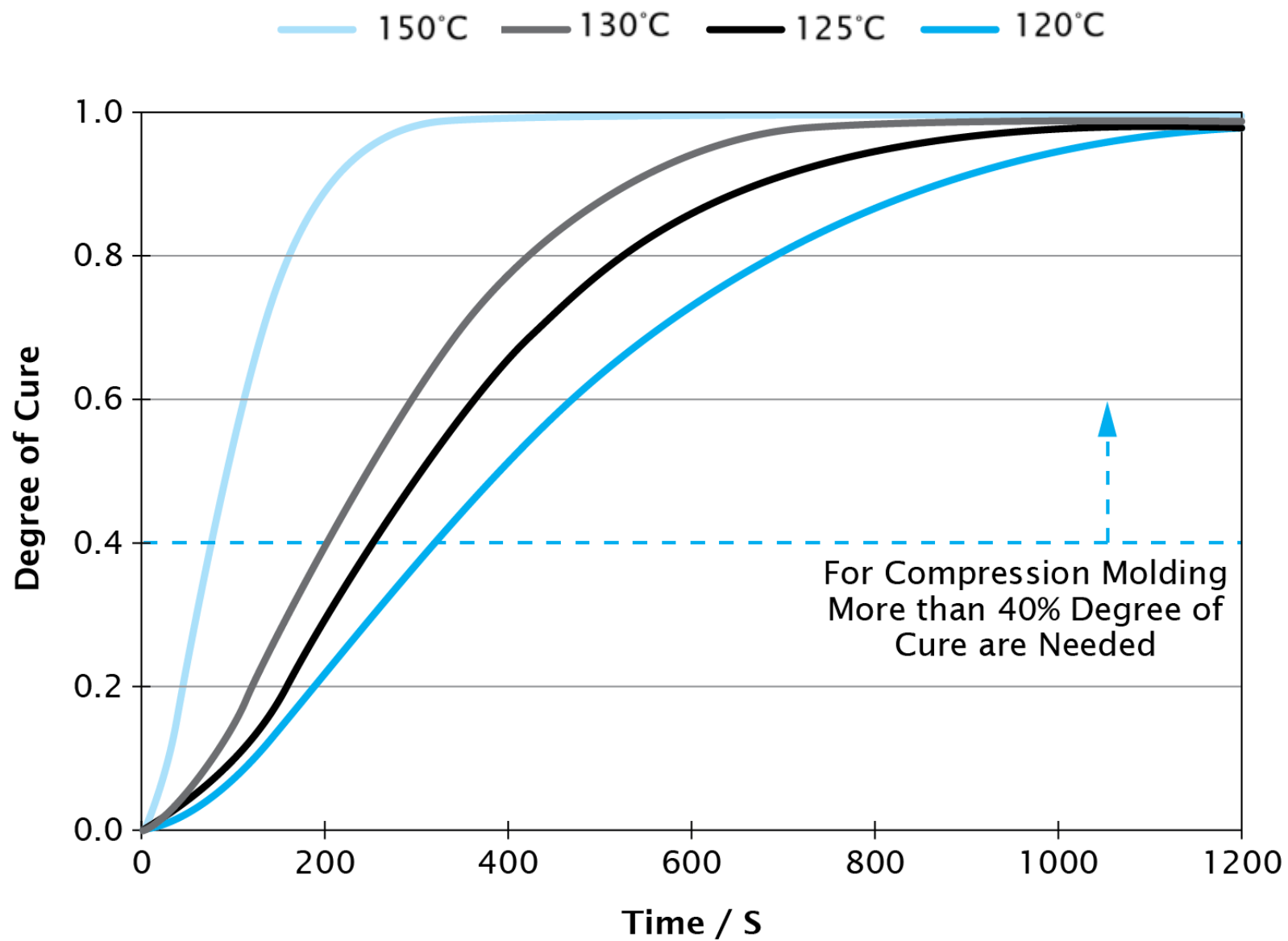
Typical Photosensitive PBO



Typical Photosensitive Polyimide







*Note figure in book is labeled incorrectly. Correct labels above.

eWFO Tools

```
graph TD; A[eWFO Tools] --> B[Device]; A --> C[Mold]; A --> D[RDL]; B --> E[• Pick-and-Place]; C --> F[• Compression Mold]; D --> G[• Lithography]; D --> H[• Physical Vapor Deposition];
```

Device

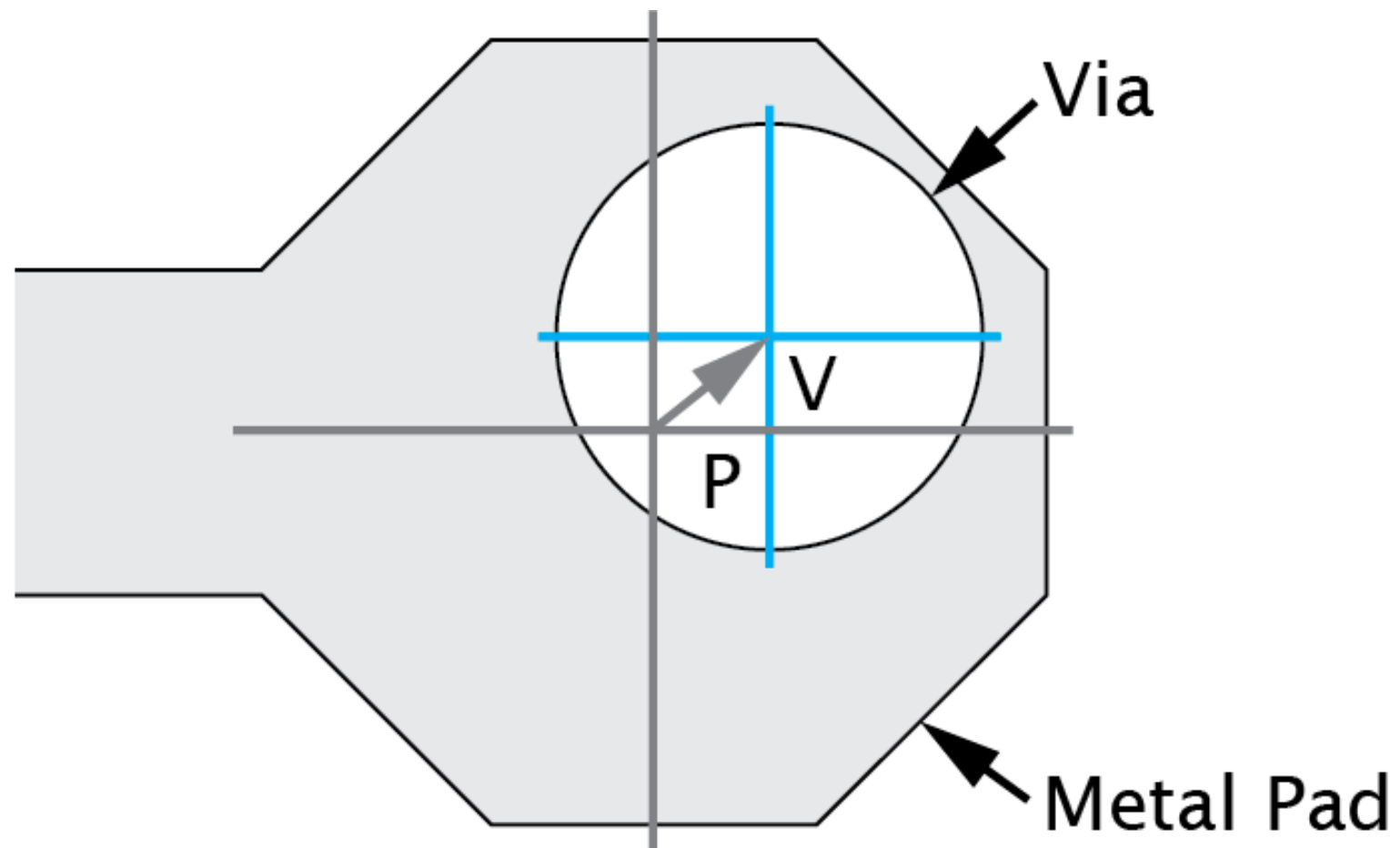
- Pick-and-Place

Mold

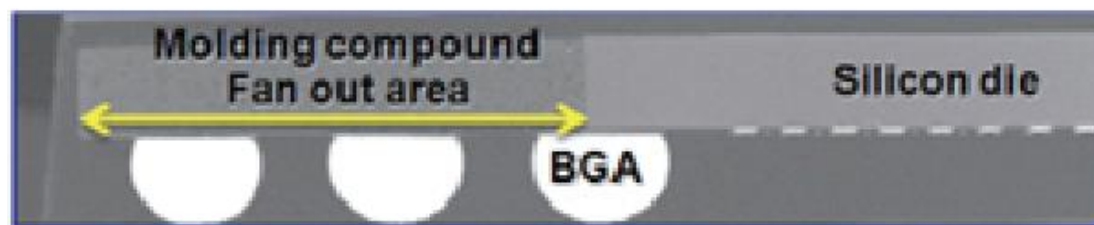
- Compression Mold

RDL

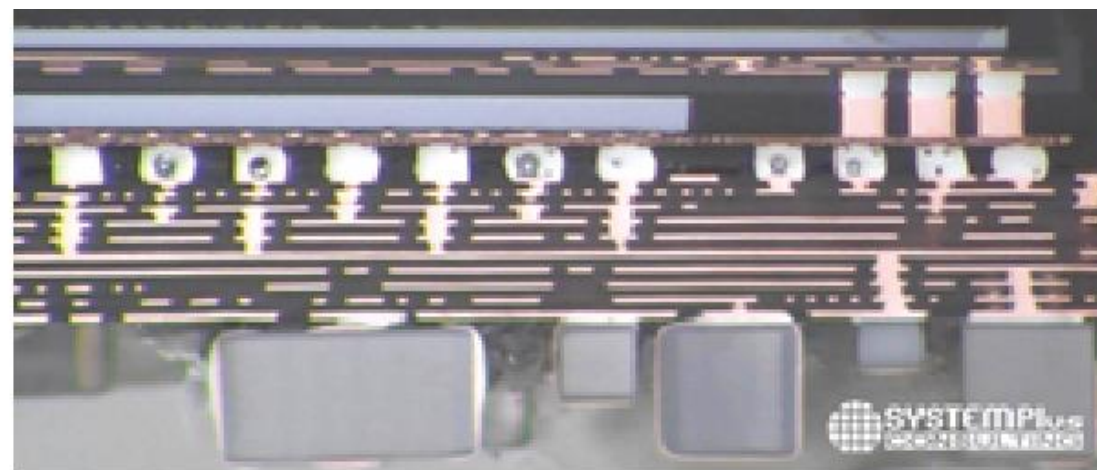
- Lithography
- Physical Vapor Deposition



P = Pad Center
V = Via Center



(a)

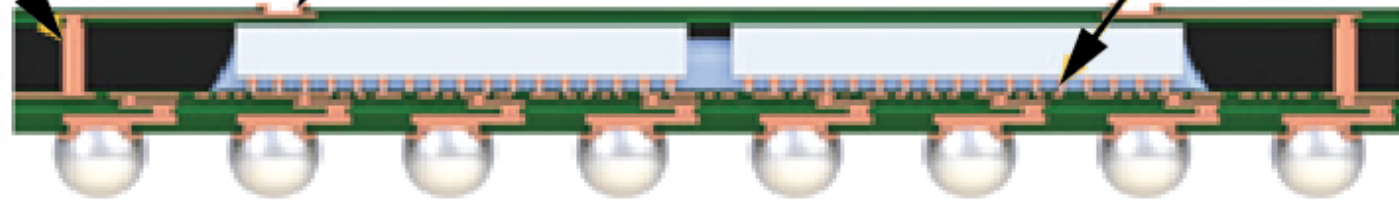


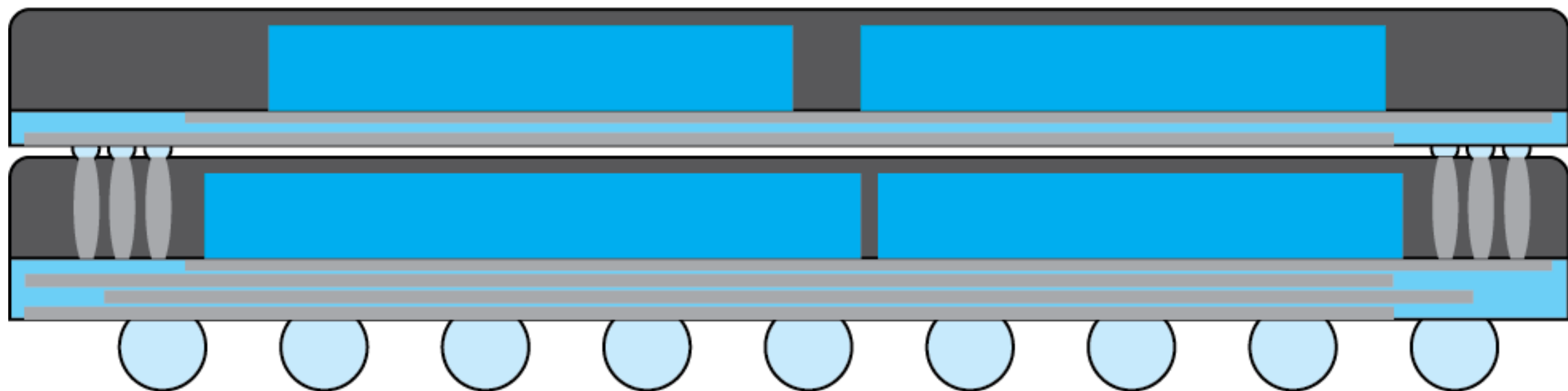
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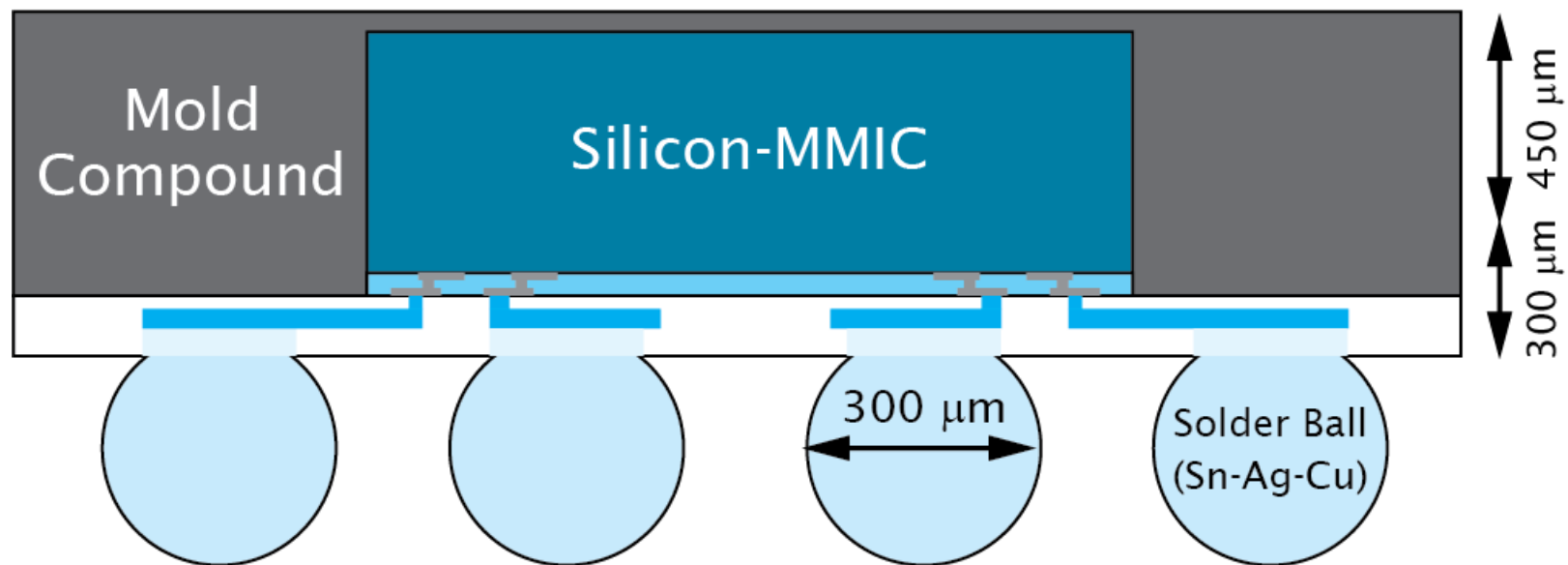
Fine Pitch Vertical
Interconnect

Fan-in RDL for
PoP Interface

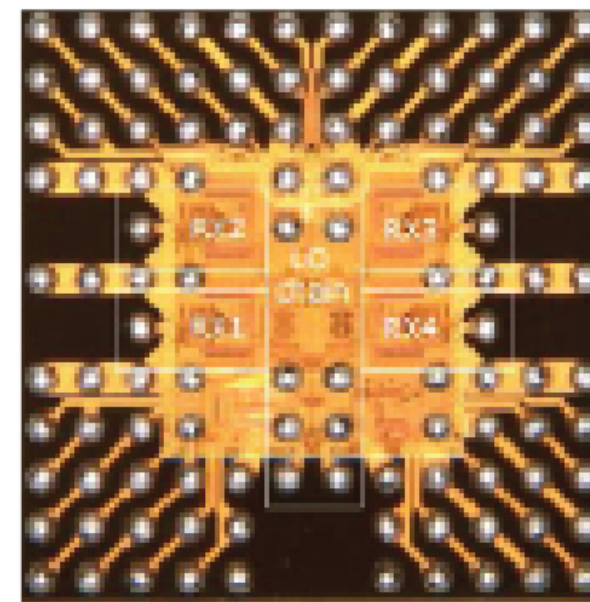
Microbumps for
Die Interconnect



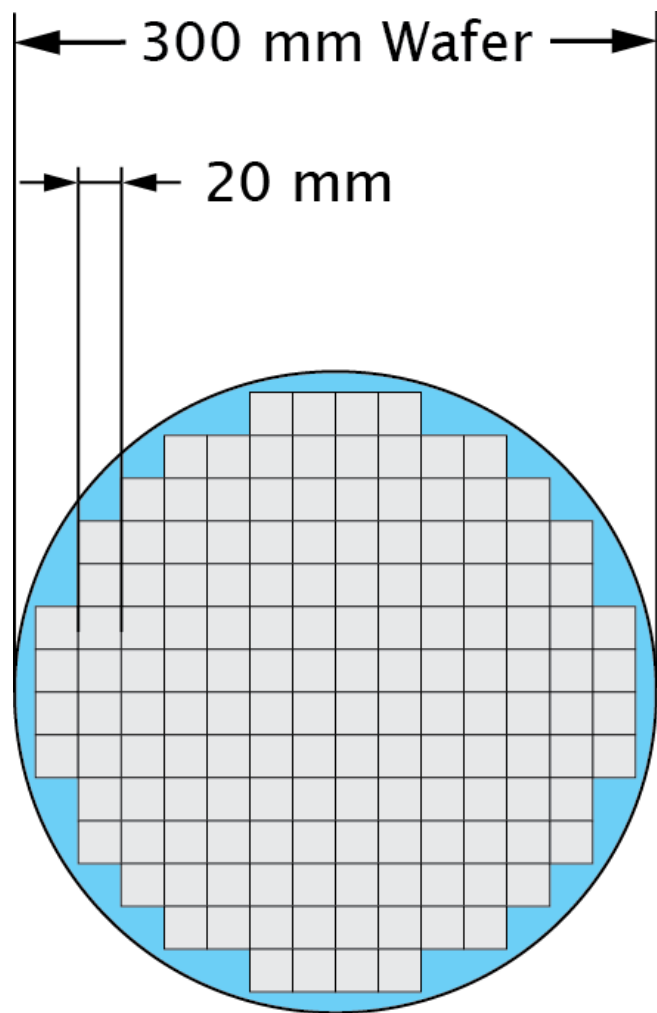




(a)

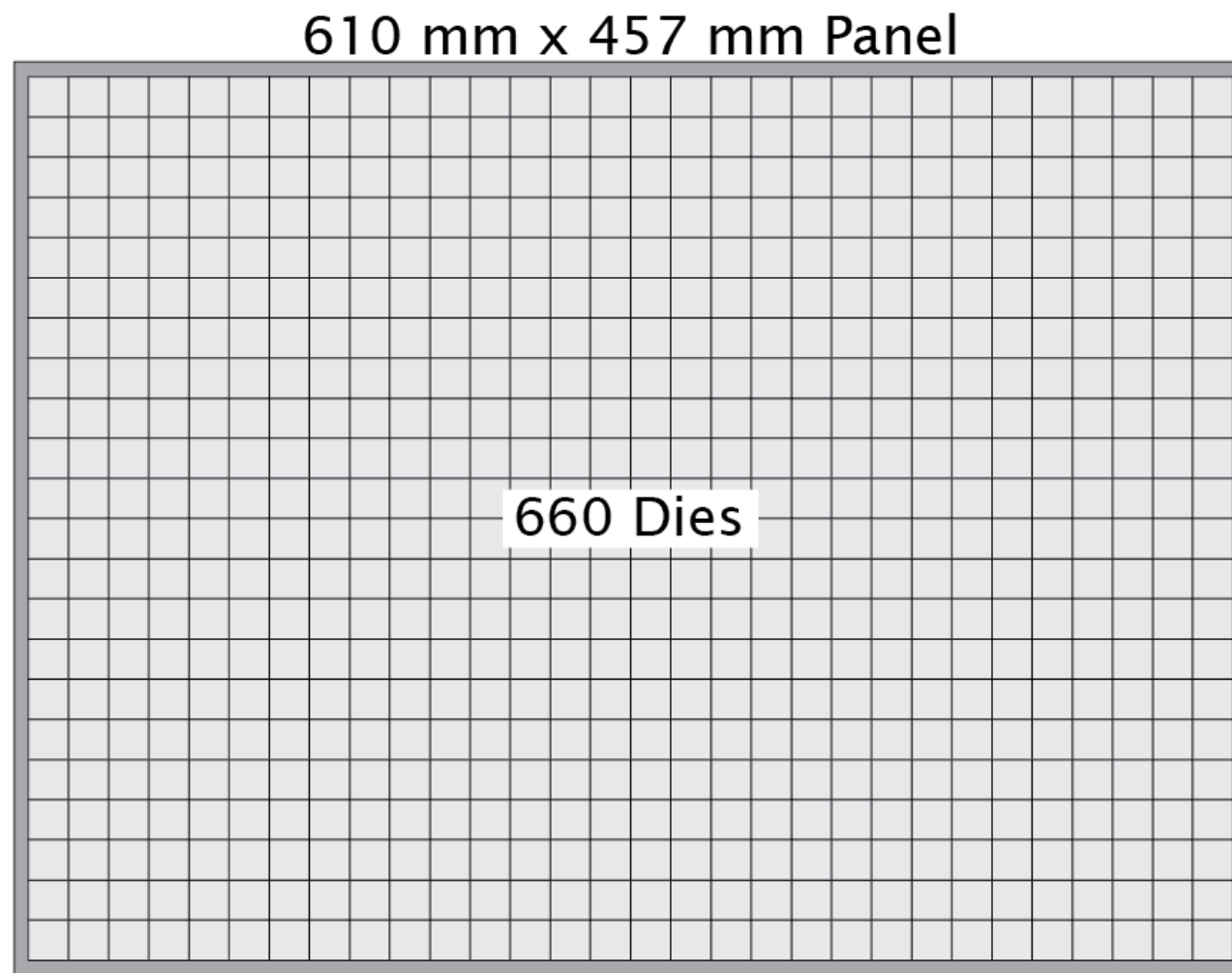


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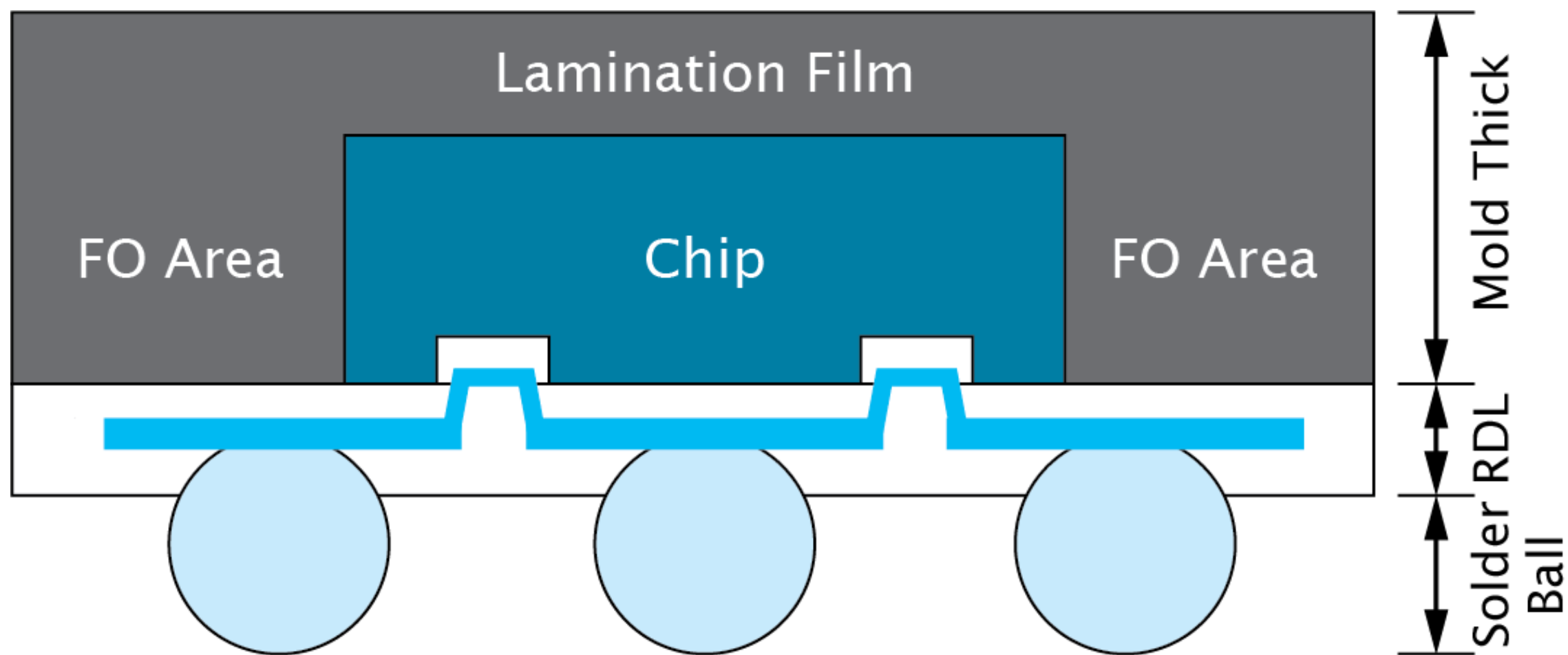


(a)

> 4x



(b)



ePFO

```
graph TD; ePFO[ePFO] --> PWD[PWD-Based]; ePFO --> LCD[LCD-Based]; ePFO --> OSAT[Build-Up OSAT]; PWD --> PWD_List["• Imbera's IMB<br>• AT&S's ECF<br>• ASE's a-EASI<br>• Fraunhofer IZM"]; LCD --> LCD_List["• SPIL's P-FO<br>• PTI's Panel-Scale<br>• Samsung's PLP"]; OSAT --> OSAT_List["• Amkor/J-Devices' WFOP<br>• ASE's Chip-Last<br>• TDK"];
```

PWD-Based

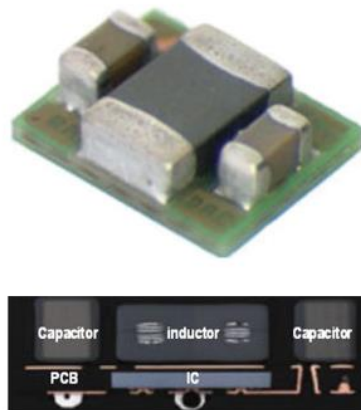
- Imbera's IMB
- AT&S's ECF
- ASE's a-EASI
- Fraunhofer IZM

LCD-Based

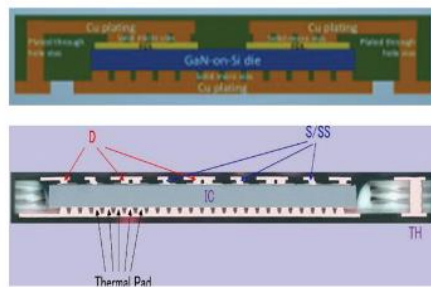
- SPIL's P-FO
- PTI's Panel-Scale
- Samsung's PLP

Build-Up OSAT

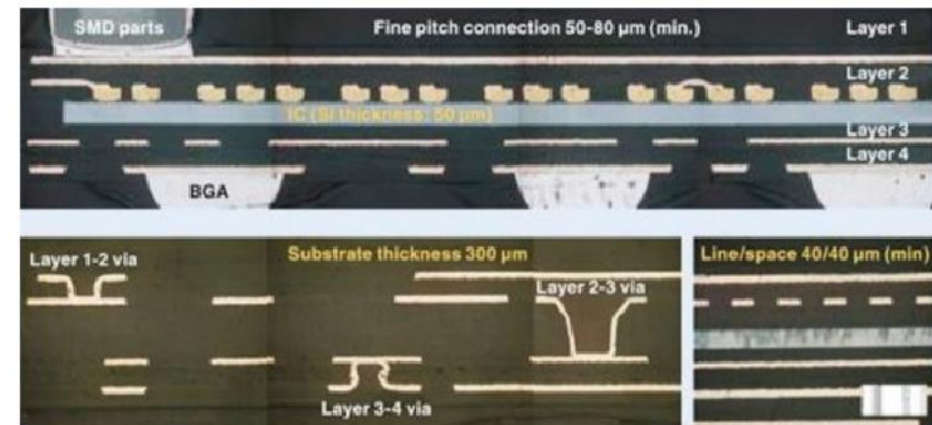
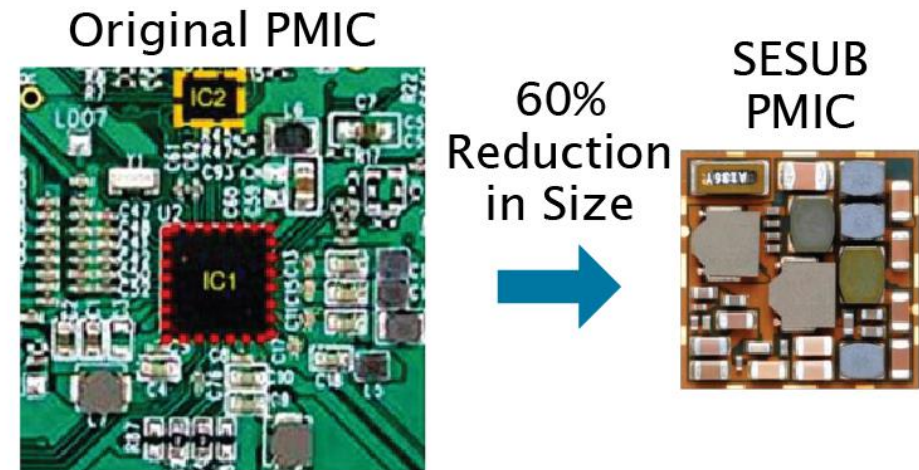
- Amkor/J-Devices' WFOP
- ASE's Chip-Last
- TDK



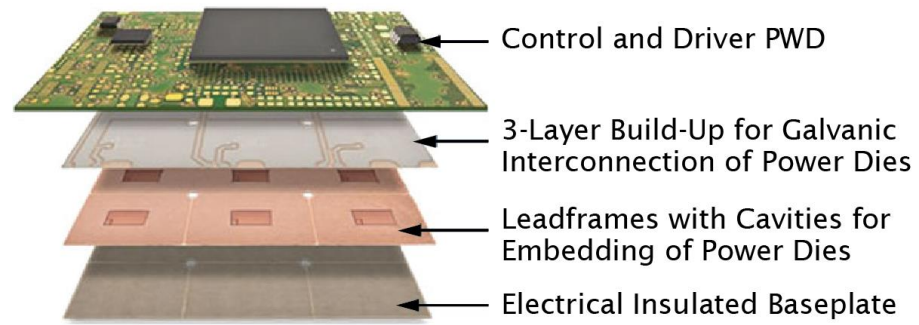
(a)



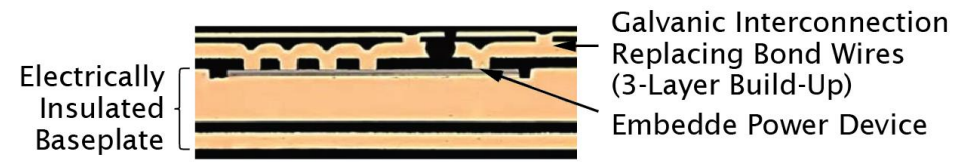
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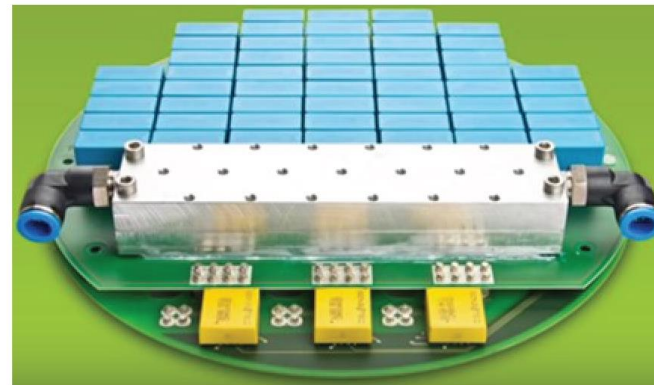
(c)



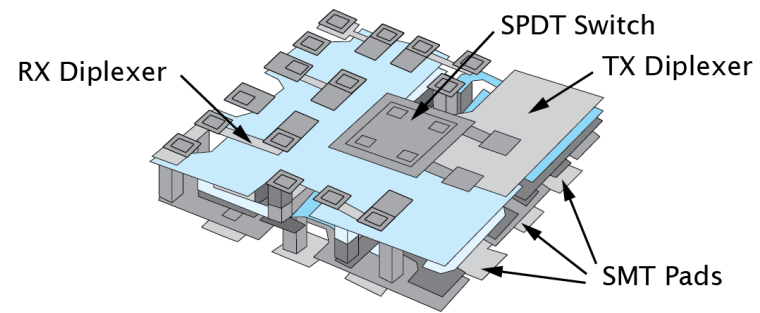
(a)



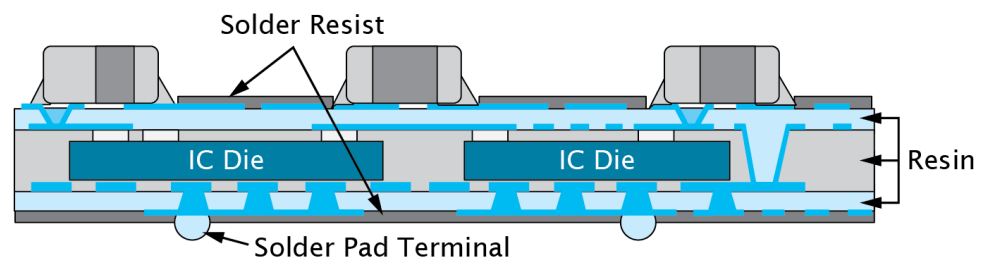
(b)



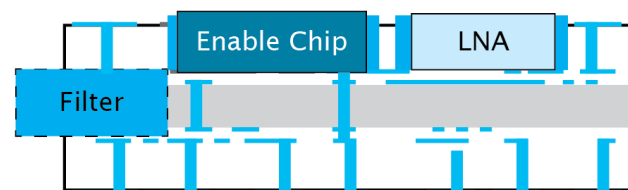
(c)



(a)

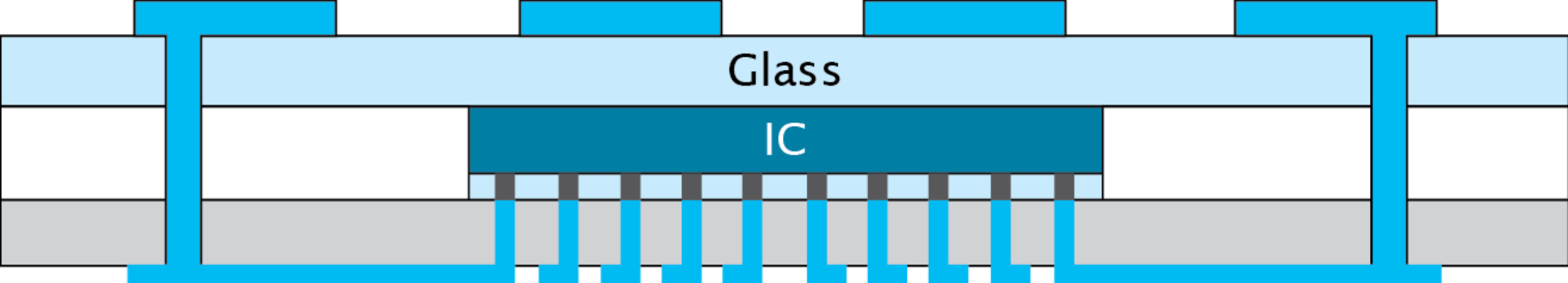








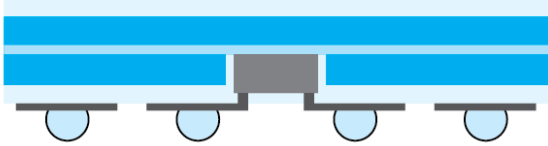
(b)

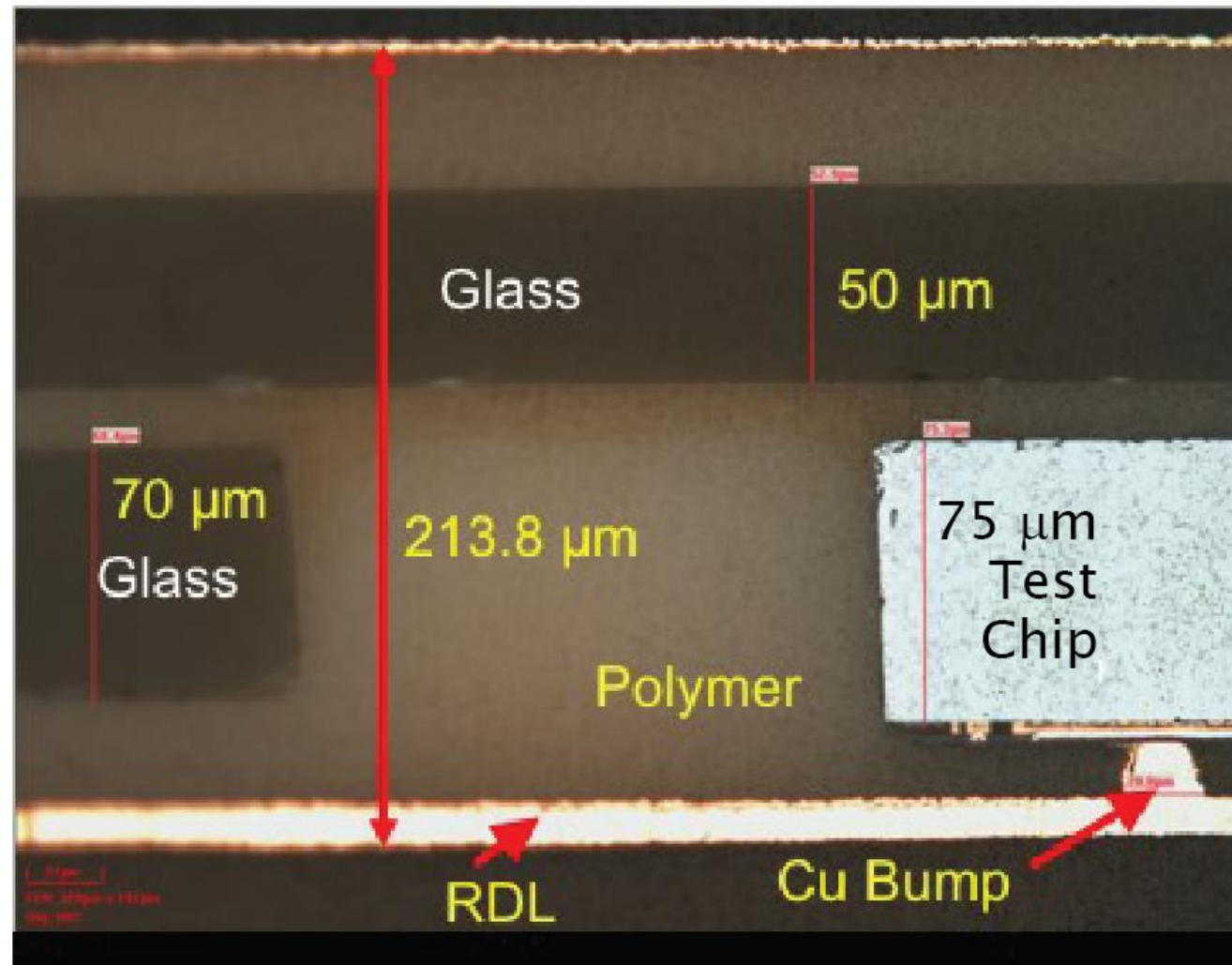


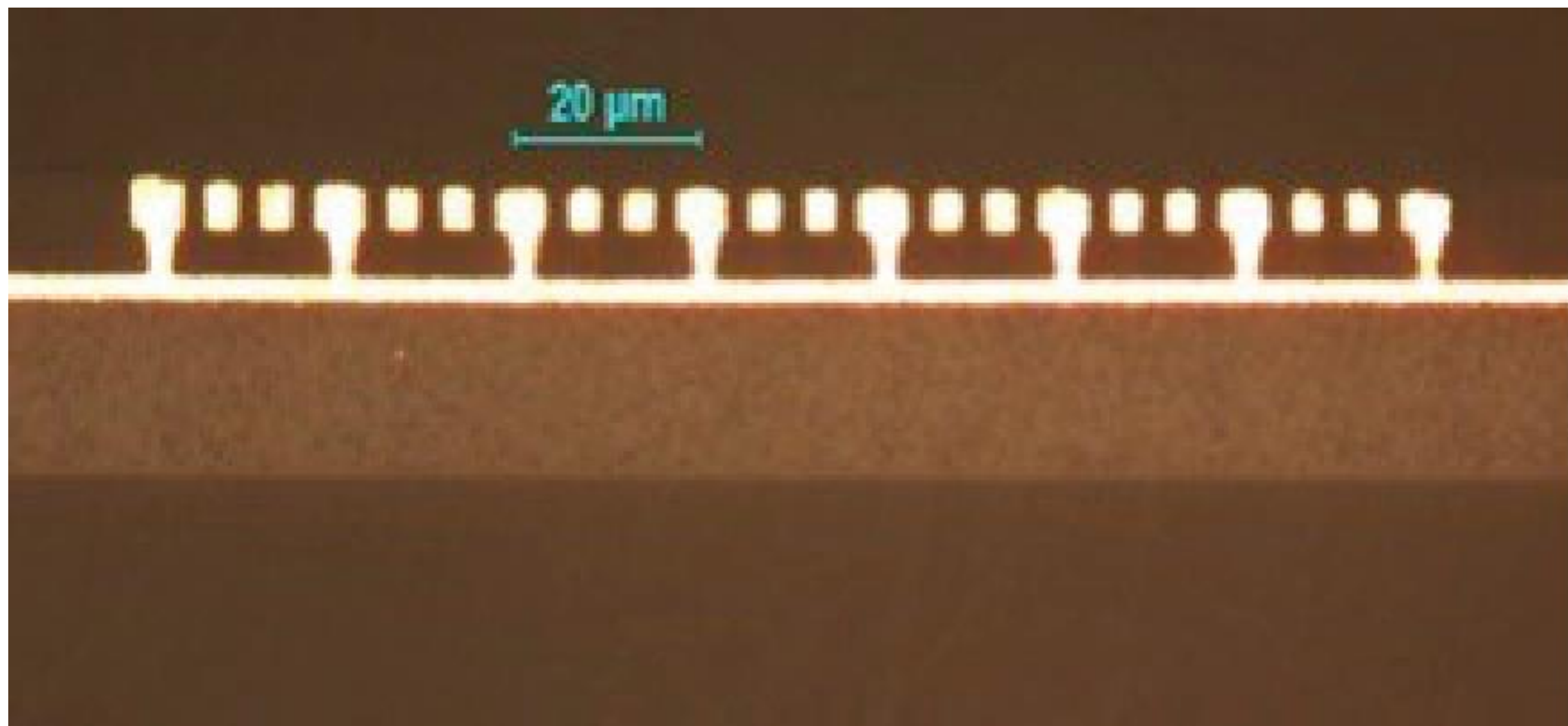
RFIC

(c)



Process Flow	Schematic
Cavity Formation	
Bonding	
Die Placement	
RDL Lamination and Curing	
Planarization	
RDL Process	
Board-Level Assembly	





Relative Wafer, Panel, PWD and LCD Size
(mm)

