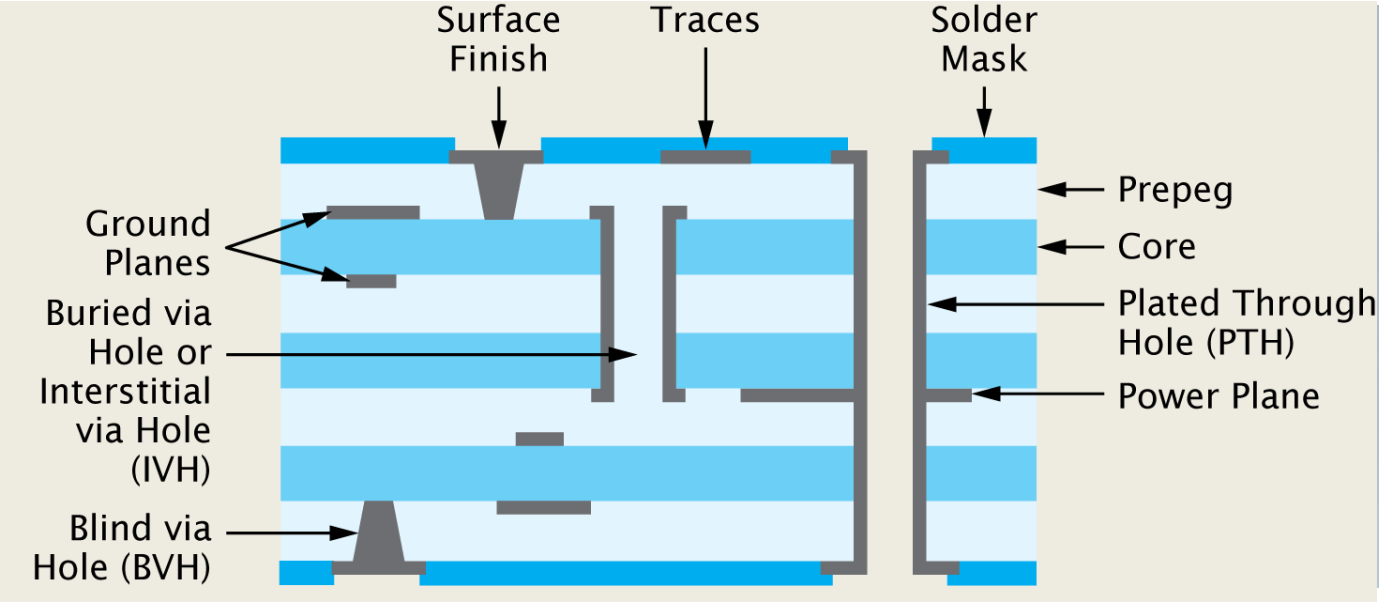
Sanmina

Module 15

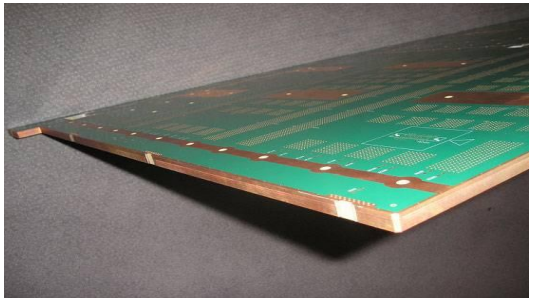
Fundamentals of Printed Wiring Board

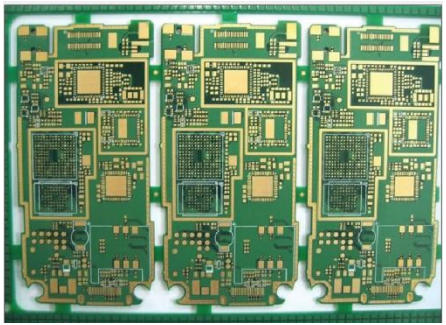
Steve Iketani



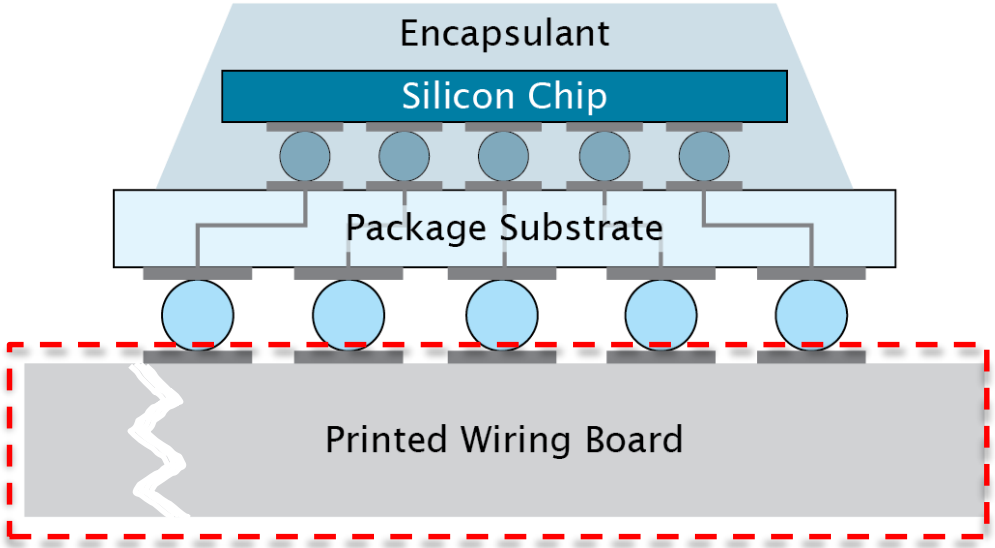
Agenda

- Printed Wiring Board Types
- Wireability / Routing Escapes
- PWB Laminate Material Properties
  - Electrical
  - Mechanical
- Basic Multilayer PWB Fab Process - step by step
- PWB Reliability
- Future Markets





System Level PWB (PCB)



- Composite of organic and inorganic materials with external and internal wiring
- Allows electronic components to be mechanically mounted and electrically interconnected.
- Must provide power to the components and conduct away heat.
- Known as system level boards because they carry all of the components required for that system or subsystem

PWB Types

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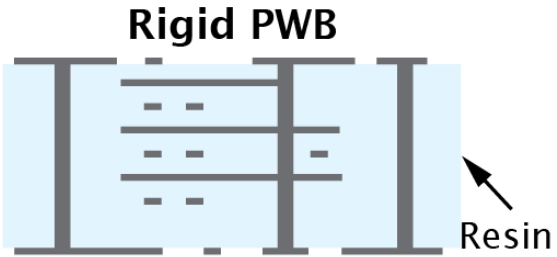
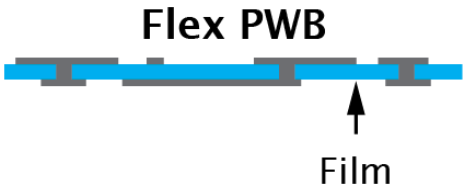
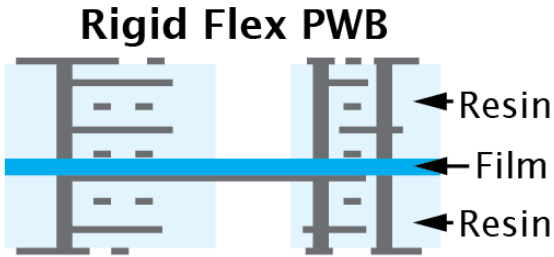




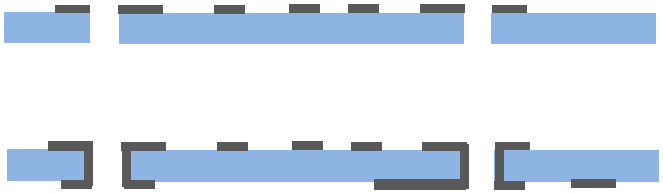


Rigid PWB:
consists of reinforcing material (like glass fiber), resin (like epoxy, BT, polyimide, or PTFE) and copper foil (ED - electrodeposited) with surface roughness for adhesion

Flex PWB:
Flexible (bendable) film with smooth copper foil for fine conductor traces; film resin can be PET for low cost, or, thermoplastic polyimide for higher reliability applications such as medical, aerospace, automotive, etc.

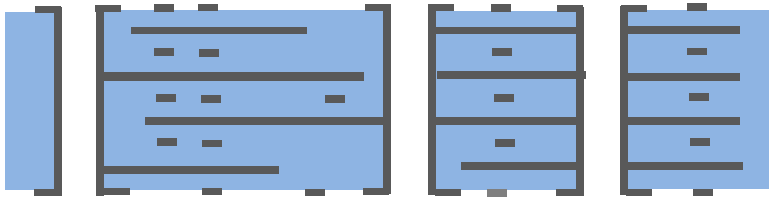
Rigid Flex PWB:
combination of the rigid and flexible PWBs, mainly used to replace short length cables or serve as a connector between two rigid PWBs for better signal integrity. More complex process and higher cost.

PWB Board Structure Types

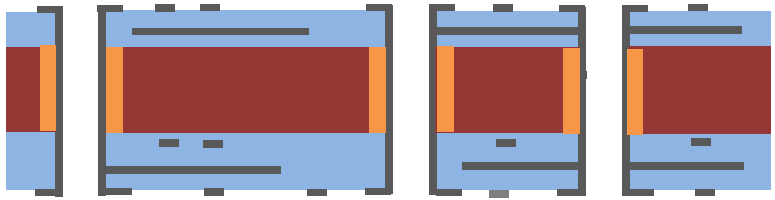


Single sided PWB: one conductive layer - low technology or low cost consumer applications – rigid or flexible PWB.

Double sided PWB: **c**onductive layers on both sides - doubles the area for mounting components, connected through plated holes – low cost, low technology PWB

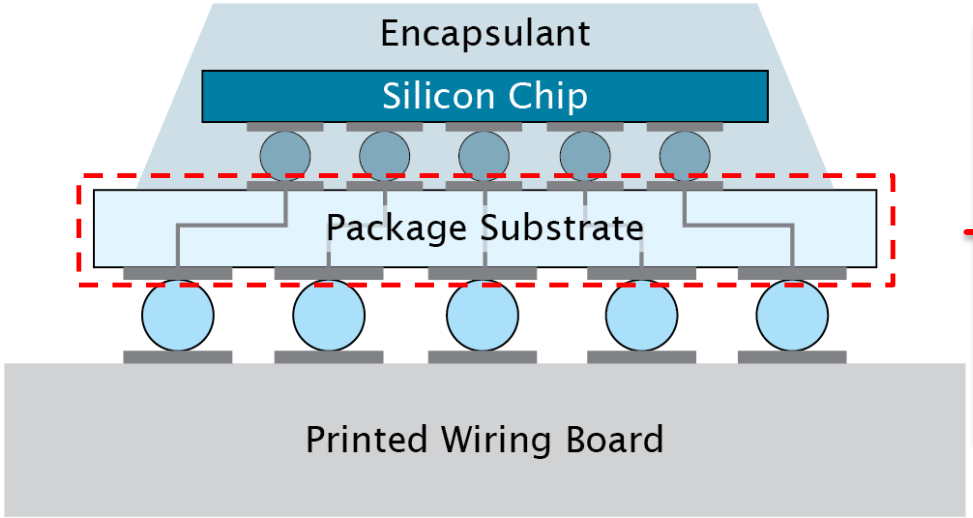


Multilayer PWBs: at least one metal inner layer (> 2 copper layers) - higher wiring density for higher density interconnect (HDI) and I/O, high performance - 4 layers to well over 60 layers - motherboards, line cards, backplanes, mid-planes, etc.



Metal core boards: utilize a substantially thick center metal plate of copper or aluminum for heat dissipation. Plated through holes for interconnect are insulated from the metal core to prevent shorting. Process of drilling oversized holes, insulating, then re-drilling with a smaller bit, and plating.

Package Substrates (Chip Carriers)



- Interposer PWB enables finer I/O ball pitch of chip to escape to a larger pitch on the main PWB (motherboard or line card).
- Typically made of co-fired ceramics, organic polymers, or flexible polyimide films (for tape automated bonding).
- Usually low layer counts and smaller form factor than the system level PWBs.

Types of Package Substrates

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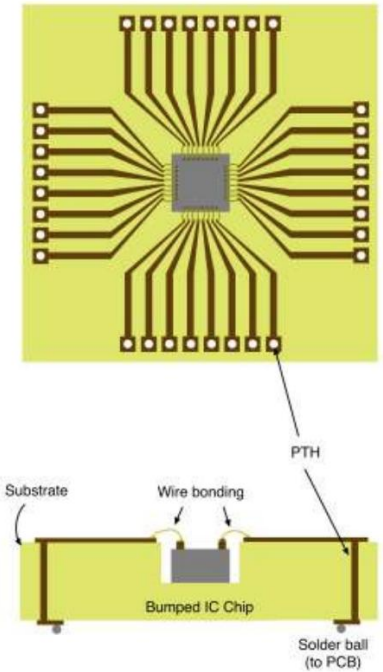
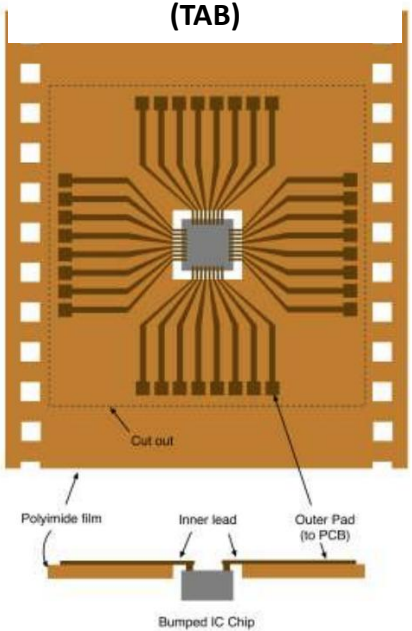
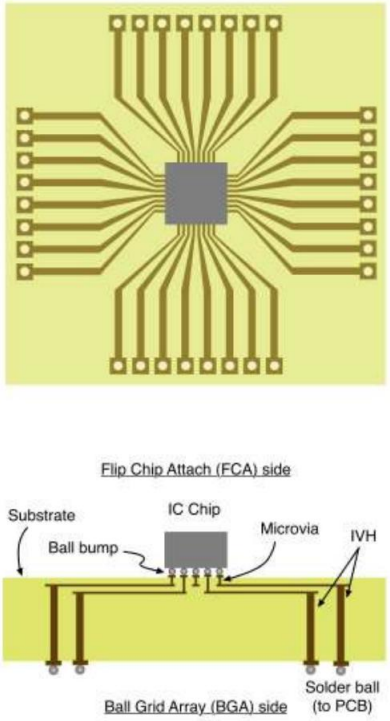
Wire Bonding



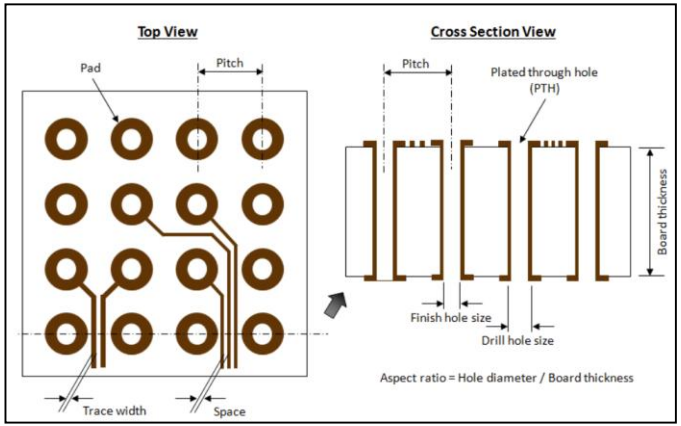
Tape Automated Bonding (TAB)

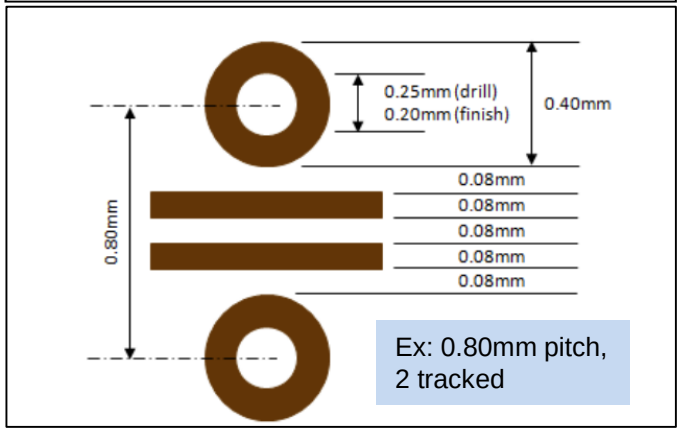


Flip Chip Package



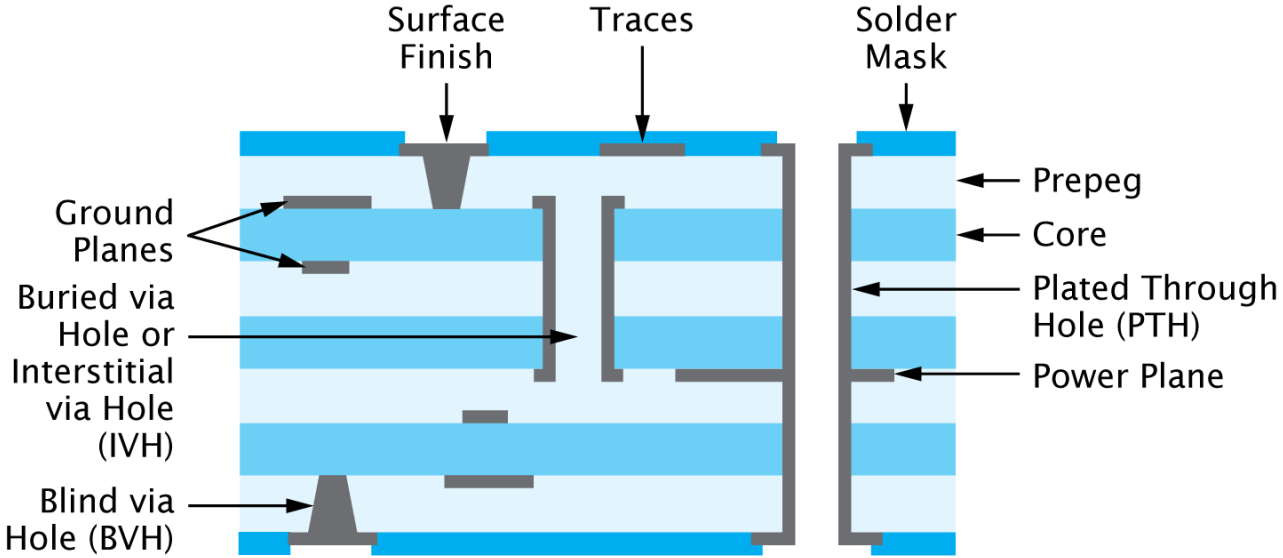
Wireability / Circuit Density

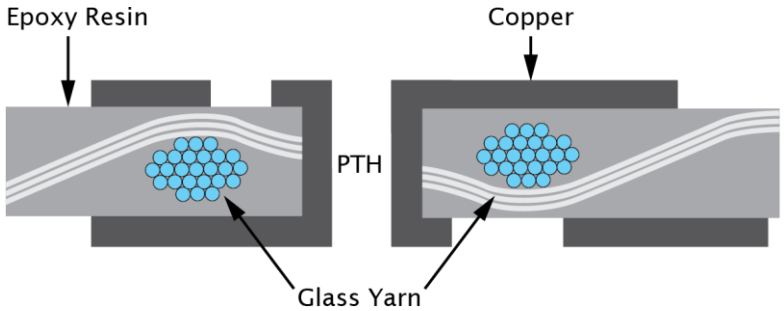




- Defined by the pitch and I/O count of active devices
  - BGA footprint pitch defines escape routing channels
  - I/O, GND, and PWR define part escape breakouts
  - Trace and spacing must be within PWB fabrication limits
  - Free field routing outside the footprint for DFM and yiield.
- Modern devices range from 1mm pitch and smaller
  - 0.5mm and smaller pitch are constrained for PWB breakouts
  - Finer pitch demands higher technology and drives cost.
- Finer pitch footprints may require SI (signal integrity) compromise to achieve escapes where routing channels are very narrow

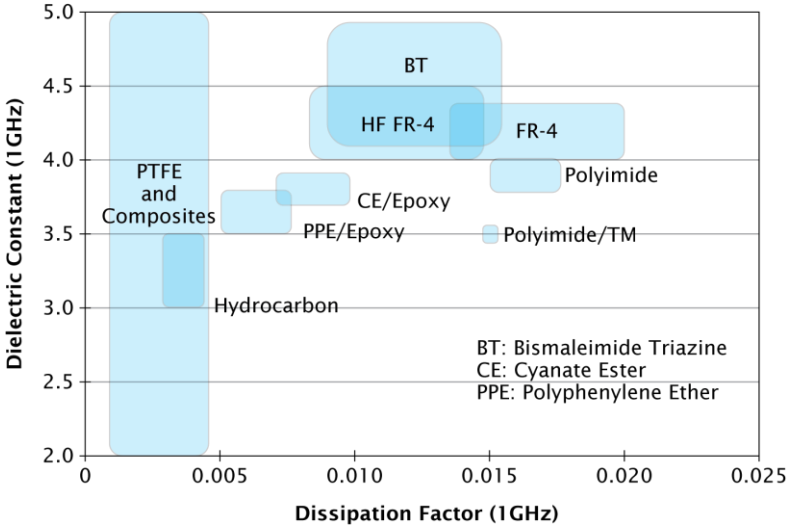
PWB Fundamental definitions: A reminder





Primary Attributes of PCB Laminate Materials

Material Dk / Impedance Control



PCB Impedance Dependencies

- Type of impedance structure
  - Stripline, microstrip, Single-ended (Zo), ZDifferential, coplanar waveguide
  - Tightly coupled, loosely coupled
- Trace width, trace height (Cu thickness), coupling airgap
  - Smaller tracewidths and airgaps should be on 0.5oz. Cu. for DFM, yield
  - Zo less sensitive to etch deltas than ZDifferential
  - Tightly coupled ZDifferential pairs are more sensitive
  - Copper plating buildup effects impedance, esp. Zdifferential (coupling)
- Dielectric Constant (Dk or ε_r)
  - Lower Dk material permits wider traces for given Zo and ref height
  - Lower Dk improves propagation rate (lowers propagation delay)
- Soldermask (Microstrips only)
  - Relatively high Dk (circa 4.0 for most commonly used masks)
  - Non-isotropic in thickness (puddling, wiping, etc.)
  - Typical thickness of 0.7mil (18um) over circuits and ~1.8mils (45um) between conductors

Material Df & Copper roughness / Attenuation

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PCB Trace Loss (attenuation) Dependencies

- Type of signal trace structure
  - Stripline (innerlayer)– Dissipation Factor (Df) defined by adjacent laminate material only
  - Microstrip (surface layers) – Df is an amalgam of underlying laminate, soldermask, and air to infinity
  - Attenuation is quantified in minus dB per unit length at a stated frequency
- Frequency
  - Trace attenuation is acutely dependent on transmission speed
  - High speed skin-depth trace losses can be a multiple of the Df-driven dielectric losses
  - Low Df rated material is still one major mitigation to offset loss impact of high speed
- Copper roughness
  - High speed propagation all have options for smooth and/or ultra smooth copper
  - Smooth copper has cost premium, and reduced adhesion strength
  - Laminate suppliers use bond enhancement chemistries to improve adhesion
- Copper weight (Z-axis height) and tracewidths
  - Signal copper weight has very little impact on trace attenuation
  - Tracewidth has only a modest effect, unless line widths drop below 4mils (100um)

Mechanical / Expansion and Thermal durablility

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PCB Material Primary Thermal-Mechanical Attributes

- Tg – Material transition temperature when mechanical properties begin to change
  - Tg is typically exceeded during PWB fab's lamination process and at reflow assembly
  - Higher Tg helps in reducing manufacturing stresses induced by thermal excursions
- Td – Temperature of decomposition, at which essential properties degrade due to weight loss
  - Key barometer of survivability through multiple lamination and reflow assembly thermal cycles
  - Td of ≥330°C at 3% weight loss is a good indicator of ability to endure Pb free assembly temps
- CTE – coefficient of thermal expansion, Z-axis CTE is especially important
  - Is broken out into α1 (below Tg) and α2 (above Tg)
  - Lower CTE-Z values ensure less expansion and so better survivability of plated interconnects
  - Reducing the laminate (PWB) CTE reduces the CTE mismatch with Chip package (esp for cofired ceramic substrates), inducing lower degrees of stress during thermal cycling
- Copper Bond strength – stated in pounds (lbs.)
  - Essential attribute for multiple PWB lamination cycle fabrication
  - Essential at outer layers to mitigate risk of pads lifting off or tilting at assembly

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Basic Multilayer PCB Manufacturing

PWB Fabrication Process Flows

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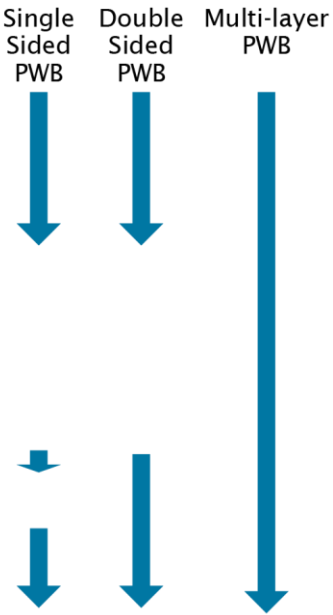
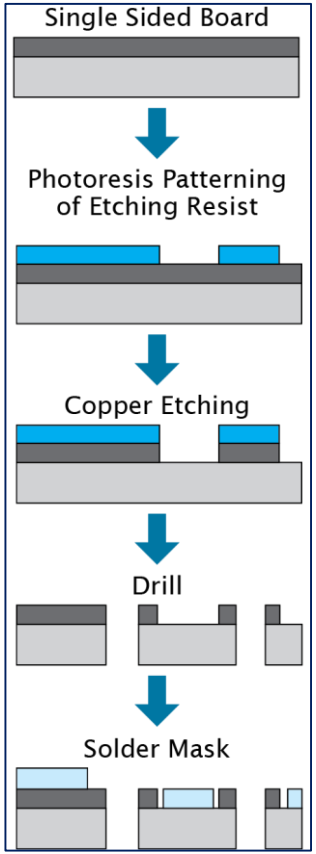
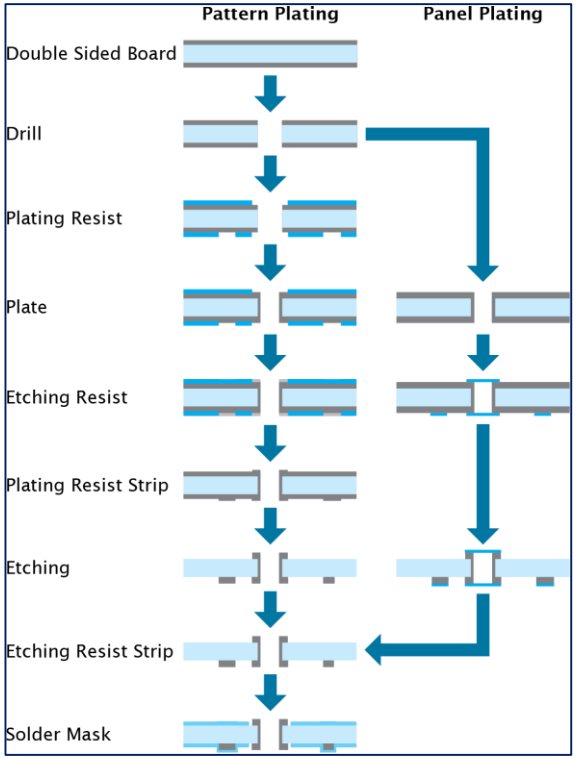
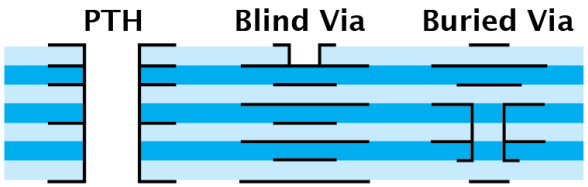
CAD output (Technology Files)
Photo Tool Preparation
Copper-clad Laminate
Photoresist on Laminate
Imaging (Exposure, Develop, Strip Resist)
Surface Preparation for Lamination
Kitting (Pile up Laminates, Prepegs and Foils)
Lamination (Usually Vacuum Press)
Break (Remove from Lamination Tool)
Routing (Prepare to Panel Format)
Drill
Plating & Outer Layer Imaging
Surface Finish
Solder Mask/Legend Print
Routing to PWB

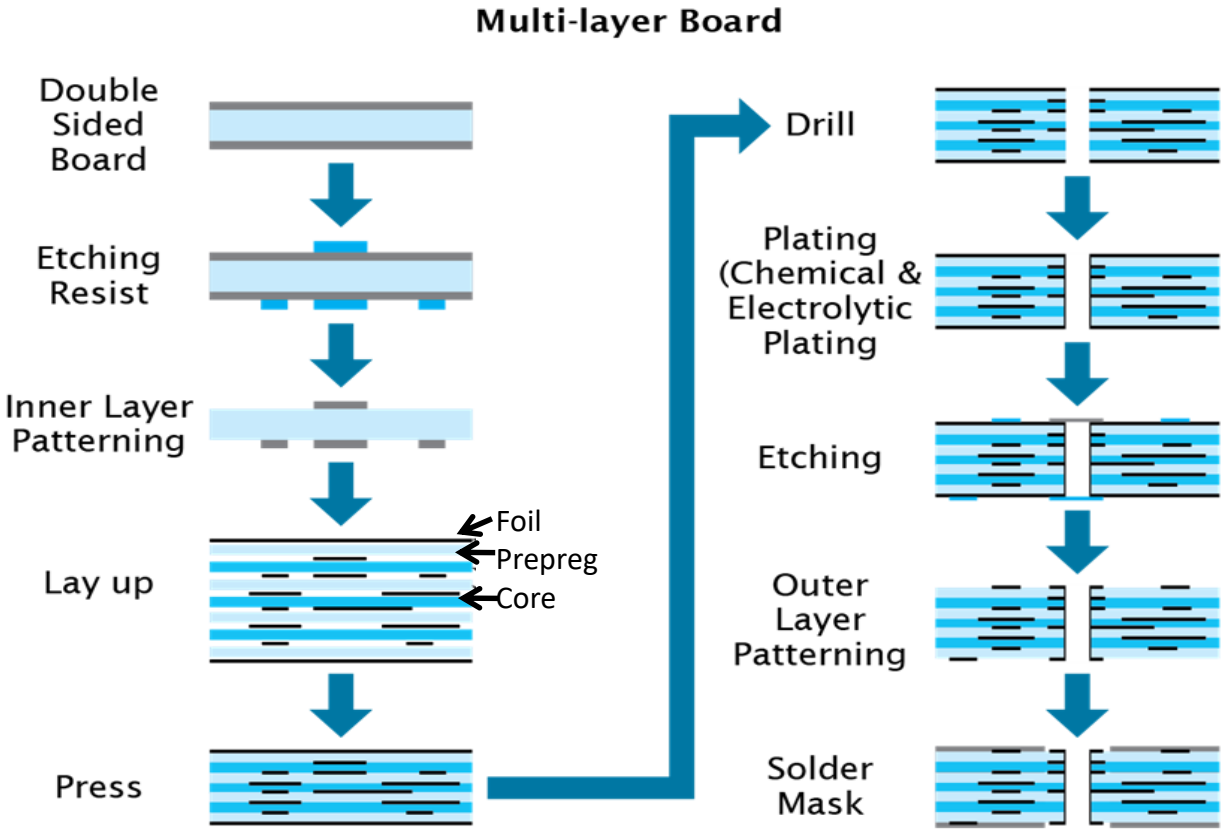








Multilayer PWB Fabrication Process Flow



Front-End Engineering w/CAM

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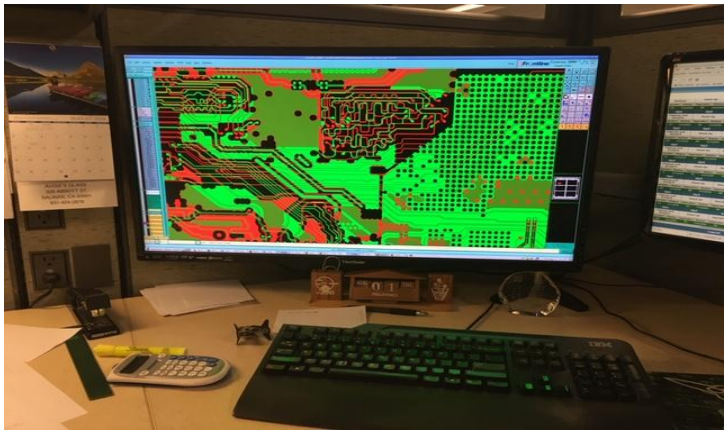
- PCB Data
- Central FTP
- Retrieve Data
- Document Control
- Product Engineering
- Panelization
- CAM Tool I/Ls
- Release I/Ls
- CAM Tools O/Ls & SMs
- Release O/Ls
- Plot/Insp/Rel SMs
- Plot/Insp/Rel Legend



CAM (Computer-Aided Manufacturing) work station

Engineering

Gerber/ODB++ Created Details:

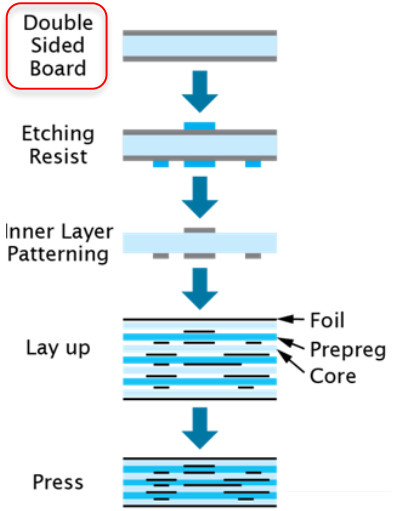
Copper Layer Artwork
Mask and Legend Artwork
Drill Files
Route Files
AOI Comparative Files
Electrical Test
- Fixture (if dedicated type)
- Netlist Comparative Files

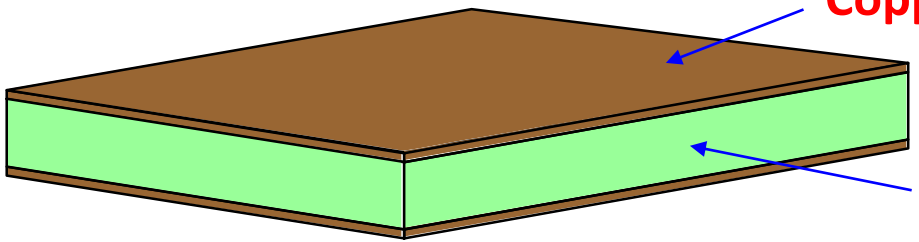
Physical and Electronic Floor Travelers

Other Input Sources:

PCB Acceptance Specification
UL (1950, 60950, etc.)
IPC (as required by PCB Specification)
RoHS (EU Leadfree Initiative)
Sanmina Fab Plant Specification

Laminate



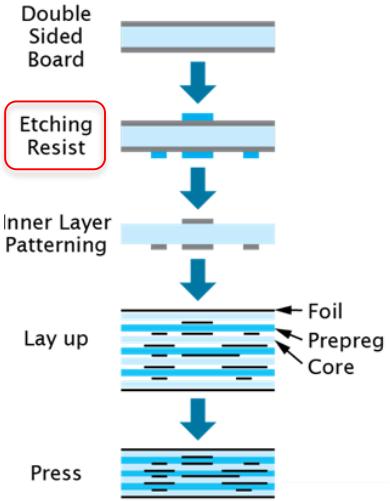


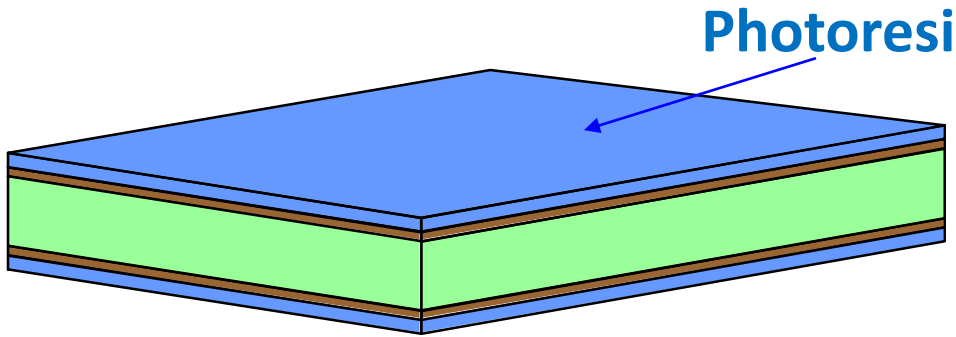
- Core (“C-stage) is fully cured and copper clad laminate
- Dielectric type, thickness, and copper weights per fab print / stackup

- Copper cladding becomes the inner layers in the most standard process.
  Cores are available from 0.000315”(8µm) to 0.063” thick (1.6mm)
  Note: Standard thin cores start at 0.002” (50µm)
  Thicker than 0.031” (0.79mm) thick cores are mostly used for D/S PCBs.

- Core panels are cut from laminator’s larger master sheet.
  - Typical master sheets are 36”x48” and 42”x54” in English scale and 1020mm x 1020mm and 1020mm x 1220mm in Metric scale.

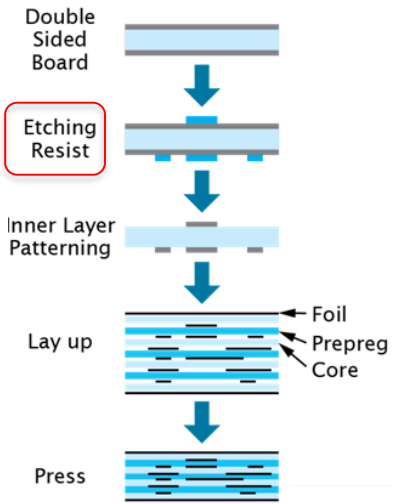
Resist Coat



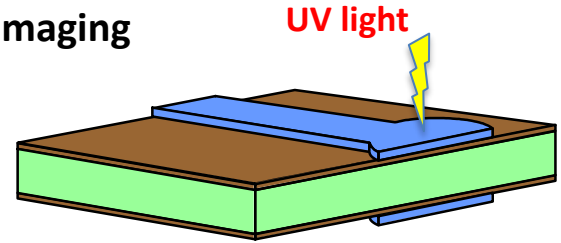


- Cores are chemically cleaned
- Photosensitive dry film is applied to both sides with heated rollers
- Dry film acts as etching resist in imaging process
  protecting what will become the retained copper features

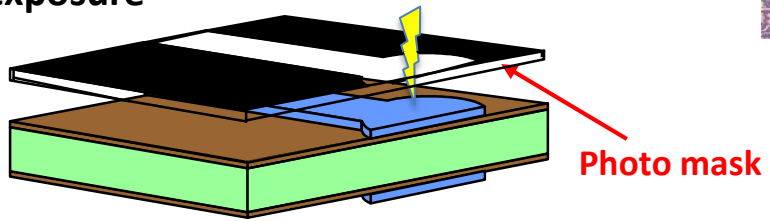
Image & Develop

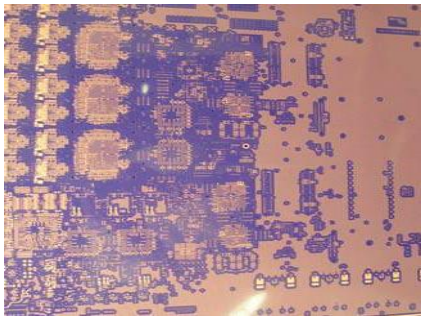


Direct imaging



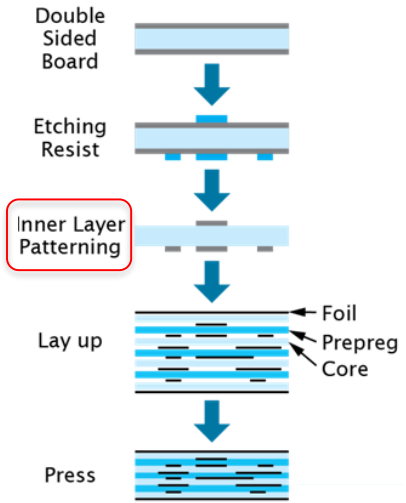
Mask exposure

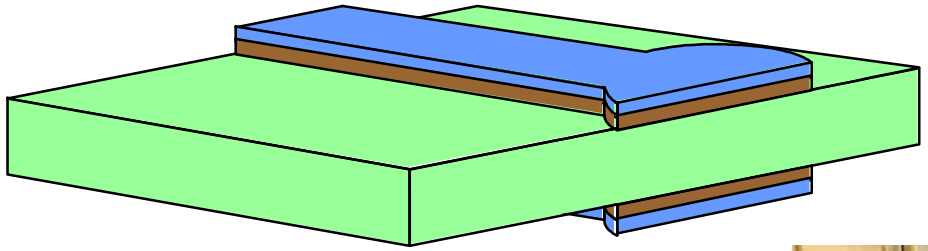


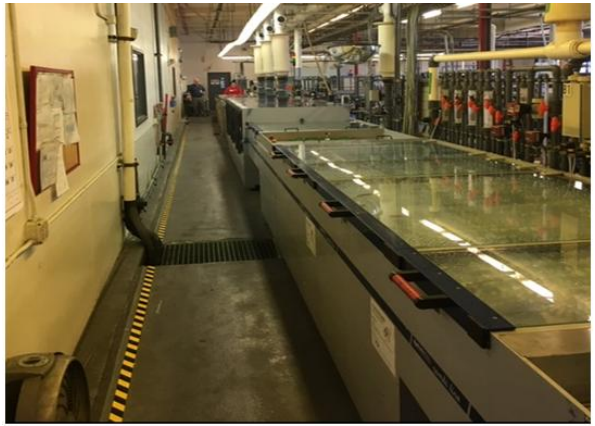


- Both sides of the circuitry are drawn onto the resist using LDI (laser direct imaging)
- Or transfer image using photo mask negatively.
- Dry film polymerizes (hardens) where laser light hits
- Unexposed areas are chemically developed away

Etch

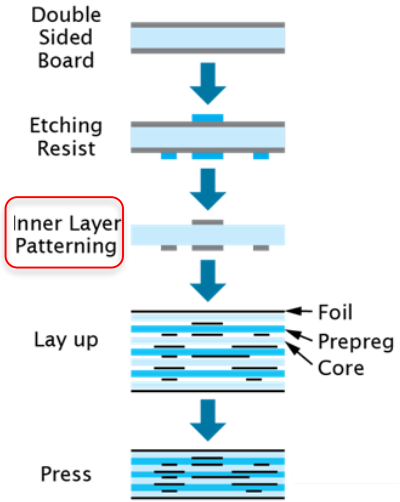


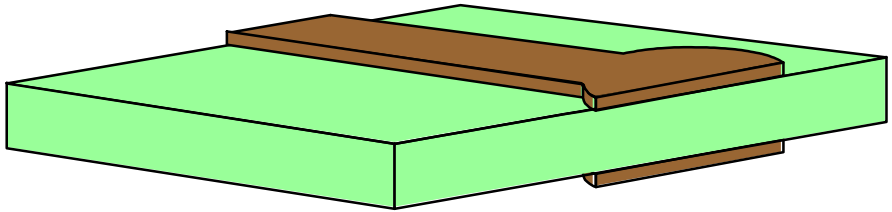




- Cores pass through cupric chloride etch
- Any unprotected copper is removed by the etchant
- Etch rate is controlled by conveyor speed and spray pressure based on copper weights being etched

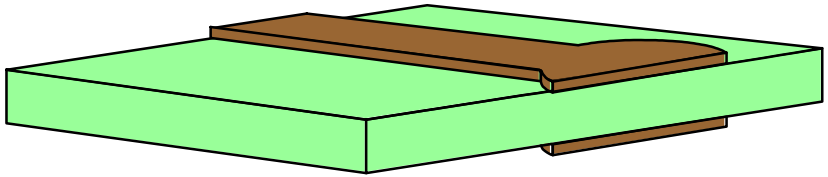
Strip Resist





- Dry film is chemically stripped off the etch defined features
- Circuitry now appears in copper
- Multilayer tooling slots are now punched into cores using a Post-Etch Punch

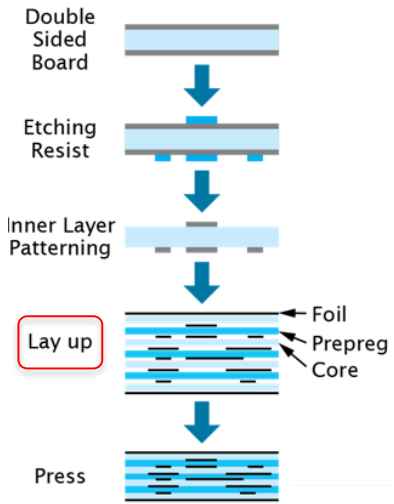
AOI – Automated Optical Inspection

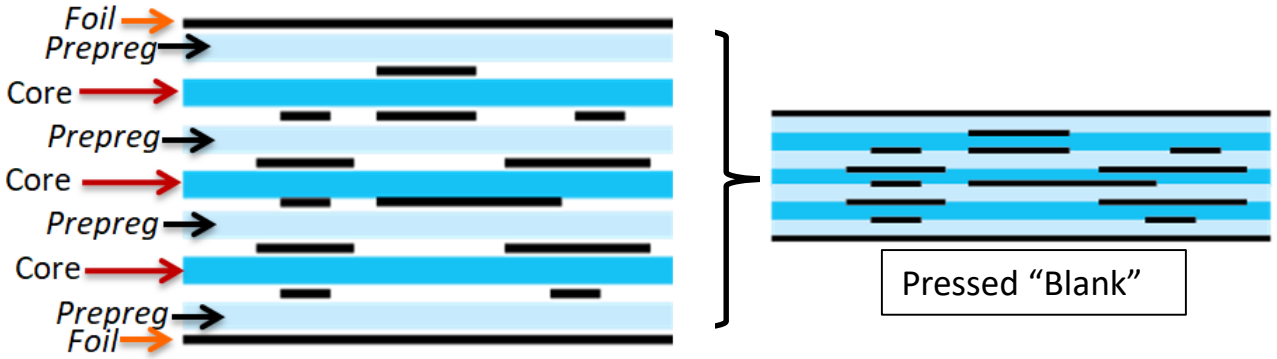


Defects detected by AOI include:

- Extra copper
- Missing copper
- Linewidth reductions
- Debris
- Mechanical damage
- Unstripped dry film resist

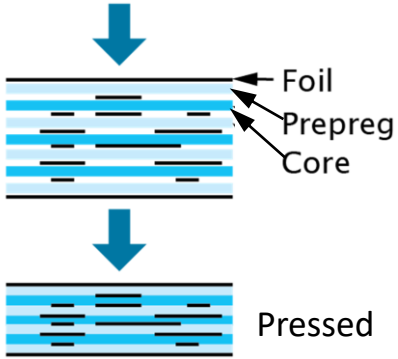
Stackup & Lamination





- Etched cores move to kitting (lay up)
- Outer layers are typically applied as bare copper foil sheet
- Prepreg ("B-stage") are bonding plies placed between cores and under outer layer copper foils
- Cores and prepregs are stacked on metal pins at the post-etch punched multilayer tooling slot positions
- Several boards go vertically into typical "book"
- Heavy steel press plates go on top & bottom of book
- Pressed item is referred to as "blank"

Stackup & Lamination

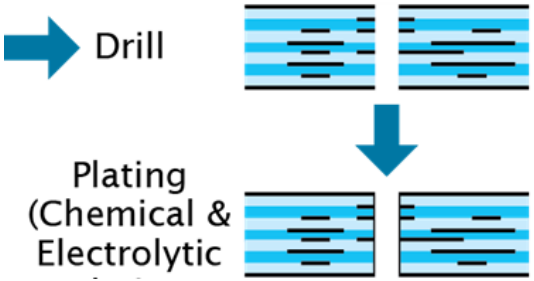


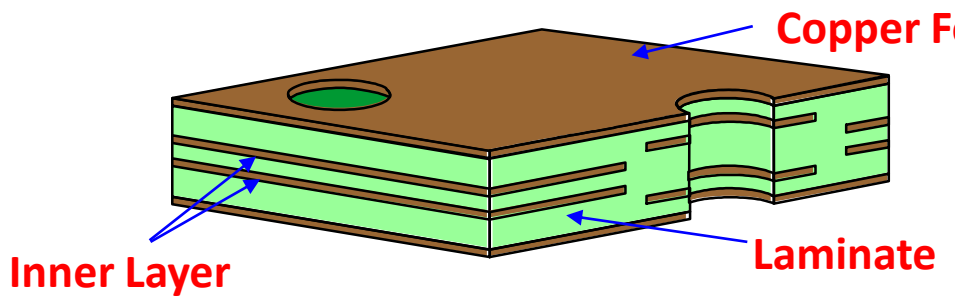
Vacuum-assisted lamination press

Particle, Temp, and RH controlled lay up rooms

- Books go into vacuum-assisted presses
- Air is removed and book is pressed together under heat and pressure
- After pressing, books are broken down into individual board blanks
- Edge flow (aka “Flash”) is trimmed away

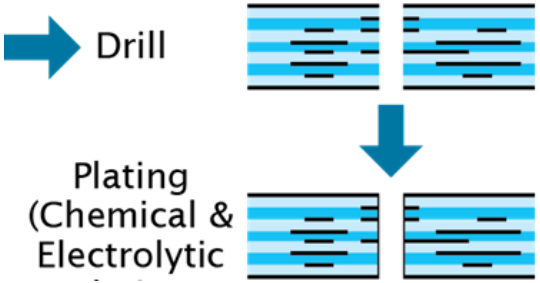
Drill & Deburr

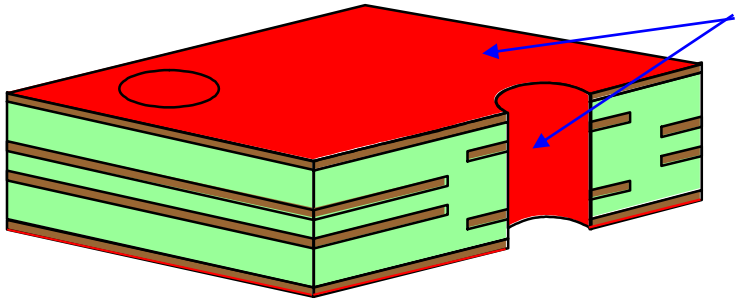




- Blanks are stacked up on pins located in drill machine table
- Blanks are drilled with carbide bits on N/C drill machines
- Machines automatically change drill sizes per program
- Drills are available from 0.002”(50µm) to 0.256” diameter (6.5mm)
- X-ray drill makes the base holes and these are used for optimized layer to layer alignment
- Laser drilling uses CO_2 laser or UV and CO_2 laser process
  Note: laser can form through-holes, limitedly
- Holes are deburred and cleaned after drilling

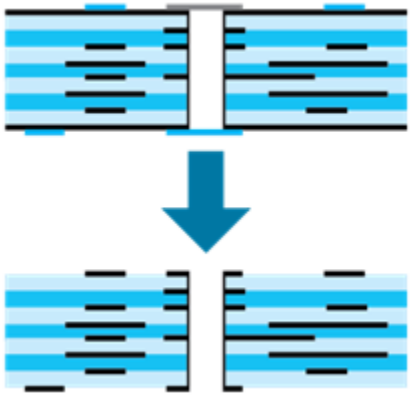
Desmear & Copper Deposition

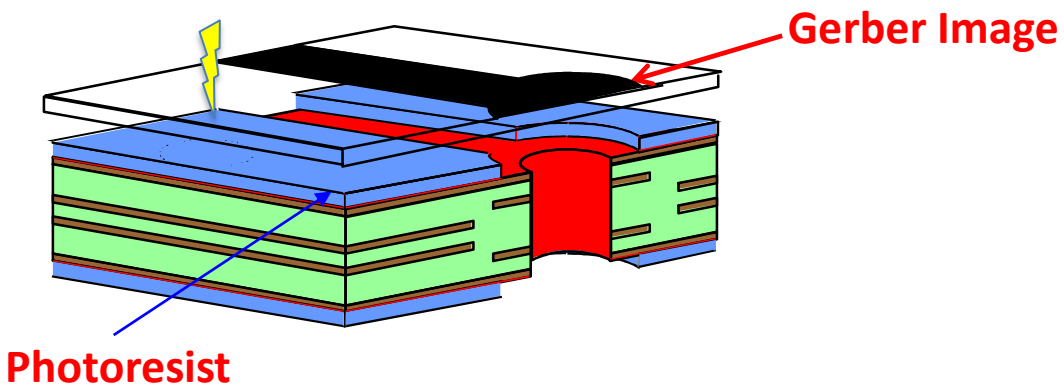




- Heat of drilling can melt & smear resin on hole walls
- Smear is removed either chemically or in a plasma chamber to assure a circuit to hole wall plated connection (Desmear)
- Desmear also lightly roughens hole wall for better plating adhesion
- Initial thin copper is plated over the all surface using electroless copper deposition
- Electroless copper provides conductive path for subsequent electrolytic copper plating (typically net of 0.001” (25µm) minimum thickness)

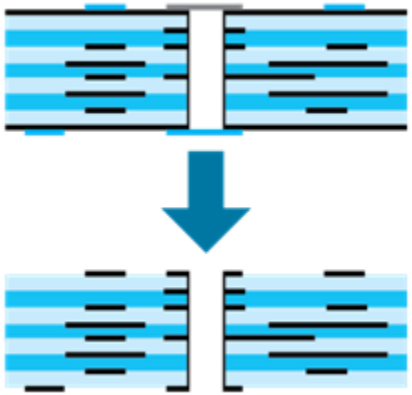
Coat, Image & Develop

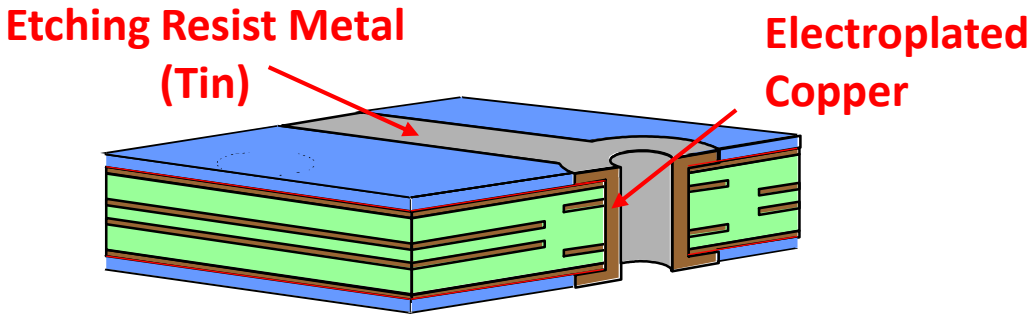




- Photosensitive dry film (plating resist) is applied to both sides of blank with heated rollers similar to inner layer cores
- Both sides are exposed by laser direct imaging (LDI) or mask exposure.
- Dry film polymerizes where laser light hits image, but is opposite polarity from inner layer process for pattern plating

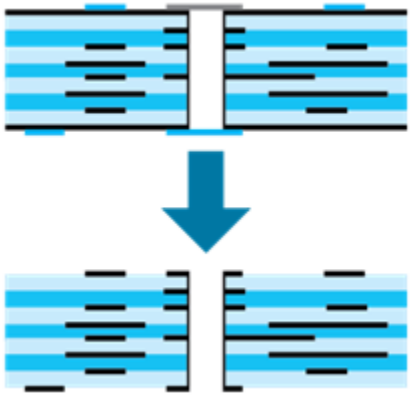
Copper & Tin Plate

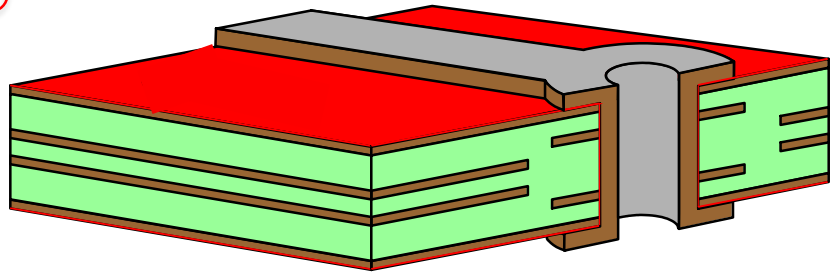




- Electrolytic copper is plated in holes and on all artwork-defined outer circuit features
- Copper deposition is typically 0.001” (25µm) thick on hole wall
- Tin is plated on top of copper in hole and on outer features to act as etchant barrier (all boards have tin on them at this point in process)
- Copper and tin plating is done with computer-controlled hoist-driven plating line

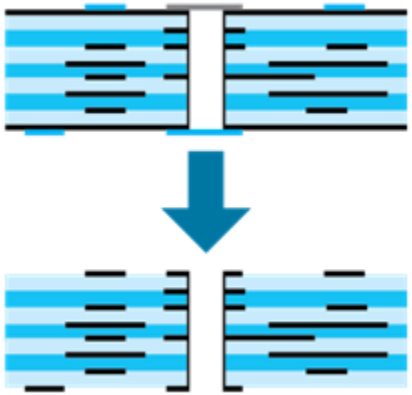
Strip Photoresist

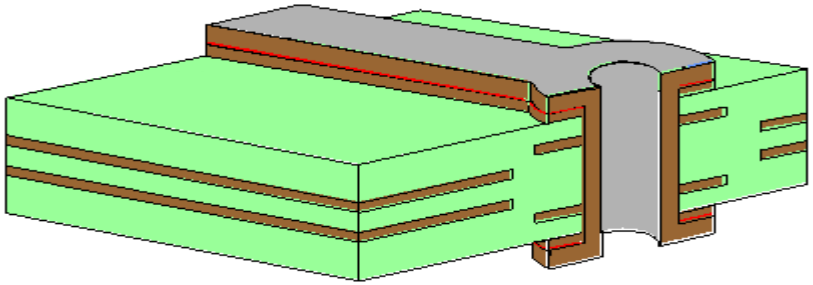




- Dry film resist is now chemically stripped away at the 1st part of a S/E/S line (strip dry film – etch copper – strip tin) exposing unwanted copper areas
- Needed the circuitry remains coated with tin

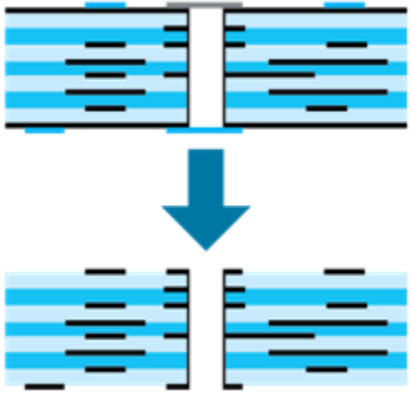
Etch





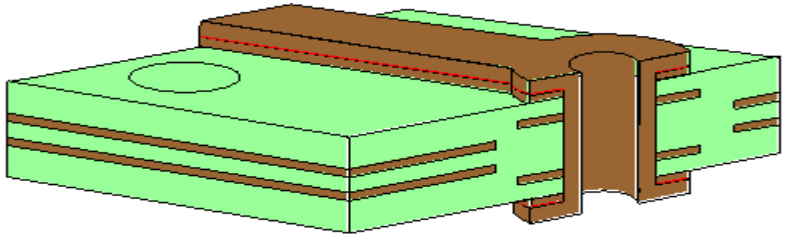
- The unwanted and exposed copper areas are now etched away with an alkaline-based etchant at the 2nd part of SES line
- Needed circuitry remains, protected by tin
- The board circuitry is now complete – all electrical connections now defined and integrated through plated vias

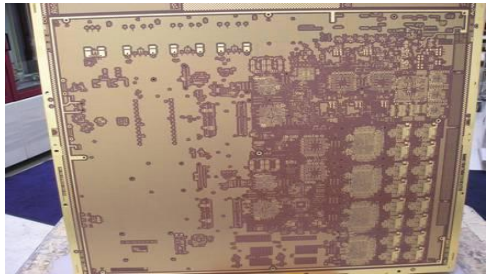
Tin Strip

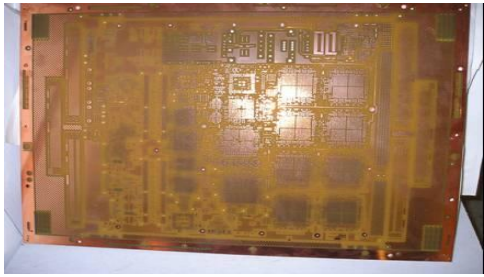


Outerlayer
Patterning

Etching

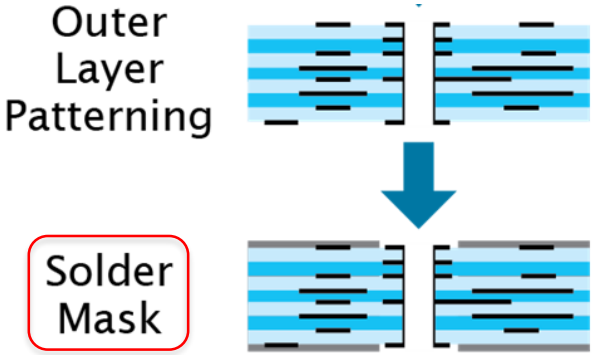


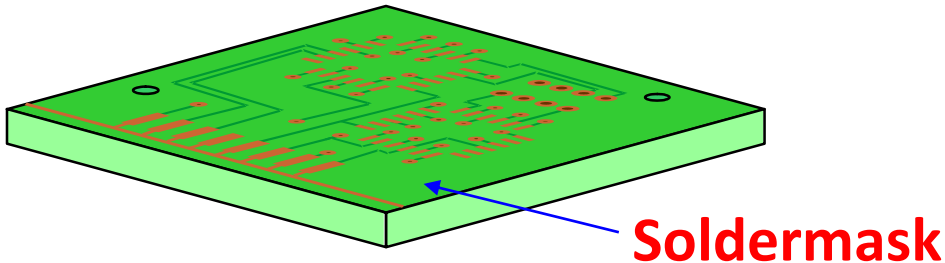




The tin that was protecting the traces, pads, and hole barrels from being etched is chemically stripped away at the end of the SES line, leaving bare copper circuitry.

Soldermask

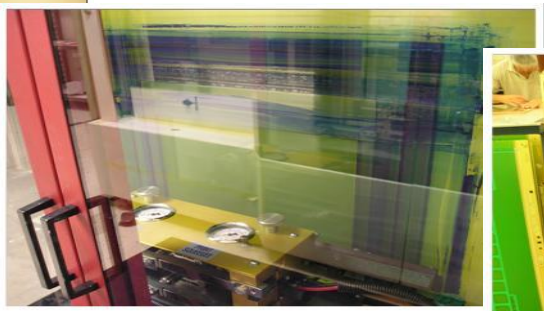


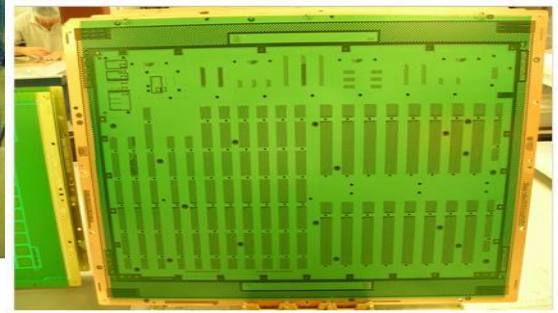


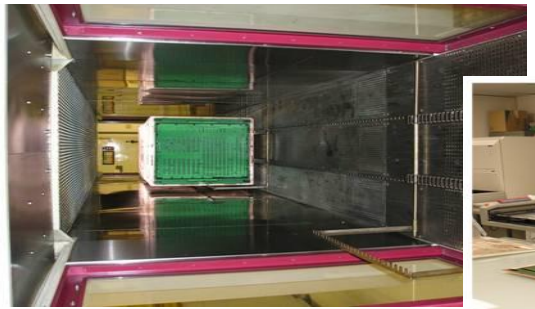
- LPI (Liquid Photo-Imageable) soldermask is applied to protect and insulate the outer circuitry. It also prevents shortages between circuits by solder.
- The color is usually green, but many color options such as blue, red, yellow, purple, black,,, are available
- Stages of pre-curing in ovens set up the mask to tack free forming an imageable coating
- Soldermask artwork is used to expose by UV or direct imaging is used if higher resolution is required.
- The uncured parts of the mask are developed off
- The panel is then baked for final curing of the mask
- Unlike dry film, the cured mask remains permanently on the board for the purpose

Soldermask

Mask Deposition





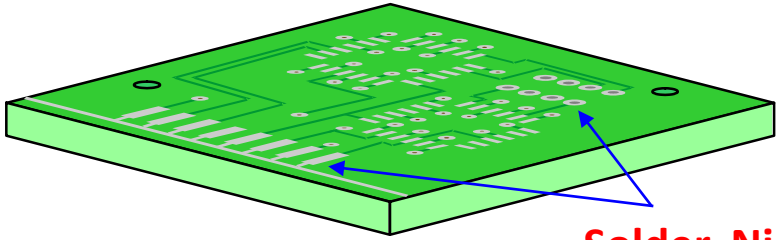


Tack Cure in Tunnel Oven

Photo or Laser Imaging

Develop Image and strip of un-imaged areas

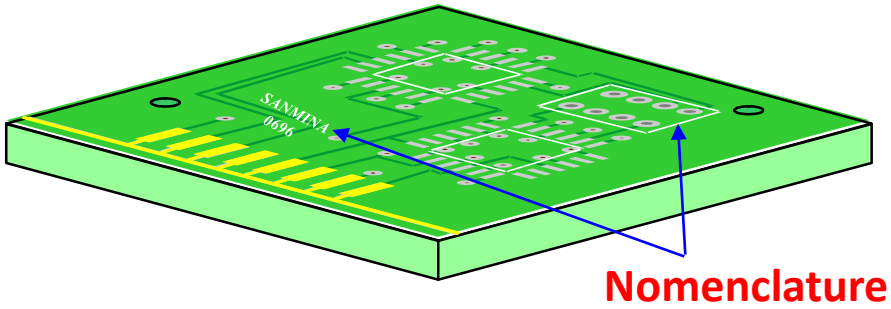
Final Surface Finish



Solder, NiAu, OSP, ENIG, Immersion Ag, etc.

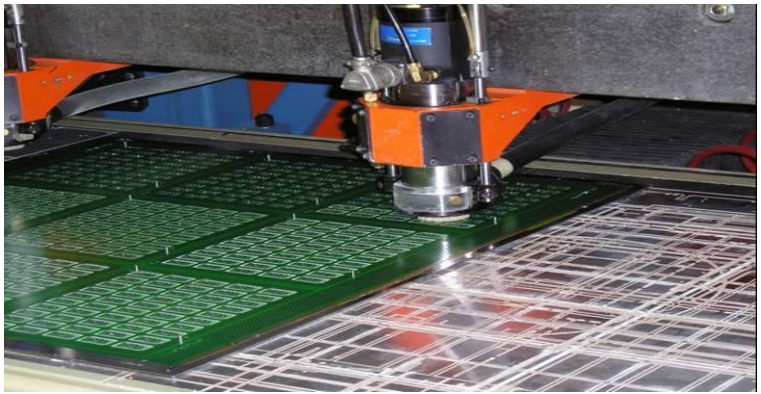
- Final metal finish is applied wherever copper is left exposed – typically on exterior pad features and in the holes
- Available finishes include tin-lead solder, hard electrolytic gold over nickel (for gold fingers), soft gold over nickel (for wire bonding pads), electroless nickel – immersion gold(ENIG), ENEPIG (adding electroless palladium layer prior to immersion gold), immersion tin, immersion silver, and OSP (organic solderability preservatives, a temporary anti-tarnish coating).
- Choice is specified by the PCB designer and purpose is to protect the outer copper from corroding while also providing a suitable surface for soldering components

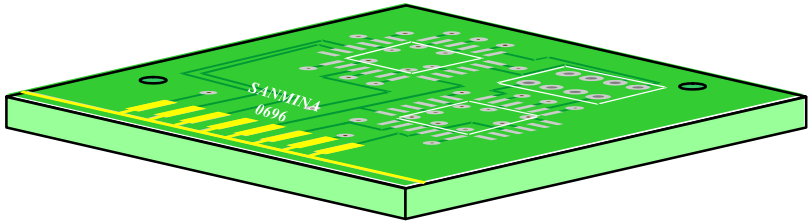
Silk Screen (Legend Ink)



- Legend information is needed for assembly and for troubleshooting boards in the field
- Nomenclature is screen-printed onto board in epoxy-based ink (usually white) using a standard squeegee/fabric screen method
  Note: Laser scribing and inkjet print are available and it allows very fine font sizes
- Once screened on, the ink is thermally cured by baking and cannot be removed

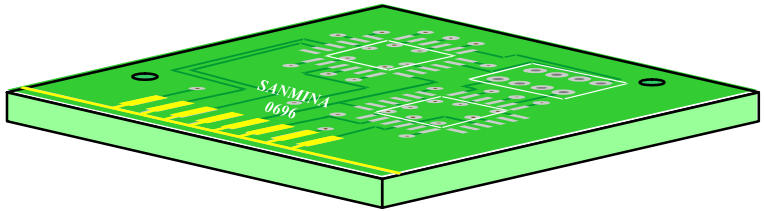
NC Routing





- Individual boards are cut out of production panels using NC (numerical controlled) routing machines
- Routing machines visually look very much like drilling machines but with the table moving under a constantly spinning tool
- Depending on board thickness, panels may be stacked 2 or more high for routing

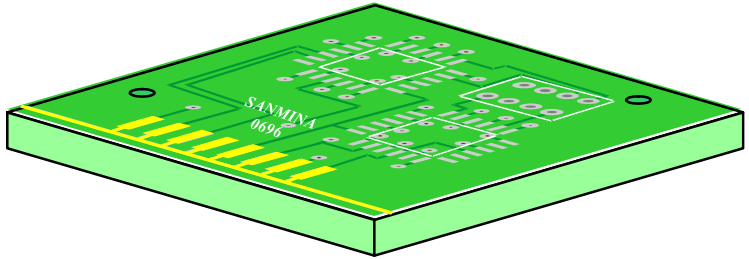
Electrical Test

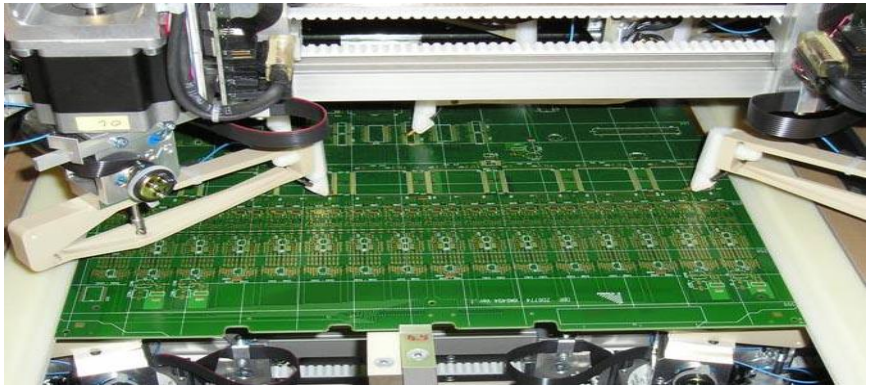


- The finished boards are tested to identify any electrical shorts, opens, or leakages (high resistance shorts).
- Some faults can be repaired whereas others cannot – board will need to be scrapped
- Tests are run against the netlist files that exactly define the connections in their design
- Tests can be fixtureless using flying probe whereby moving arms make contact with the circuits net by net or by dedicated fixture to contact all circuits at once

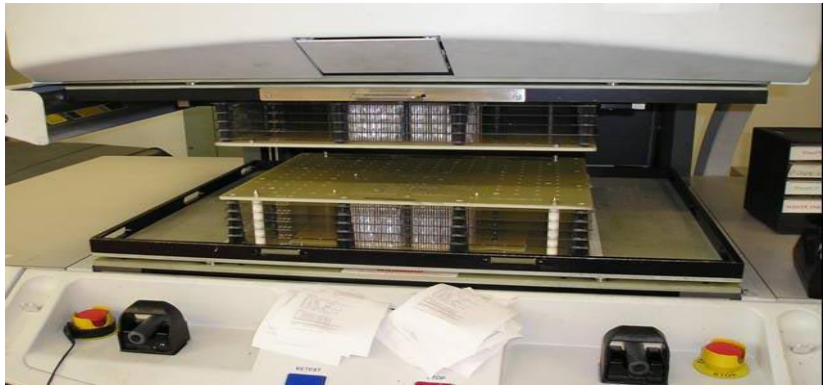
Note: The cost can select the testing method whether the dedicated fixture with universal tester or flying probe tester. Fine features may not be contacted by fixture probes.

Electrical Test





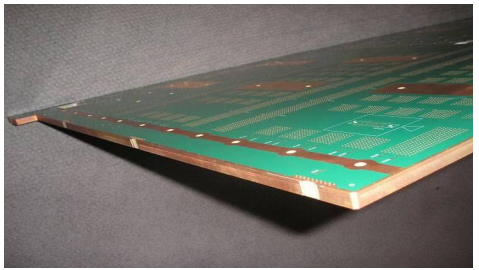
Flying Probe
Fixtureless Tester

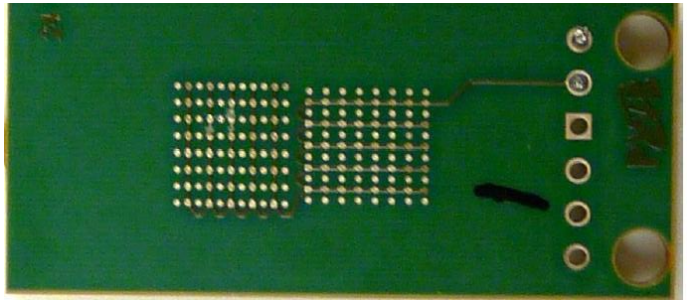


“Clamshell” Bed-of-Nails
Universal Tester with Dedicated Fixture

Reliability

- Long term reliability focuses on the ability of the product to resist shorts or opens during the expected service life
- These defects are most frequently identified using accelerated testing techniques
- Shorts : Electrochemical migration is tested using temperature, humidity and bias
  - Conductive anodic filament (CAF) growth
  - Foreign materials that can create a pathway
- Opens : The propensity for opens is tested using thermomechanical stress
  - PTH cracks or separation
  - Interconnection defect (ICD)
  - Microvia separation
  - Delamination



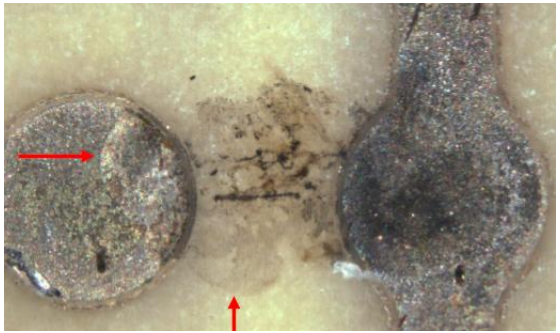


Typical CAF Test Coupon

Reliability: Shorts

- IPC TM650 2.6.25 outlines the CAF testing methodology and criteria
  - Numerous variants of TH and B (Temperature, Humidity & Bias)
  - 50C/80RH, 65C/65RH, 85C/85RH for 500 hours at voltage NOTE: This is RELATIVE humidity, so the amount of water in the chamber is much, much greater than field conditions
  - Detect defects using resistance change (after preconditioning)
- Typical defect causes
  - De-wetted glass fibers (“triple” points), hollow filaments
  - Foreign materials

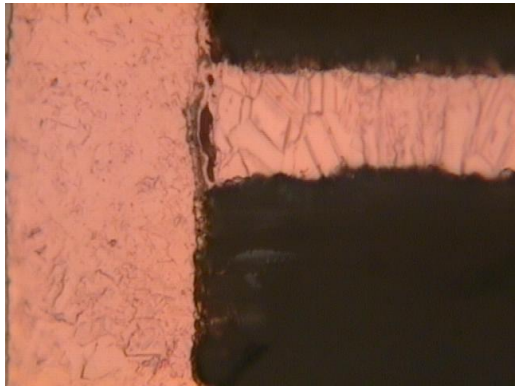
Growth between glass filaments



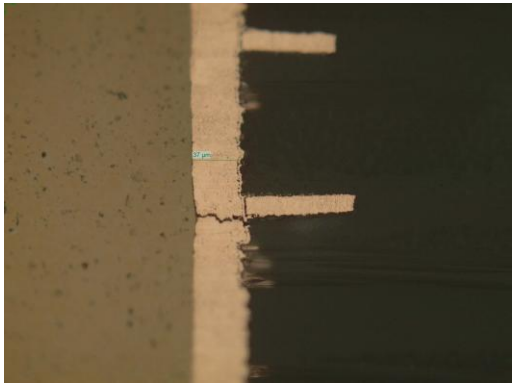
Foreign material / contamination

Reliability: Opens

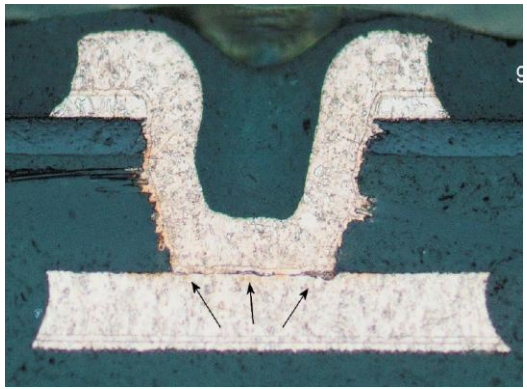
- IPC TP650 2.6.26 (IST) and 2.6.27 (Reflow simulation) outline the testing methodology and criteria
  - Thermomechanical stress using electrical heating or air to air methods
  - Repetitive cycling until specific cycles or a resistance degradation threshold is met
- Typical defects
  - PTH cracks, separation or ICD
  - Microvia separation
  - Delamination



Interconnect Defect (ICD)



PTH Barrel Crack

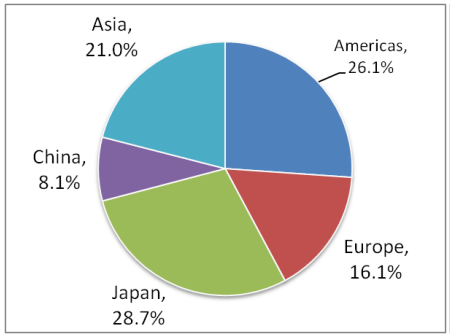


Microvia Separation

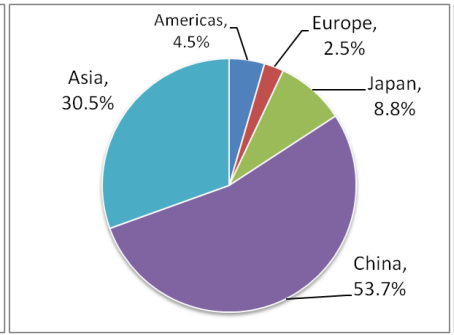
Delamination

Future Markets

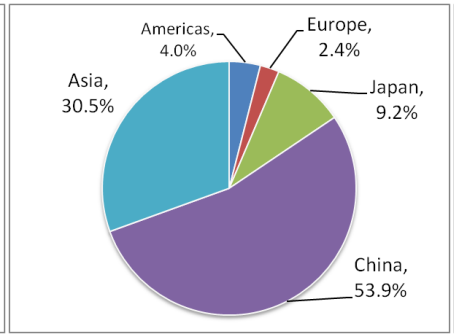
PCB Production by Geographical Region



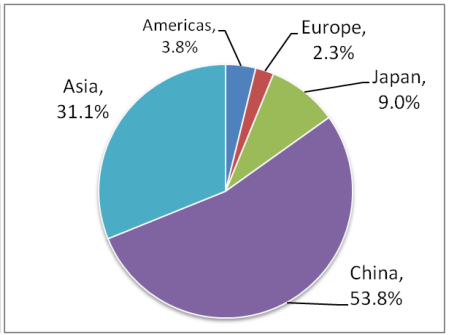
2000, US$41.6B



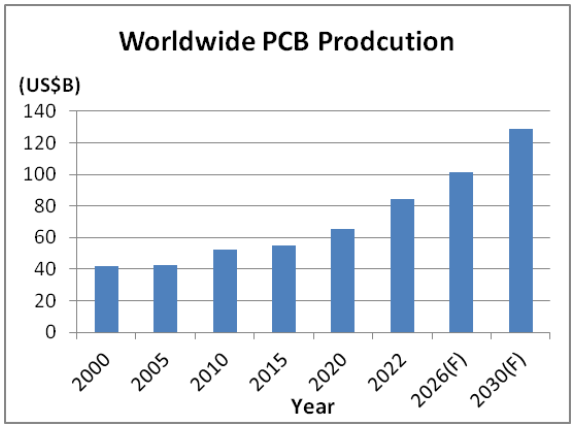
2020, US$65.2B



2022, US$84.3B



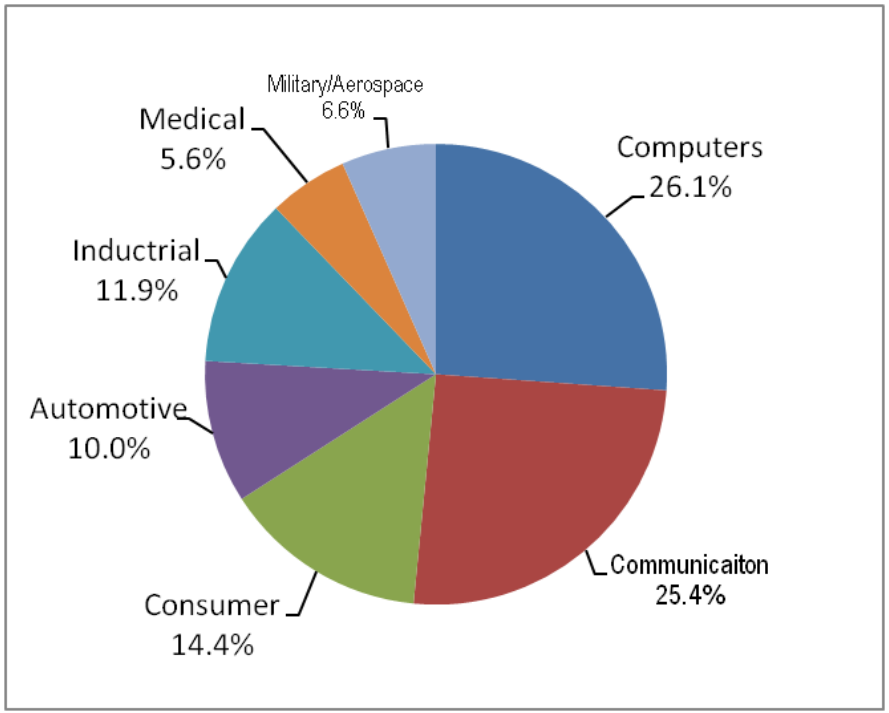
2026F, US$101.6B



- PCB Production is mostly in Asia: China, Taiwan, S Korea & Japan make 90%+ of PCBs by value.
- This distribution ratio is expected to stay the same for the next few years, but the total value keeps growing. It is expected to grow at about 5% of CAGR in the next 10 years.

* Data from Prismark Partners LLC and web search.

PCB Production by Market – 2022



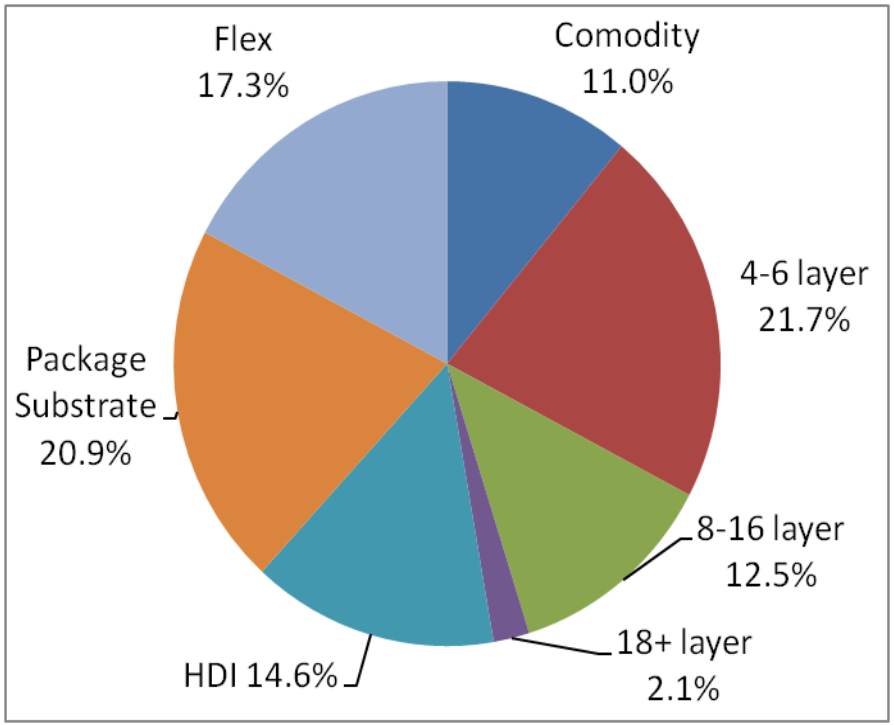
US$84.3B

- Computing and Communications markets drive majority of PCB demand
- Growth in Data and Broadband needs
- Growth in Consumer - Smartphones
- Increasing electronics content in modern cars especially in EVs
- Products connecting network

* Data from Prismark Partners LLC

PCB Production by Type – 2022

SANMINA



US$84.3B

- Highest growth rates for HDI technology and IC Package substrates.
- Driven by demand in High performance applications in Computing, Communications, and Mobility
- Hyperscale, AI/ML – Computing & Network
- Optical communications
- Automobile sensors
- Wireless 5G / Smartphones / LEO Sattelite
- 2.3/3.0D packaging

* Data from Prismark Partners LLC

Sanmina PCB Division

Thank You