

Fundamentals of Opto-electronics Packaging

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Outline

- Introduction to optoelectronics/Photonics packaging
- Optoelectronics/Photonics Packaging Fundamentals
- Packaging Photonic Integrated Circuits

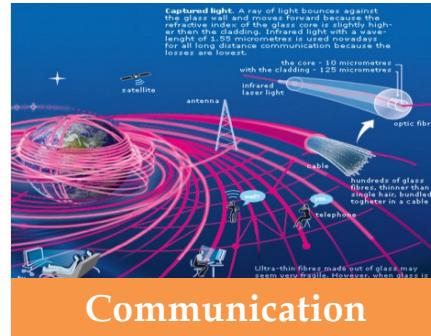
Photonics Packaging

Photonics Packaging combines principles from optics, electronics, mechanics, and materials science to ensure the functionality, reliability, and performance of devices and circuits.

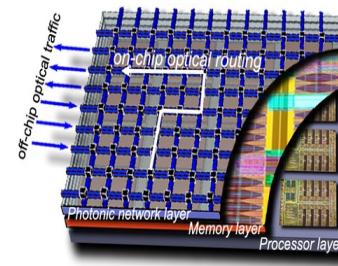
Photonics/Opto-Electronics Applications



Data centers



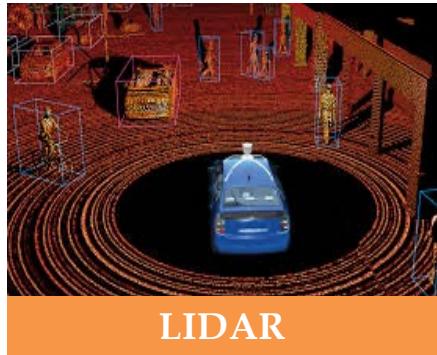
Communication



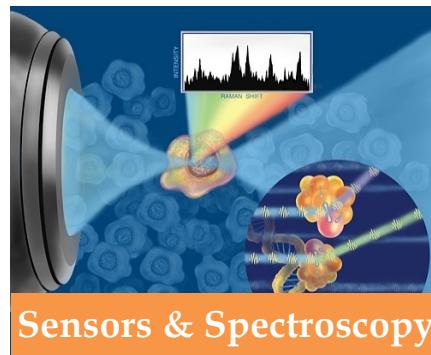
Optical Interconnects



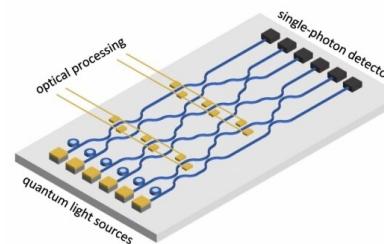
Path to 6G



LIDAR



Sensors & Spectroscopy



Quantum Photonics

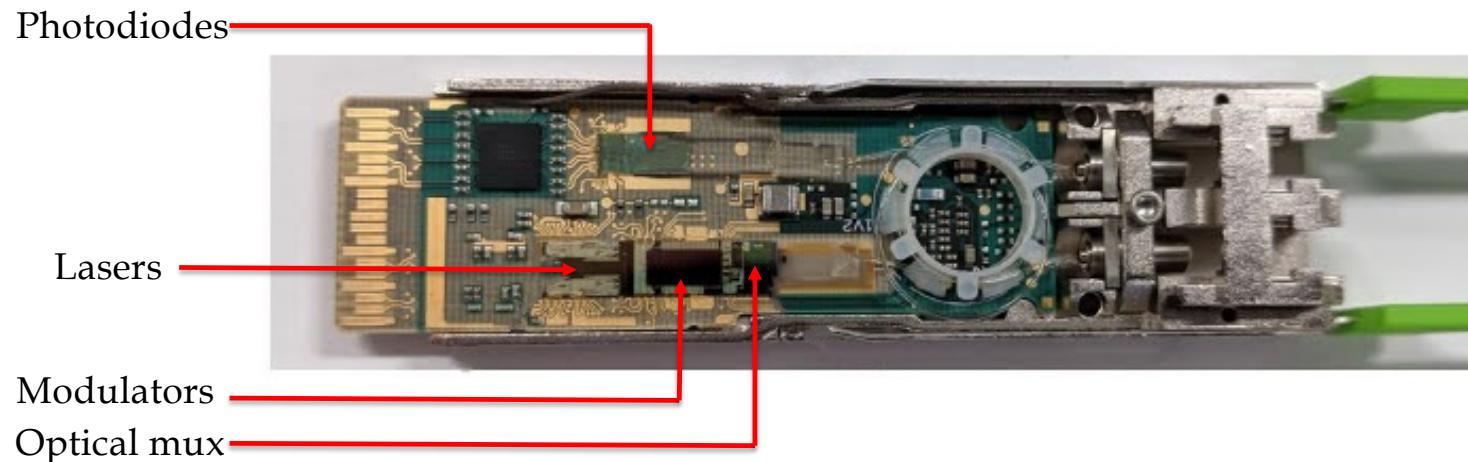


Lighting

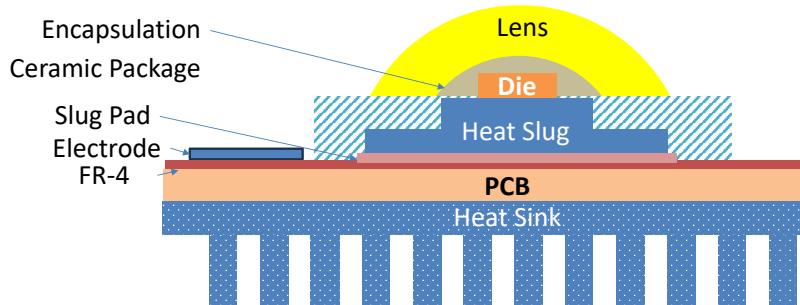
Each of these applications necessitates sophisticated co-packaged optics technology, which varies from chip-level to system-level packaging requirements.

Example 1: Photonics Transceiver Packaging

Intel's SiPh high volume transceivers 100G CWDM4 with no hermetic packaging.

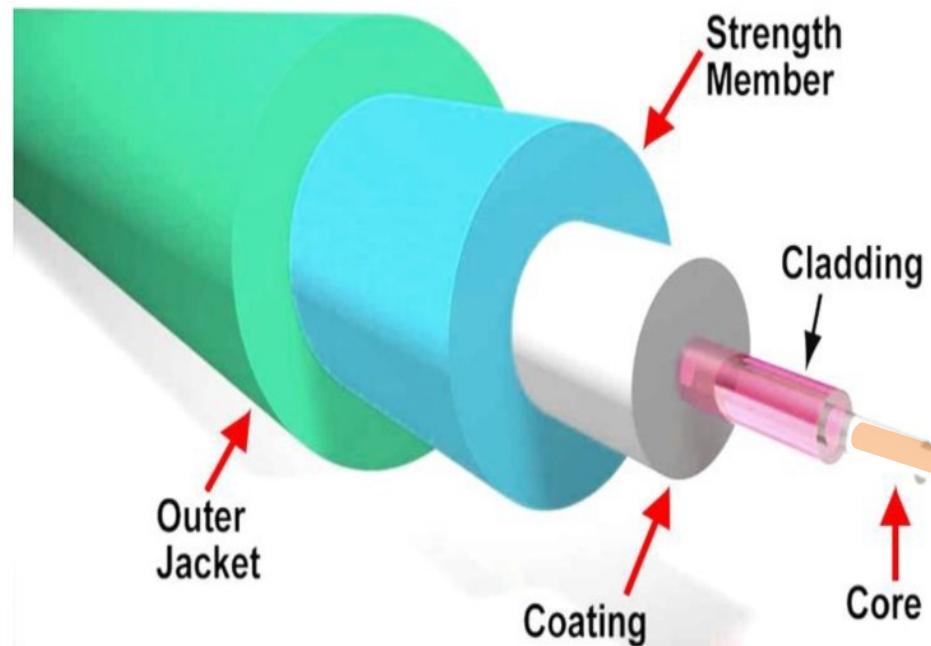


Example 2 : LED Packaging



LED Type	T-Pack	Surface Mount	Chip on Board
Device Image			
Packed Array (10mm x 10mm)			
Density	9 LEDs	40 LEDs	342 LEDs
Array Power	0.4 Watts	4 Watts	68 Watts

Example 3: Optical Fiber Packaging



Photonics Packaging Hierarchy & Examples

Chip Level

1. Laser Diodes
2. Photodetectors or Photodiodes
3. Electro-optic Modulators
4. LEDs (Light Emitting Diodes)
5. VCSELs (Vertical-Cavity Surface-Emitting Lasers)

Module Level

1. Optical Transceiver Modules
2. Arrayed Waveguide Gratings (AWG)
3. Optical Amplifier Modules
4. Micro-optic Modules
5. MEMS Optical Switch Modules

System Level

1. Fiber Optic Communication System
2. Passive Optical Networks (PON)
3. LIDAR Systems
4. Optical Interconnect Systems
5. Optical Metrology and Imaging Systems

Difference between Electronics and Photonics Packaging

Aspect	Electronics Packaging	Photonics Packaging
Primary Focus	Protect, interconnect, and thermal management of electronic components.	Protect, interconnect, thermal management of both electronic and optical components.
Signal Type	Electronic signals and their propagation through circuits. Bandwidth in Hz.	Both electronic signals and optical pathways, including light emission, transmission, and detection. Bandwidth in Hz for electronics and THz or nm for optics.
Material Choices	Based on electrical properties: conductivity, insulating properties, resistance to electromagnetic interference. Resistivity in $\Omega \cdot \text{m}$.	Cater to both electronic and optical requirements: transparency to certain light wavelengths while maintaining desired electronic properties. Refractive index for optics with $\Omega \cdot \text{m}$ for resistivity.
Additional Components	Does not usually include optical components.	Involves optical components like lenses, waveguides, filters, and fiber couplings.
Design Considerations	Does not focus on optical pathways or light interaction. PCB trace widths in mm.	Emphasizes on optical paths, refractive indices, optical losses, distortions, and precise optical alignments. Fiber core diameter in μm or waveguide dimensions.
Performance Sensitivity	Electrical parasitics; signal-to-noise ratio (SNR) in dB.	Optical losses; drastically affected by misalignments, especially in high-speed or high-resolution optical applications. Bit error rate (BER) and insertion loss in dB.

Photonic Packaging Fundamentals



Nature of Light

Basics of Light Propagation

Optical Interfaces

Wave Optics Concepts

Optical Losses in Materials

Optical Coupling

Modes and Multimode Propagation

Polarization

Thermal Effects on Optical Properties

Optical Testing, Reliability, and Characterization

Optical Design Considerations in Packaging

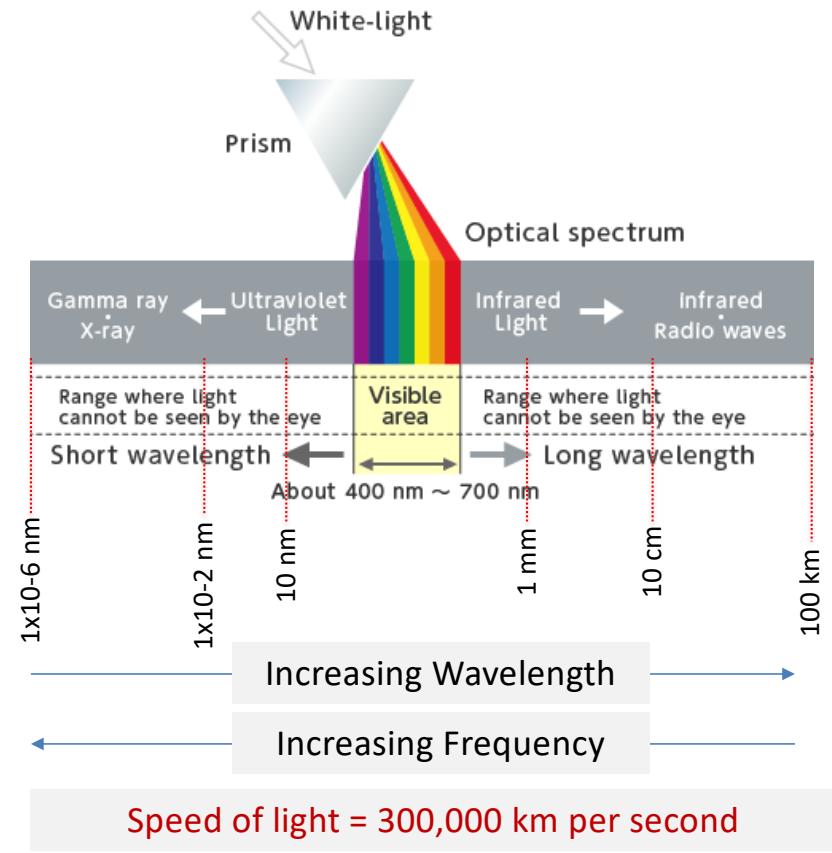
Nature of Light

The "**Nature of Light**" explores light's characteristics, such as its behavior across the electromagnetic spectrum, including the visible range, as well as its speed and properties that vary with wavelength and frequency.

Nature of Light

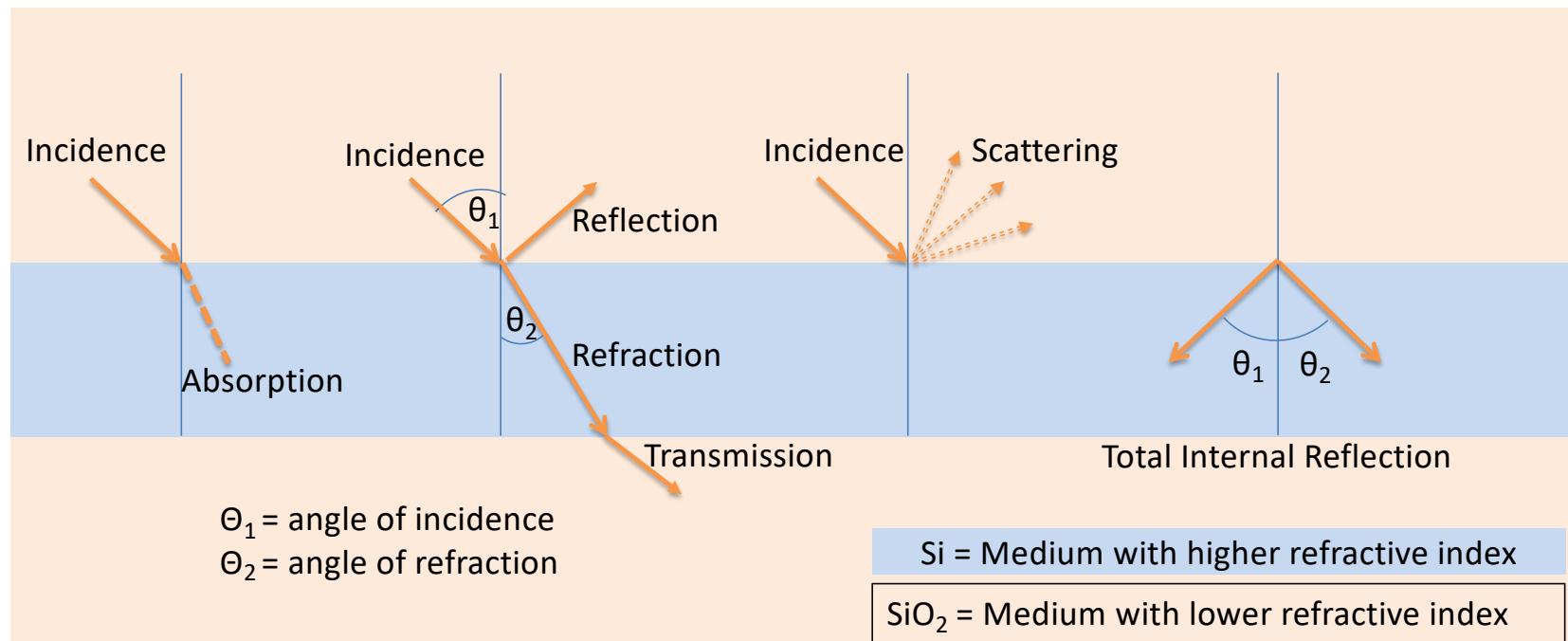


The electromagnetic waves emitted by the sun are of a broad spectrum ranging from X-rays with a wavelength of 2 nm to radio waves with a wavelength of 10 meters. The most intense of these to reach the earth's surface is visible light, with a wavelength around 500 nm.



Basics of Light Propagation

Basics of light propagation



Refractive Index

Refractive index is a ratio of the speed of light in a medium relative to its speed in a vacuum.

- **Refractive index of a bulk material is**
 - $n = \frac{1}{\text{Wave impedance}}$ for the light wave, relative to vacuum.
 - Wave impedance is the ratio of transverse components of electric and magnetic field

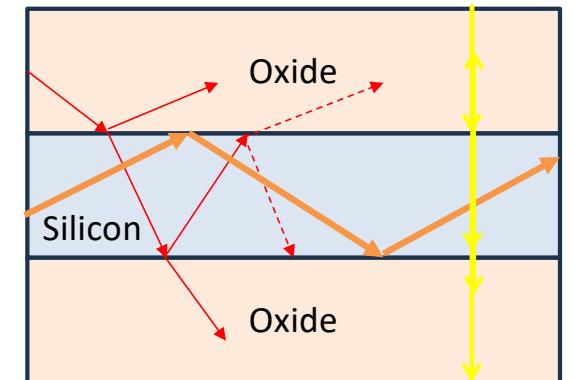
- **Reflections are caused by abrupt changes in n**
 - Slow (adiabatic) changes in refractive index (n) don't cause reflections
 - Abrupt changes in n also make off – angle light change direction (refraction)
 - Absorption also works the same way – abrupt changes in absorbance cause reflections

Material	n
Silicon	3.5
Nitride	2.0
Oxide	1.4-1.5

Optical Interfaces

Optical Interfaces and Relevance to Packaging

- **Refractive index and its impact on optoelectronic packaging**
 - Managing the change in light direction, or refraction, at the interface of two materials with different refractive indices is key for optimal performance.
- **Refractive index matching in materials to minimize reflection losses**
 - Mismatches can lead to reflection losses, reducing device efficiency.
- **Importance of anti-reflection coatings**
 - Anti-reflection coatings maximize light transmission and minimize reflection losses, ensuring optimal performance in photonics packaging



Paths taken by 3 incident rays

Wave Optics

Wave optics concepts and its relevance to Packaging

Characteristics	Relevance to Photonics Packaging
Rectilinear Propagation	Ensures accurate fiber-to-chip or chip-to-chip alignment in packages.
Absorption	Used in designing packaging materials that minimize unwanted absorption, improving signal integrity.
Reflection	Anti-reflective coatings in packaging interfaces to minimize back-reflections and increase transmission.
Refraction	Design of optical elements in integrated photonics packages, like lenses or waveguides.
Dispersion	Managing chromatic dispersion in multi-wavelength systems to ensure consistent packaging performance.
Interference	Thin-film interference coatings in packaging for wavelength selection or signal modulation.

Wave optics concepts and its relevance to Packaging

Characteristics	Relevance to Photonics Packaging
Diffraction	Grating couplers in packages for efficient light coupling between fibers and photonic chips.
Polarization	Polarization-maintaining packages to ensure consistent signal transmission in certain applications.
Photoelectric Effect	Ensuring compatibility between photodetectors in the package and external light sources or signals.
Modulation	Packaging for modulators must ensure efficient modulation and protection from external factors affecting it.
Coupling	Packaging designs incorporate lenses or structures to enhance coupling efficiency and alignment accuracy.
Evanescence Waves & Total Internal Reflection	Packaging must ensure conditions for total internal reflection are met and minimize undesired evanescent wave coupling.

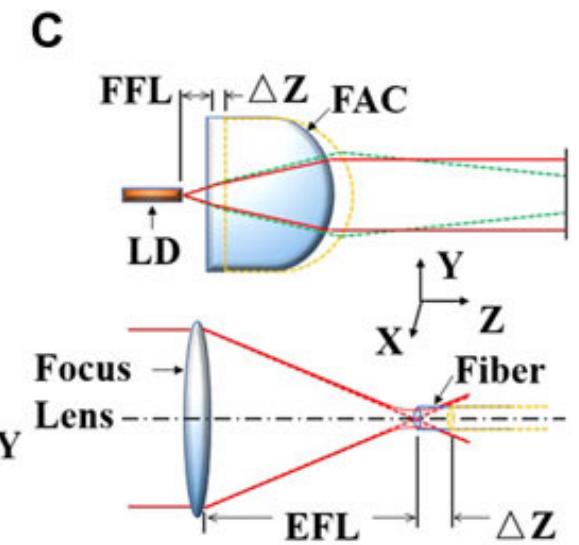
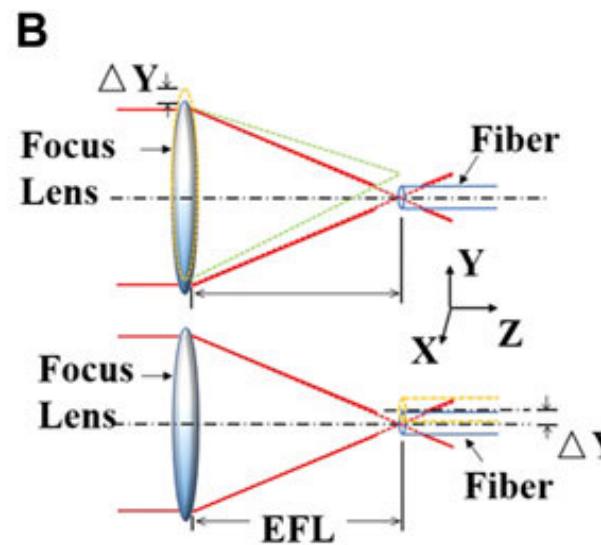
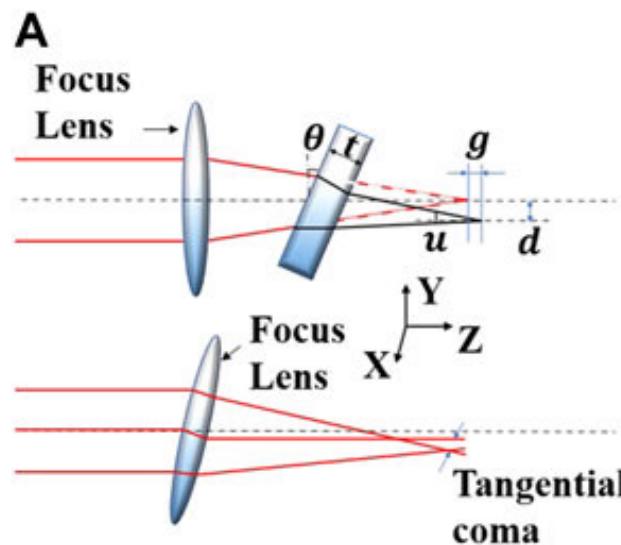
Optical Losses in Materials

Optical Losses in Materials

1. Optical Coupling Losses
2. Package – induced absorption
3. Back-Reflection (or feedback) losses
4. Scattering losses within the package

Optical Coupling

Optical Coupling: Loss due to optical component misalignment



Optical component in a semiconductor laser package include (1) collimator, (2) reflector, converging lens, fibers.

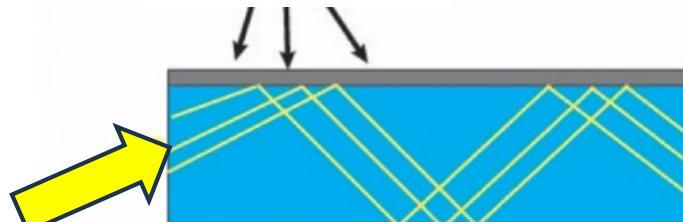
Types of optical components misalignment in a semiconductor laser package: (A) Tilt (rotation); (B) Decenter; (C) Defocus.

Mode and Mode Propagation

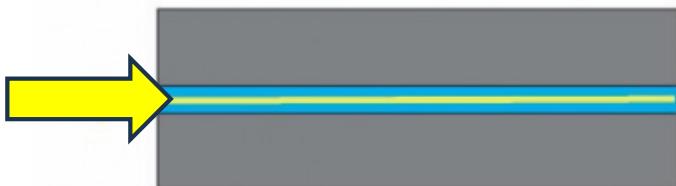
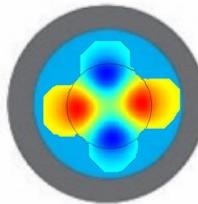
Mode propagation of light and its relevance to Packaging

- Spatial distributions of EM fields in waveguides and fibers with distinct field distribution and propagation constant.
- Selection of single mode or multimode propagation affects device design, alignment precision, and system metrics like bandwidth and dispersion.

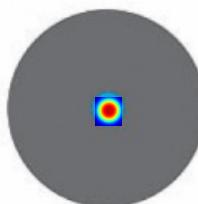
Different modes



Multi Mode Fiber (MMF)



Single Mode Fiber (SMF)



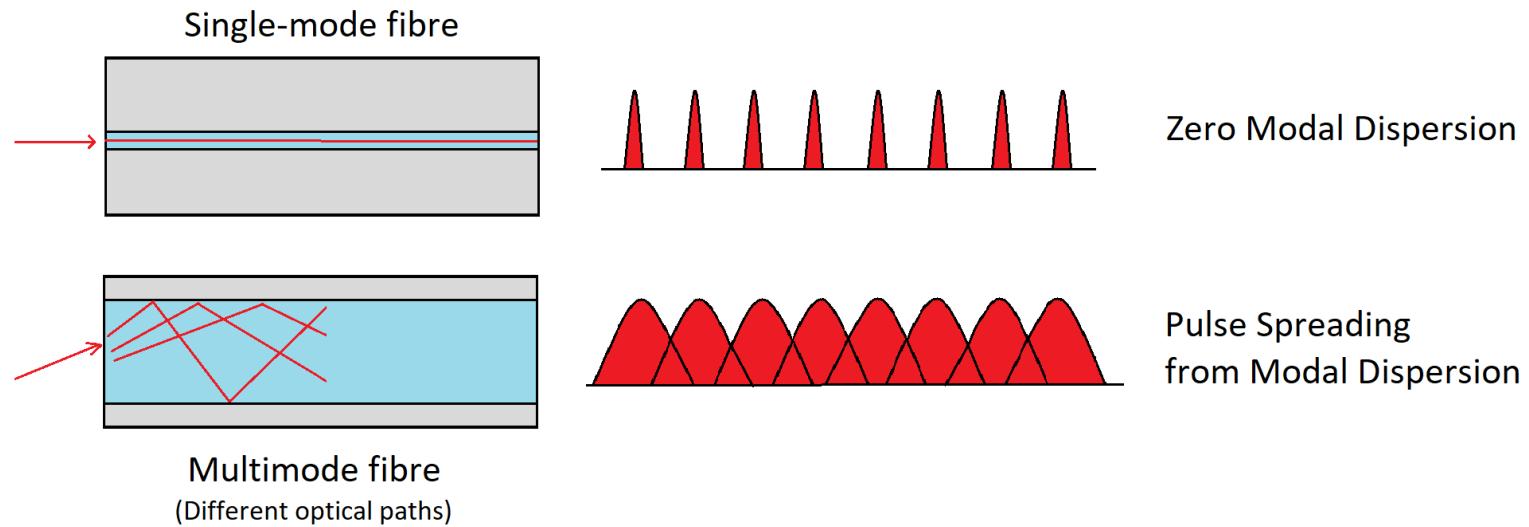
SMF Advantages:

- Minimum dispersion: all the modes (waves) take the same path, same time to travel through the waveguide. A pulse can be reproduced at the receiver very accurately. Less attenuation, therefore, can transmit over longer distance without repeaters
- Larger bandwidth and higher information rate

SMF Disadvantage:

- Difficult to couple light in and out of the tiny waveguide
- Highly directive light source is required

Modal Dispersion and relevance to Packaging



Topic	Description/Insight	Packaging Implications/Considerations	Examples
Modal Dispersion & Packaging	Different modes in multimode fibers propagate at varied velocities, resulting in pulse spreading.	Incorporate graded-index fibers in packaging to ensure all modes travel approximately the same distance, mitigating modal dispersion effects.	Graded index multimode fibers like OM3

MM and SM propagation of light & relevance to packaging

Topic	Description/Insight	Packaging Implications/Considerations	Examples
Intermodal & Intramodal Crosstalk	Interference where signals in one mode affect signals in another mode (intermodal) or within the same mode due to reflections (intramodal).	Packaging requires proper design of junctions, connectors, and splices. Utilization of specialized materials and advanced fabrication techniques.	Issues in dense wavelength division multiplexing (DWDM) systems due to crosstalk
Advanced Packaging Techniques	VCSELs & MMF: VCSELs, with broader emission profiles, are used with multimode fibers. Integrated Photonics: On-chip waveguides support varied modes.	Consider mode compatibility for VCSELs. Ensure efficient light transfer between on-chip and off-chip components for integrated photonics.	Use of VCSELs in high speed datacom applications; silicon photonics chips for integrated circuits

Polarization

Polarization describes the orientation of the oscillations of the electric field vector of an EM wave.

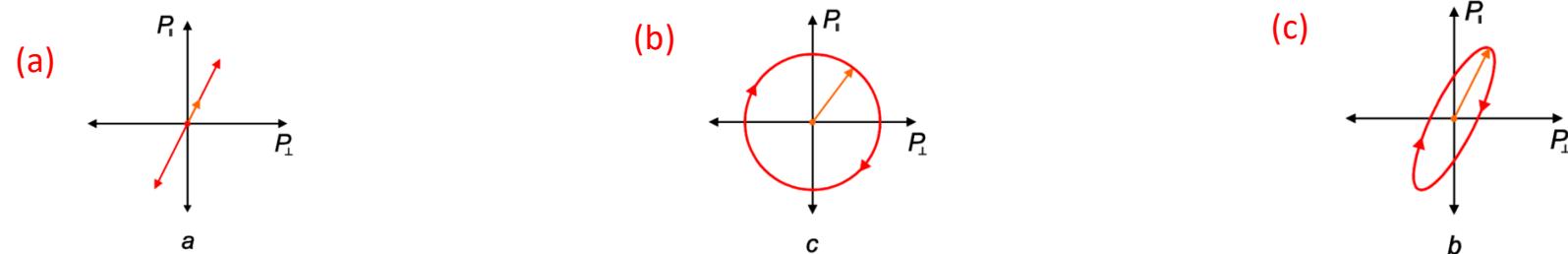
Polarization

Types of Polarization

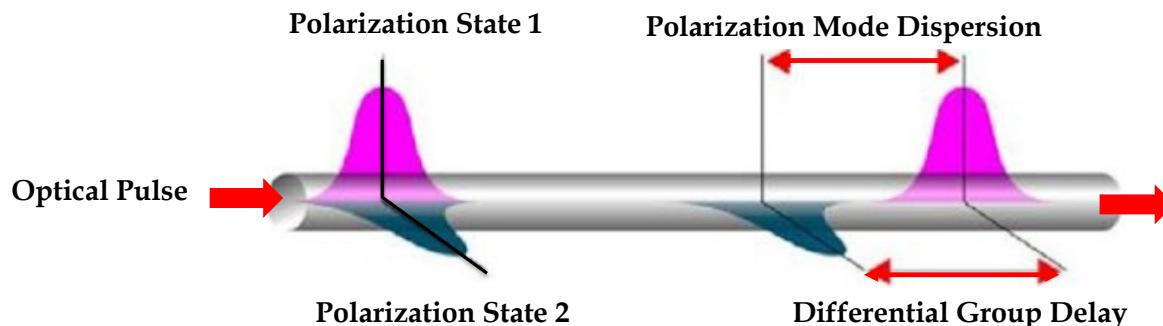
(a) Linear Polarization	Electric field oscillates in a single plane.
(b) Circular Polarization	Electric field oscillates in a circular manner, resulting from the combination of two linearly polarized waves 90° out of phase.
(c) Elliptical Polarization	General form where the electric field traces an ellipse over one period.

Polarization: Relevance to Packaging

Alignment & Coupling	Proper alignment is essential to ensure the intended polarization state enters or exits a device. Misalignment can lead to undesirable polarization losses.
Polarization Maintaining (PM) Packaging	PM components are designed to preserve the polarization state of light. Special considerations in packaging, often using stress-induced birefringence or geometric asymmetry.



Polarization Dispersion and relevance to Packaging



Polarization-Related Phenomena & Challenges

Polarization Mode Dispersion (PMD)	Phenomenon in optical fibers where different polarizations travel at different speeds, leading to pulse broadening. Relevant for long-haul communication systems.
Polarization Dependent Loss (PDL)	Variation in loss depending on polarization. In packaging, connectors, splices, or waveguides can introduce PDL.
Polarization Crosstalk	Unwanted coupling between different polarization modes, leading to interference.

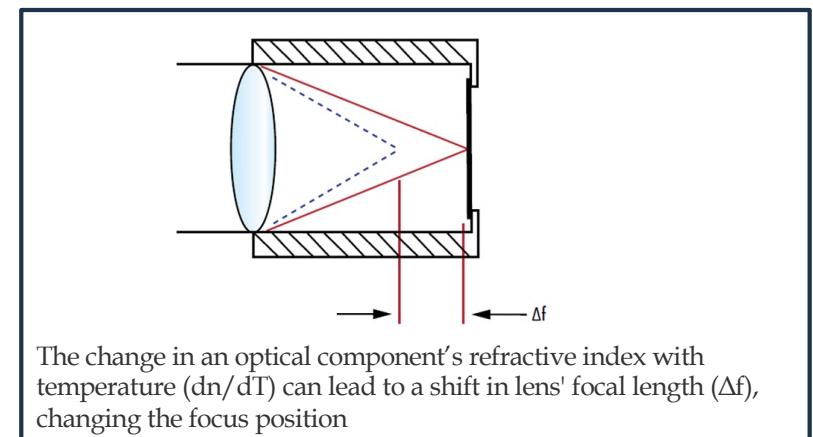
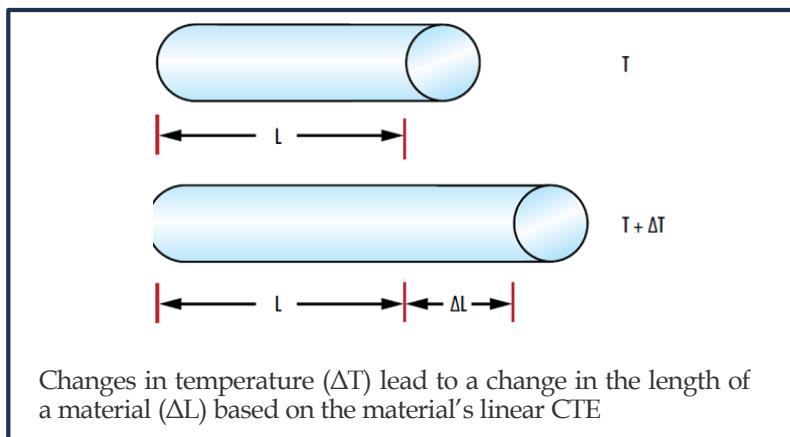
Practical Implications in Packaging

Material Selection	Materials with certain birefringence can change polarization; careful selection and orientation are crucial.
Thermal Considerations	Temperature changes can affect birefringence of materials, altering polarization. Packaging designs need thermal stability.
Mechanical Stress	Mechanical stress in packaging can induce unwanted birefringence, leading to unintended polarization changes.

Thermal Effects

Fundamental Understanding of Thermal Effects

- Thermal Expansion
- Refractive Index Change
- Bandgap Shift
- Nonlinear Thermal Effects
- Thermal Stress and Strain



Implications of Thermal Effects to Photonics Packaging

- Wavelength Shift in Lasers
- Performance Degradation
- Thermal Crosstalk
- Thermal Runaway

Packaging Solutions to Mitigate Thermal Effects

Thermal Management Effective heat sinks, thermoelectric coolers, and other cooling mechanisms are integral to optoelectronic packaging design to dissipate heat efficiently and maintain device performance.

1. High-conductivity ceramics
2. Thermal interface materials (TIMs)
3. Epoxy resins

Materials Choosing the right materials that have more stable optical properties can reduce the impact of thermal effects.

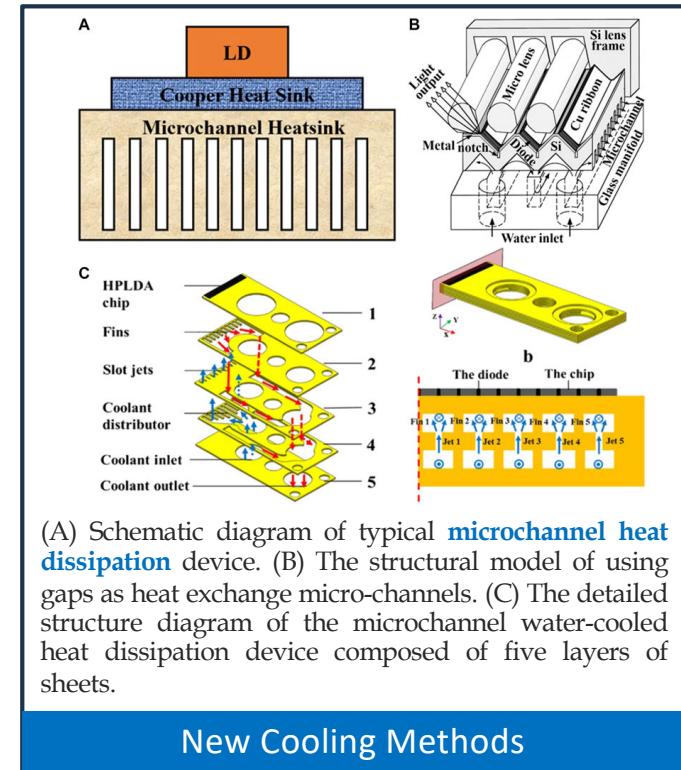
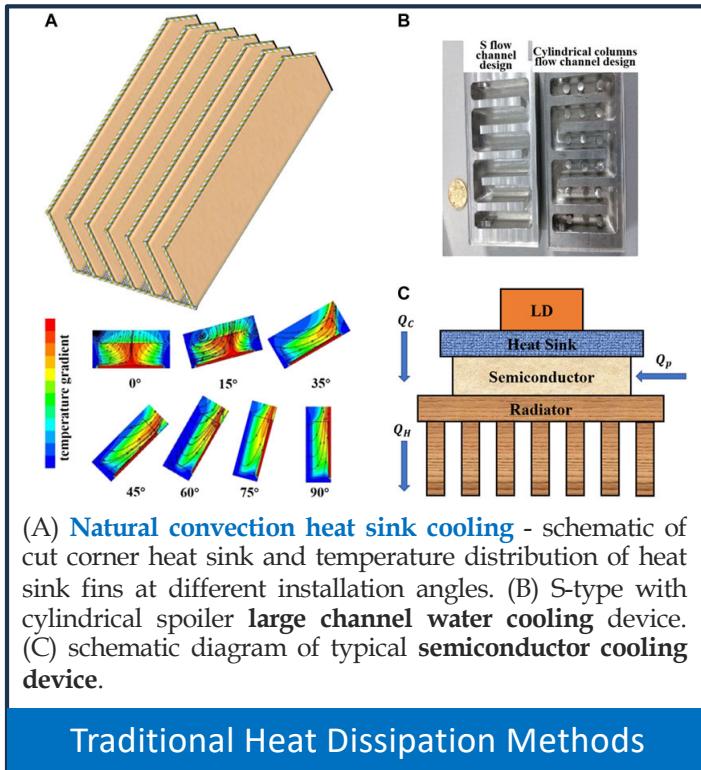
1. Low-outgassing epoxies
2. Silicone encapsulants
3. Glass or ceramic packages
4. Optical-grade polymers

Isolation Thermally isolating components from each other can prevent thermal crosstalk and maintain optimal temperatures.

1. Dielectric materials
2. Hermetic seals
3. Optical isolators

Example: High-Power Semiconductor laser packaging

Thermal Management solutions through design innovations



Materials in Optoelectronics Packaging

	Substrates	Encapsulants	Die Attach Materials	Packaging Glasses	Polymers
Opportunities	<ul style="list-style-type: none"> Platform for device mounting, interconnection, and heat dissipation. 	<ul style="list-style-type: none"> Protects the device from environmental factors. 	<ul style="list-style-type: none"> Strong bond between die and substrate. 	<ul style="list-style-type: none"> Superior optical clarity and stability. 	<ul style="list-style-type: none"> Versatility in engineering specific properties.
	<ul style="list-style-type: none"> Engineered for specific optical properties, enabling improved light manipulation. 	<ul style="list-style-type: none"> Enhances optical properties if designed appropriately. 	<ul style="list-style-type: none"> Offers thermal management capabilities. 	<ul style="list-style-type: none"> Robust environmental protection. 	<ul style="list-style-type: none"> Cost-effective and easier to shape compared to glasses.
Challenges	<ul style="list-style-type: none"> Must provide electrical and optical functionality. 	<ul style="list-style-type: none"> Potential for optical degradation over time. 	<ul style="list-style-type: none"> Avoid introducing optical impurities or scattering centers. 	<ul style="list-style-type: none"> Brittleness and potential for breakage. 	<ul style="list-style-type: none"> UV sensitivity and degradation potential.
	<ul style="list-style-type: none"> Maintain optical integrity under varying conditions. 	<ul style="list-style-type: none"> Maintain clarity and avoid yellowing with age. 		<ul style="list-style-type: none"> Handling and integration challenges. 	<ul style="list-style-type: none"> Varying thermal stability.
Difference from Electronic Packaging Materials	<ul style="list-style-type: none"> Requires transparency or specific refractive properties. 	<ul style="list-style-type: none"> Must be transparent and not interfere with device's optical function. 	<ul style="list-style-type: none"> Optical clarity and minimal light absorption are crucial. 	<ul style="list-style-type: none"> Specialty glasses with specific refractive indices or transmission properties. 	<ul style="list-style-type: none"> Need for specific optical properties such as transparency at certain wavelengths or light guiding.

Optical Testing, Reliability and Characterization

Optical Testing and Characterization

Both electronics and photonics packaging could share test capabilities, there are a few exclusive tools.

Packaging and Integration Characterizations:

- Alignment and Coupling Efficiency
- Thermal Testing
- Mechanical and Environmental Testing
- Optical backscatter reflectometer (OBR)

Optical Measurements

- Power and Energy Measurements
- Wavelength Measurements
- Optical Signal-to-Noise Ratio (OSNR)
- Bit Error Rate (BER) Testing

Device Level

- Laser Diode Testing
- Photodetector Characterization
- Optical Amplifier Characterization
- Optical Filter and Multiplexer Testing

Advanced Testing Techniques

- Interferometry
- Polarization Measurements
- Time-Resolved Measurements
- Phase Measurements

Reliability and Testing

Ensuring the long-term performance and reliability of optoelectronic components & circuits is critical due to their usage in critical applications such as telecommunications, medical diagnostics, and sensing. E.g., Fiber-optic connections in undersea cables that require high reliability due to the difficulty and expense of repair (Sensitivity to environmental factors - Humidity causing condensation, temperature affecting efficiency, Mechanical stresses - Stress leading to optical misalignment, Material degradations - Prolonged exposure to light degrades materials)

Category	Testing Methodology
Environmental Testing	<ul style="list-style-type: none"> • Temperature cycling • Humidity Testing • Vibration Testing • Mechanical Shock
Optical Testing Methodologies	<ul style="list-style-type: none"> • Optical Power Measurement • Wavelength and Spectrum Analysis • Optical Alignment and Coupling Efficiency
Endurance and life testing	<ul style="list-style-type: none"> • Assessing the longevity and performance retention of devices over extended usage
Electrical Testing Methodologies	<ul style="list-style-type: none"> • Current-Voltage, capacitance, impedance at various frequencies
Failure Analysis	<ul style="list-style-type: none"> • Techniques such as Electron microscopy

Packaging Design Considerations

Package Designs and Configurations

	Surface Mount Devices	Through-Hole Devices	Chip-on-Board	Ball Grid Arrays (BGA)	Other Configurations
Examples	<ul style="list-style-type: none"> • Photodiodes, • LEDs, • phototransistors. 	<ul style="list-style-type: none"> • Traditional LED indicators, • certain phototransistors. 	<ul style="list-style-type: none"> • High-intensity LED light engines, • arrays of photodiodes. 	<ul style="list-style-type: none"> • Advanced optoelectronic transceivers, • integrated optoelectronic modules 	<ul style="list-style-type: none"> • OptoBGA, Chip-on-Glass (COG), • Ceramic packages with windows
Configurations	<ul style="list-style-type: none"> • Mounted directly onto PCBs • Compact, high-density • Clear or diffused packaging 	<ul style="list-style-type: none"> • Leads penetrate the PCBs • Solder to Pads on the opposite side • Clear or diffused packaging 	<ul style="list-style-type: none"> • Chip attached to the board • Wire-bonded connection pads • Improves thermal performance 	<ul style="list-style-type: none"> • Dense array of connection points • Electronic and optoelectronic integration • Maintains optical pathways 	<ul style="list-style-type: none"> • Specialized packaging for optical components • Includes windows, lenses, waveguides • Balances connectivity, thermal management
Differentiation from Electronics Packaging	<ul style="list-style-type: none"> • Clear or diffusive encapsulation • May include lenses for focusing • Prevents optical crosstalk 	<ul style="list-style-type: none"> • Requires critical positioning and alignment • Transparent or diffusive materials 	<ul style="list-style-type: none"> • Preserves optical signal integrity • Thermal management for high-power LEDs • Uses silicone lens for shaping light 	<ul style="list-style-type: none"> • Incorporates optical interfaces like lenses • Prevents interference between optical and electrical pathways 	<ul style="list-style-type: none"> • Seamless integration of optical and electrical • Considerations for thermal management, signal integrity, and crosstalk

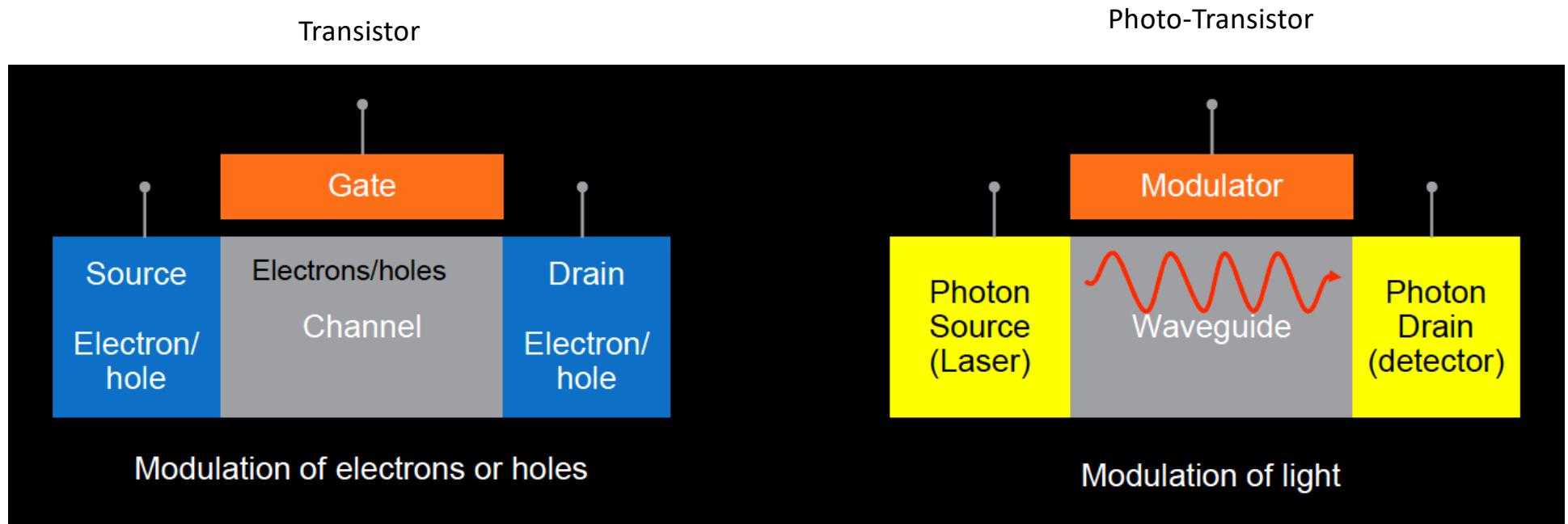
Advanced Packaging Techniques

Packaging Technique	Overview	Examples
Wafer-Level Packaging (WLP)	Method where packaging is done at the wafer level before dicing. Suitable for high-volume, low-cost applications	semiconductor components such as LED arrays, VCSELs, with efficient manufacturing.
3D Packaging	vertically stacking of chips or wafers, and interconnecting them for high density and performance	Stacking photodetector layers on electronic amplification layers; advanced ROIC circuits
MEMS Packaging in Optoelectronics	Packaging for MEMS integrating optical components. Requires alignment precision and controlled atmosphere	MEMS-based optical switches with microscopic mirrors.
Photonic Component packaging	Tailored packaging for integrated photonic components such as lasers, detectors, or modulators.	Silicon photonics component packaging with specialized alignment techniques.
PIC Packaging/ Integrated Photonic System packaging	Packaging for PICs with multiple photonic functions. Requires careful alignment of fibers or waveguides to the PIC components, thermal management, electrical drivers etc.	Multi-channel transceivers in data centers with advanced packaging techniques.
Flip-Chip Packaging	Chip/die is flipped and bonded to the substrate.	High-speed laser diodes with reduced inductance.
Flexible and Stretchable Packaging	Techniques for flexible optoelectronic devices.	Flexible OLED displays in wearables.
Panel-Level Packaging	Evolution of WLP, packaging performed on large panels.	Large-scale production of photonic devices like ambient light sensors.

PIC Packaging

- Introduction to PIC packaging
- Fiber Integration
- Laser Integration
- Interposers
- Assembly
- Summary

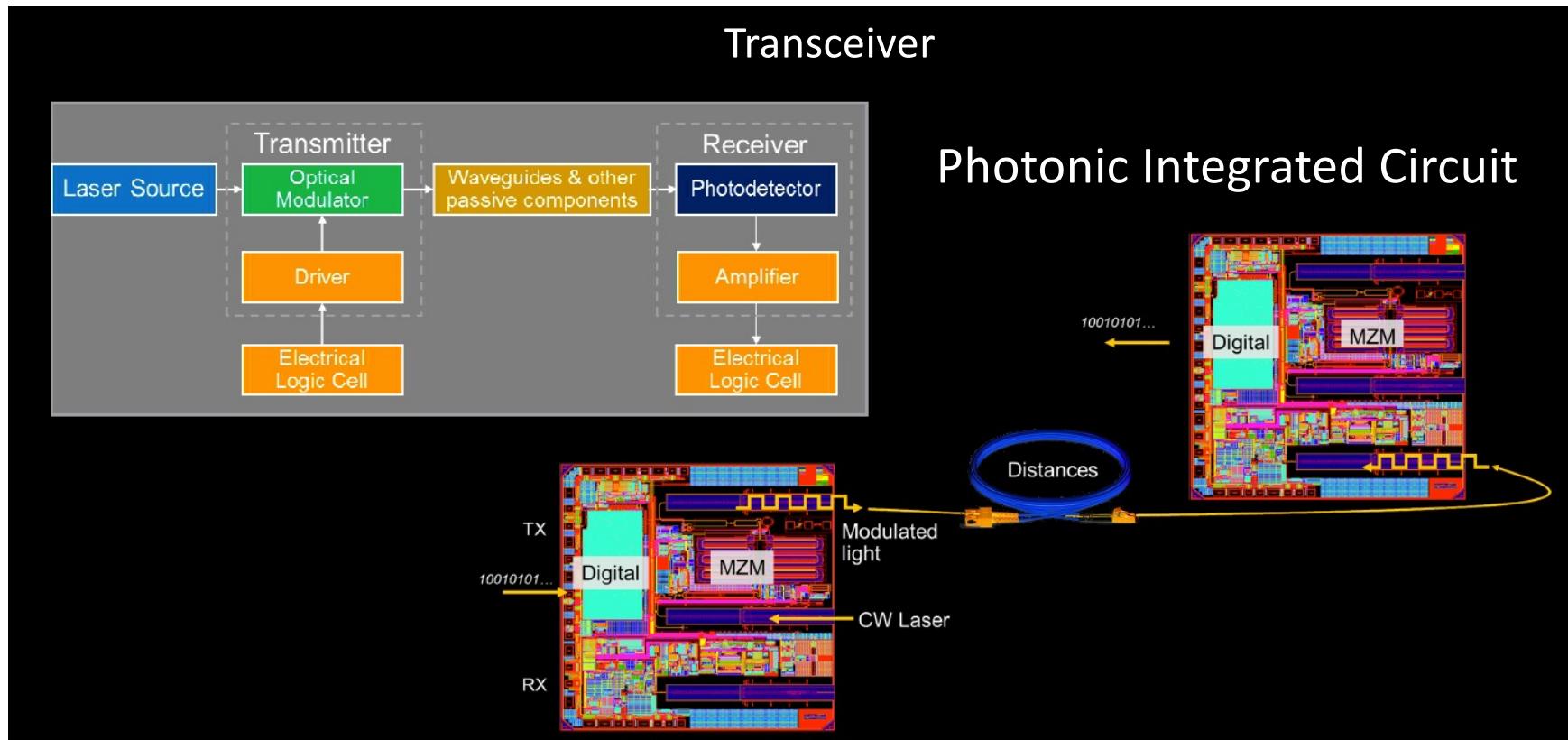
Fundamental building blocks of electronics and photonics looks similar



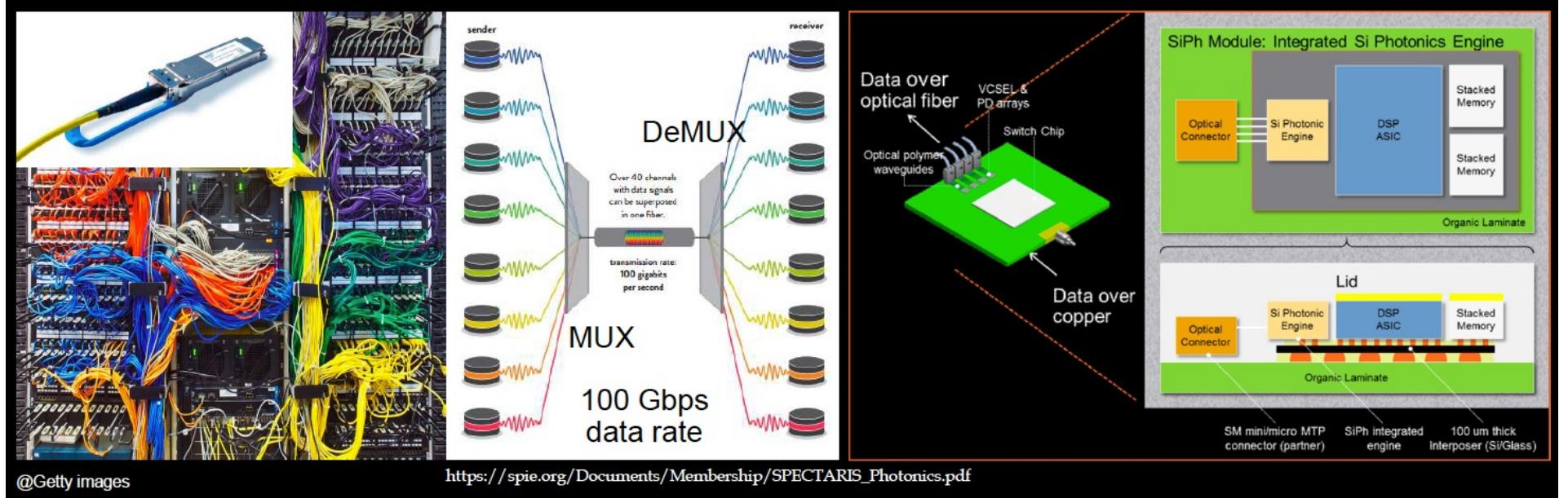
Intelligent interconnect of each of the transistor
builds an electronics integrated circuit

Intelligent interconnect of each of these photonic
components builds a photonic Integrated circuit

Photonic Integrated Circuit



System design and Packaging



- Photonics Integrated chips (PIC) helps us transfer data to the server and access data from the servers (cloud)
- Dozens of data signals can be coupled in one single optical fiber and be separated again at the receiver end.
- The signal can be very finely distinguished by their wavelength (spectral color), polarization, and phase
- 1310 nm Inter-Data Center QSFP+ module (shorter distances)

PIC integration schemes: Packaging Challenges

Hybrid Silicon Photonics



Alignment precision, thermal management, increased assembly complexity, cost, and sensitivity to environmental factors.

Monolithic Silicon Photonics



Ensuring thermal dissipation, mechanical stability, environmental protection, and maintaining integrity of sensitive components.

Heterogeneous Silicon Photonics



Integration of dissimilar materials, interface quality, thermal expansion mismatches, and complex assembly processes.

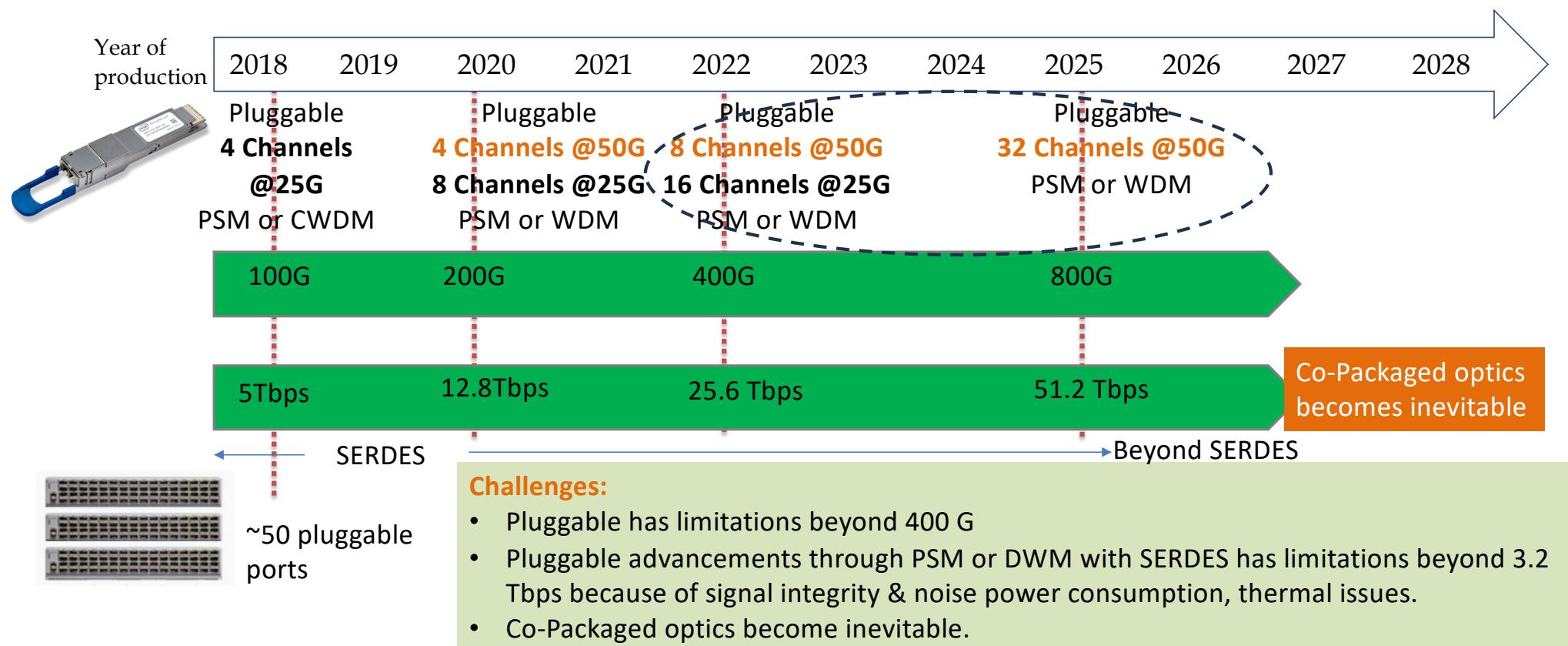
Fully Monolithic Silicon Photonics



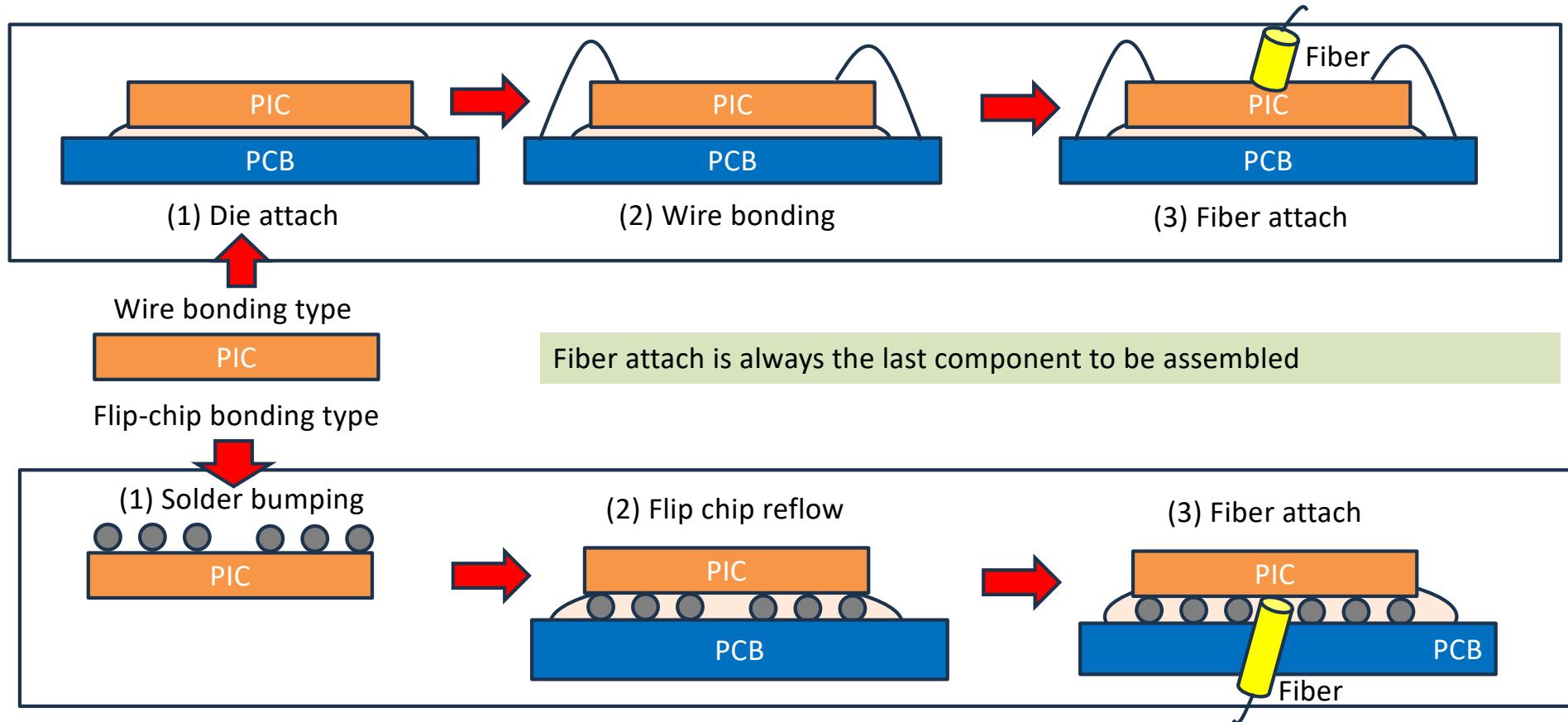
Advanced thermal management solutions, environmental sealing, stress management, and long-term reliability of the dense package.

- A.P.Jacob, 2020 IEEE 70th Electronic Components and Technology Conference, June 3 – June 30, 2020
- A. P. Jacob et. al., Photonic-integrated circuit fabrication and test approaches, in Integrated Photonics for Data Communication Applications, Elsevier (2024)

Silicon Photonics System Research Roadmap

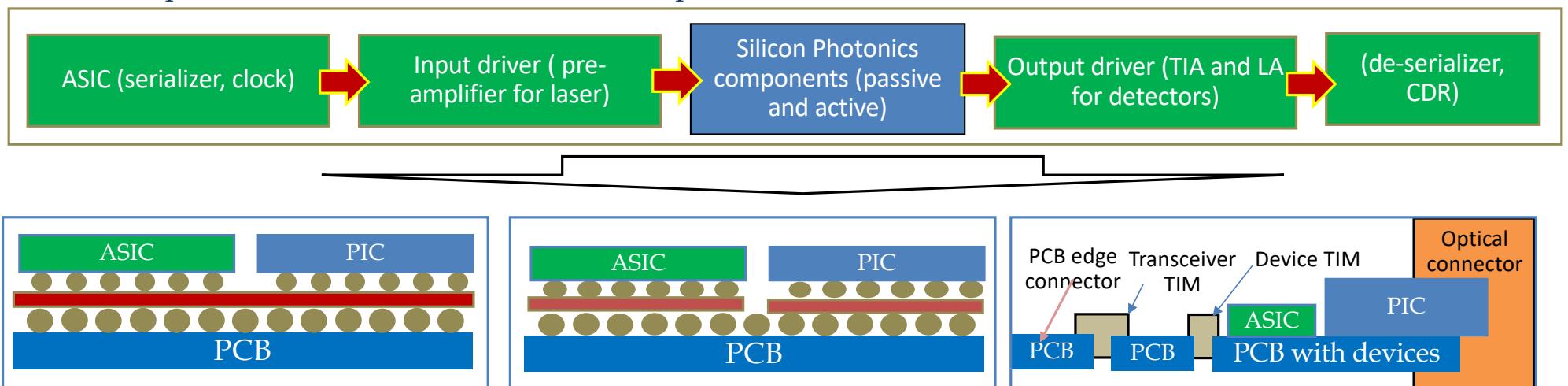


Generic Packaging flow for PIC devices



MCM OE, Mid board AOC and Pluggable CXP are few solutions currently available to meet the demand (optical link)

An optical link consists of electronics and optics



Optically enabled multi chip module (MCM-OE) – Fiber interconnect solution using SiPh

- Interposer type on the PCB; higher density

Mid-board – Active optical cables (AOC) - edge of the board (EOB)

- Flexibility in switching between Cu and optics
- Thermal dissipation can be contained

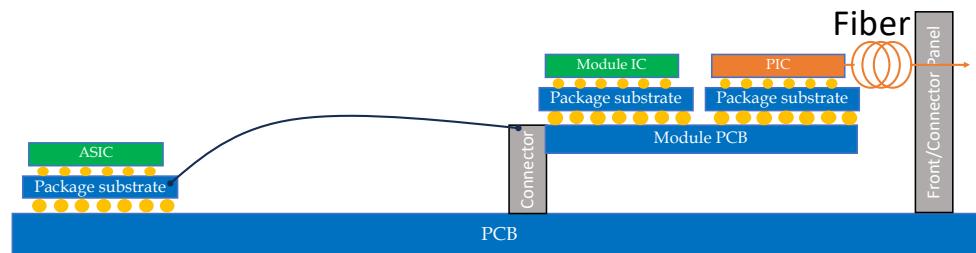
Pluggable transceiver modules = edge of the board (EOB)

- Small form factor
- Low cost

Optical I/O Solutions

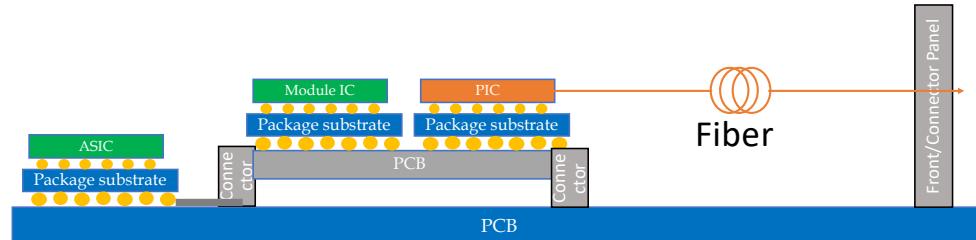
1990's

Pluggable optics



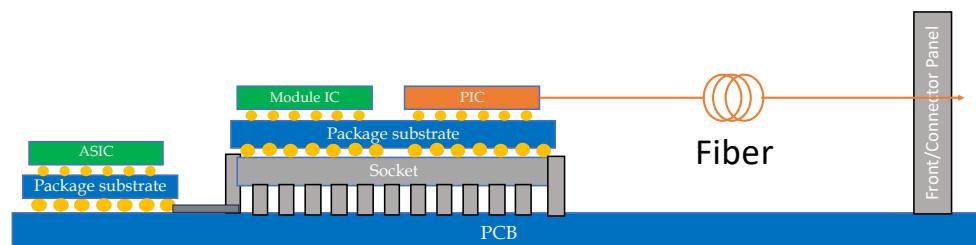
2010's

On-board optics (OBO)



2010's

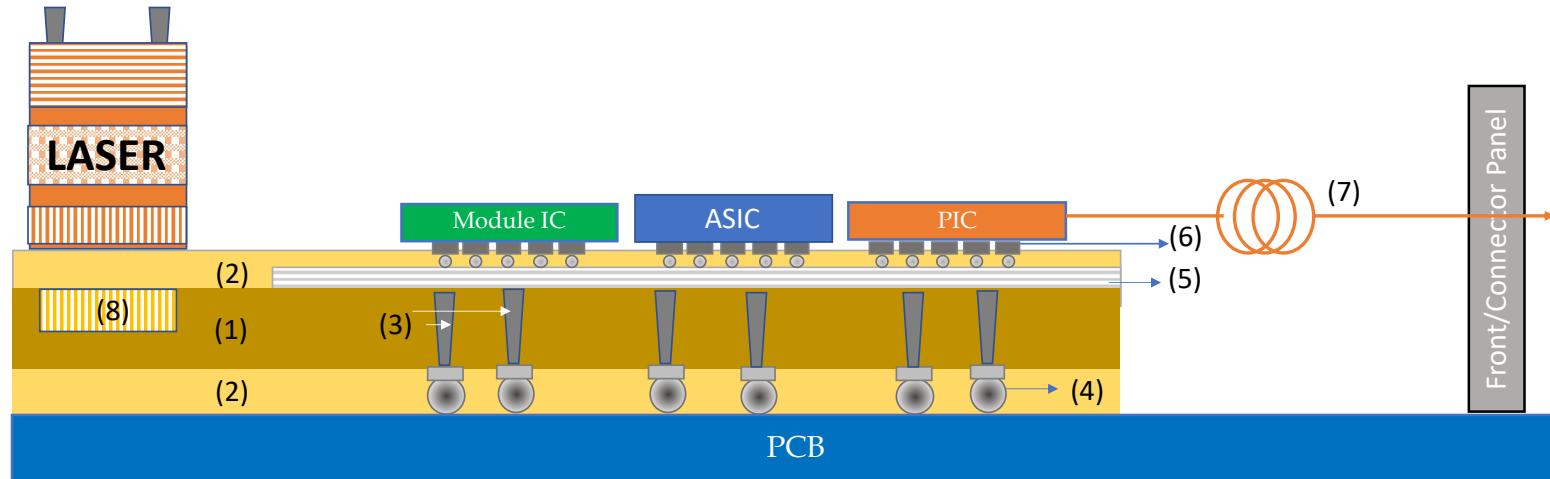
Near Package optics (NPO)



Challenges:

1. High speed and advanced modulation techniques
2. Power consumption and Heat Dissipation
3. Signal Integrity and Link Performance
4. Cost and Complexity
5. Technology Evolution and Compatibility

2.5 D Heterogeneous Integration: Co-packaged Optics



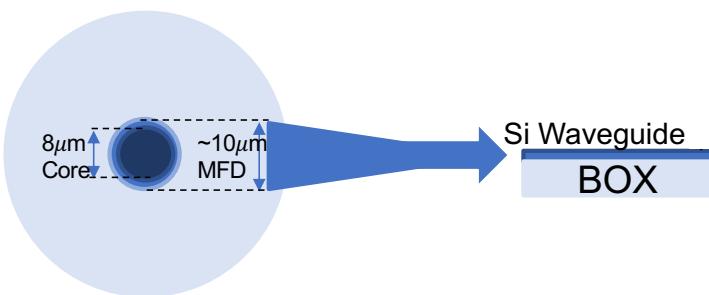
(1) Silicon Photonics Interposer, (2) underfill, (3) Through silicon via (TSV), (4) Solder Bumps, (5) RDL redistribution and communication layers (6)Copper bumps, (7) optical fiber I/O, (8) Grating coupler

- CPO integration options:
 - Multi-Stage vs Single Stage CPO
 - Single stage CPO is simple, single package, high speed, low-latency, and high-density optical communication within a compact form factor. Multistage is integration flexible, scalability, modularity
 - 3D CPO, integrated laser CPO – LUMOS project from DARPA

Fiber Integration

Optical I/O - PIC coupling Fundamentals

- Large Refractive Index contrast between Silica (1.444) and Silicon (3.47).
- Mode Mismatch Mode Area SMFs ($50\mu\text{m}^2$) vs Silicon Waveguides ($400\text{nm} \times 220\text{nm}$) ~ 600 times
- Optical coupling: for efficient transfer of optical energy from one component to another, their respective mode profiles should overlap as much as possible.
- Insertion Loss: efficiency with the power is transferred from one optical component unto another component.

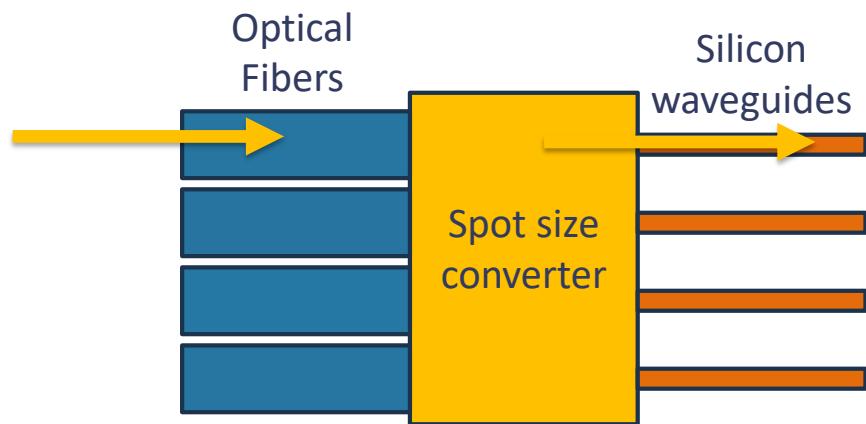


MFD = Mode Field Diameter

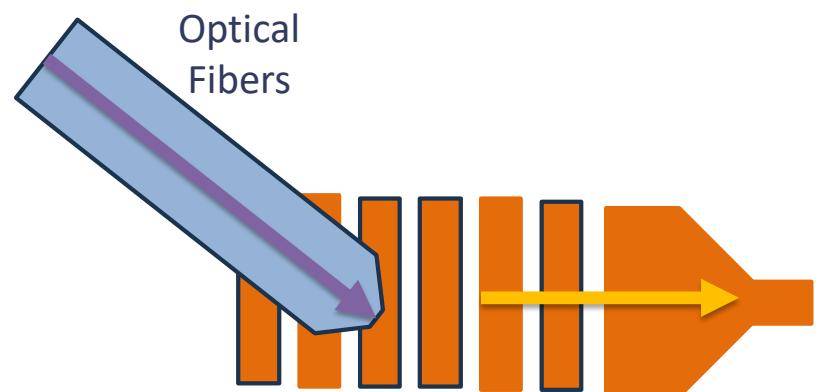
$$IL [dB] = -10 \log_{10} \frac{P_2}{P_1}$$

P1 = input power
P2 = output power

Popular Fiber Coupling Techniques



Edge Coupler



Grating coupler

Comparing in-plane vs out of plane couplers

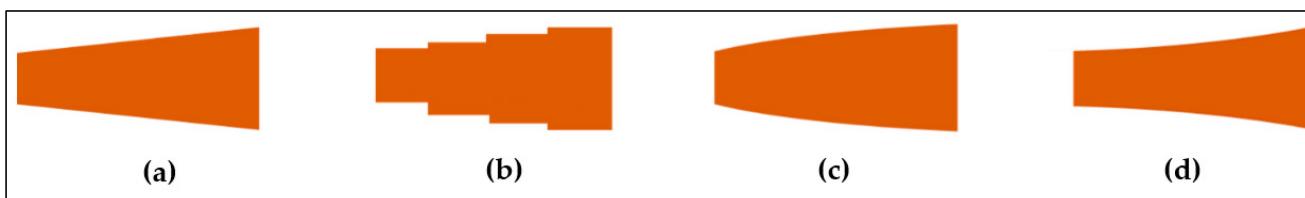
Feature	In-Plane Coupling	Out-of-Plane Coupling
Direction	Along the plane of the chip (sideways)	Perpendicular to the plane of the chip (upwards)
Waveguide Alignment	Precise lateral and vertical alignment required	Less strict alignment; wider tolerance for angles
Coupling Technique	Butt-coupling or tapered waveguides	Grating couplers or mirrors
Efficiency	Can be very high with optimal alignment	Generally lower due to scattering and reflection
Alignment Sensitivity	Sensitive to lateral misalignment	More tolerant to misalignment
Ease of Use	Challenging for frequent connections	Easier for frequent connections and disconnections
Design Complexity	Simpler design for the coupling interface	More complex design due to grating/mirror patterns
Typical Application	Permanent connections in devices	Testing and characterization of PICs
Polarization Dependency	Highly polarization-dependent; requires careful design to manage polarization issues	Typically designed to be polarization-independent or less sensitive to polarization changes
Bandwidth	Limited by the mode size and refractive index contrast; can be broad with optimized waveguide design	May be limited by the bandwidth of the grating coupler design; can be broadened with apodization or other design techniques

* note: Fiber could be coupled to a grating coupler vertically or horizontally (using mirrors)

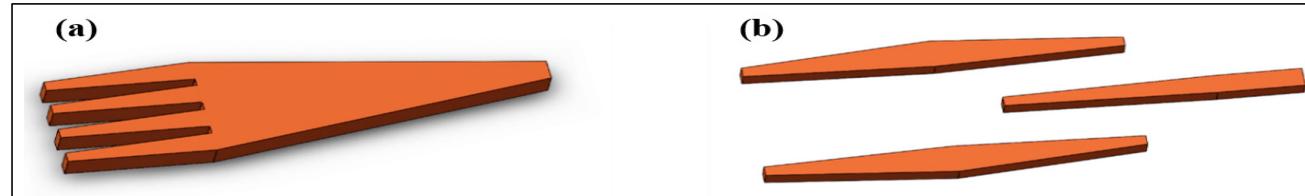
Comparing different Optical I/O Coupling Schemes

Coupling Scheme	Alignment Tolerance	Insertion Loss (dB)	Return Loss (dB)	Fabrication Complexity	Remarks
Butt Couplers	Low	3 - 7	40 - 50	Low	High precision required for alignment; mode mismatch issues
Inverse Tapers	Medium	1 - 3	30 - 50	Medium	Better mode size matching; moderate alignment precision
Surface-Emitting Gratings	High	3 - 6	20 - 30	Medium-High	Easier fiber alignment; sensitive to vertical displacement
Edge-Emitting Gratings	Medium-High	1 - 5	30 - 40	High	Combines edge coupling with easier alignment
Through Silicon Vias (TSVs)	N/A	3 - 10+	N/A	Very High	Used for 3D integration; complex fabrication
Fiber Tapers	High	0.5 - 2	40 - 60	High	Very low loss; fragile and precise tapering needed
Micro-Lenses	Medium	1 - 4	30 - 45	High	Less critical alignment; complex lens design
Prism Couplers	Low	1 - 4	40 - 55	Medium	Good efficiency; precise alignment necessary

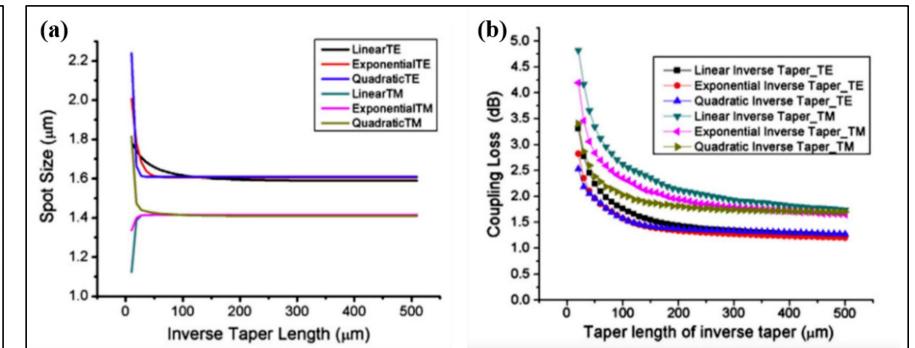
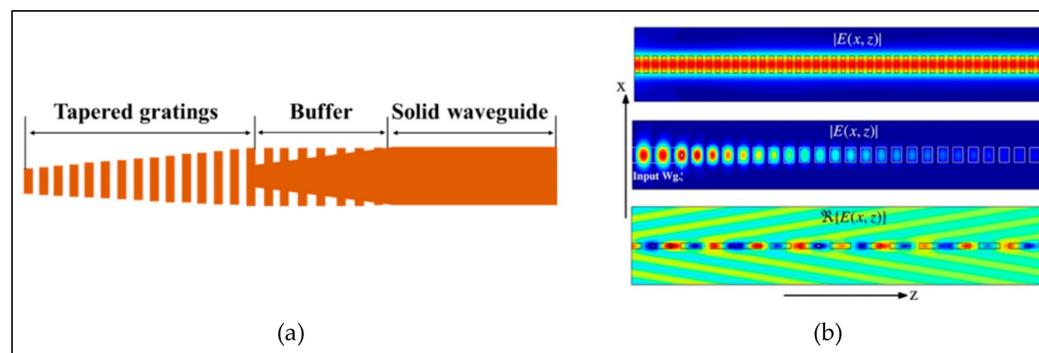
Spot Size converters - Edge Couplers



Schematic of the (a) linear; (b) multi-sectional; (c) parabolic; and (d) exponential Si inverse tapers (top view).

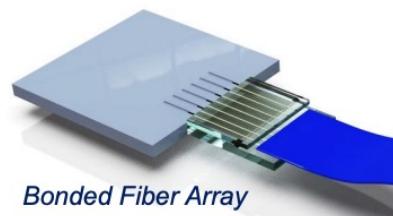
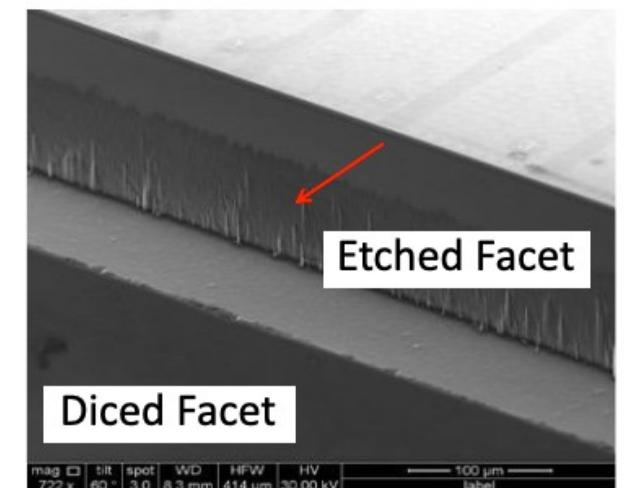
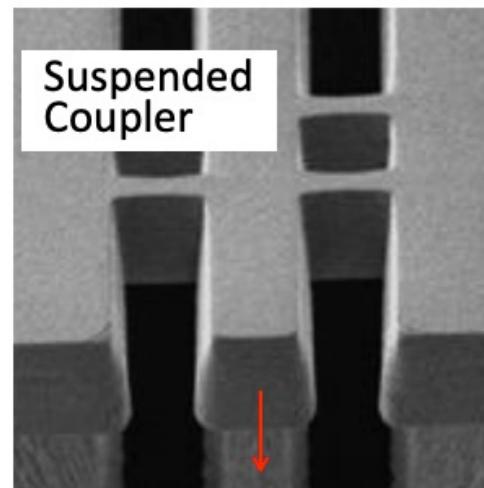
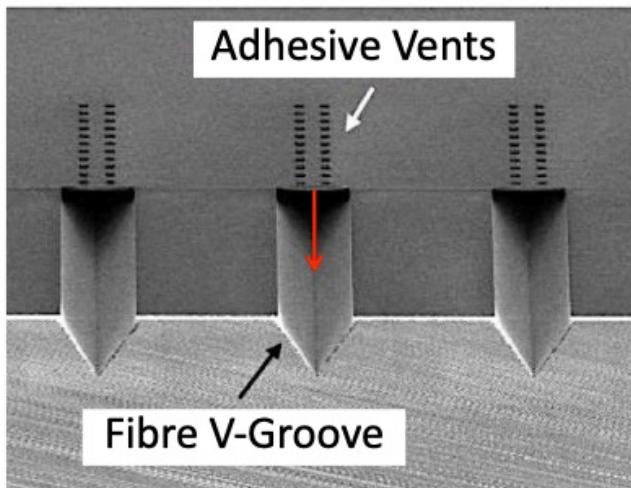


(a) a multi-tip taper and (b) multiple tapers.



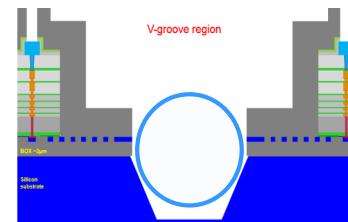
Subwavelength gratings

Silicon Edge Couplers

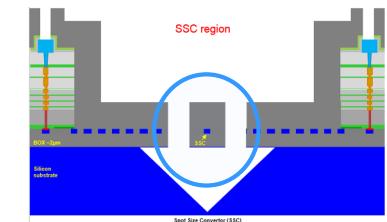


Example 1: Edge Coupler Integration

- V-groove etch in handle substrate for passive fiber alignment
- 3 stage spot converter for mode transition between SMF `10um mode and SOI SM waveguide
- Advanced lithography and OPC for optical coupling



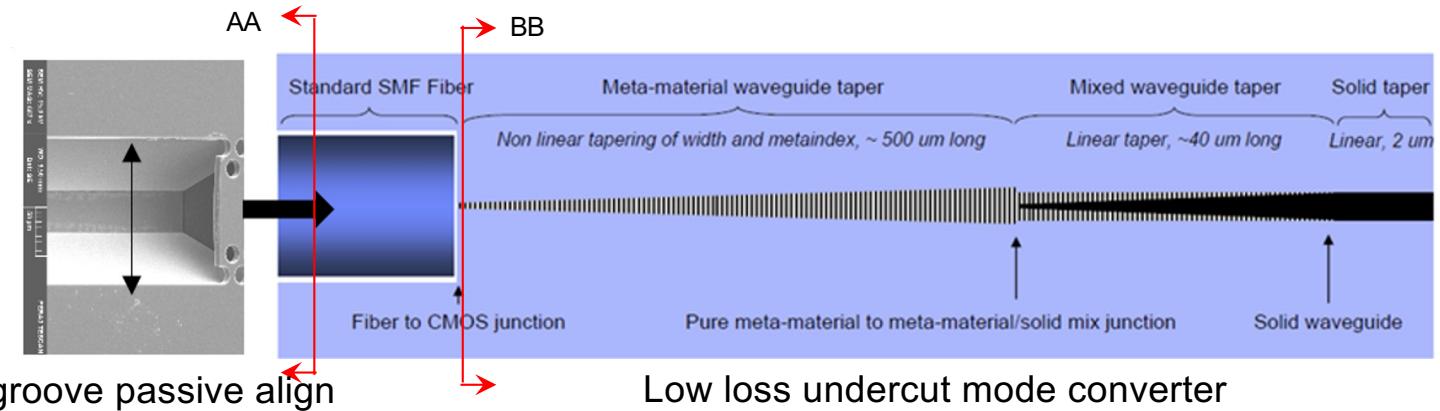
Section view AA



Section view BB

V0.9 IOSMF Design	TE IL (dB)	TM IL (dB)	TE ORL (dB)	TM ORL (dB)
Low PDL (RX in)	-1.3	-1.5	-18	-30
Low ORL (Laser in TX out)	-0.9	NA	-30	-30

- Layout can be optimized for low PDL, use for RX input &
- optimized for low ORL, use for laser input, and TX output
- Moisture Barriers

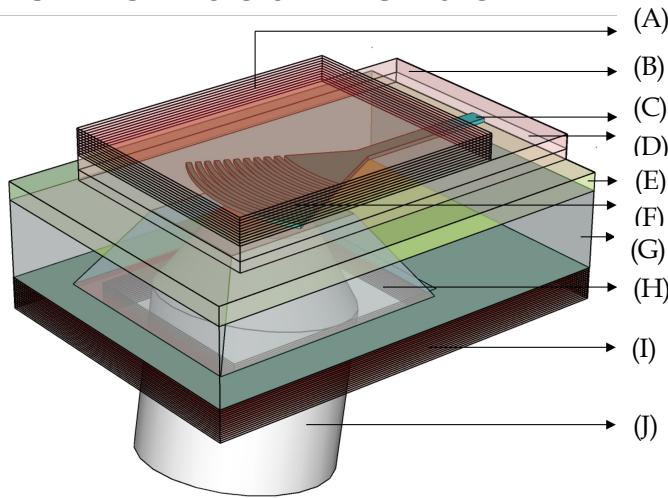


Comparing different Spot Size Couplers (SSC)

Spot Size Converter (SSC) Type	Conversion Principle	Typical Insertion Loss (dB)	Alignment Tolerance	Fabrication Complexity	Remarks
Tapered Waveguides	Adiabatic mode expansion	0.5 - 2	Moderate to high	Moderate	Simple design, but requires precise fabrication
Inverse Tapers	Adiabatic mode expansion	0.5 - 1.5	Moderate	Moderate	Shorter taper length compared to regular tapers
Lensed Fibers	Mode field shaping	0.3 - 1	High	N/A (fiber side)	High coupling efficiency; expensive fiber processing
Fiber to Waveguide Grating	Grating coupling	1 - 3	High	High	Facilitates out-of-plane coupling; complex design
Vertical Tapers	3D mode expansion	1 - 2	Moderate	High	Good for vertical integration schemes
Mode Expansion Sections	Gradual mode expansion	0.2 - 1	Moderate	Moderate	Requires extra chip space
Multimode Interference (MMI) Couplers	Interference based mode expansion	0.2 - 0.8	High	Moderate	Low loss; polarization dependent
Plasmonic SSCs	Metal-dielectric interface	1 - 4	Moderate	High	Useful for sub-wavelength mode sizes

Example 2: Backside Optical Coupler Design

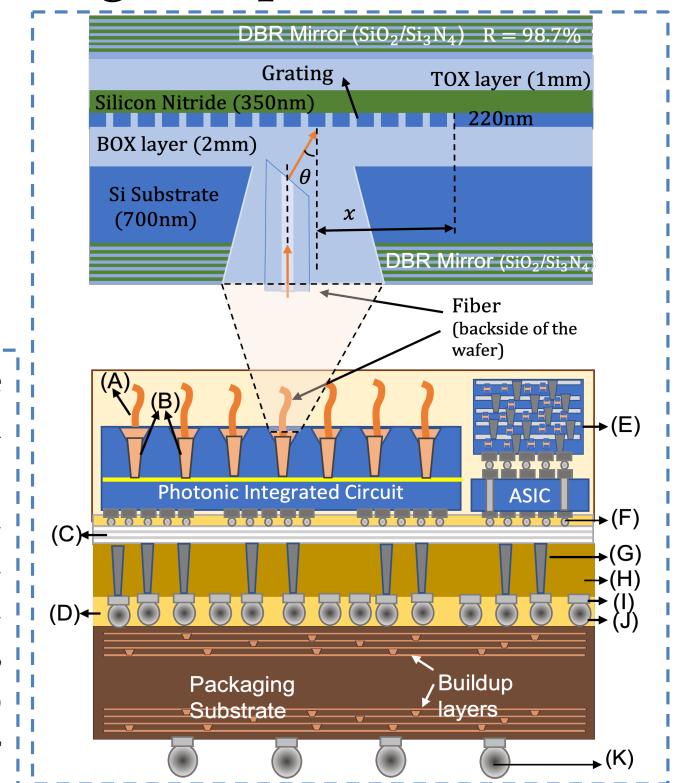
3D embodiment of



(A) DBR Mirror (topside) (B) TOX Layer (C) Si Waveguide (D) Si₃N₄Layer (E) BOX Layer (F) Focused Grating (G) Si Substrate (I) DBR Mirror (backside) (J) Optical Fiber

Cross-sectional image of the BOC with fiber attached to the V-groove formed on the backside of the wafer

Co-Packaged Optics with BOC

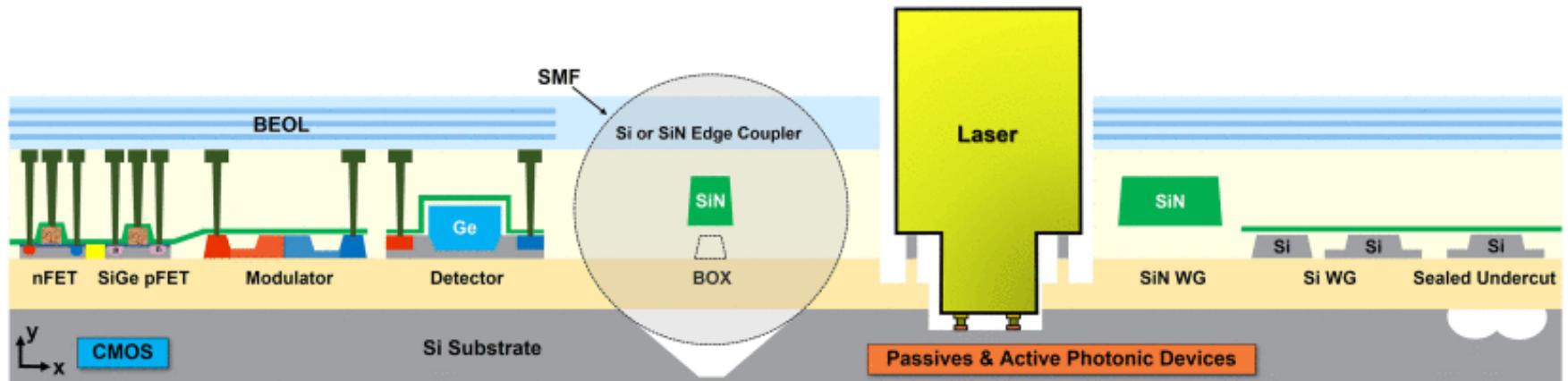


Epoxies used in fiber attach

Epoxy Type	Cure Type	Viscosity	Thermal Conductivity	Curing Temperature	Refractive Index	Max Temp	Special Properties	Examples
UV-Curable Epoxies	UV-light	Low-Moderate	Low	Room Temp - 100°C	~1.50-1.56	~150°C	Rapid curing, environmental stability	Dymax OP-67-LS
Thermal-Cure Epoxies	Thermal	Moderate-High	Moderate-High	80°C - 150°C	~1.50-1.56	~200°C-300°C	Strong bonds, high temp resistance	Epo-Tek 353ND, Henkel Loctite Hysol EE4215
Anaerobic Epoxies	Absence of air	Low-Moderate	Low-Moderate	Room Temp - 100°C	N/A	~150°C	Fills small gaps, air-restricted cure	Loctite 648
Optically Clear Epoxies	UV-light/Thermal	Low-Moderate	Low-Moderate	Room Temp - 150°C	~1.40-1.56	~150°C	High optical clarity, low loss	Norland Optical Adhesive 61 (NOA61)
Low-Outgassing Epoxies	Thermal/UV	Moderate	Moderate	80°C - 150°C	~1.50-1.56	~200°C	Minimized outgassing for vacuums	Master Bond EP30LV
High-Temperature Epoxies	Thermal	High	High	150°C - 250°C	~1.50-1.56	>300°C	Withstands high temp without degradation	Cotronics Durabond 952
Flexible Epoxies	Thermal/UV	Low-Moderate	Low	80°C - 150°C	~1.50-1.56	~150°C	Flexibility for thermal cycling	3M Scotch-Weld Epoxy Adhesive DP125
Single-Part Epoxies	Thermal	Moderate	Moderate-High	100°C - 150°C	~1.50-1.56	~200°C	Convenience, no mixing required	Henkel Loctite STYCAST US 0150
Two-Part Epoxies	Thermal	Varies	Varies	Varies	Varies	Varies		

Laser Integration

Laser to PIC integration

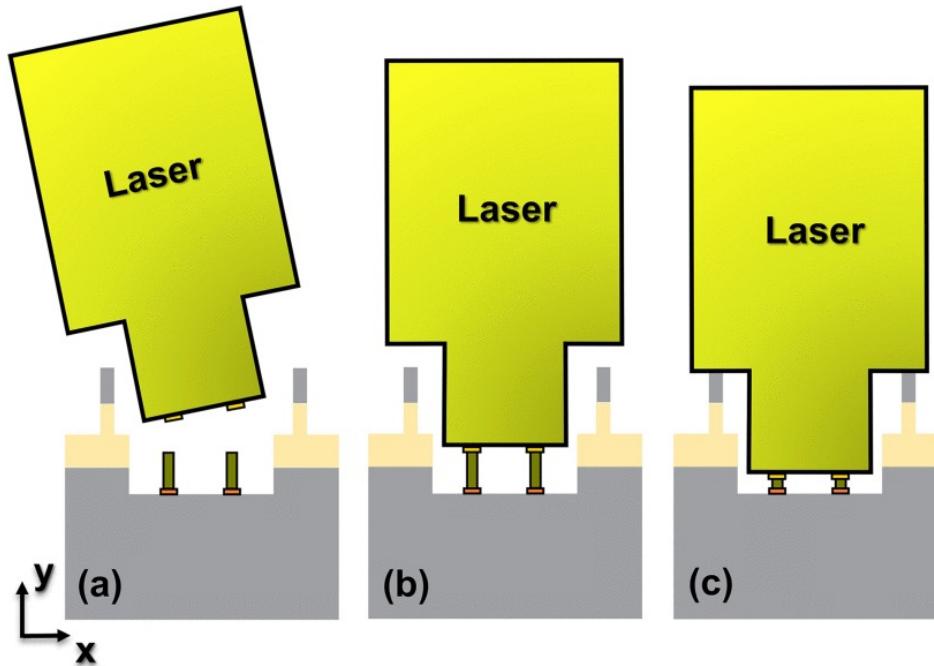


- GF monolithic SiPh platform integrates:
 - Laser attach
 - V-groove-based fiber attach (Si or SiN edge coupler)
 - Si and SiN-based passive and active photonic building blocks
 - CMOS components
- Utilizes dual Si thicknesses and dual contact modules
- Enables high-performance photonic and CMOS devices
- Integration on the same silicon-on-insulator (SOI) wafer
- **The III-V laser source is flip-chip bonded in the SiPh cavity**
- Coupled to a spot-size converter with mechanical stops on the SOI substrate
- **Includes optical alignment features on the PIC and laser**
- Drawing not to scale

Comparing various hybrid laser integrations Schemes

Integration Method	Coupling Efficiency	Link Budget Considerations
Flip-Chip Bonding	~40-70%	<ul style="list-style-type: none"> Good coupling efficiency contributes to a favorable link budget. Precise alignment and good thermal management are necessary to maintain performance.
Eutectic Bonding	~40-70%	<ul style="list-style-type: none"> Similar to flip-chip, with a strong, stable bond that benefits the link budget. Assumes optimal alignment and thermal management.
Edge Coupling	~30-60%	<ul style="list-style-type: none"> Decent coupling efficiency. Alignment drift can affect link budget negatively over time. Service loops or extra fiber length may be necessary to compensate for losses.
Adhesive Bonding	~30-60%	<ul style="list-style-type: none"> Variability in the adhesive layer's refractive index can affect coupling. Typically provides enough efficiency for a moderate link budget.
Vertical Coupling (Grating Coupler)	~20-40%	<ul style="list-style-type: none"> Lower coupling efficiency impacts link budget. May require amplification to mitigate losses, especially in longer links or more complex circuits.
Benign Integration	~20-50%	<ul style="list-style-type: none"> The reversible nature of this method may affect long-term stability and link budget. Requires careful design to ensure sufficient performance.

Flip chip bonding process of the laser on to the PIC



- Schematic process flow:

- Illustrates the flip-chip bonding process of the laser inside the SOI cavity on a monolithic CMOS SiPh platform.

- (a) Before alignment:

- The setup prior to aligning the laser for flip-chip bonding.

- (b) During alignment:

- The state of the assembly during the alignment of the laser.

- (c) After reflow:

- The configuration following the reflow process where the laser is permanently bonded.

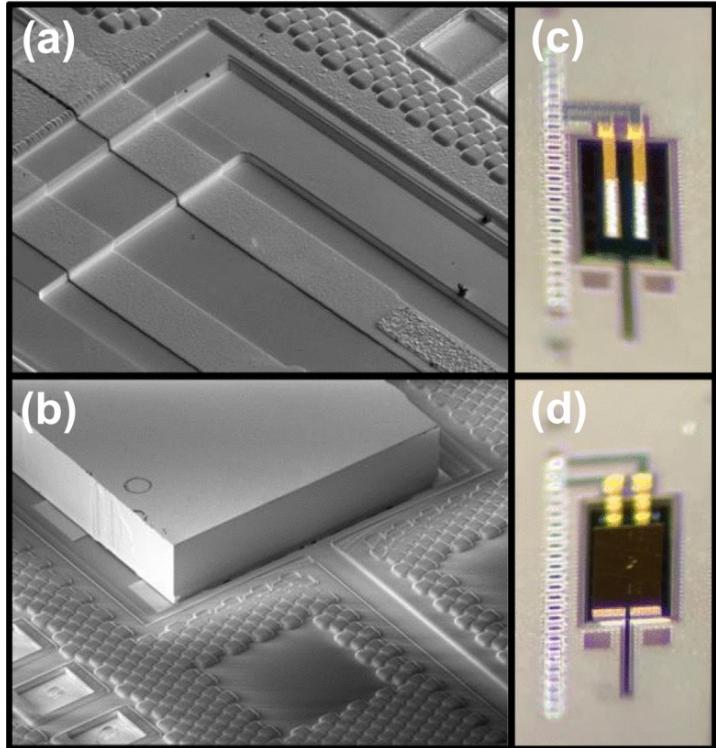
- Stability during reflow:

- The laser is securely held in place during the reflow process.

- Placement accuracy checks:

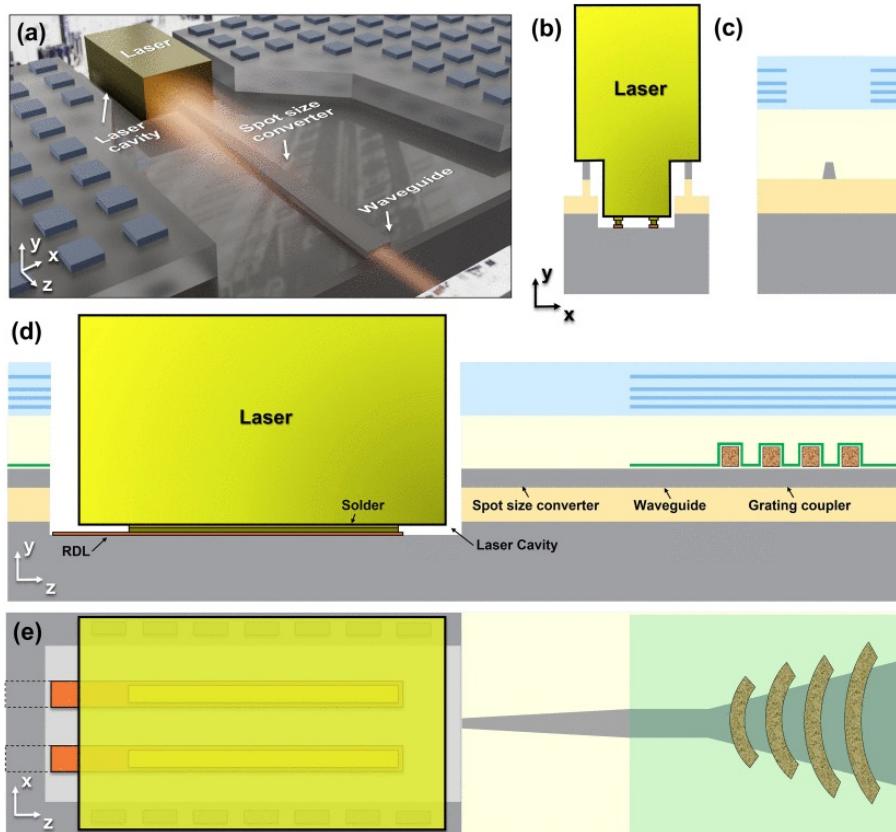
- In-situ placement accuracy measurements are conducted before and after reflow.
- This ensures that there is no significant lateral misalignment during the laser attach process.

SEM and optical images of the fabricated laser cavity and laser-integrated PIC.



- SEM images of the fabricated laser cavity and laser-integrated PIC.
 - (a) SEM image showing the laser cavity with wiring layers before laser integration.
 - (b) SEM image of the laser-Si interface after the laser has been attached.
- Optical images of the fabricated laser cavity and laser-integrated PIC.
 - (c) Optical image of the laser cavity including wiring layers before laser attachment.
 - (d) Optical image of the laser-integrated SiPh circuit with various functional photonic components monolithically integrated on the same SiPh platform.

3D and 2D schematics of a laser integrated with a PIC



- The laser source is:

- Flip-chip bonded in the SOI cavity
- Coupled to a Si SSC with mechanical stops on the PIC
- Features optical alignment on the laser and SOI substrate

- SSC selection:

- Can be either straight or angled
- Designed for efficient butt-end coupling with the laser

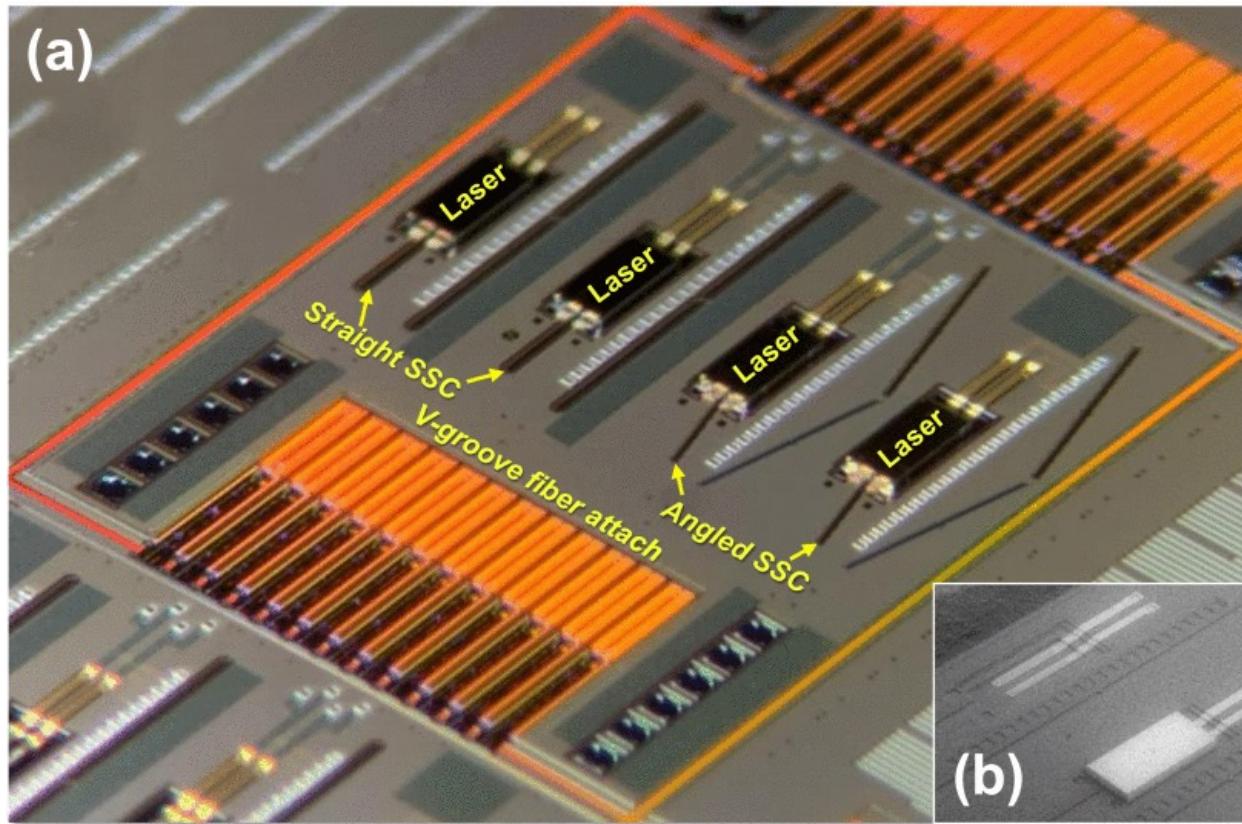
- Index matching glue:

- Incorporated during actual measurement

Image descriptions:

- (a) 3D perspective view of the laser-integrated chip
- (b) Cross-sectional view of the laser
- (c) Cross-sectional view of the Si SSC
- (d) Side view where the laser sits inside the cavity and directly couples to the SSC, which connects to a Si WG and a grating coupler
- (e) Top-down view of the laser-integrated SiPh chip
- Redistribution layer (RDL) not shown on the back side of the laser diode in (e), indicated by dashed rectangular lines
- The grating coupler can be replaced with:
 - V-groove-based fiber attach
 - Photodetector for power monitoring

Optical image of a SiPh chip with integrated laser



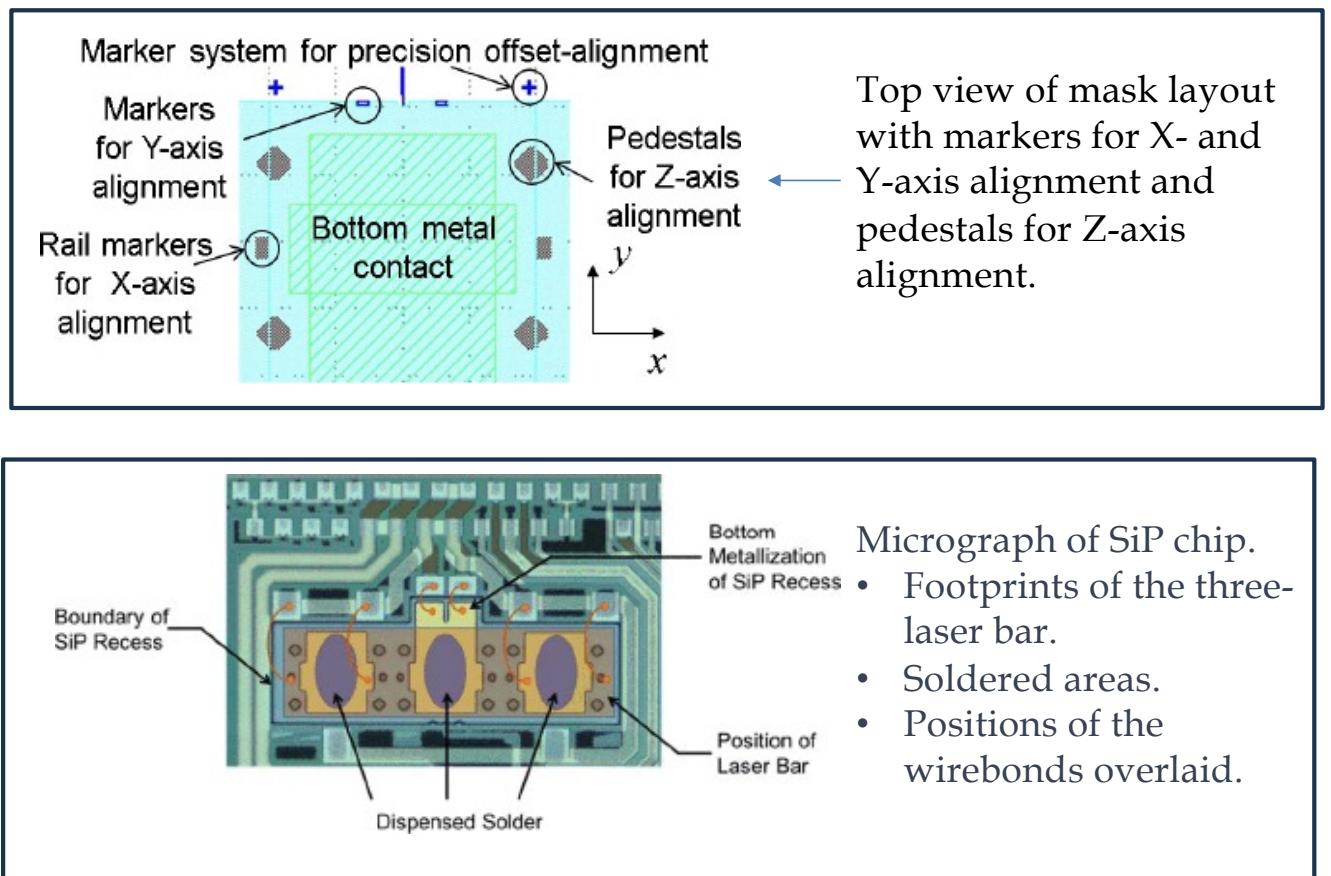
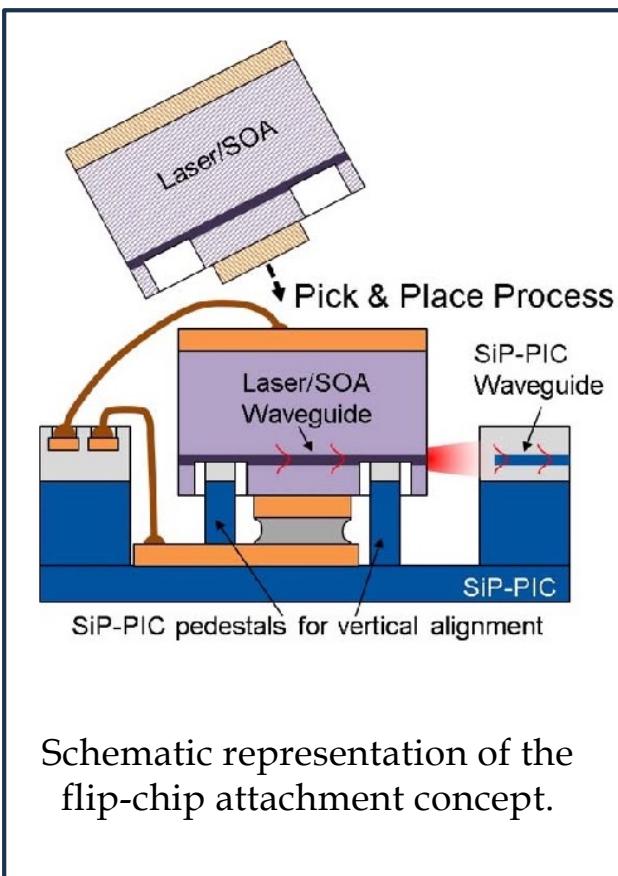
(a) Optical image of a monolithic SiPh chip.

- Integration of lasers flip-chip bonded inside SiPh cavities.
- Inclusion of Grating Couplers (GCs).
- Presence of V-groove-based fiber attach test structures.
- Applicability for both wafer and module level characterizations.

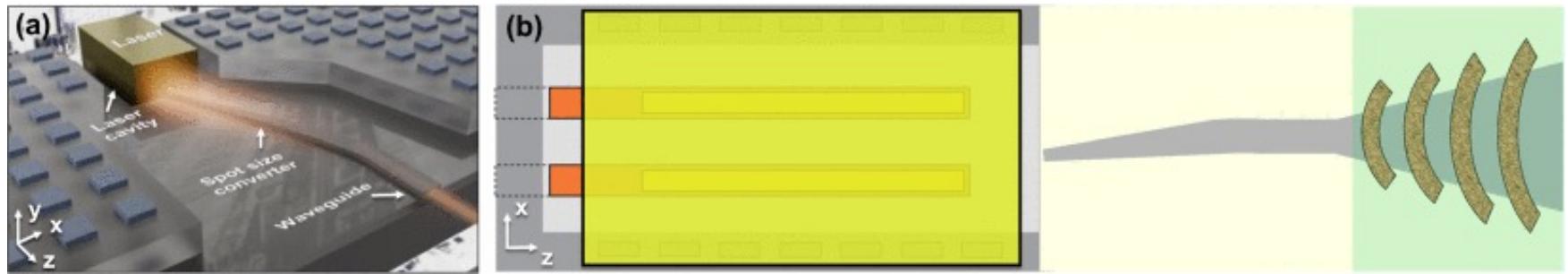
(b) SEM image of a laser cavity.

- Display of wiring layers prior to laser attachment.
- Depiction of a laser flip-chip bonded to the cavity.

Laser Attach on a hybrid PIC

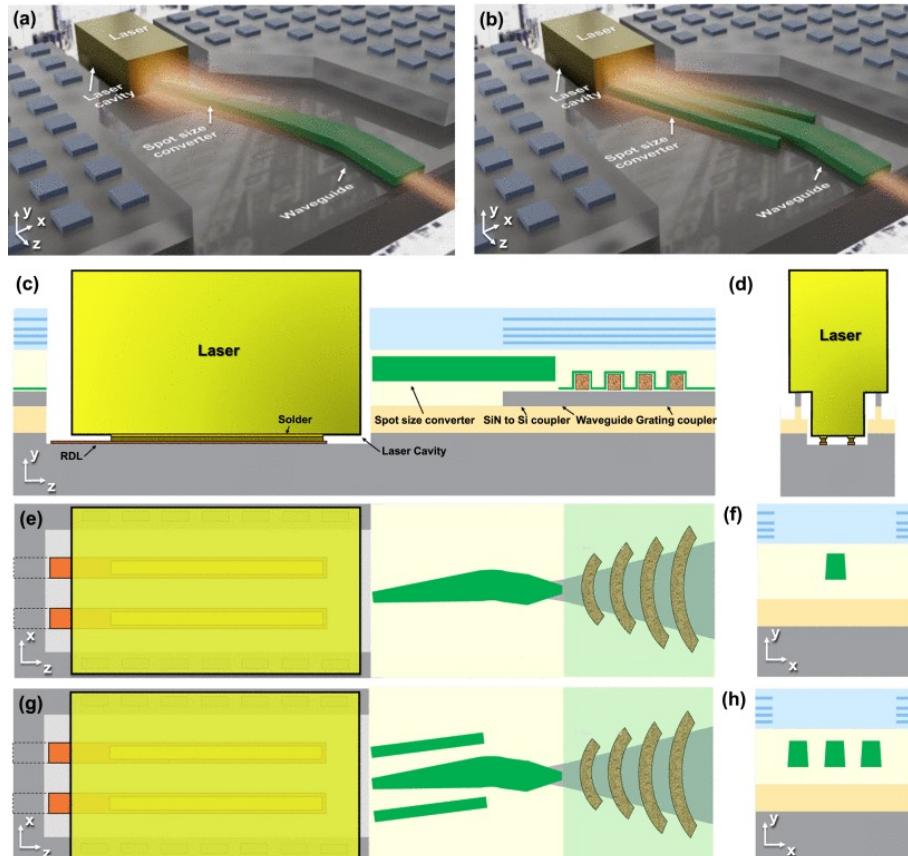


How to reduce optical return loss?



- (a) 3D schematic:
 - Depicts an alternative PIC chip integrating a laser with an angled Si SSC
 - Designed for optical return loss reduction
- (b) 2D schematic:
 - Provides a two-dimensional representation of the alternative PIC chip
 - Showcases the integration of a laser with an angled Si SSC for reduced optical return loss
- Note:
 - Drawings are not to scale.

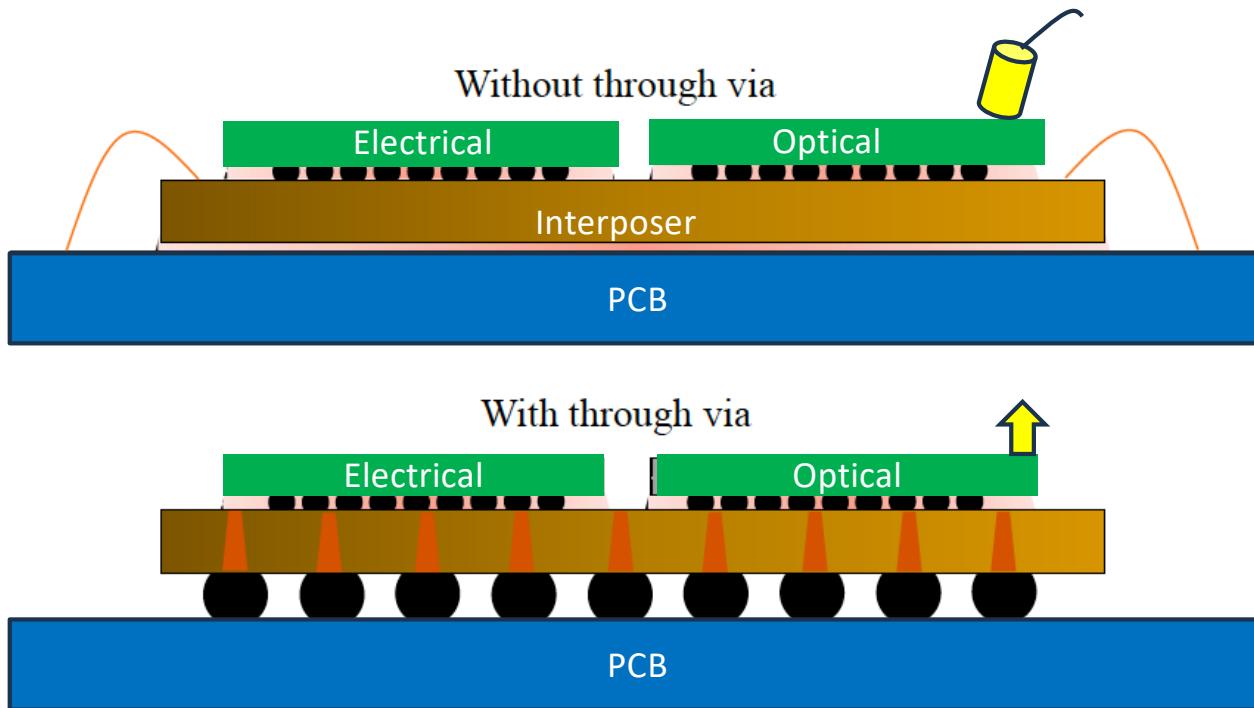
How to handle higher power?



- 3D and 2D schematics display III-V laser integration with a monolithic SiPh chip.
- Integration utilizes a pure SiN-based SSC for butt coupling.
- The SiN SSC aims to surpass the pure-Si-based counterpart in power handling and minimize power-dependent loss.
- 3D perspective views are provided of:
 - (a) Laser-integrated chip with a single-tip SiN SSC.
 - (b) Laser-integrated chip with multi-tip SiN SSCs.
- A side view of the PIC is presented.
- Cross-sectional views show:
 - (d) The laser.
 - (f) A single-tip SiN SSC.
 - (h) Multi-tip SiN SSCs.
- Top-down views of the PICs are illustrated in:
 - (e) and (g).
- Note: Drawings are not to scale.

Interposer

Generic Interposer for hybrid PIC integration

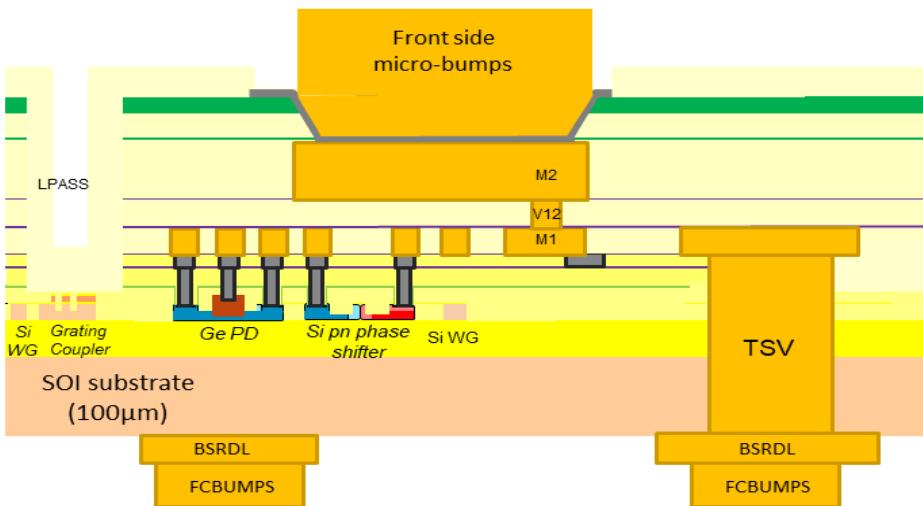


Interposer Materials

Ceramic: Large Via and Pitch
Glass: Fine via and pitch
Silicon: very fine via and pitch

Electrical interfacing between devices and system board – part of PIC packaging.
The package would have in-plane or out-of-plane fiber I/O.

imec's PIC Interposer platform with TSVs



- 300mm SOI Wafer Base:** Utilizes a 300 mm Silicon-on-Insulator (SOI) wafer with a 220 nm layer of crystalline silicon over a 2 μm buried oxide (BOX) layer.
- CMOS Compatible Integration:** Passive waveguides and active photonic devices are co-integrated on a single SOI substrate using CMOS-compatible front-end-of-line (FEOL) modules, which include tungsten contacts and copper interconnects.

- Interposer Platform with TSVs:** The hybrid Photonic Integrated Circuit (PIC) can be designed as an interposer platform incorporating TSVs for the integration of lasers and electronics.
- Diverse Optical Functionalities:** The platform supports multiple optical functionalities such as various etch depths for passive Si waveguides, Poly-Si layers for advanced optical devices, Si ring modulators, and Germanium photodetectors.
- Thermal and Electrical Control:** Incorporates metal heaters for thermal control and TSVs for electrical connectivity.
- Two-Level Copper Interconnects:** Features two levels of copper interconnects for complex routing and signal integrity.
- Frontside and Backside Connectivity:** Equipped with frontside copper micro-bumps for flip-chip integration and a backside copper redistribution layer (RDL) along with backside micro-bumps for assembly onto a Printed Circuit Board (PCB).
- Mechanical Stability:** A TSV size of 10 μm diameter with a 100 μm Si interposer thickness is selected to ensure mechanical stability during packaging after die singulation.
- Advanced TSV Integration:** The TSV-middle approach is employed, where TSVs are fabricated after the FEOL processing and before the Metal 1 copper interconnect layer, addressing challenges like TSV copper filling and wafer warpage management.

Photonics Interposer Technology

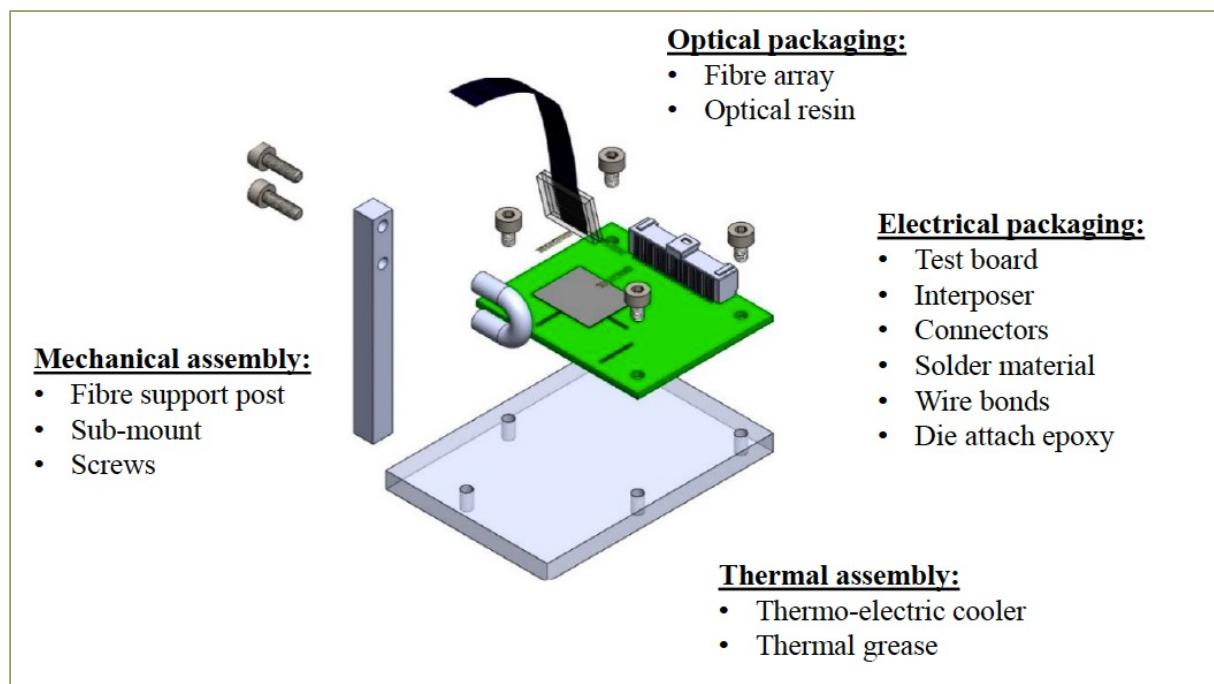
Feature	Description
Hybrid Integration Platform	Combines different photonic materials on one substrate for best-in-class material functionality.
Coupling Efficiency	Incorporates various couplers for efficient light coupling between heterogeneous components.
Broadband and Wavelength-Agnostic	Accommodates diverse operational wavelengths, suitable for DWDM systems.
High Precision Alignment	Features precision alignment for accurate photonic element positioning, reducing manufacturing costs.
Thermal Management	Handles thermal loads with thermal vias and heat spreaders for stable operation.
Advanced Packaging Techniques	Compatible with various bonding techniques for robust packaging, including 3D stacking.
Electrical Interconnects	Provides electrical routing for power and signal transmission, including high-speed transceivers.
Scalable Manufacturing	Utilizes semiconductor and PCB techniques, enabling wafer-scale and panel-scale production.
Low Insertion Loss	Minimizes insertion loss for integrated waveguides and couplers, maintaining signal integrity.
Signal Integrity and Bandwidth	Maintains high signal integrity for optical data transport, supporting terabit-scale bandwidths.
Customizable Layouts	Allows for design flexibility to meet specific application needs in a compact package.
Testing and Reliability	Designed for easy testing and characterized by proven reliability in harsh conditions.

Comparing Interposer Technology

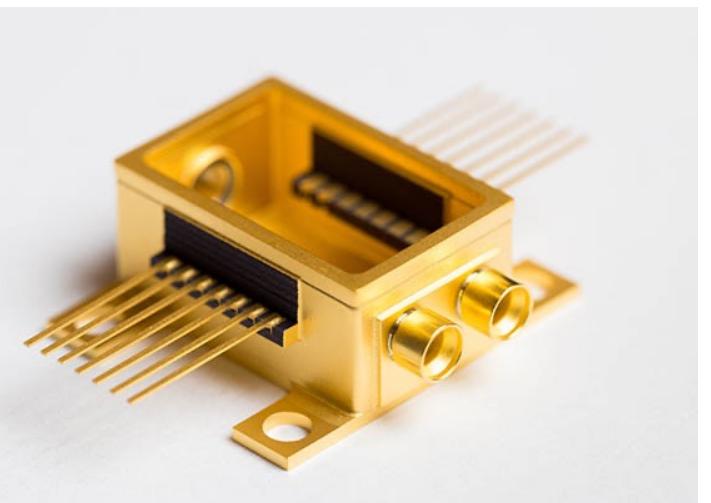
Attribute	Silicon Interposer	Glass Interposer	Ceramic Interposer
Thermal Conductivity & CTE	High (around 150 W/mK); matched to silicon chips (2.6 ppm/k)	Low (1-3 W/mK); CTE can be tailored, generally low (3-9 ppm/k)	Moderate to High (~24-240 W/mK depending on type); CTE can be matched to silicon (~3-7 ppm/k) or other materials
RF Performance	Excellent for HF applications due to high conductivity, very dense transmission lines	Good, low loss at high frequencies, dense transmission lines	Good, ceramic materials can offer low losses, sparse transmission lines
Optical Transparency	Not transparent, requires etching for optical paths	Transparent, allowing for easier optical integration	Typically not transparent
Cost	Moderate to high	Low to moderate	Moderate to high
Process Complexity	High, compatible with semiconductor processes	Moderate, requires specific processes	High, ceramic processing can be complex
Mechanical Strength	Brittle, but strong in thin layers	Good mechanical strength	Very high mechanical strength
Layers	Multi metal layers possible	Typically, two metal layers	Typically, single metal layers
Integration with Active Devices	Direct integration possible, thanks to semiconductor properties,	Indirect; requires additional layers or bonding techniques,	Indirect; generally used as a passive interposer
Via	Very fine Via and Pitch	Fine Via and Pitch	Large Via and Pitch

Assembly

Generic Assembly of a PIC Package



Butterfly package – Active and passive Techniques



Generic assembly of a silicon photonic package, consisting of thermal and mechanical considerations, in addition to optical and electrical packaging

Pluggable Optical Assembly

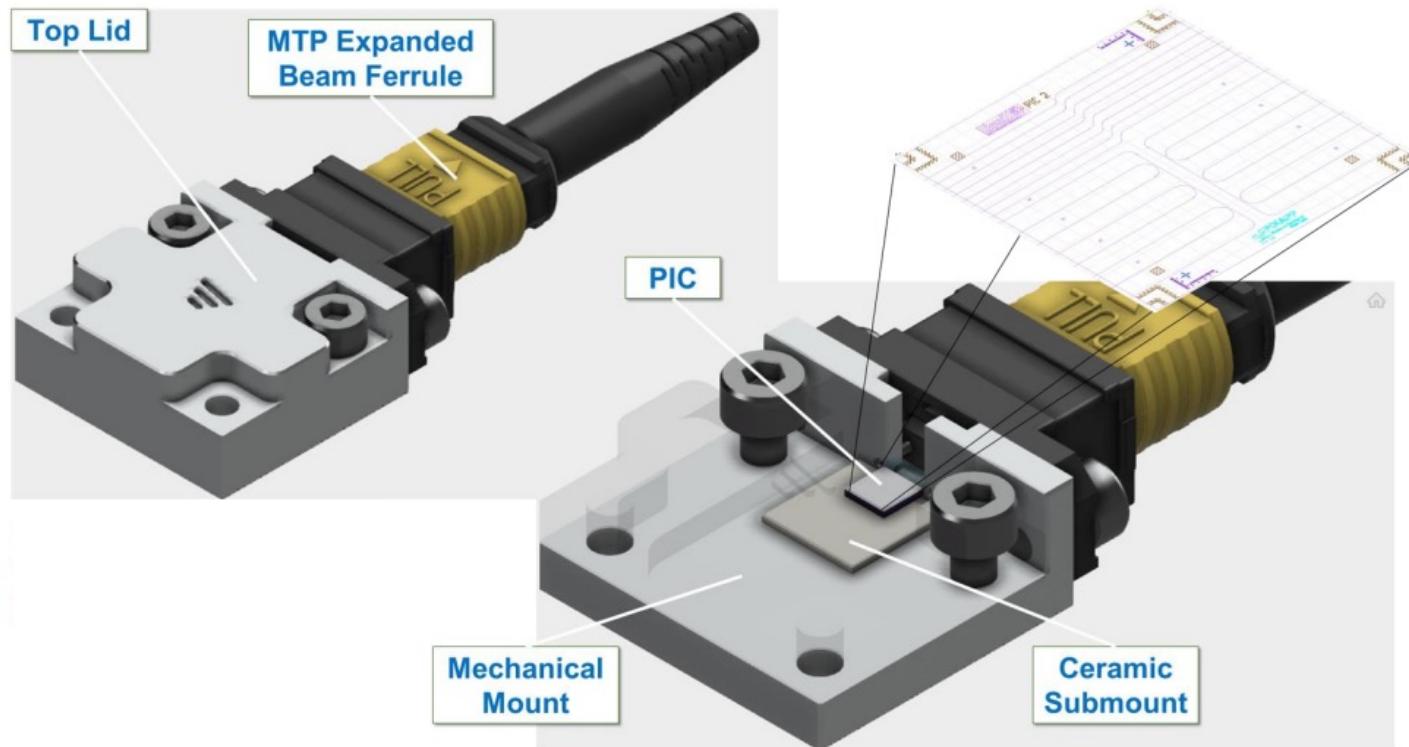


Image from iNEMI

Summary

- Presented an overview of the field, highlighting the process of packaging photonic devices.
- Presented the fundamental physics principles that underpin optoelectronics packaging, emphasizing the importance of material properties, thermal management, etc.
- Presented the unique challenges and solutions in packaging PICs, focusing on the key optical I/O packaging schemes

Thank You