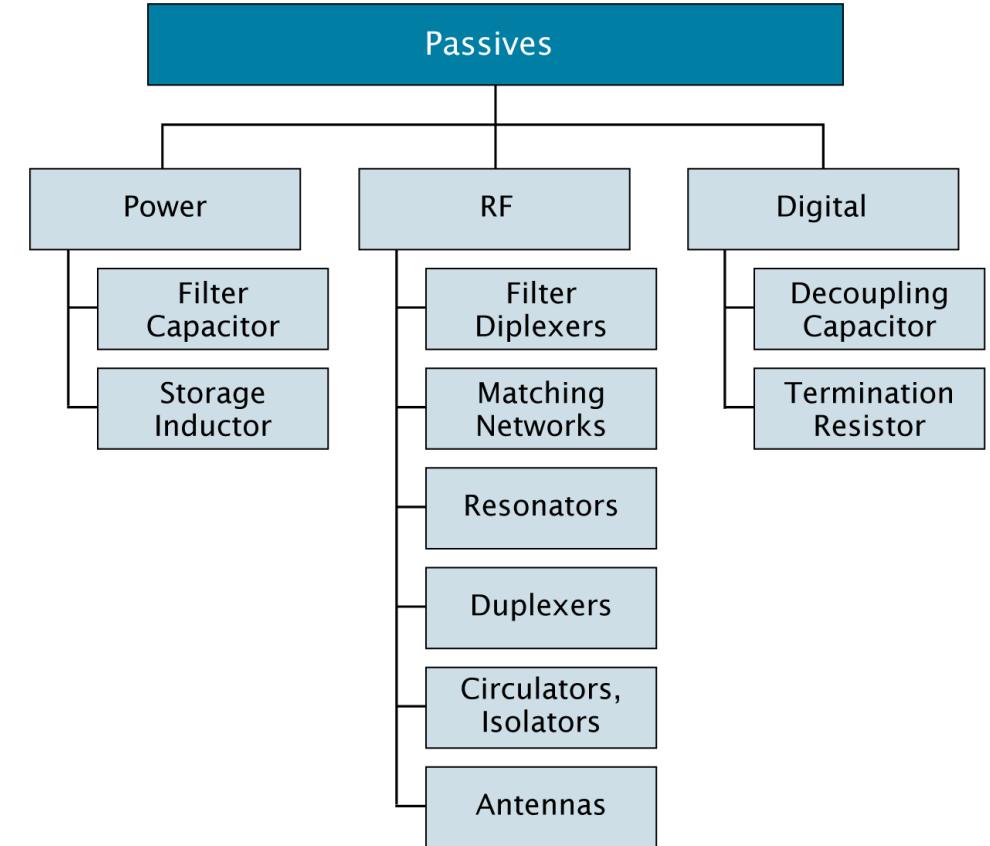
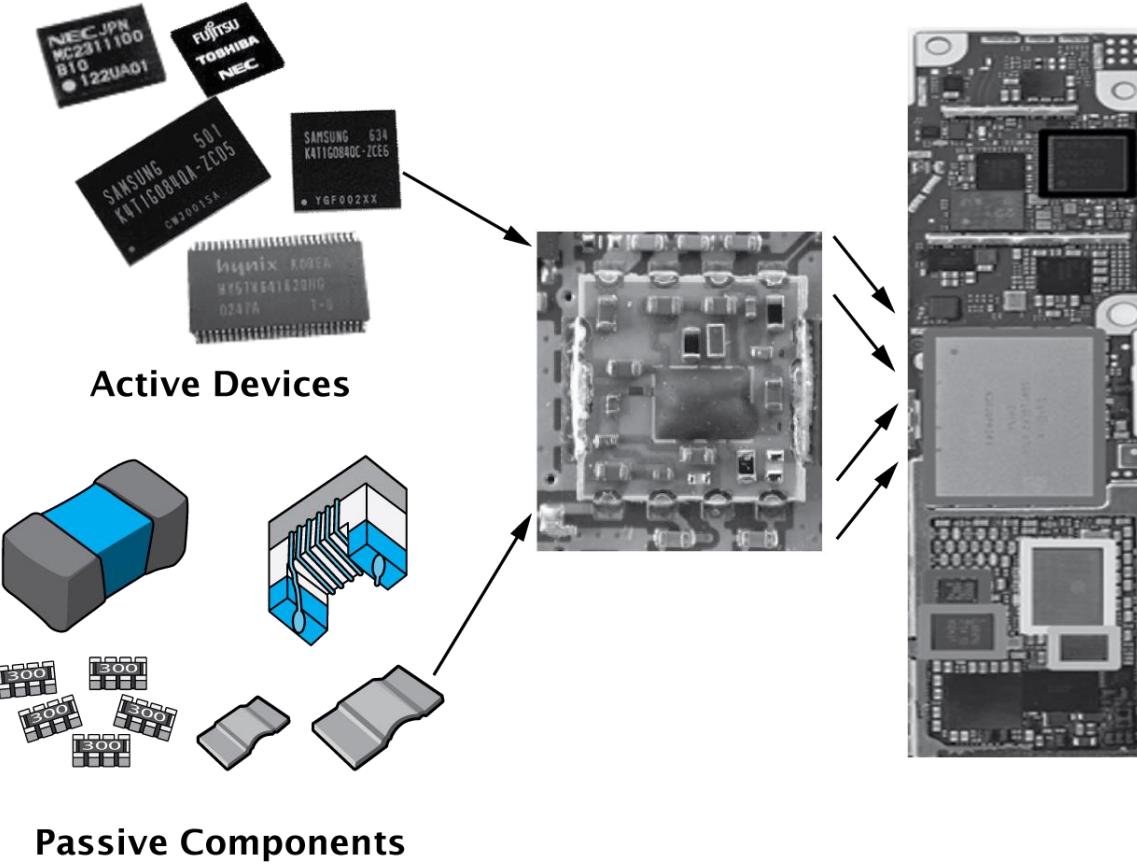


# **Fundamentals and Passive Components and Active-Passive Integration**

P M Raj (Florida International University)

# What are Passive Components and Why?



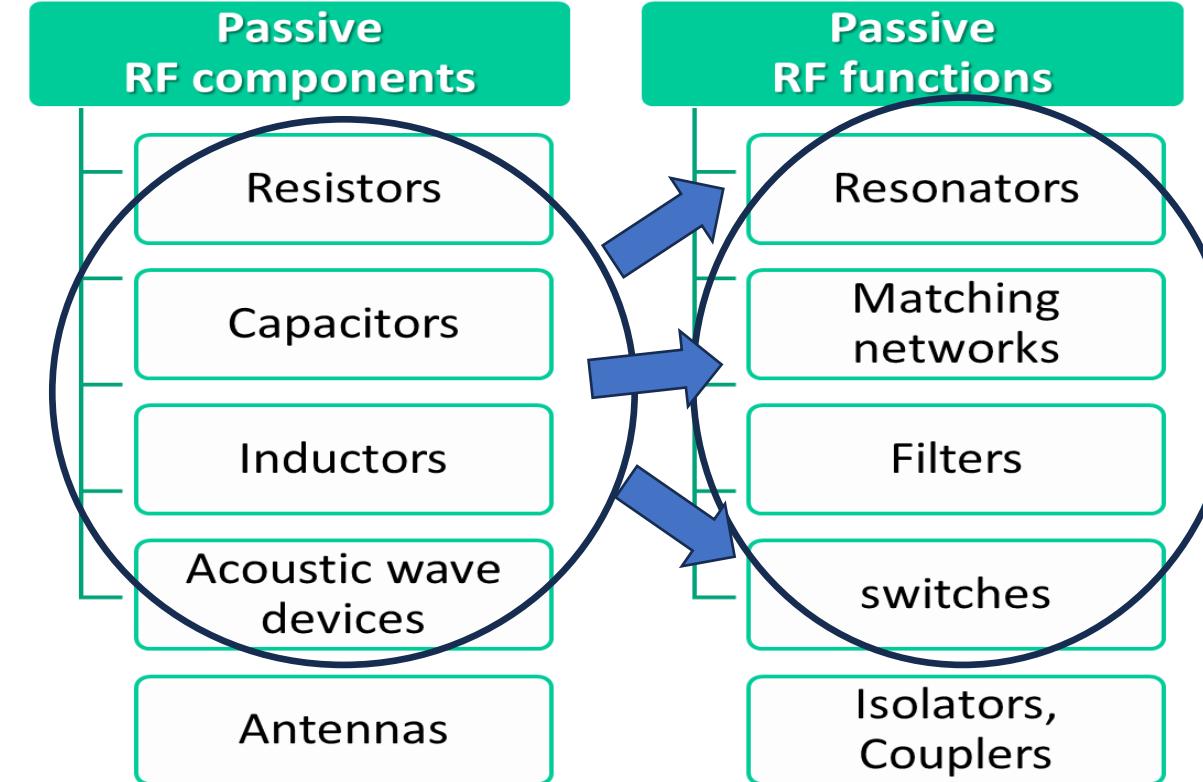
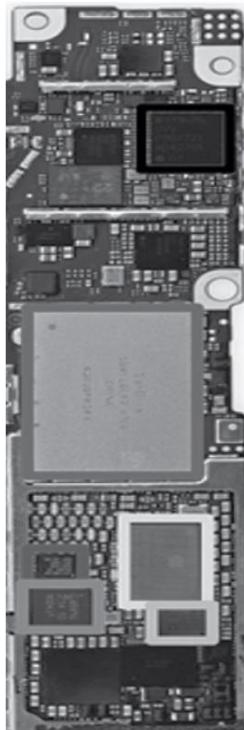
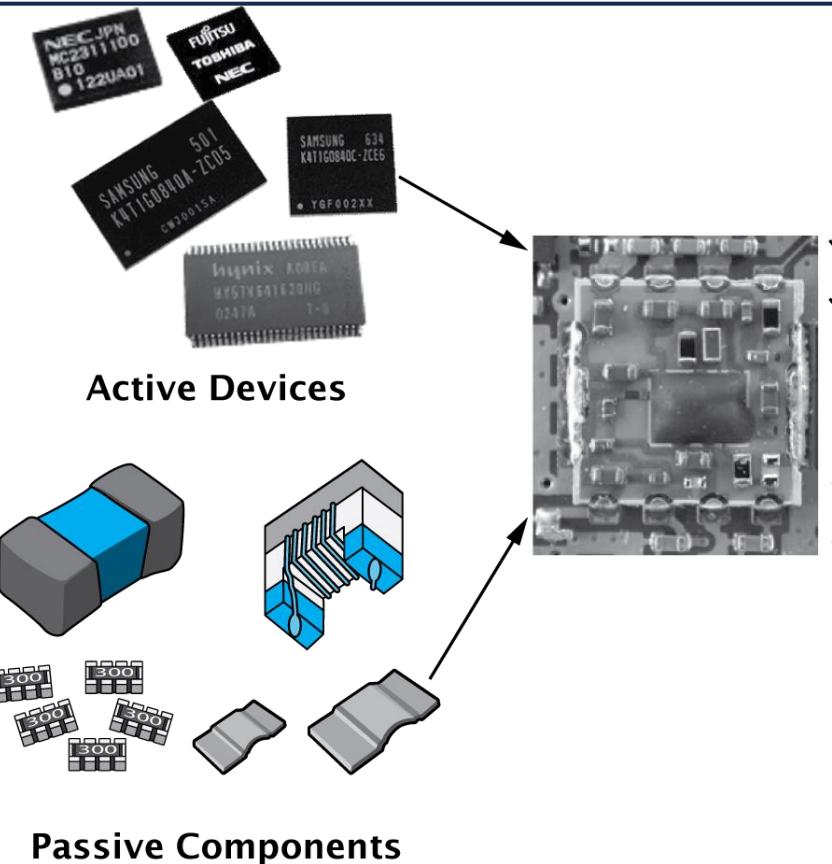
Definition of passives:

Components that do not require power for their basic operation.

Key characteristics:

- Cannot amplify or provide gain, which fundamentally differentiates them from active devices
- Filter, attenuate, modulate, sense, and monitor currents.
- Perform various important functions:
  - Power: noise suppression, energy storage and release,
  - RF: filtering, matching, phase shift, power divider, terminations in and others

# What are Passive Components and Why?



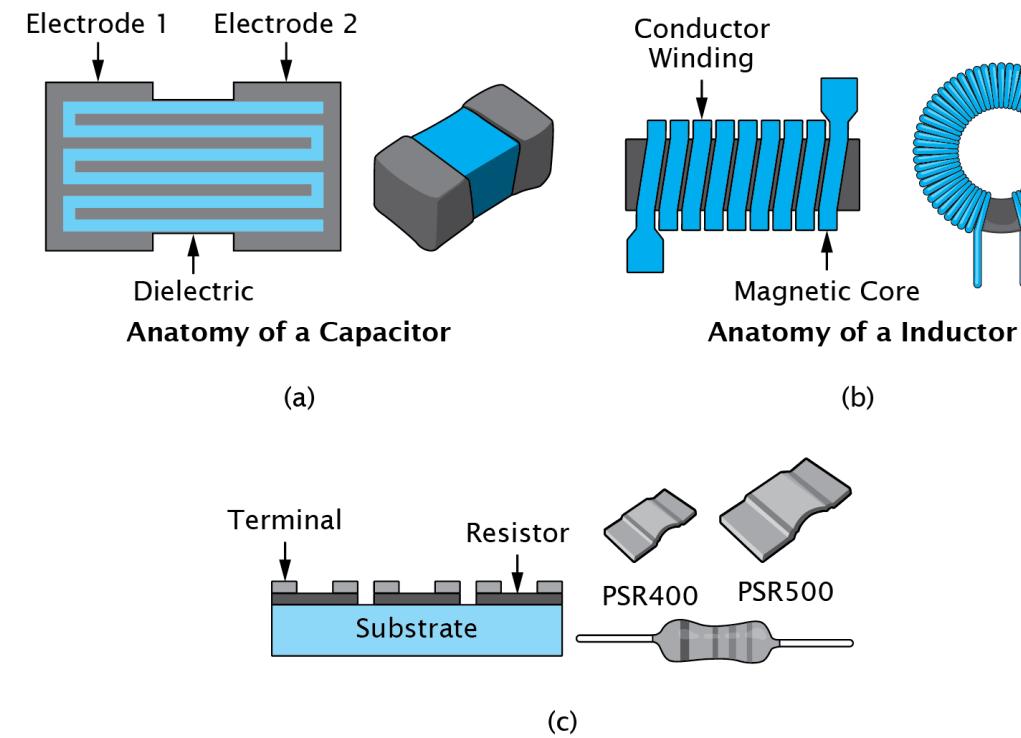
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# Anatomy of Passives



**Basic units:**

Capacitors: Conductors separated by an insulator;

Inductors: Conductors surrounded by a magnetic

(or vice versa: magnetic core surrounded by conductors;

Resistors: Partial conductors with metal terminations

**Actual passives:**

Combination of the basic units to perform various functions

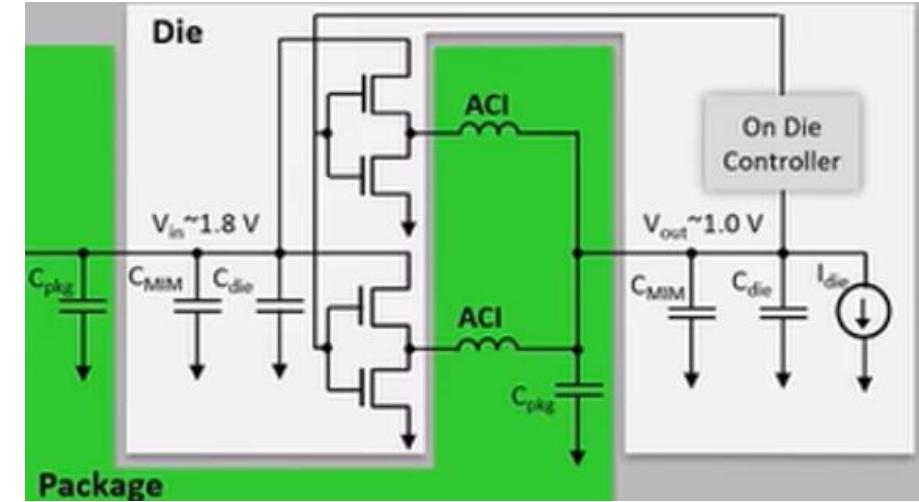
# Capacitors (or Inductors) Vary a Lot Based on their Functions (or Circuits they Serve)

**Important to understand capacitors (or inductors) in the context of their circuits and functions**

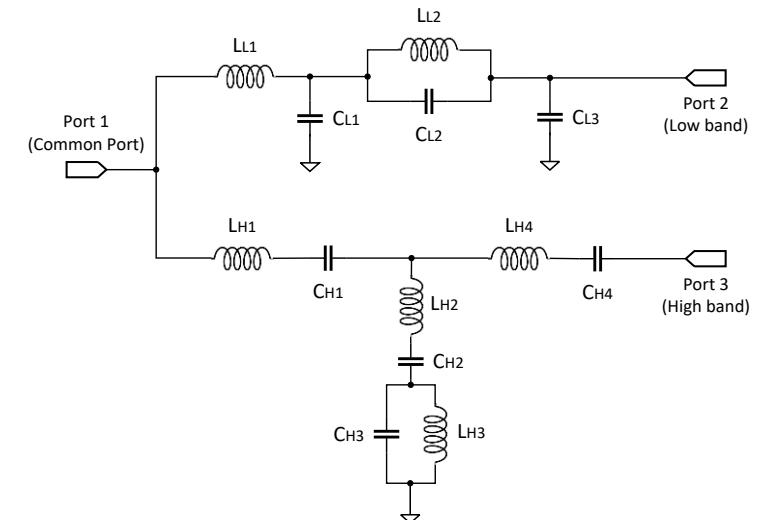
For ex: Capacitors in a power supply path are optimized for energy storage and output power by attaining lowest impedance;

Inductors are optimized for magnetic energy storage and release with high Quality factor

**Example  
of a  
Power  
Circuit**



**Example  
of a RF  
Circuit**



Capacitors and inductors in a RF circuit are optimized for precise impedance control and quality factor

These are very different from the above capacitors and inductors

# Passives Components in Hand-held Products

System	Total Passives	Total ICs	Passive to Active Ratio
<b>CELLULAR PHONES</b>			
Ericsson DH338 Digital	359	25	14:1
Ericsson E237 Analog	243	14	17:1
Philips PR93 Analog	283	11	25:1
Nokia 2110 Digital	432	21	20:1
Motorola Mr1 1.8 GHz	389	27	14:1
Casio PH-250	373	29	13:1
Motorola StarTAC	993	45	22:1
Matsushita NTT DoCoMo	492	30	16:1
<b>CONSUMER PORTABLE</b>			
Motorola Tango Pager	437	15	29:1
Casio QV10 Digital Camera	489	17	29:1
1990 Sony Camcorder	1226	14	33:1
Sony HandyCam DCR-PC7	1329	43	31:1
<b>OTHER COMMUNICATIONS</b>			
Motorola Pen Pager	142	3	47:1
Infotac Radio Modem	585	4	24:1
Data Race Fax Modem	101	8	13:1
<b>PDA</b>			
Sony Magic Link	538	74	7:1

# Passive Components in Recent Products

Component Type	Unit cost	Sum of Qty	Total component cost USD
Capacitors	0.0014	127	0.18
Coupler/Balun	0.04	1	0.04
Filter	0.094	5	0.47
Inductors	0.01	27	0.28
Oscillator	0.7	1	0.7
Resistor	0.0016	31	0.05
Total	0.0089		1.72

# Passives in Power Supply

# Power from a battery or outlet goes through varies stages of conversion

## 1) PCB: voltage step-down

*For systems with >3-5V system bus*

## 2) SiP: IVRs

*Significantly improve performance-per-watt*

- Bypass majority of PDN
- Fine-grain power management

## 3) Load die: LDOs

*Optionally provides additional voltage regulation*

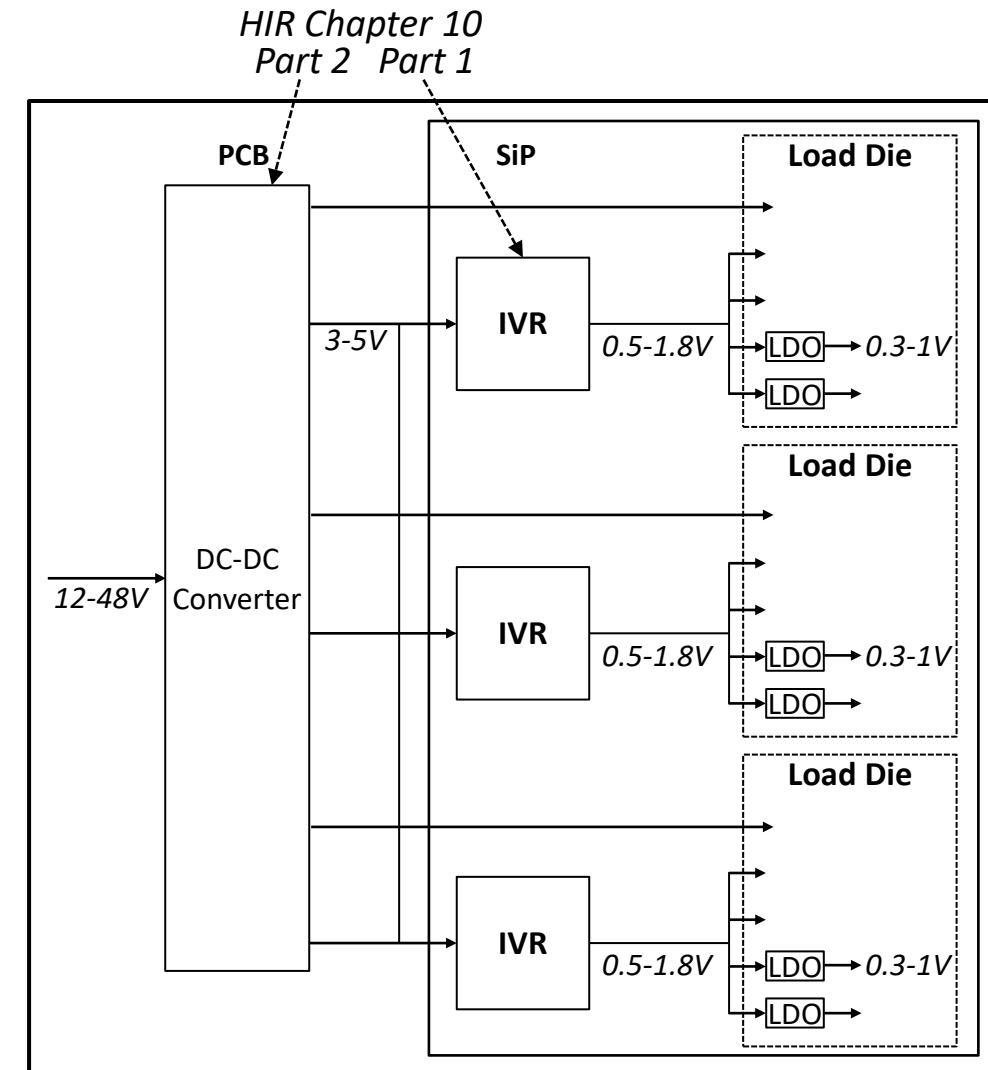
PCB = Printed Circuit Board

SiP = System in Package

PDN = Power Distribution Network

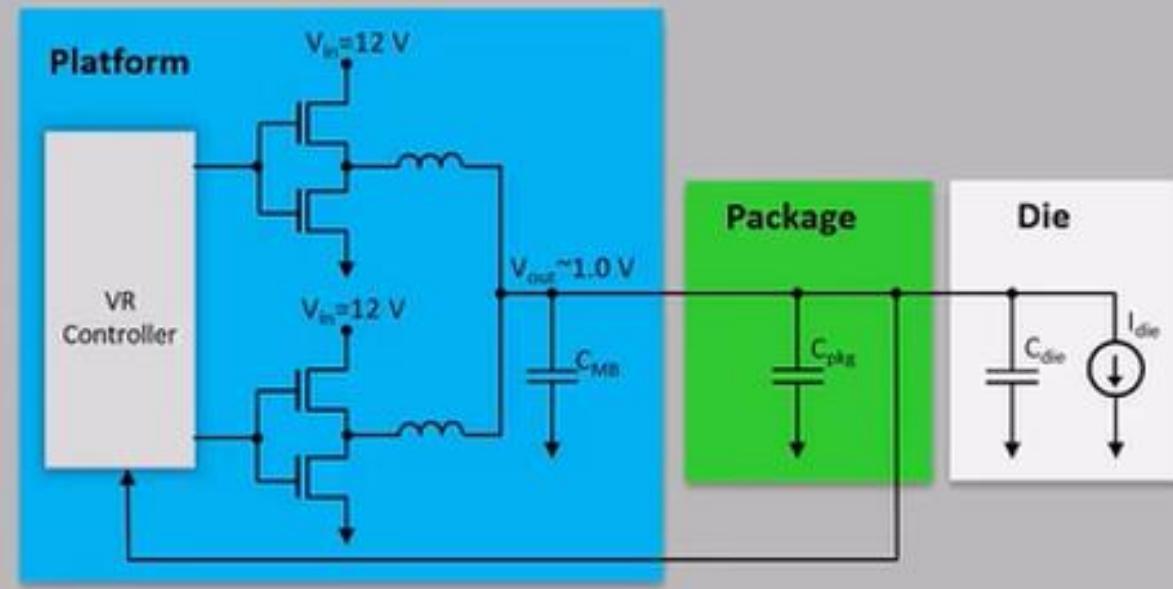
IVR = Integrated Voltage Regulator

LDO = Low Drop Out linear regulator

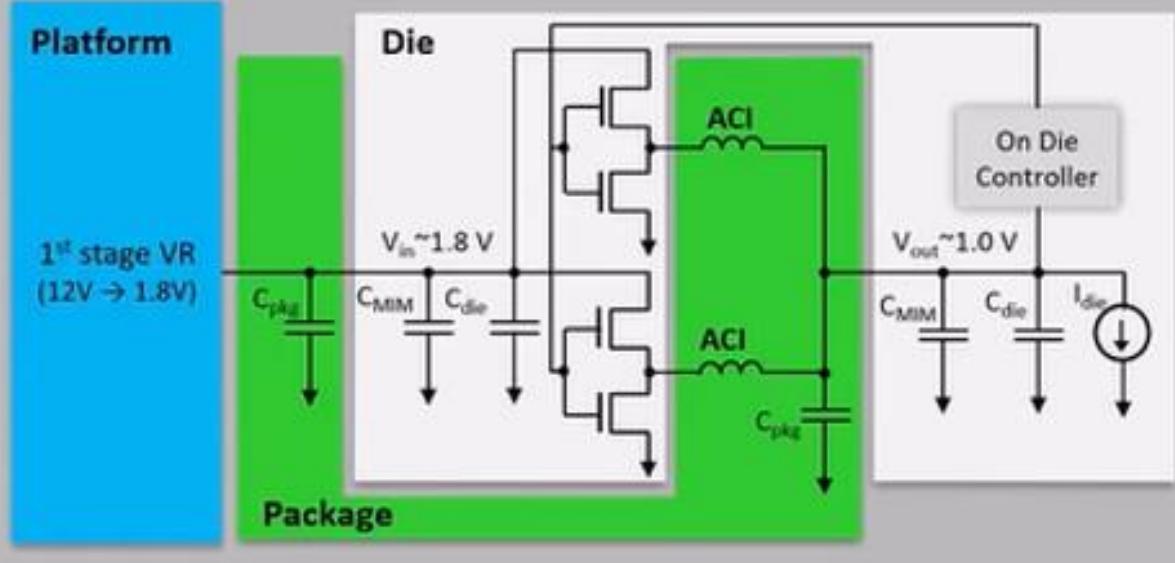


# Integrated Power Delivery in the Package Key for High-Performance in Computing

**MBVR (3<sup>rd</sup> Generation Intel® Core™ Processor)**



**FIVR (4<sup>th</sup> Generation Intel® Core™ Processor)**



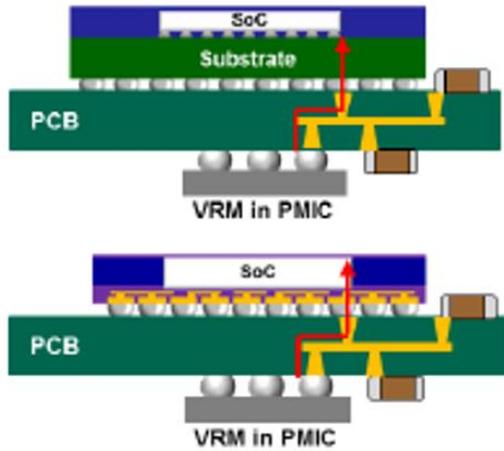
Previously Voltage regulator is designed on the PCB

Few filter capacitors in package

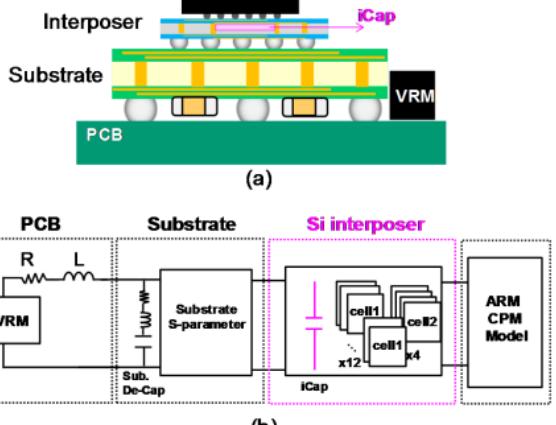
Now, Voltage regulator is moving into the package

More filter capacitors moving into the package

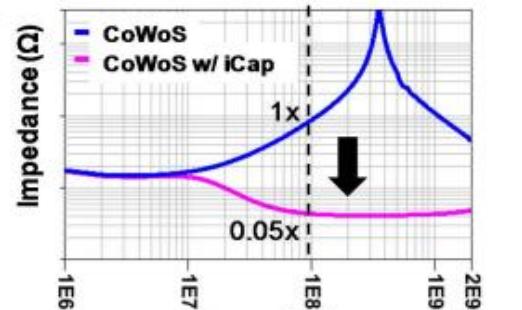
# Bring Power Conversion Closer to the Processor



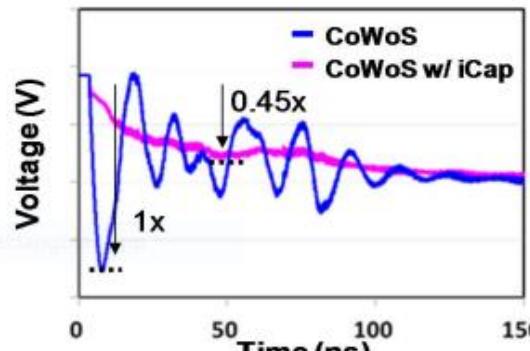
TSMC, pwr soc 16



Maintain low impedance in broader frequencies  
Suppress droop and ripple in the voltage  
(TSMC, IEDM 2019)



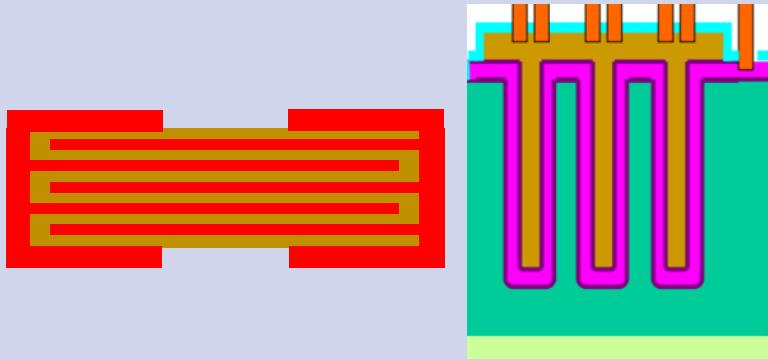
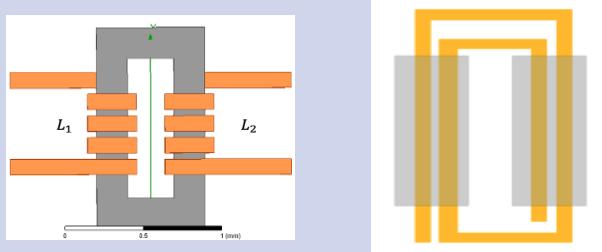
(a) Power delivery network impedance



(b) System Level Voltage droop

Need high-energy-density capacitors and inductors in the power delivery network to maintain low impedance over broad frequencies

# Storage Components: Capacitors and Inductors

Capacitors		Density	High K dielectrics; Enhance electrode surface area; New dielectrics and deposition processes
		Frequency stability	Electrodes and connectivity with lower parasitics
		Integration	Thinner form-factors; Substrate or wafer or fan-out embedding
Inductors		Density	Higher permeability with saturation field and high resistivity
		Efficiency	Low coil DC losses ; Low core losses with low coercivity and eddy currents
		Integration	Substrate- or wafer-compatible process
		Current-handling	Design innovations; Scalability in thickness to handle higher current

# Inductor Technologies and Integration Strategies

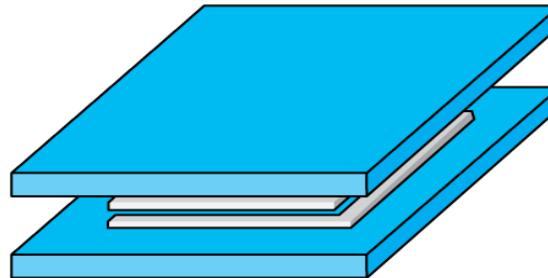
## Discrete Ferrite Inductors

Surface-mounted  
on Board



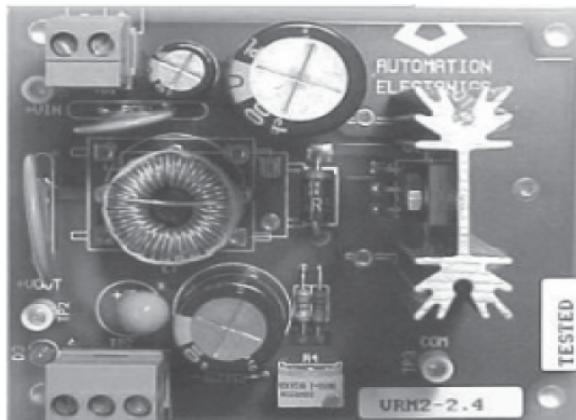
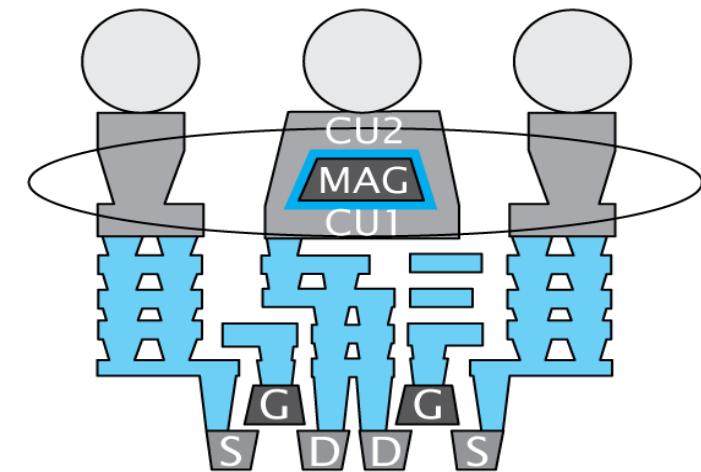
## Planar -Thickfilm Ceramic or Metal Composite Core

Packaging-embedded

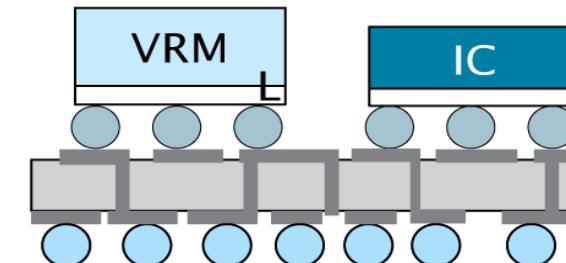
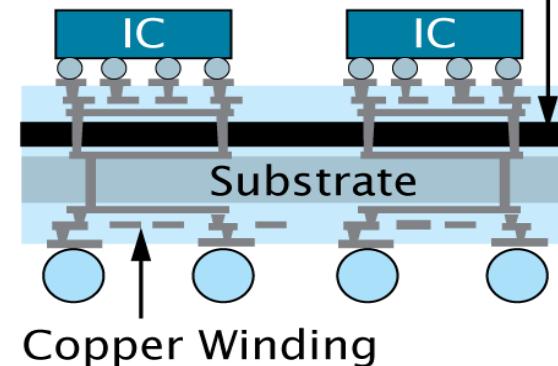


## Planar -Thickfilm Inductors

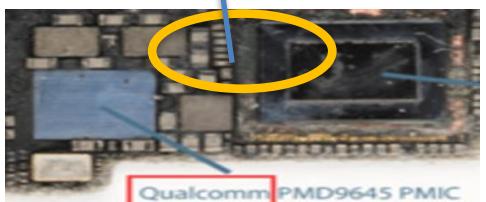
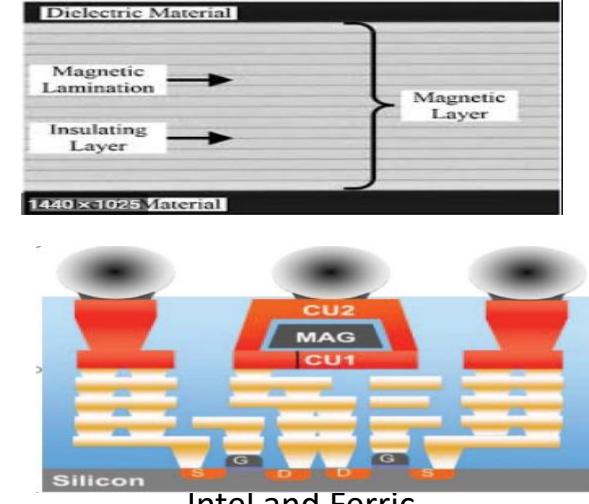
Package or  
On-chip Embedded



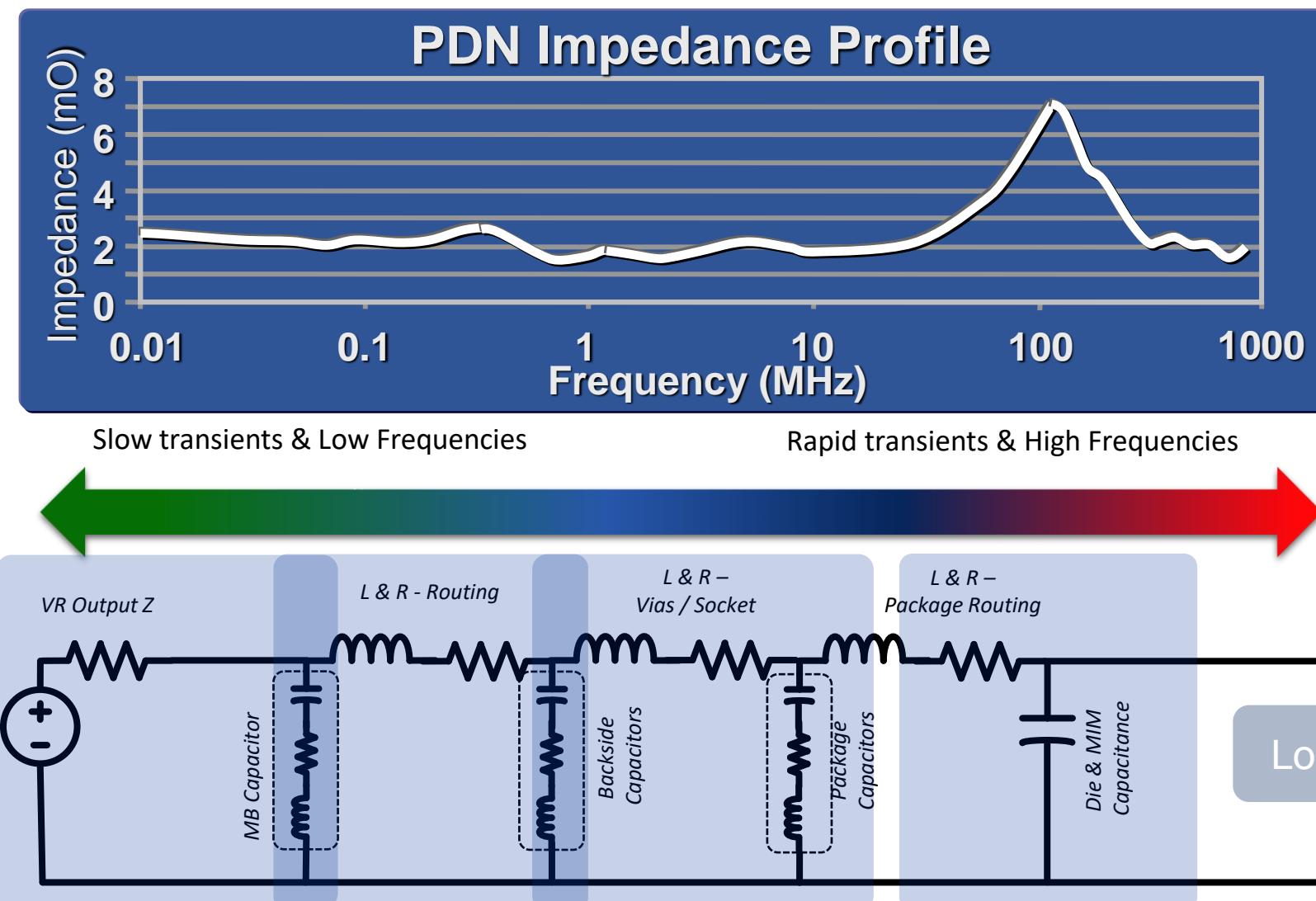
## Magnetic Sheets



# Inductor Technologies

	Discrete (Ferrite or Metal powder)	Magnetic composites –substrate-embedding	Nanomagnetic films: On-chip
L/Rdc nH/milliohm	15-25	5-10	0.1-0.2
Q	>20	<10	5
Current-handling A/mm <sup>2</sup>	0.01 – 0.1	0.1 – 1	5-10 A/mm <sup>2</sup>
Thickness	200- 500 microns	50 - 200 microns	25 microns
Cost	Low	Low	High
	<p>Discrete (Ex.0.5 x 0.1 x 0.5 mm)</p> 		

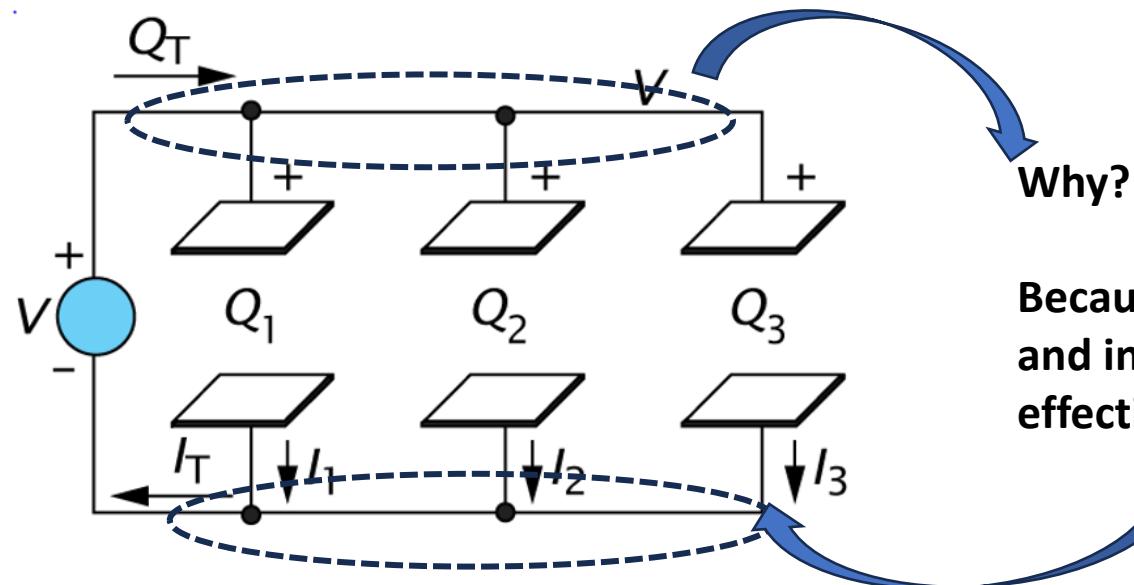
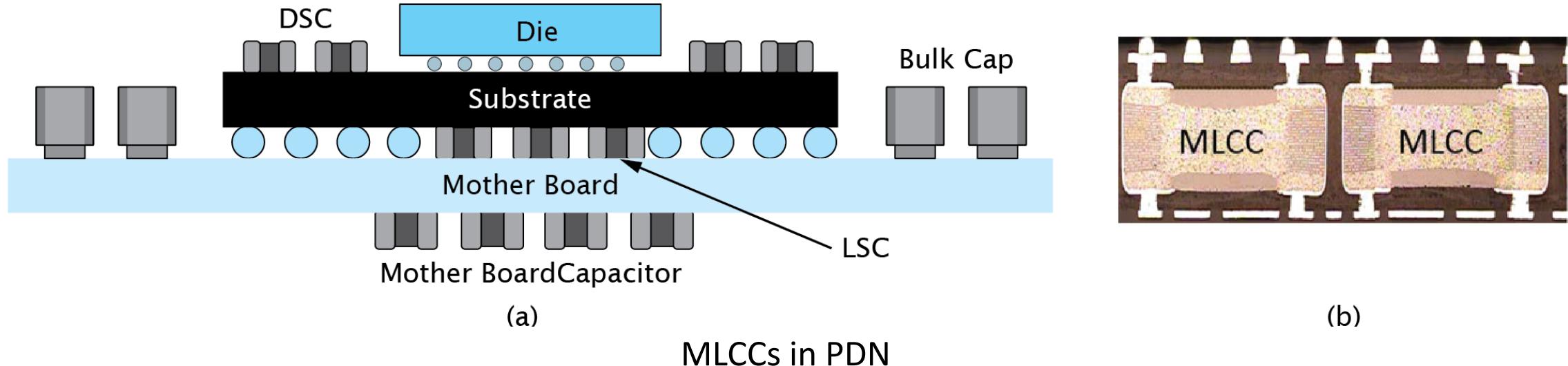
# PDN Components and Operation



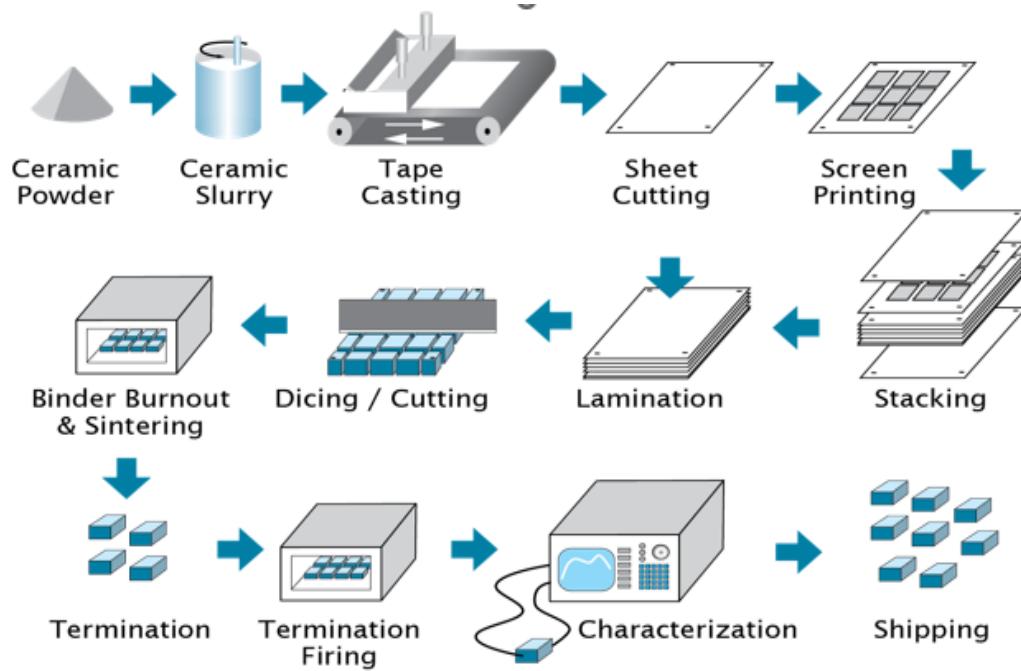
## PDN Impedance Profile

- Summarizes all of the PDN electrical behavior
- Thévenin equivalent circuit
- Typically design for flat as you can afford
- DC Impedance – aka “DC Loadline” is choice determined by many tradeoffs

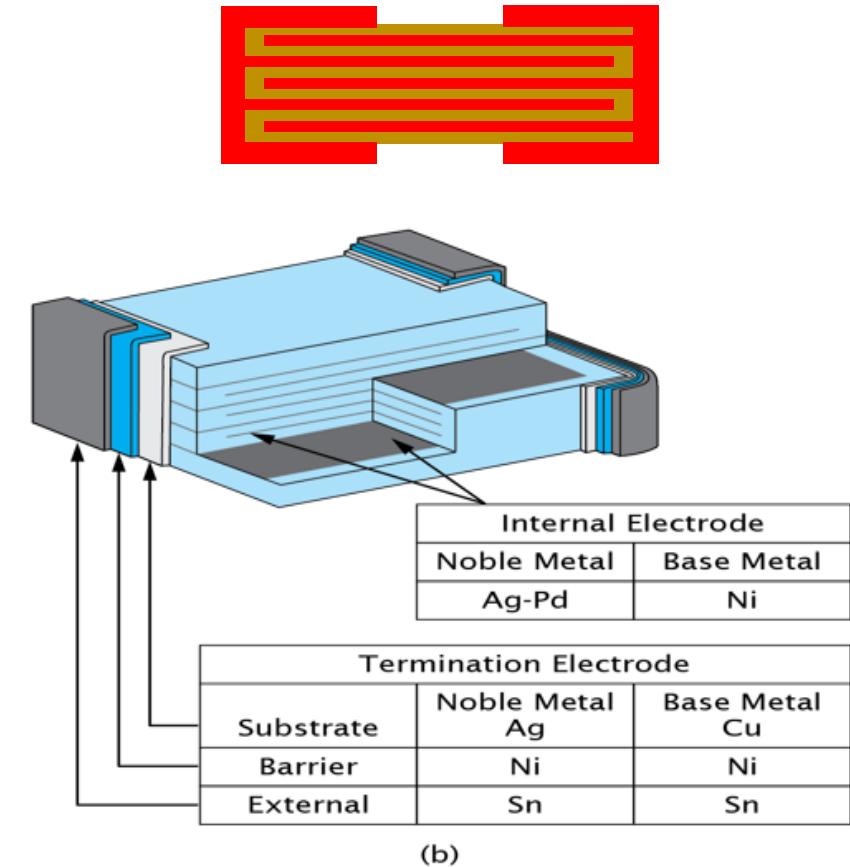
# Integrate Capacitors Closer to the Processor (Need them to be thin and high-density)



# Multilayered Ceramic Capacitors: Achieve highest capacitance densities and lowest parasitics



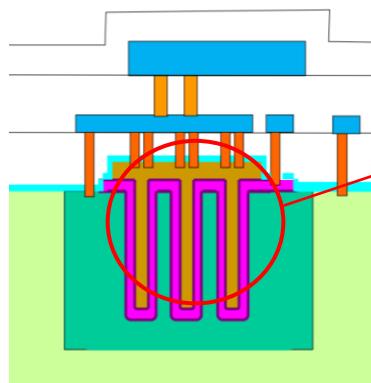
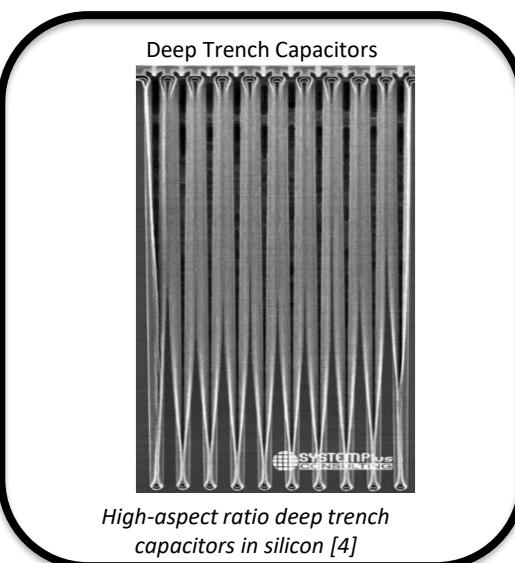
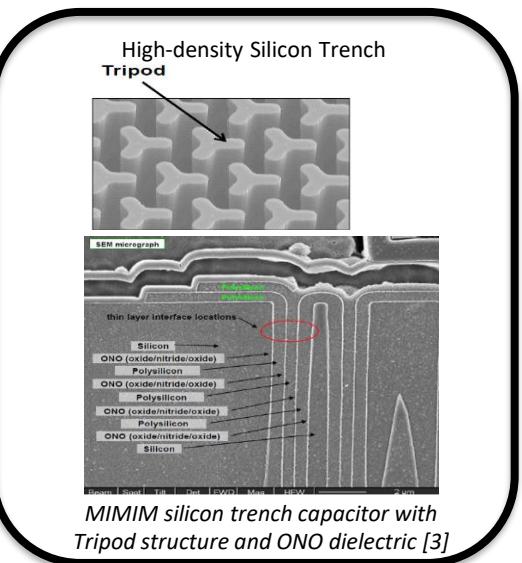
MLCC Fabrication



MLCC Fabrication

# Deep Trench Land-Side Inserted Si Capacitors

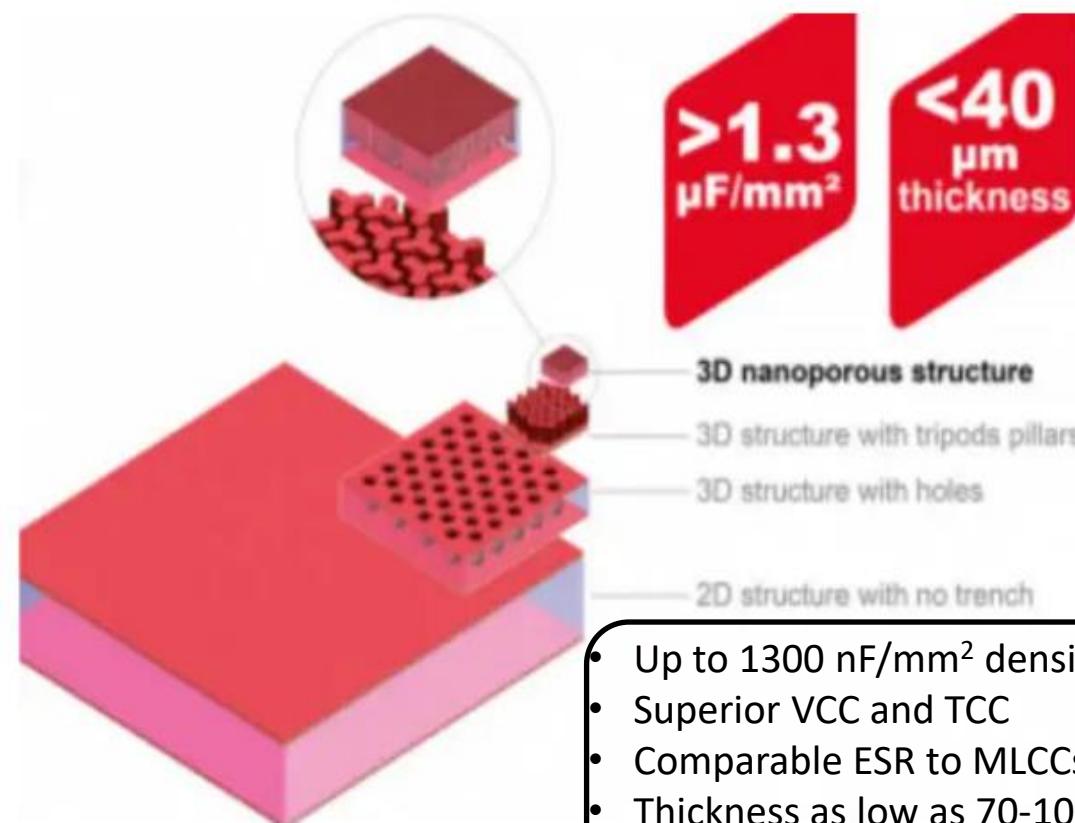
*Land-side on-Si capacitors for integrated fan-out packaging*



Deep trench capacitor structure

- Cost of process
- Density still limited without high-k materials

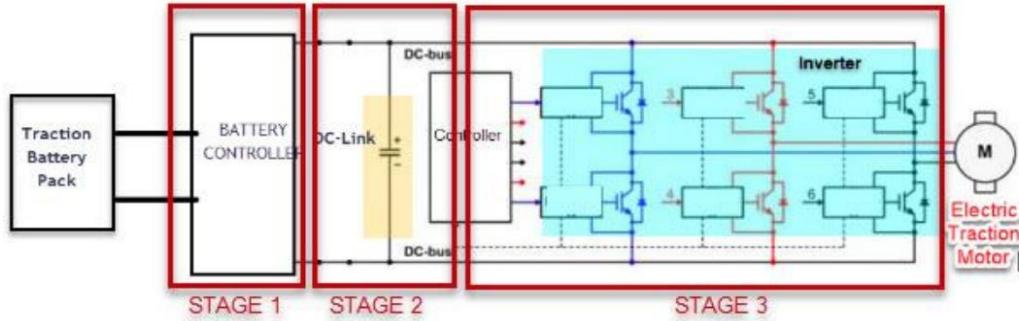
Source: Shinsuke Abe, Murata, powersoc 2021  
Mohamed Jatloui, Murata, 3D PEIM 2023, ECTC 2022



- Up to 1300 nF/mm<sup>2</sup> density
- Superior VCC and TCC
- Comparable ESR to MLCCs
- Thickness as low as 70-100  $\mu\text{m}$

Density, nF/mm <sup>2</sup>	Breakdown Voltage, V	TDDB, V	Max Voltage rating, V
180	16.1	7.0	4.5
250	14.3	6.8	4.2
500	6.5	4.5	3.2
600-700	4.0	3.8	2.5-1.2

# DC link and snubber capacitor in High-Power Inverters



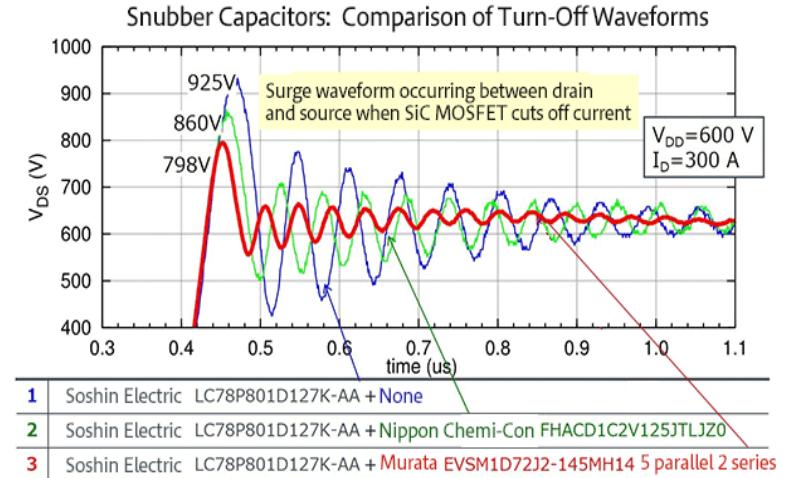
Balance fluctuating instantaneous power on the rails injected by activity from the first and third stages

Stabilizes the “ripple” generated by Stage III’s high-frequency power switching circuits.

The DC-Link capacitor (located in Stage II) must stabilize and smooth out the voltage and current on the rails  
(i.e., decoupling spikes caused by switching).

$$C_{min} = \frac{I_{out} \times dc \times (1 - dc) \times 1000}{f_{sw} \times V_{P(max)}}$$

where  $C_{min}$  = required minimum capacitance,  $I_{out}$  = output current,  $D_{cycle}$  = duty cycle,  $f_{sw}$  = switching frequency,  
 $V_{pp(max)}$  = peak-to-peak ripple voltage.



\*Apart from the position of capacitor installation, the surge voltage also differs for different parasitic inductances due to the circuit structure

Connected to a large-current switching node to reduce parasitic inductance of electric wiring.

Prevents large surges at switch-off (when the current is blocked), so they don't exceed component ratings

The surge waveforms between drain and source when the SiC MOSFET is turned off and current, surge suppression with snubbers are shown

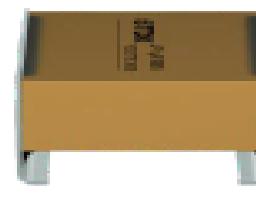
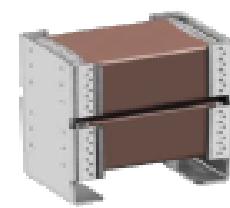
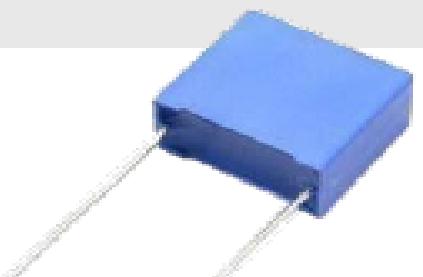
ROHM Electronics

DC Link Capacitor, KEMET

# Comparison of DC capacitors of nominal 1 $\mu$ F/400V<sub>op</sub>

	MKP film capacitor	BTO Class 2 MLCC (e.g. X7T)	CeraLink™
<b>Nominal / rated capacitance</b>	100 %	100 %	100 %
<b>No bias voltage 0.5 V<sub>RMS</sub>, 25°C</b>	100%	100 %	35 %
<b>DC link voltage 0.5 V<sub>RMS</sub>, 25°C</b>	100 %	35 %	60 %
<b>DC link voltage 20 V<sub>RMS</sub>, 25°C</b>	100 %	35 %	100 %
<b>Typical capacitance density @ DC link voltage 20 V<sub>RMS</sub>, 25°C</b>	0.7 $\mu$ F/cm <sup>3</sup>	2.5 $\mu$ F/cm <sup>3</sup>	★ 4.9 $\mu$ F/cm <sup>3</sup>
<b>Typical current rating per capacitance @ 100 kHz, 105°C</b>	<1 A/ $\mu$ F	<4.5 A/ $\mu$ F	★ 12 A/ $\mu$ F

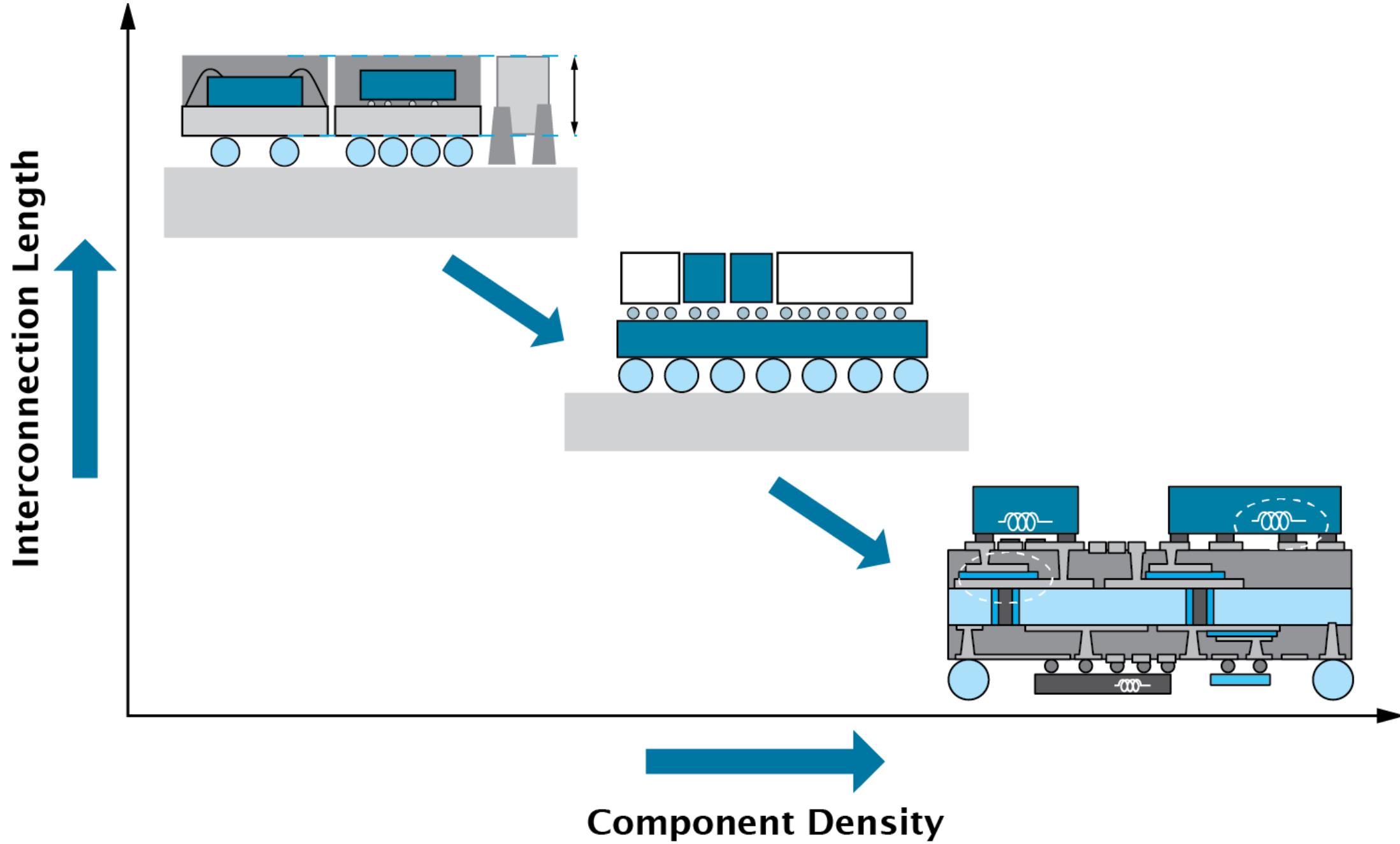
Dan Krueger, TDK



# Summary – Power Modules

- Power delivery in computing systems
  - Integrated voltage regulator: power conversion closer to the load
  - Capacitors and Inductors: >10 MHz; Impedance < 1 milliohms
  - Inductors: High  $L/R_{dc}$  ratio, high current handling, low hysteresis loss

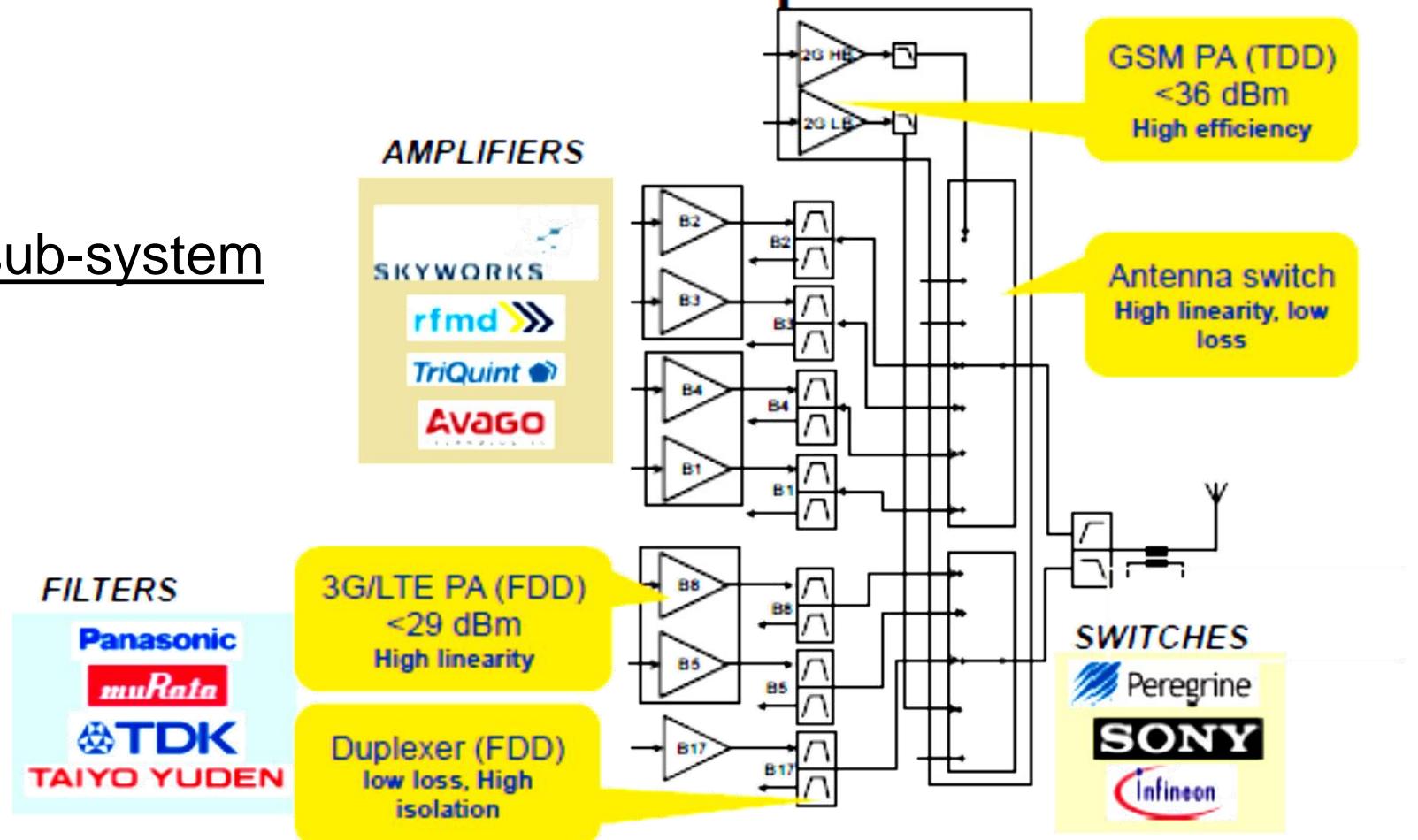
# Passives in RF Modules



# RF Component Integration Needs in Smartphones

## RF Content in a smartphone

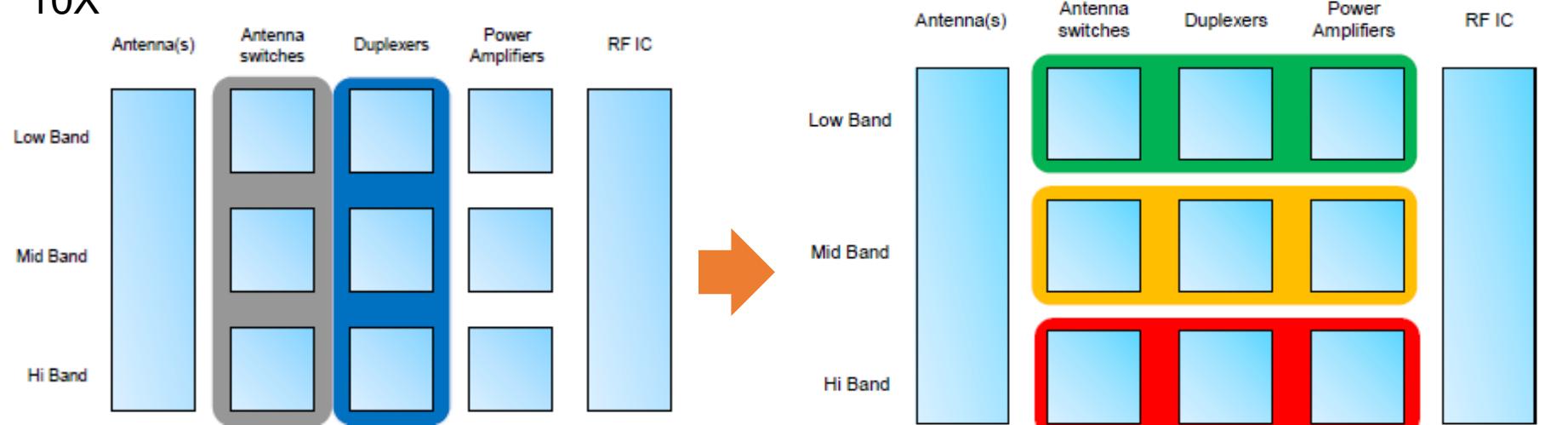
### Example of RF sub-system



Courtesy: Arjun Ravindran and Chrisitan Hoffmann, TDK EPCOS

# Strategic Needs

- More functionality – proliferation of RF bands
- Order of magnitude component density increase
- Order of magnitude reduction in form factor, cost and power consumption
- Components with high Quality factor and linearity
- Higher reliability in spite of increased thermal loads
- Integration of Passive components that typically outnumber the active components by 10X



Integration of individual blocks  
(Eg. Switch bank, Duplexer bank)

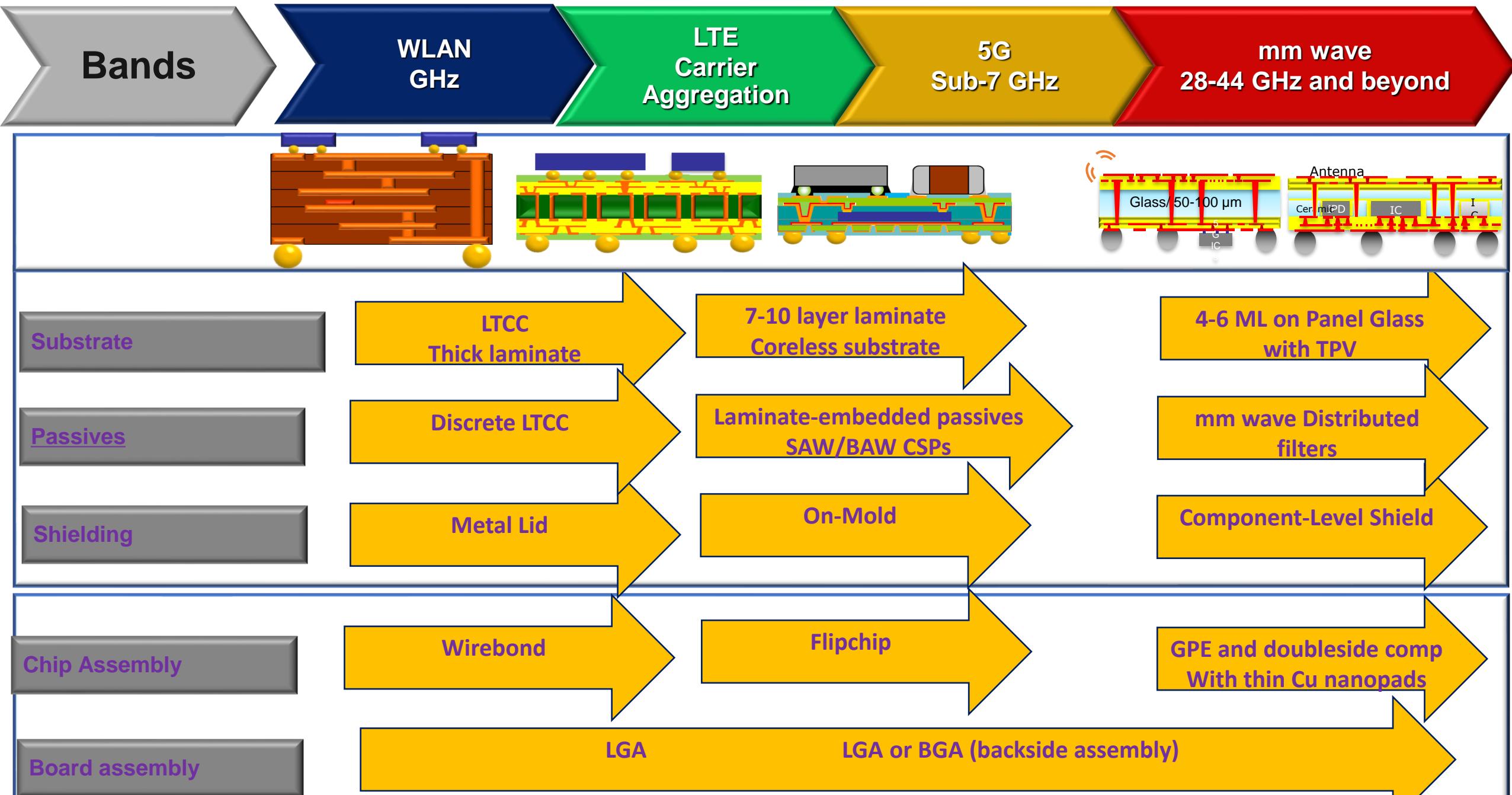
Fully integrated RF Module  
(PA with switch and duplexer)

# Materials: LTCC to Laminates, FOWLP and Glass

- Glass is a promising candidate for next-generation substrate material for 5G applications

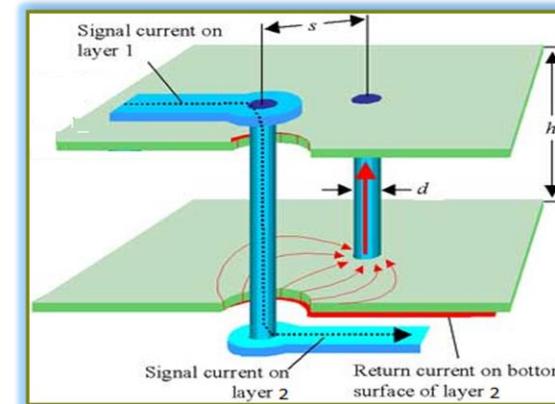
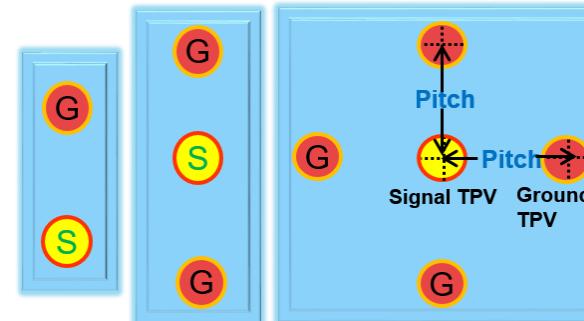
	Flip-Chip			Chip-Embedding	Flip-chip & Embedding
Characteristic	PCB-based	LTCC	Organic laminates	FO-WLP	Glass
<b>Material Properties</b>					
Relative dielectric constant ( $\epsilon_r$ )	4	5 – 10	2.9-3.2	3.68	2.7 – 7
Loss tangent $\times 10^4$ ( $\tan\delta$ @ GHz)	20 @ 10	12 @ 10	40 @ 60	80 @ 58	3 – 50 @ 10
Surface roughness (nm)	300-5800	177	400-600	> 1000 on EMC	<1
Coefficient of thermal expansion - CTE (ppm/K)	17	5.5 – 7.2	17	30 (EMC)	3-8.5
Dimensional stability - Young's Modulus (GPa)	21 – 24	90-150	10-40	22	50-90
Water absorption	0.1%-0.25%	0	0.040 %		0
<b>Process Challenges</b>					
Multi-layer process alignment					
Small-feature patterning					
Thin substrate reliability	Warpage		Warpage		Cracking

# RF Module Evolution of technology Blocks



# Why Laminated Glass for RF?

- High-density and low-loss transmission lines:
  - High-density RF and digital in the same package
- Seamless layer-to-layer and 3D interconnects
  - Impedance-matched TPVs
  - Minimal signal discontinuities and reflections with ultra-fine vias and pads
  - Better termination of E-fields with multiple ground vias or arrays – Lower noise coupling with less mutual and self-inductance
  - Minimal ground bounce and resonance effects with small clearances (less intrusion) in power planes
- Precision circuitry for impedance matching
- Smooth surface for low losses
- Package- and board-level reliability
- Availability in 30-100 microns
- Large-area panel processing

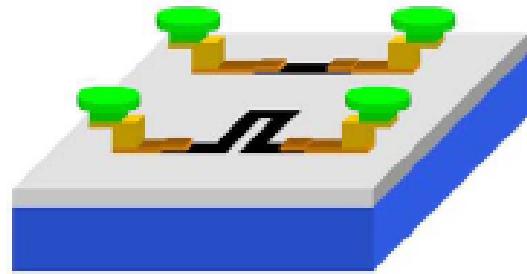


Wafer  
~ 600  
Packages  
(8mm x  
8mm)

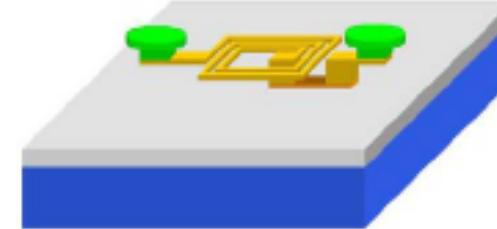
8X lower cost

Panel  
~ 4800  
Packages  
(8mm x 8mm)

# Passive Components – Building Blocks



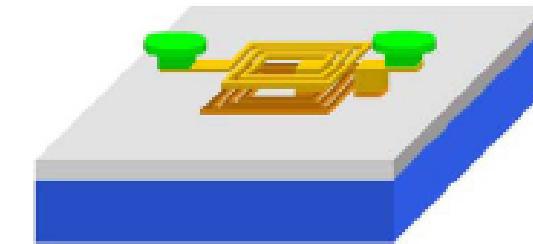
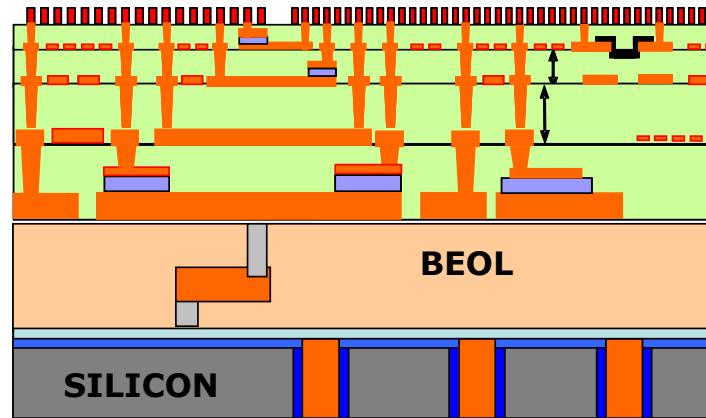
Resistor



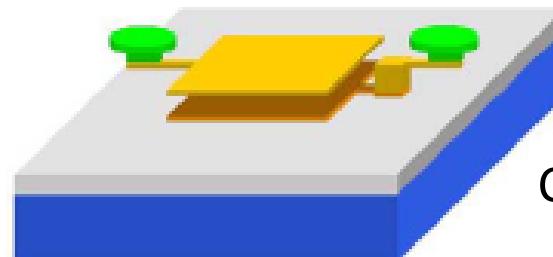
Single layer coil



Transmission line



Double layer coil



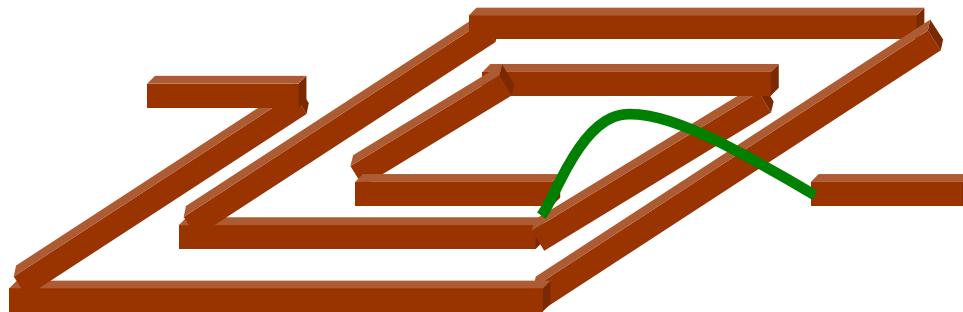
Capacitor

# RF Inductor Options

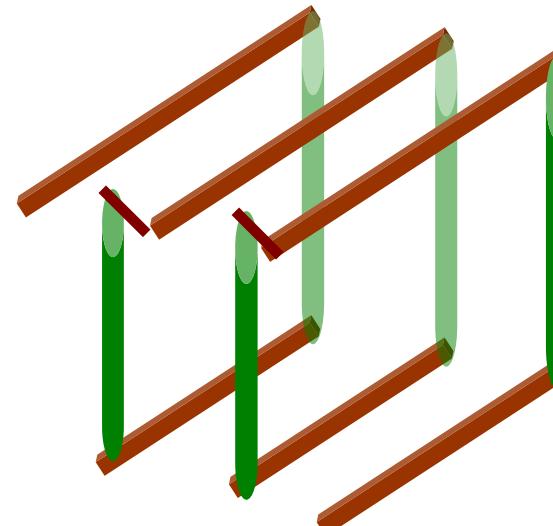
Si	LTCC	Organic-Thick (LCP)	Glass IPDs
<ul style="list-style-type: none"><li>■ Low Q (&lt;15)</li><li>■ Low L (&lt;5 nH)</li><li>■ Lower frequency</li><li>■ Precision</li></ul>	<ul style="list-style-type: none"><li>■ High Q( &gt; 100)</li><li>■ High L ( &gt; 20 nH)</li><li>■ Higher frequency (up to ~ 110GHz)</li><li>■ High cost</li></ul>	<ul style="list-style-type: none"><li>■ High Q (&gt;200)</li><li>■ High L (&gt;20 nH)</li><li>■ Low to High frequency (up to ~110 GHz)</li></ul>	<ul style="list-style-type: none"><li>■ High Q( &gt; 100)</li><li>■ High L ( &gt; 20 nH)</li><li>■ Higher frequency</li><li>■ Precision</li><li>■ <b>LOW COST</b></li></ul>

# Inductor Designs

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**SPIRAL INDUCTORS**



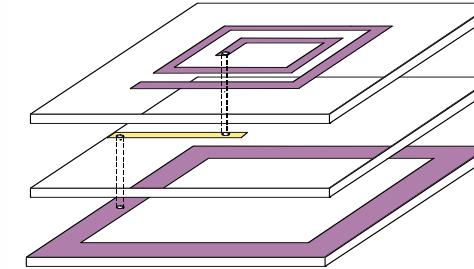
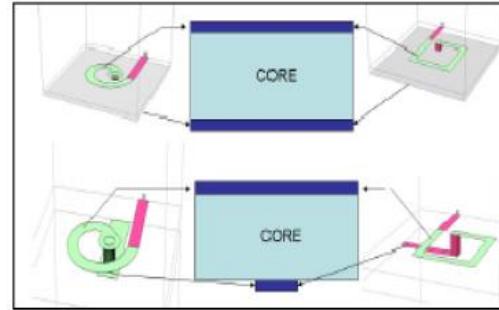
**HELICAL INDUCTORS**

# Leading-Edge RF Inductors

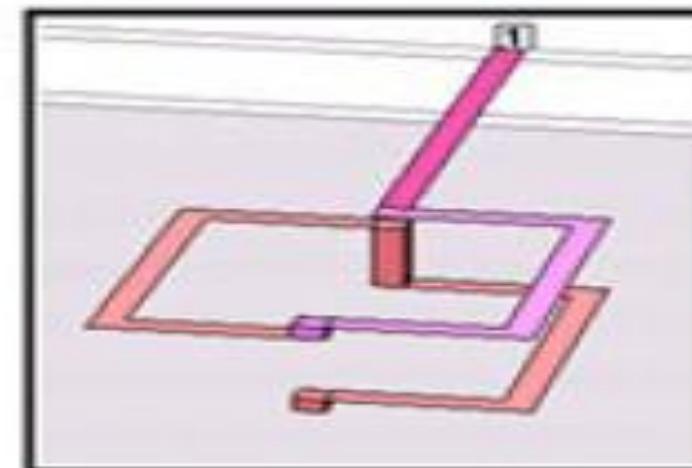
	Objectives	Prior Art	Challenges
Performance with miniaturization	<ul style="list-style-type: none"><li>• 3-10 nH for</li><li>• 1 mm<sup>2</sup></li><li>• <b>Q &gt; 100 at 2.4GHz</b></li><li>• SRF &gt; 10GHz</li><li>• <b>50-100 μm</b></li></ul>	<p><b>Qualcomm glass inductor:</b></p> <ul style="list-style-type: none"><li>• 3D inductor</li><li>• 1.8 – 4.5nH</li><li>• Q ~ 60 at 1GHz</li><li>• Glass thickness : 250 μm</li></ul> <p><b>TSMC glass inductor:</b></p> <ul style="list-style-type: none"><li>• 2D inductor</li><li>• Glass thickness : 50μm</li><li>• Q range: 27 - 30</li></ul> <ul style="list-style-type: none"><li>• 3D inductor</li><li>• Glass thickness : 200μm</li><li>• Q range: 56 - 63</li></ul>	<ul style="list-style-type: none"><li>• Trade-offs in Q and inductance density</li><li>• Limited Q enhancement with spiral inductors;</li><li>• 3D inductors with solenoid structures utilize TPVs that add cost</li><li>• Deviation in electrical characteristics because of process variation in Cu TPV thickness, line width and space</li></ul> <ul style="list-style-type: none"><li>• Introduction of magnetic films enhances inductance density but creates additional losses</li></ul>

# Design Approaches to High Q

- Create ground plane opening under inductor footprint;
- Circular loops instead of rectangular
- Increase spacing and create off-set between half loops; Decrease series capacitance with increased spacing between the loops
- Optimize line-width and spacing for high Q and inductance density



Hollow ground



# Integrated Resistors

Material	Resistivity Range ( $\mu\Omega\text{-cm}$ )	Film Thickness	Sheet Resistance ( $\Omega/\text{square}$ )	TCR (ppm/ $^{\circ}\text{C}$ )
TaN <sub>x</sub> , CrSi, NiCr, TiN <sub>x</sub> , NiP	100 - 500	500 Å	20 - 100	+/- 50 with process optimization
NiP (Ohmega-Ply®)	~2000	1000 - 4000 Å	up to 250 1000 in development	0 - 100
NiP (MacDermid)			up to 100 higher in development	
TiN <sub>x</sub> O <sub>y</sub>	up to 7000	500 Å	up to 1400	+/- 100 with process optimization
LaB <sub>6</sub> (DuPont)	$10^7$	10 $\mu\text{m}$	10,000	+/-200
PTF (several vendors)	very wide, depending on filler	1 - 2 mil	$10 - 10^7$	~200
cermets	$10^4 - 10^{10}$ depending on metal/glass ratio	1 $\mu\text{m}$	$100 - 10^8$	close to zero or slightly negative

Key is to achieve:

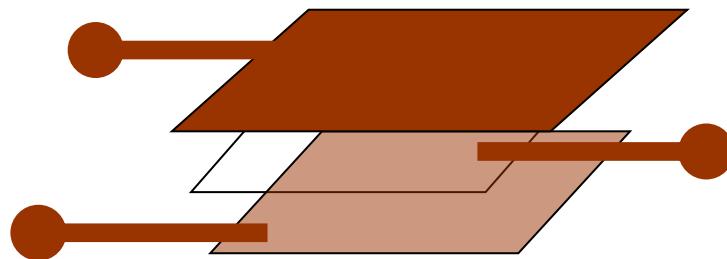
Tolerance (<5%)

Stability with temperature and humidity

Easy integration with minimum process compatibility issues

# RF Capacitor Requirements

Application	Req. Range	Q Factor	Tol.	Freq.	Comments
RF Filter Cap.	1-100pF	>100	<5%	0.1-8 GHz	<ul style="list-style-type: none"><li>• High self resonance freq.</li><li>• Large Q values</li></ul>
Matching	1-100 pF	>100	<5%	1-10 GHz	<ul style="list-style-type: none"><li>• Tight tolerance required</li></ul>



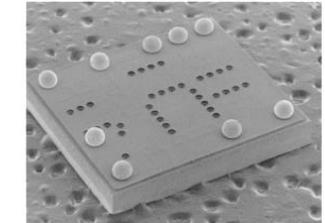
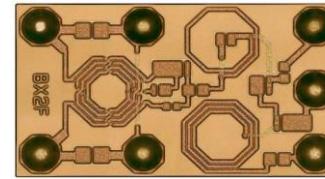
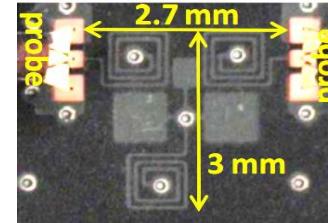
**PARALLEL PLATE CAPACITORS**



**INTER-DIGITAL  
CAPACITORS**

# RF Passive Technology Evolution

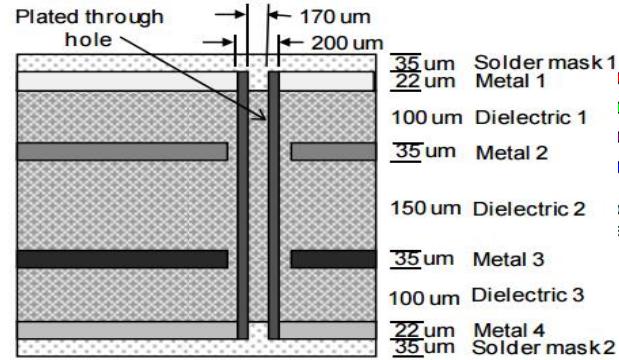
- Lower loss and higher band-selectivity – Components with higher Q
- Thickness and footprint reduction
- Utilization of thinfilm technology for higher density
- Integration of discrete passive components into IPDs



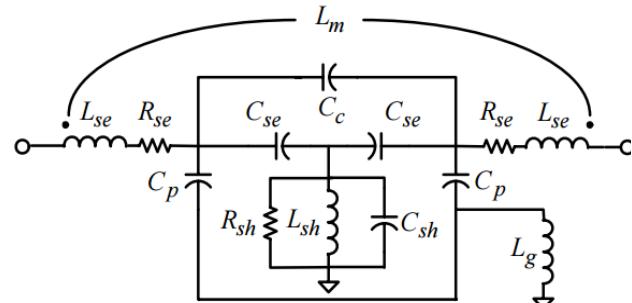
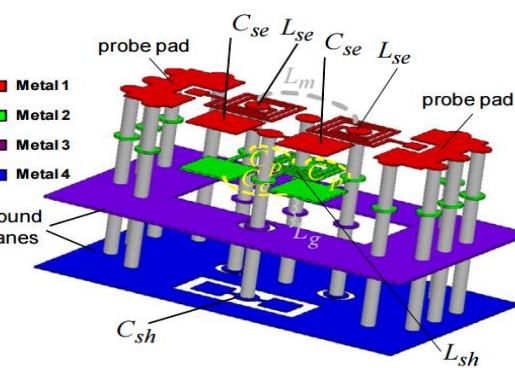
	LTCC	Laminate	Silicon	Acoustic Wave	3D Glass
Performance	Low loss	Substrate loss	Substrate loss	High selectivity	Low loss
Thickness	Thick	Thin	Thin	Thin	Thin
Size	Small footprint	Moderate footprint	Moderate footprint	Small footprint	Small footprint
Density	Low density	Moderate density	Moderate density	High density	High density
Frequency	Low - high	Low - moderate	Low - moderate	Low	Low - high
Cost	Mass production	Less in demand	High	High	Not in market

# RF Passives - Laminates

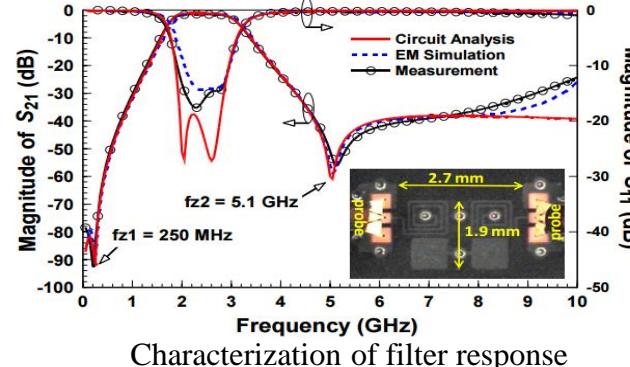
## C.-H. Chen, et al., Bandpass Filter on BT



Substrate stack-up and filter EM model



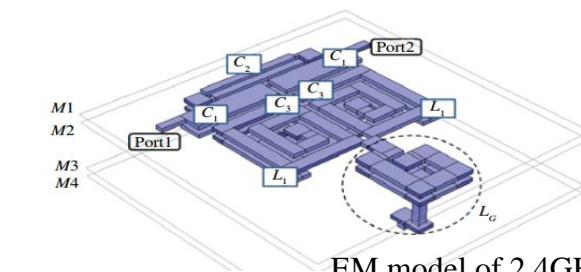
Filter equivalent circuit model



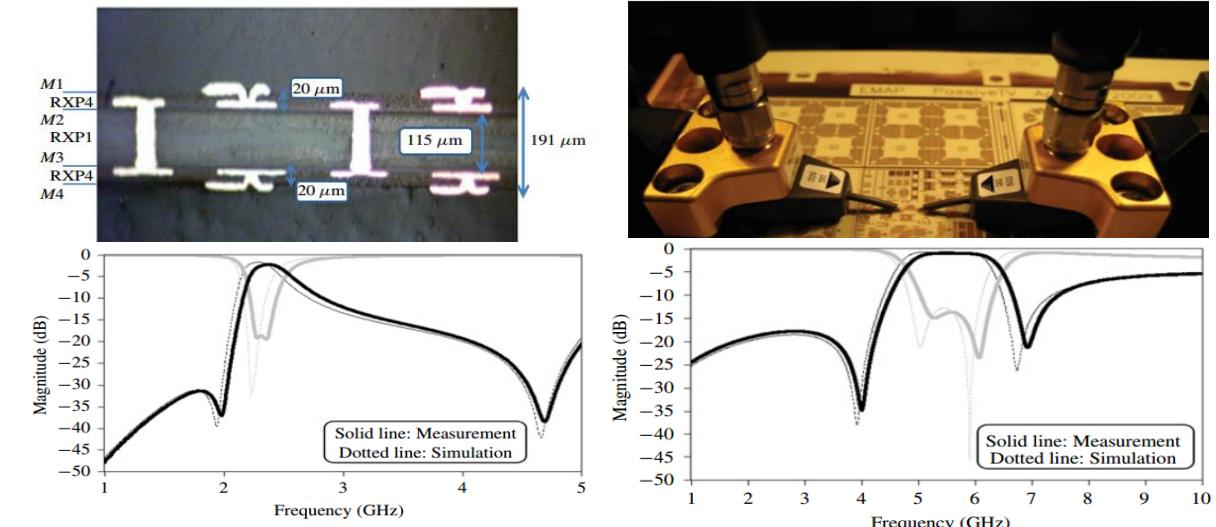
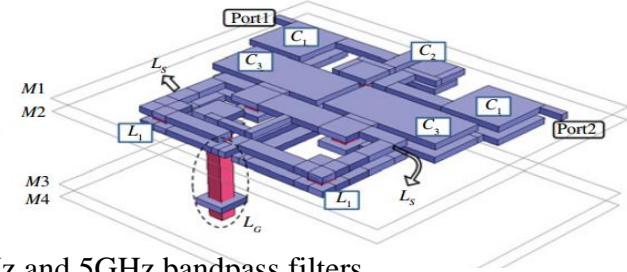
Characterization of filter response

- ✓ High rejection with multiple transmission zeros
- ✓ Double-side passives integration
- ✓ Small size ( $2.9 \text{ mm} \times 1.7 \text{ mm}$ )
- ✗ Large thickness ( $> 0.5 \text{ mm}$ )
- ✗ Moderate loss (1.6dB passband IL)

## Seunghyun H., et al., Bandpass Filters on RXP



EM model of 2.4GHz and 5GHz bandpass filters

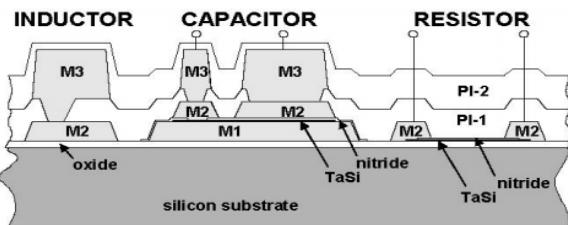


Fabrication and characterization results of 2.4GHz and 5GHz bandpass filters

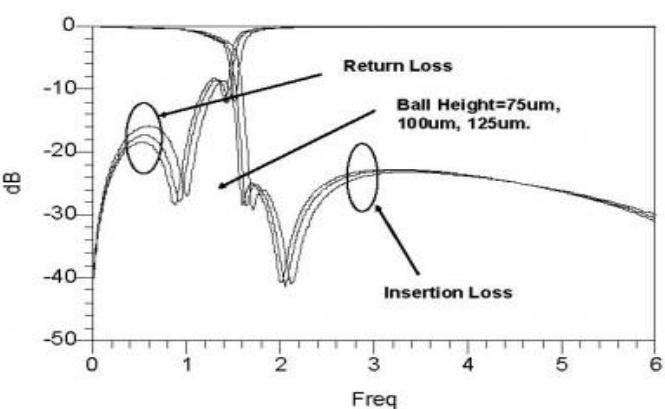
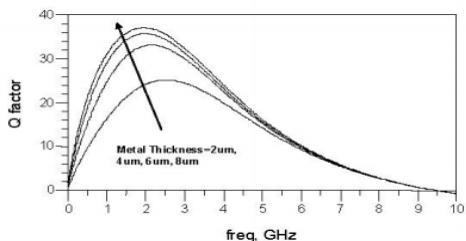
- ✓ Double-side passives integration
- ✓ Small size ( $2.2 \text{ mm} \times 3 \text{ mm} \times 0.2 \text{ mm}$  @ 2.4GHz)
- ✗ Moderate loss (0.97dB @ center freq)
- ✗ Process variation induced band deviations

# Silicon IPDs

## Kai L., et al., Lowpass Filter on Silicon



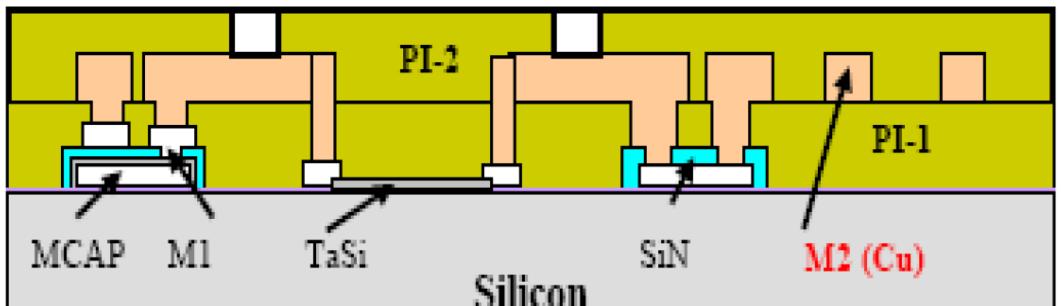
X-section of silicon IPDs



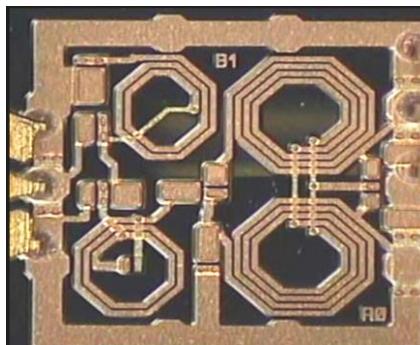
- ✓ High rejection
- ✓ High-density thinfilm capacitors
- ✓ Small size ( $1 \text{ mm} \times 0.85 \text{ mm} \times 0.35 \text{ mm}$  including ball height )
- ✗ Moderate loss (0.55dB @ 850 MHz)
- ✗ High-cost BEOL process

## Silicon

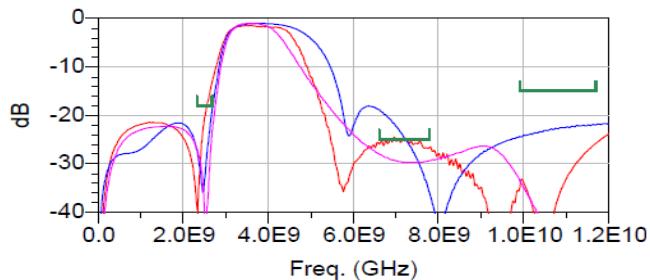
## Arun Chandra K., et al., Diplexer on Silicon



X-section of silicon IPDs



Fabricated IPD

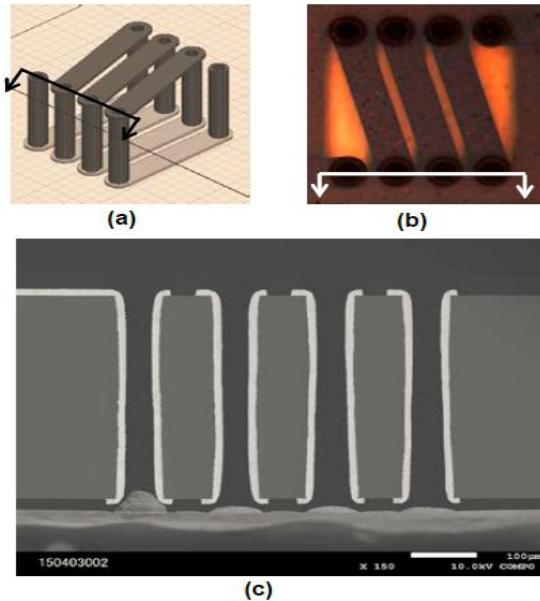


Comparison of diplexer performance on LTCC, silicon and glass (Red: Silicon)

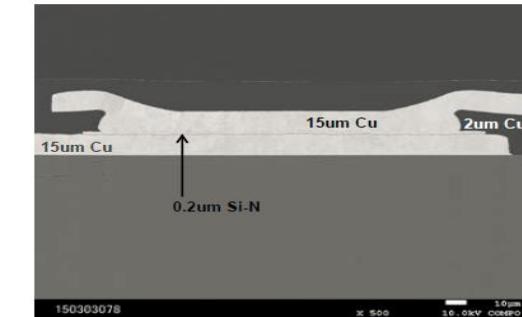
- ✓ Integration high-density thinfilm capacitors
- ✓ Small size ( $1.55 \text{ mm} \times 1.55 \text{ mm} \times 0.25 \text{ mm}$ )
- ✗ Higher loss compared to LTCC and glass
- ✗ Single-side passives integration

# Glass IPDs from GT-PRC Partners : Corning, Qualcomm, Unimicron

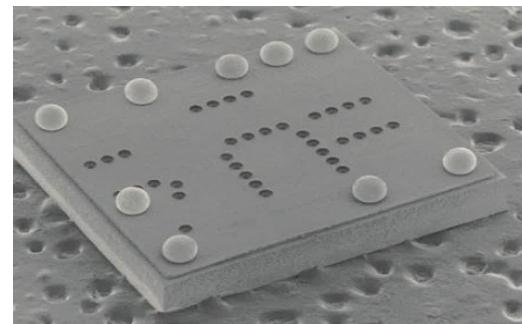
## A. B. Shorey, et al., TGV Technology for RF Corning Inc and Qualcomm



TGV-based high-Q inductors

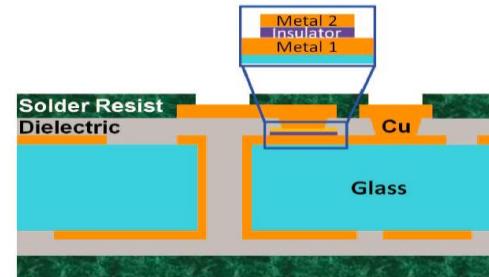


X-section thinfilm MIM capacitors (Si-N)

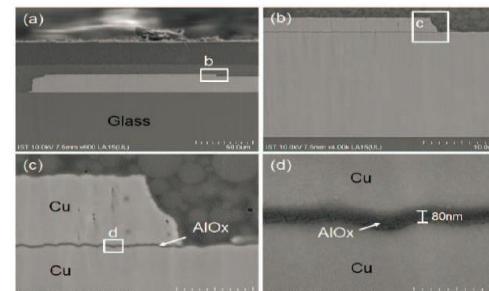


SEM image of LC filters on glass for RF

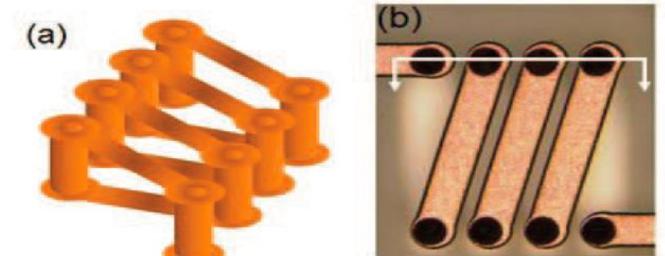
## Yu-Hua Chen, et al., Glass IPD Manufacturing Unimicron



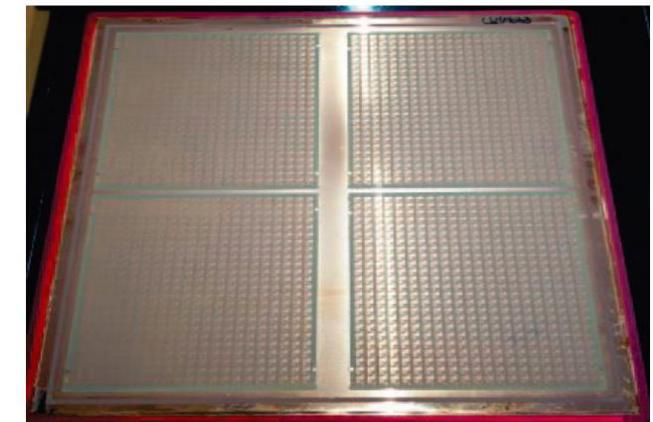
X-section of glass IPDs



X-section of thinfilm MIM capacitors (Al-O)



TGV-based high-Q inductors

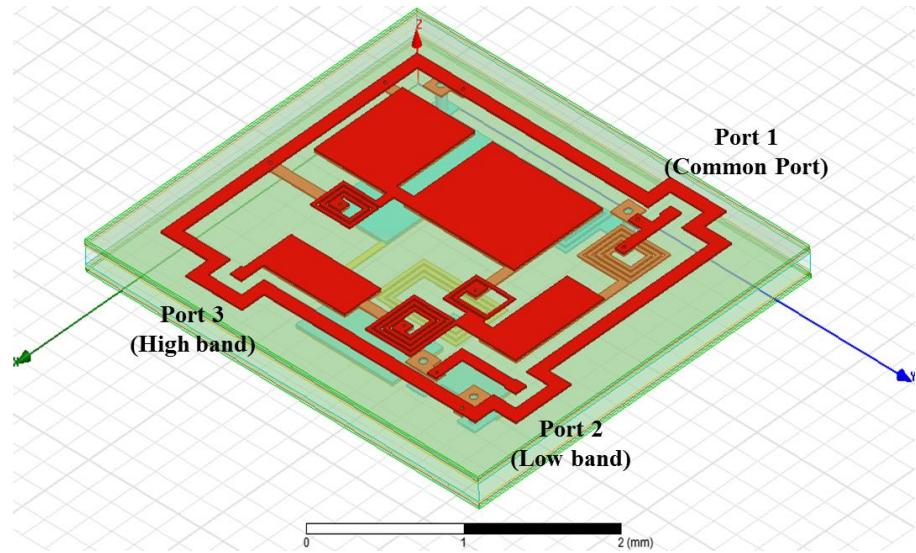


Manufactured 508mm x 508mm glass (300um thick) panel

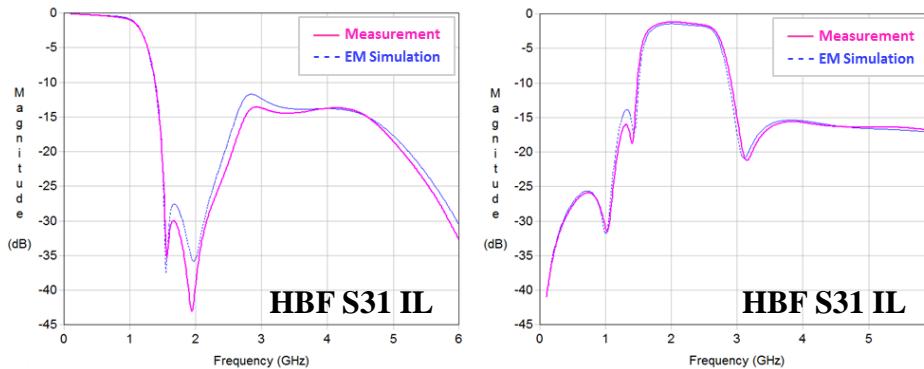
- ✓ Capability of scaling to panel size for potential low cost
- ✓ High performance due to high-Q passives
- ✗ Process precision control

# 3D IPDs on Glass

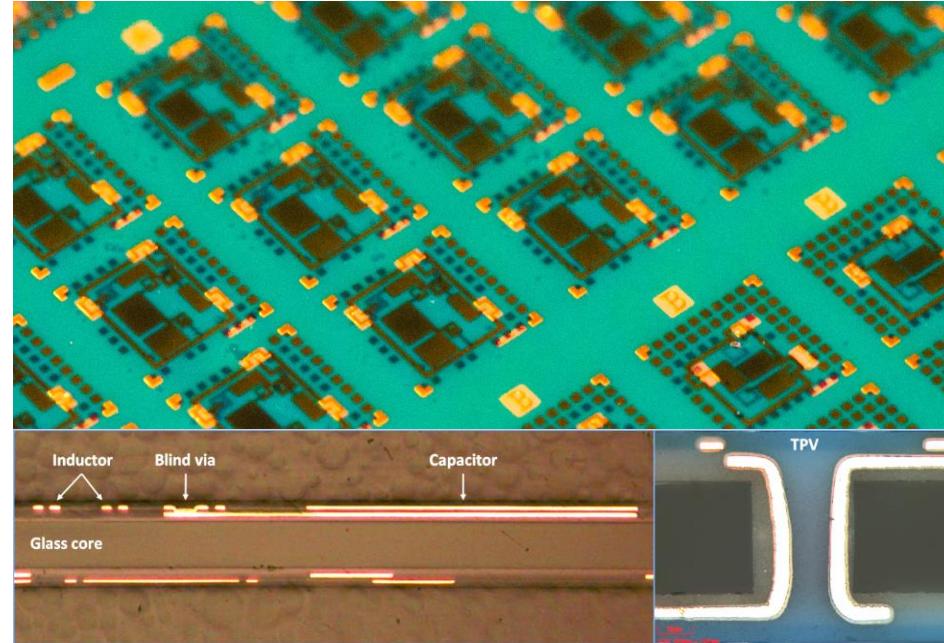
## 3D IPD LTE Diplexers on Glass



*EM model of designed LTE diplexer*



*Good correlation between simulation and measurement*

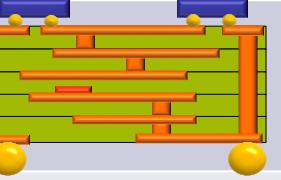
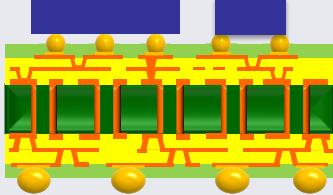
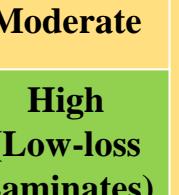
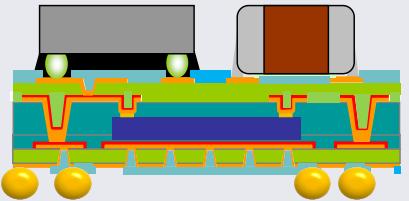
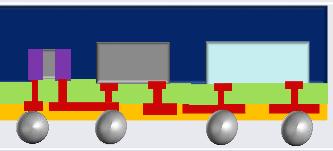


*Fabricated diplexers on 6'' × 6'' glass panel*

- ✓ Double-side integration of passives on glass
- ✓ Ultra-small size: 2.3 mm × 2.8 mm × 0.2 mm
- ✓ Good process variation control

*Courtesy: Zihan Wu, GT-PRC*

# RF Module and Key Performance Indices

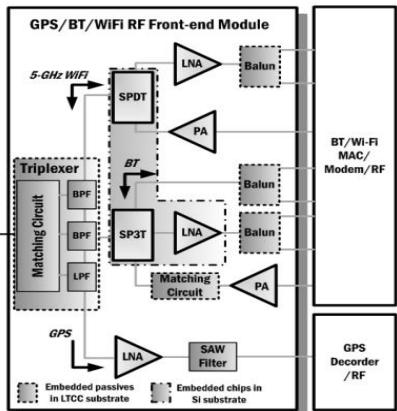
Technology		Performance	Thickness	Footprint	Component Density	Cost
Modules on LTCC		High	Thick	Small	Moderate	Moderate
MCMs on laminates		Moderate	Moderate	Large	Low	Low
		High (Low-loss Laminates)				
Embedding in Laminates		High	Thin	Small (Chip-first)	Moderate (Chip-first)	Low (Chip-last)
Fan-out wafer-level packaging		High	Thin	Moderate	Moderate	
3D IPAC on Glass		High	Ultra-thin	Small	High	Low

- Module thickness reduction
- Passives or actives embedding for interconnection loss reduction
- Components with higher Q
- Increasing need for component-level electromagnetic interference (EMI) shielding

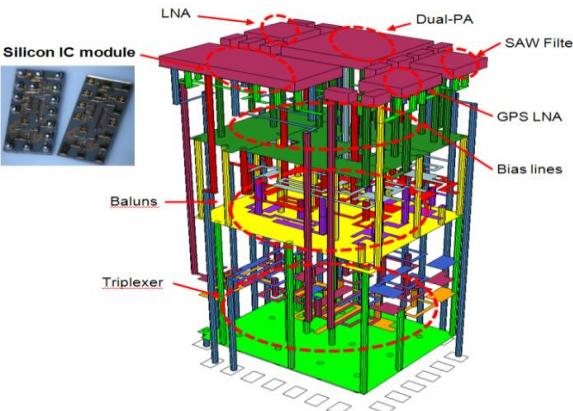
# Modules: LTCC to Laminates

LTCC

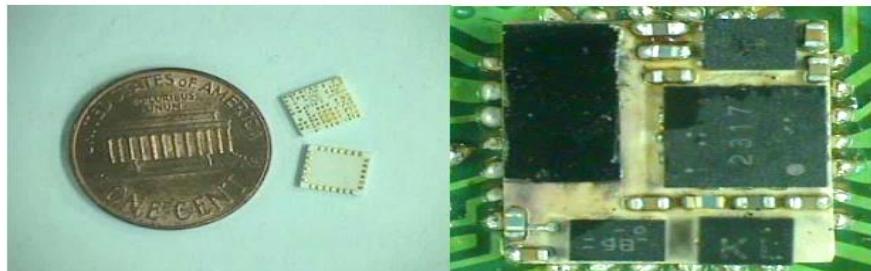
Beom Cheol Ham, et al., GPS/BT/WiFi Triple-mode RF FEM on LTCC Substrate



Block diagram of GPS/BT/WiFi RF FEM



3D FEM model

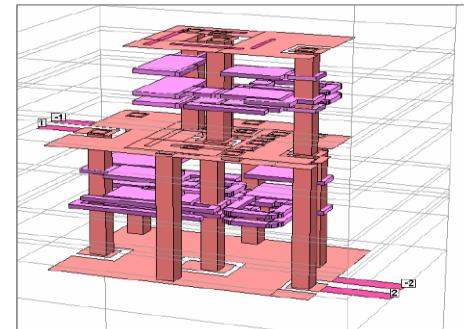


Fabricated RF FEM

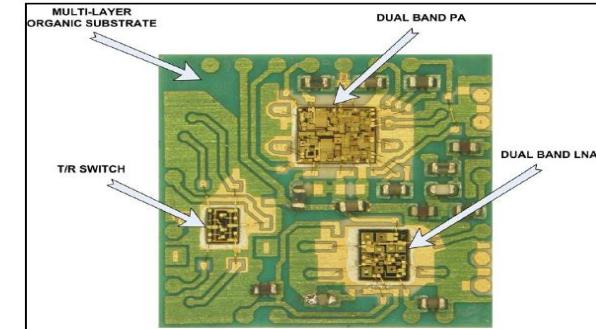
- ✓ Low loss
- ✓ Small footprint due to passive embedding
- ✗ Large thickness

Module on Laminate

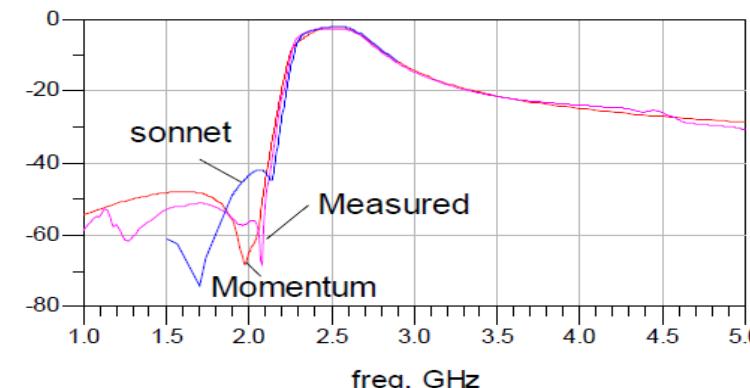
Dalmia et al., RF FEM on LCP Substrate



Substrate-embedded IPDs



MIMO FEM



Measurement vs.  
Simulation

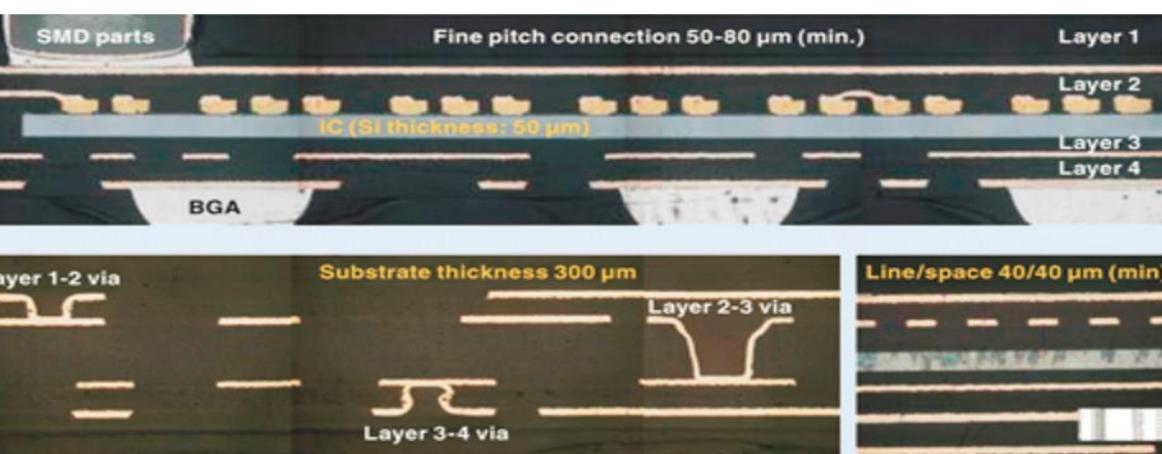
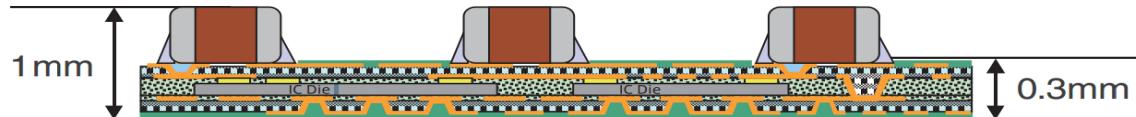
- ✓ Low cost approach
- ✓ Substrate-embedded passives
- ✗ Low component density
- ✗ Process precision control

# RF Modules - Embedding

## Embedding in Laminate

TDK, Semiconductor Embedded in Substrate

### Cross-section view of SESUB



Cross-sectional images of fabricated module package

- ✓ Ultra-short interconnections leading to low loss
- ✓ Small thickness due to semiconductor embedding
- ✗ Die loss due to chip-first embedding

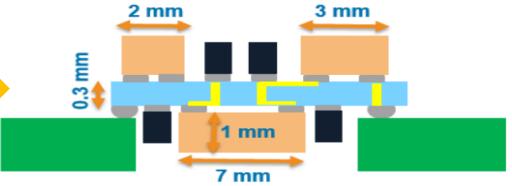
## 3D Module on Glass

TE Connectivity, RF Module using Glass Interposer Technology

### Current Layout



### Layout using 3D bonding on thin Glass Interposer



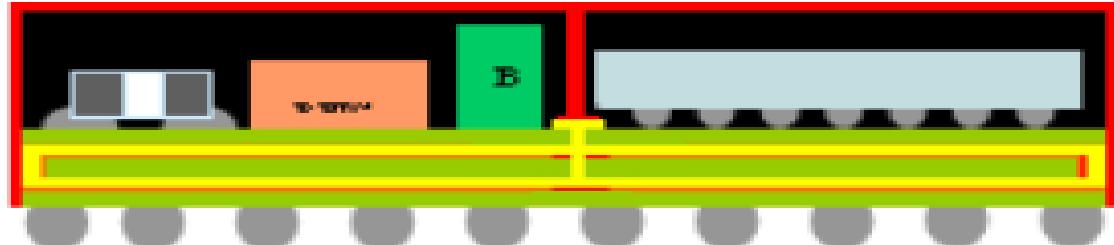
Top side of glass module



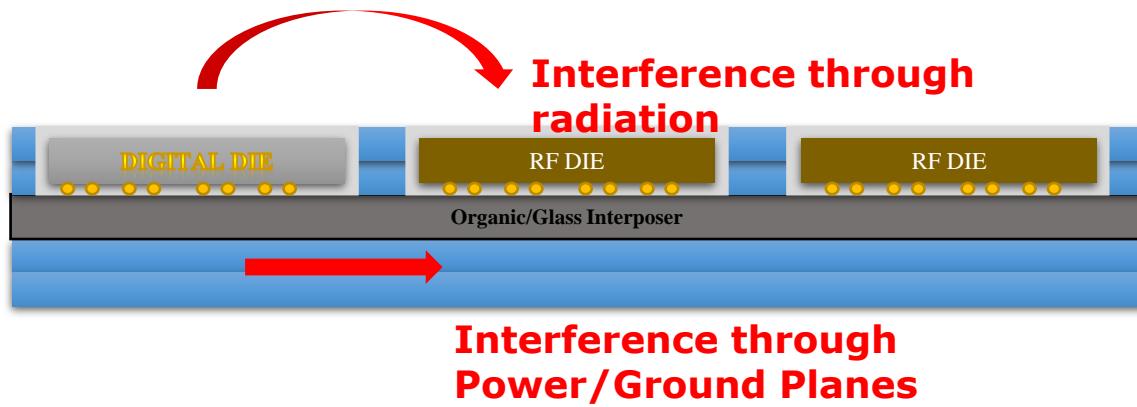
Back side of glass module

- ✓ Double-side assembly of components
- ✗ Large thickness
- ✗ Discrete components
- ✗ Complicate board-level assembly

# EMI Shielding



Today's molded package-level shielding



Future shielding need for embedded components

Shield Effectiveness = Absorption loss (A) + Reflection loss (R)+ Effect of thin shields (B)

Effect of thin shields lowers the shield effectiveness (negative term).

Therefore, thickness of shield is critical for effectiveness.

# Passives in 5G and Beyond

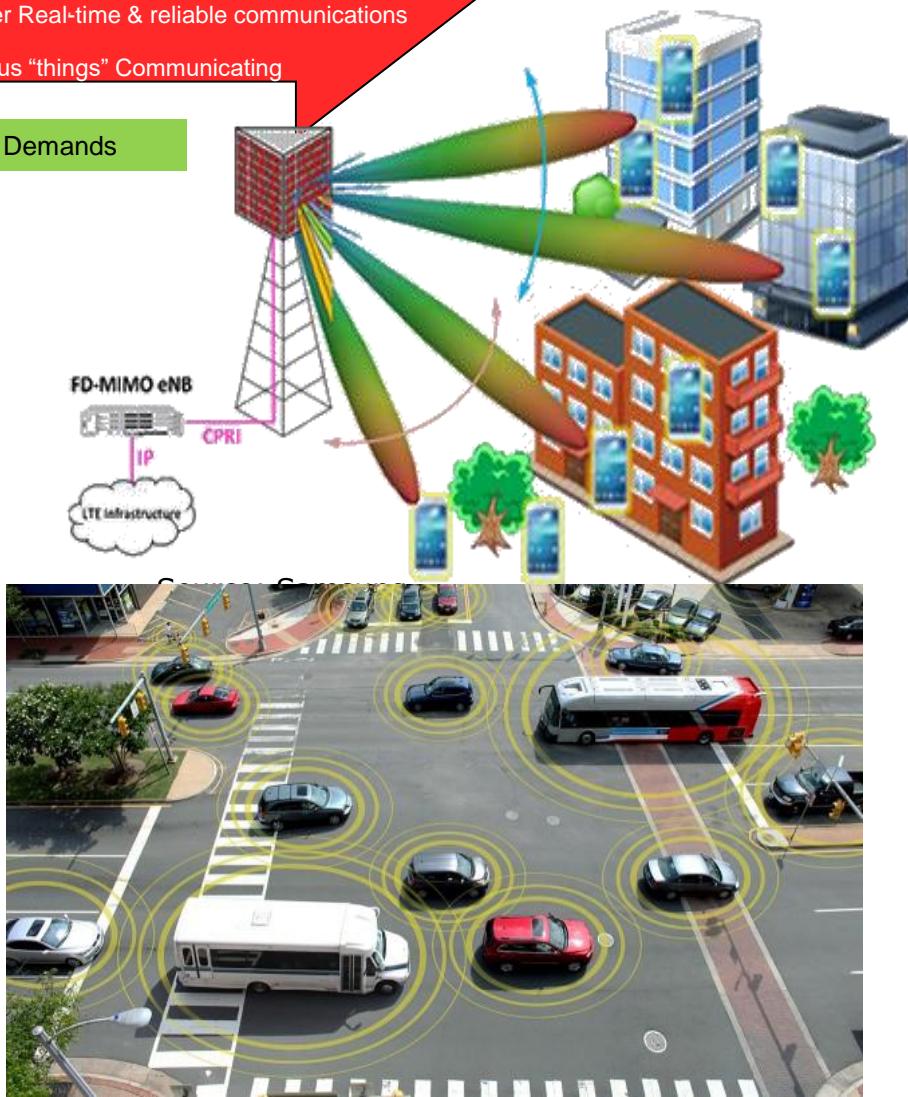
Amazingly Fast

Great Service in a crowd

Super Real-time & reliable communications

Ubiquitous "things" Communicating

New Market Demands

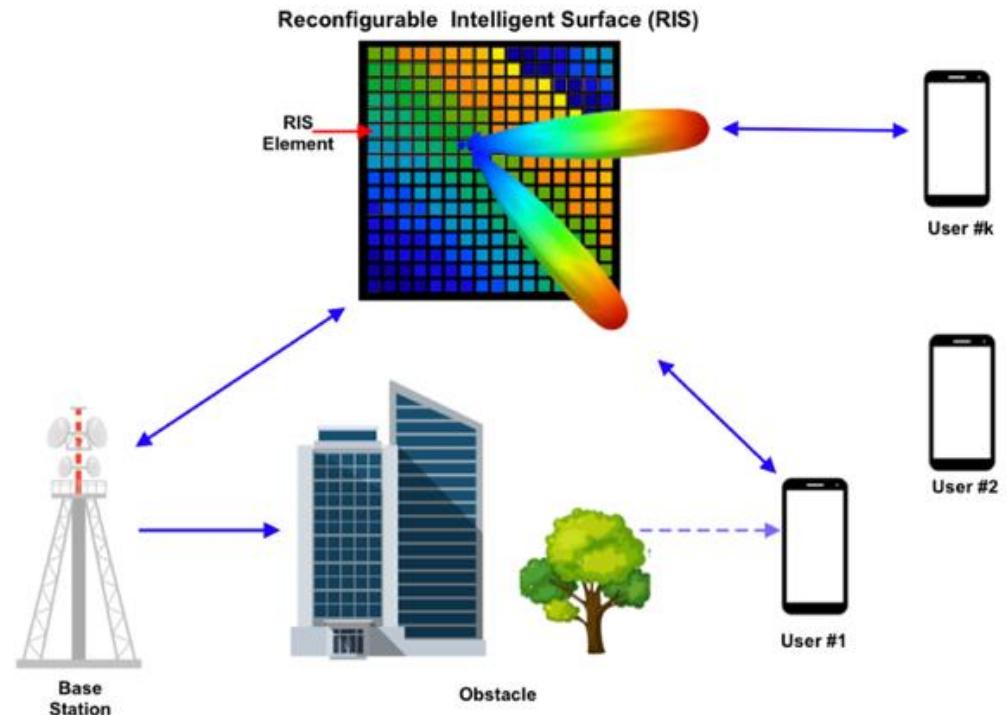


Source: <https://www.extremetech.com/extreme/176093-v2v-what-are-vehicle-to-vehicle-communications-and-how-does-it-work>

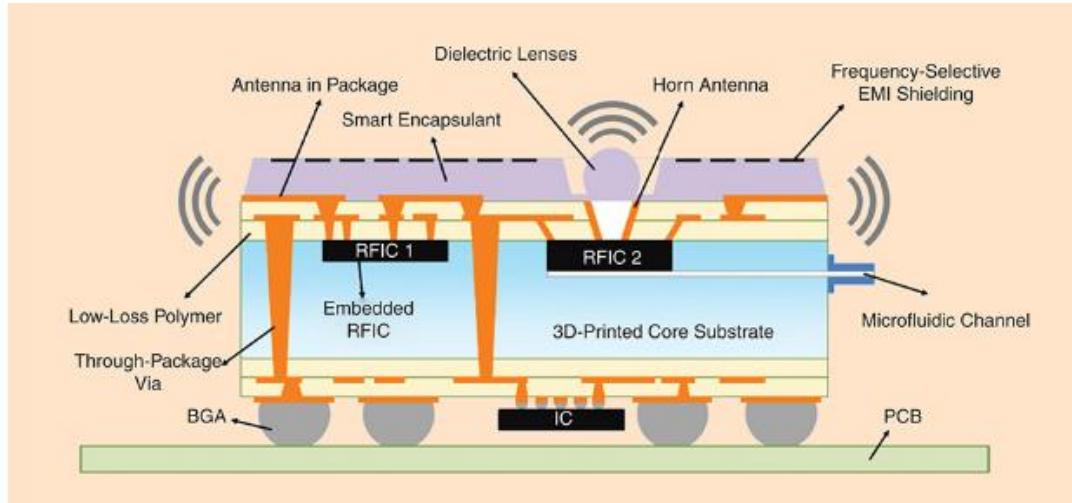
Small wavelengths at 5G/6G mm-Wave frequencies are subject to path losses and multipath scattering leading to beam blockage

**Reconfigurable Intelligent Surfaces (RIS)** supersede relay performance using large apertures with simple circuitry.

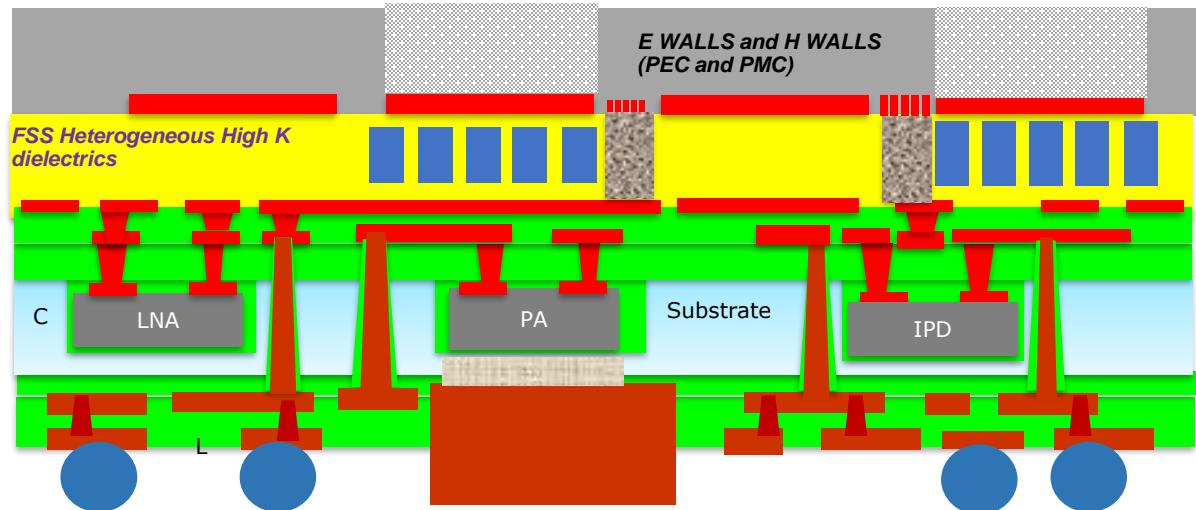
- ✓ Spectrally more efficient
- ✓ RIS reduce hardware complexity.



# 5G/mmWave Package Integration



- High-density and low-loss transmission lines:
- Ultra-fine vias and TPVs for seamless 3D interconnects
- Precision circuitry for impedance matching
- Smooth surface for low losses



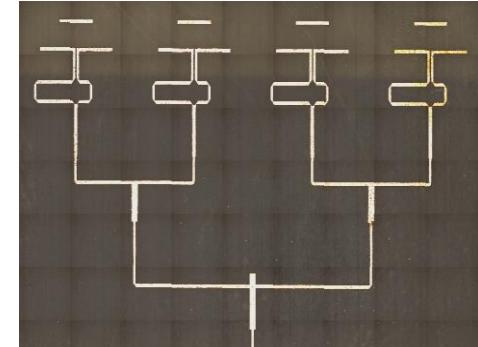
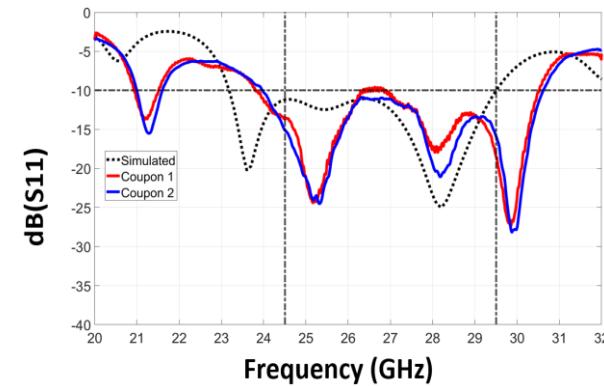
- RF and digital in the same package
- Advanced antenna array for wideband and gain
- Embedded FSS for improved performance
  - Heterogeneous high-K superstrates as lenses,
  - E walls, H walls, AMCs
- Package- and board-level reliability
- Large-area panel processing

	LTCC	Laminates	Glass
Substrate thickness	>500 mm	>300 mm	<150 mm
Feature size with 5% precision	100 µm	40-50 µm	10-20 µm
Through-via diameter and pitch	100µm/ 300µm	100 µm / 300 µm	25 µm/ 50 µm
Through-thickness variation	>25 µm	>10 µm	0.5 -1 µm
Manufacturing Panel size (metric for cost)	150-200 mm	510 mm	510 mm

# Power Dividers and Antenna Arrays in Package

Power-dividing networks and High-Gain Antenna Arrays

Power Divider and Yagi-Uda Antenna Array	Added Insertion Loss	Realized Gain (27 GHz)	Antenna Array Efficiency
Two-Way, 2x1	0.4 dB	6.96 dBi	80%
Three-Way, 3x1	0.6 dB	8.24 dBi	85%
Four-Way, 4x1	0.86 dB	9.51 dBi	82%



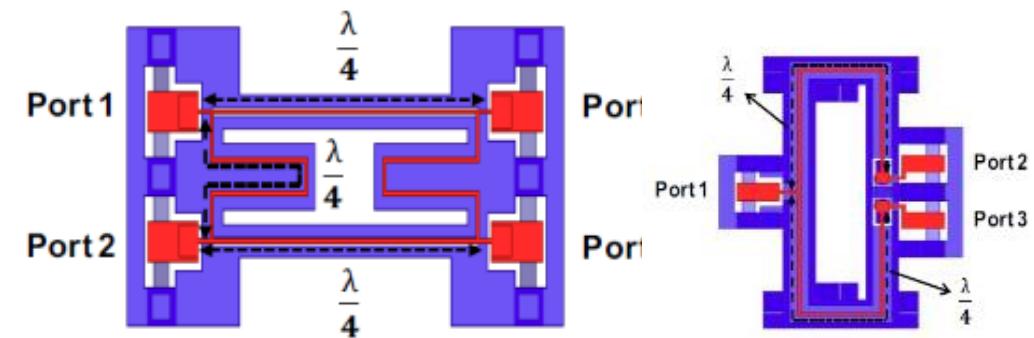
With Atom Watanabe, Muhammad Ali, Tong-Hong Lin, Manos Tentzeris, Rao Tummala et al., (Georgia Tech PRC)

Power-dividing networks and High-Gain Antenna Arrays

InFO (EMC)



Transmission line insertion loss 0.34 dB/mm  
Passive element insertion loss 4.3 – 4.9 dB



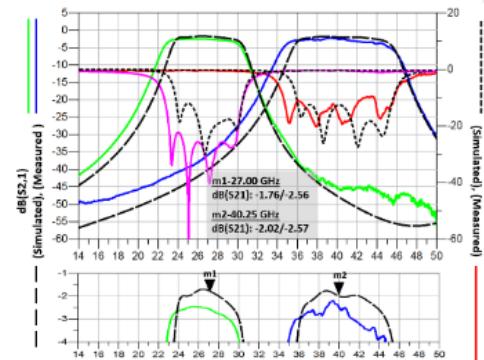
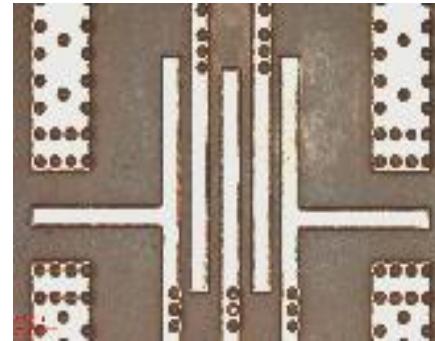
# High-Performance 5G and LTE Passive Devices

## 5G Filters in 50-100 micron glass- or ceramic-core laminates (Muhammad Ali et al., GT-PRC)

- Ultrathin filters: 2X thickness in reduction compared to offchip filters;
- Lower insertion loss compared to on-chip filters

### High Q Inductors and LTE Diplexers in glass and glass-core laminates

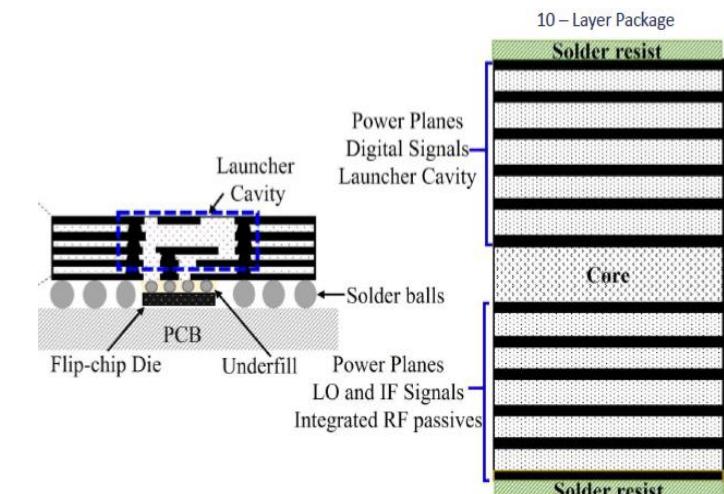
On-Chip	4 dB	0.1 dB/mm	Very Small ( $<4\lambda_0^2$ )	Very Small ( $<500\mu\text{m}$ )
Traditional Off-Chip On-Package – 3D Module	2 dB	0.5 dB/mm	Small-Med. ( $\sim 4\lambda_0^2$ )	Med.-Large ( $\sim 500\mu\text{m}$ )
	2.5 dB	0.2 dB/mm	Very Small ( $<4\lambda_0^2$ )	Small ( $<500\mu\text{m}$ )



- Ultra-fine mm-wave structures with high precision
- Footprint smaller than 0.5
- Innovative topologies for low insertion loss

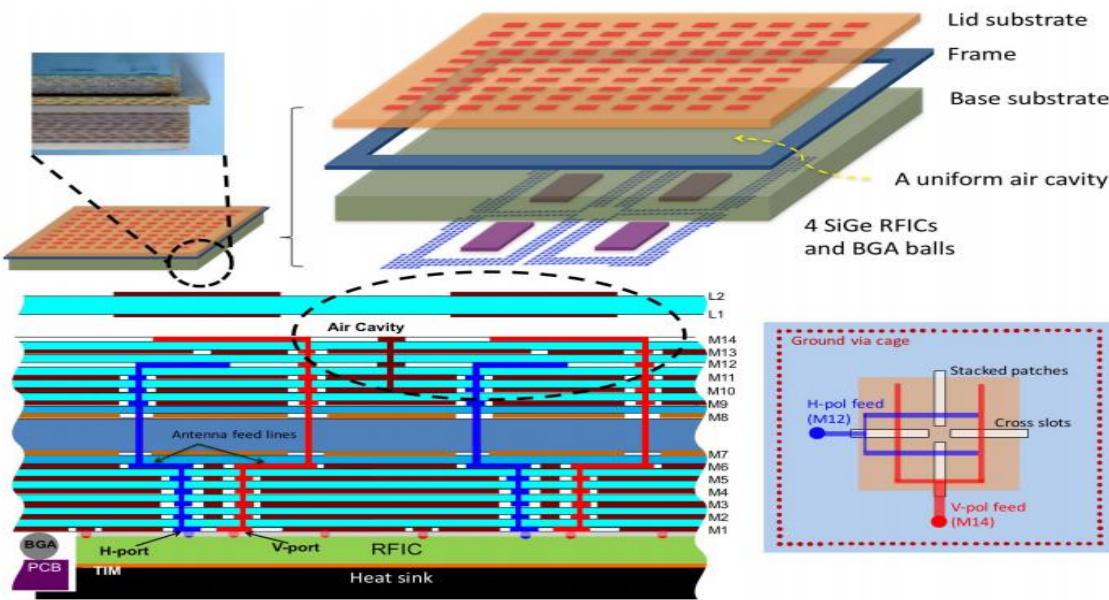
## Filters in the 100-330 GHz bands (from Neelam Gaunkar et al., Intel)

Parameter				
w	10	3.2	2	3
IL (dB)	4-5	3-5	1.7	5-7
Size (mm x mm)	1.9 x 1.35	2 x 0.26	20 x 20 x 40	0.7 – 1.1
Type	Microstrip	Stripline	RWG	SIG
Substrate	Organic	Silicon BCB	Metal	Organic
Operation band	100-140	125-152	200-225	225-330



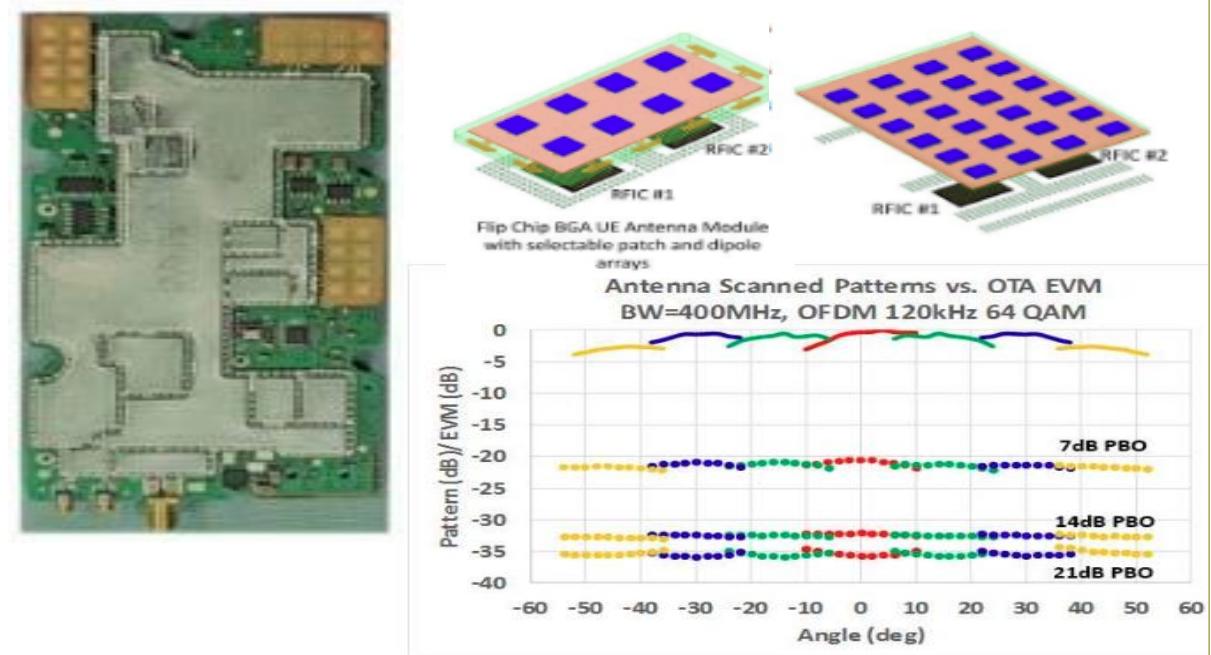
# High-Density Packaging: Chip-last mm-wave packages

## Organic laminates for Base-station (IBM)



- ✓ High bandwidth because of the air cavity
- ✓ Large-scale antenna array
- ✗ Thick substrate with many metal layers
- ✗ Mechanical reliability

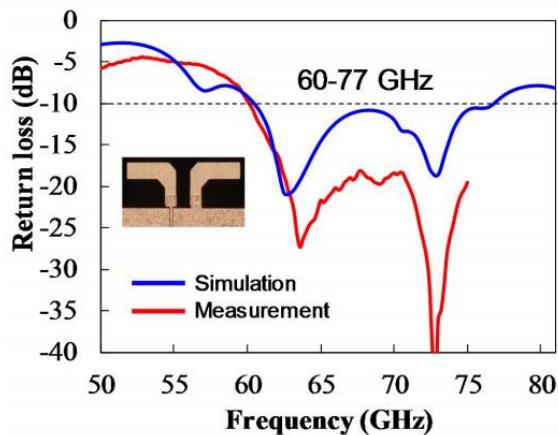
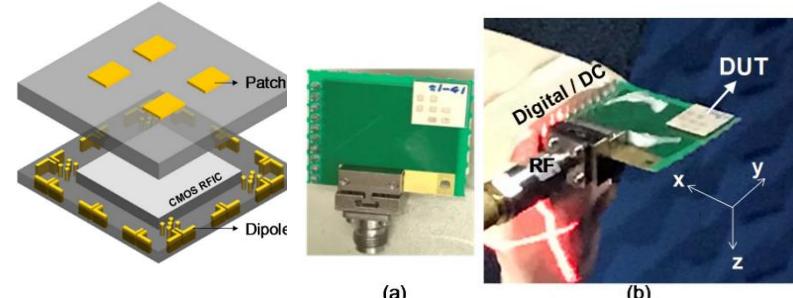
## Organic laminates for UE (Qualcomm)



- ✓ Demonstration for handset AiP
- ✓ Co-design from CMOS through AiP
- ✗ Thick substrate with many metal layers

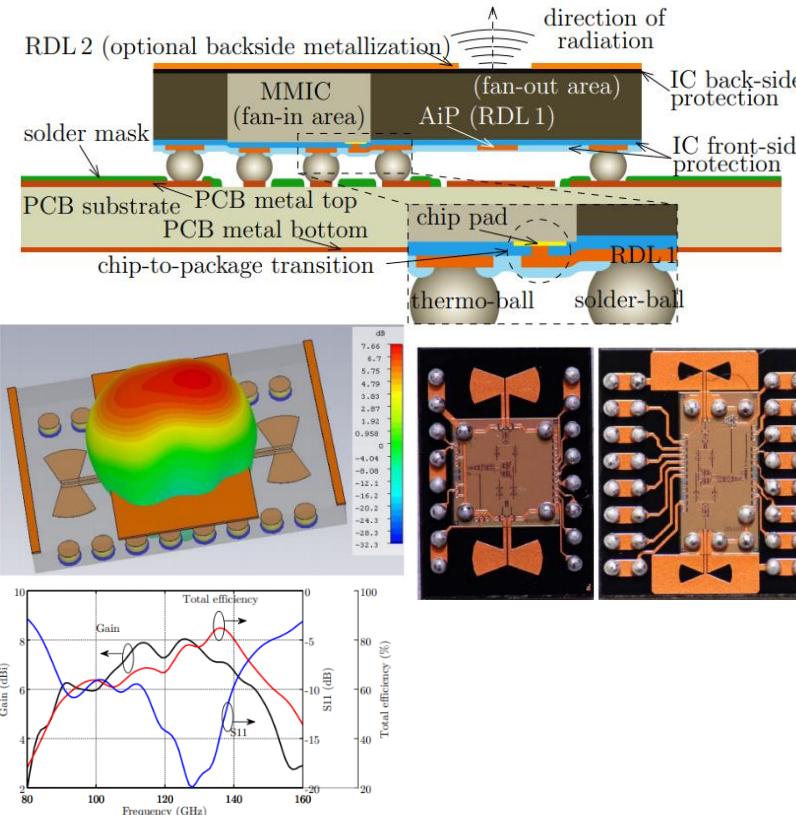
# High-Density Packaging: Chip-first mm-wave packages

## InFO-AiP (TSMC)



- ✓ Thickness reduction
- ✓ Low signal loss from Chip to Antenna
- ✗ Unbalanced stack-up – Warpage
- ✗ Patterning precision on molding compound

## eWLB (Infineon)



- ✓ Thickness reduction
- ✗ Distance variation from Gnd to Patch
- ✗ Patterning precision on molding compound

## Fan-out AiP (ASE)

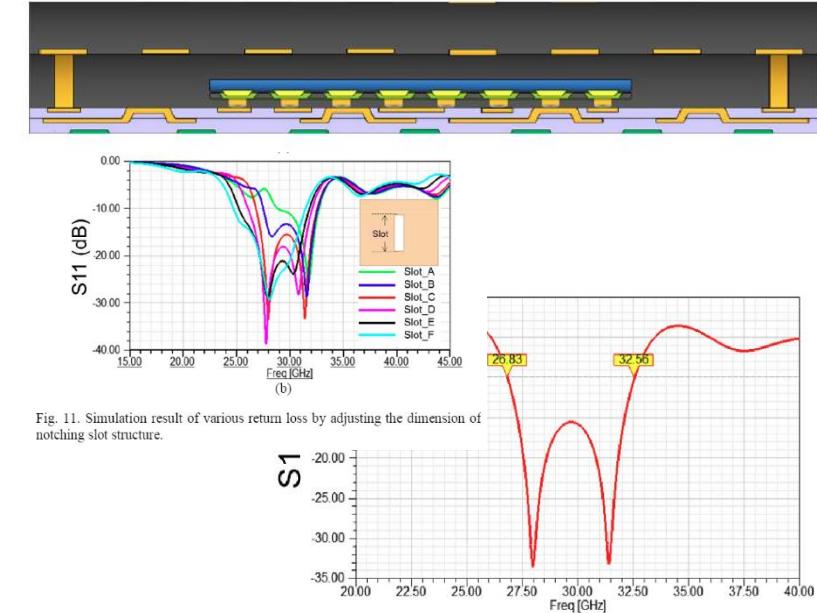


Fig. 11. Simulation result of various return loss by adjusting the dimension of notching slot structure.

Fig. 12. Simulation result of stacking patch antenna

- ✓ Thickness reduction
- ✗ High signal loss in through-mold vias
- ✗ Mold-on-mold causes thickness variations

# Summary: RF Passives

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- Passive components determine the size of multiband RF modules
- Evolution of RF module, based on passive and active integration:
  - Ceramics to organics to glass packages
- RF materials and processes:
  - Critical to have low loss, stability, good tolerance
- Glass-enabled precision IPDs such as filters, diplexers etc.
- Antenna size is a concern for RF Integration – need for advanced RF designs and dielectrics:
  - mm wave is enabling antenna integration in packages (AiP)
- Advanced multilayered structures and copper shields for EMI isolation
- Laminated glass explored for 5G components and integration