CAM CELL BASED MEMORY ARCHITECTURE FOR EXTREME SEARCHING OPERATIONS

SRINIVAS RAHUL SAPIREDDY

Department of Computer Science Electrical Engineering, University of Missouri Kansas City, MO, USA
E-mail: sapireddyrahul@gmail.com

Abstract- This paper discusses about content addressable memory (CAM) architecture based on different device technologies. The paper explains about the Magnetic Content Accessible Memory using magnetic tunneling junctions (MTJs) which has an advantage of parallelism in its architecture. A memory structure like SRAM or DRAM arrays store the address and retrieve the required data by giving the complete address. Whereas in CAM based architecture, we can access the information stored by giving the key (either full data or part of the data) as an input, rather than an address. Here we explain about magnetic tunneling junction (MTJ) based CAM architecture which can handle both searching and storing the data using content addressable memory architecture where we can replace a single MTJ in place of more than 8 CMOS transistors.

Keywords- Associative memories, magnetic memories, memory array.

I. INTRODUCTION

Content Addressable Memories are important for searching purposes. It is also called as associative array/storage. Usually a Content Addressable is used for searching the given data by comparing with the given data (Key) as an input. Several device structures are built to implement CAM structures for various purposes. Unlike the standard memory arrays where we use a RAM which returns the data on supplying the address.

Whereas for the Content Addressable Memories (CAM's) searches its memory to see whether searched address is present in it by information provided by the user. If the searched word is found that is, if we have a match the CAM returns the address where the data is matched or else it indicates that there is a mismatch [1][3]. Thus, the CAM is called as associative array. This type of approach is very useful in searching a large amount of data in a short period of time.

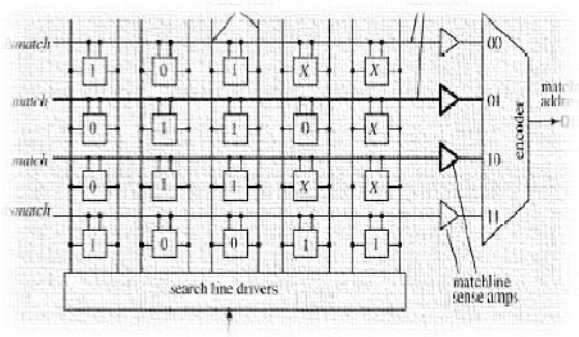

Fig.1 CAM Structure

In this paper we discuss about the different Content Addressable Memories using CMOS, Memristor and Magnetic Tunneling Junctions. We present a new CAM cell design using MTJs which will decrease the challenges experienced in device fabrication using CMOS devices. These types of MCAM cell design allow swift progression of system development in future with increasing searching speed and higher endurance.

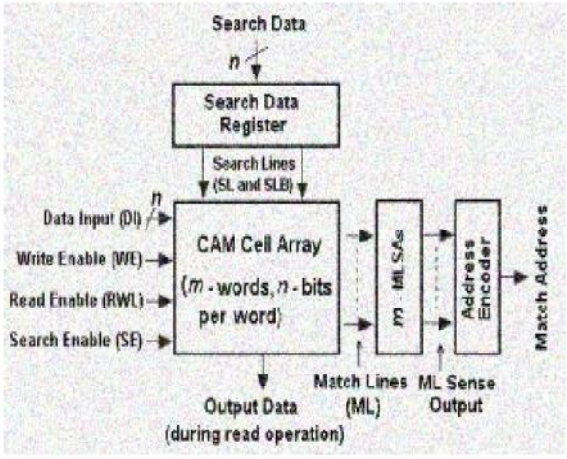

Fig.2Basic CAM structure

Numerous devices are produced by integrating this type of device technologies. For example, some of the semiconductor companies like IBM, QUALCOMM, and Intelimplemented different types of CAM based architecture. Content Addressable Memories are faster than Random Access Memories in which complete memory can be searched for required data word in a single clock cycle [1]. CMOS devices have a complex design cell structure unlike MRAM which has simple cell structure. In a fully parallel CAM architecture, there should be associative circuit for comparison purpose to recognize whether the input key is matched to the stored bit.

Furthermore, the total match signal is produced by combining the match signal from each CAM cell. For producing a match signal we require supplementary circuitries which increase undesired properties of the CAM array such as increase in power dissipation,

manufacturing cost. The CAM cell designs discussed in this paper are designed for minimum cost and increased searching speed. Besides its disadvantage of power dissipation, manufacturing cost we use CAMs as it has simple cell structure and show very high searching speed.

1.1 CMOS CAM Cell Structure

The simplest class of Content Addressable Memorybased on ones and zeros is a Binary CAM. For example, consider stored bits in CAM are 1XX00 then we can have four combinations of search word bits as 10000 10100 11000 11100. In this way the CAM cell array searches its data and returns the words which match with the input key word. CAMS are often used in computer networking devices, database engines, networking packet routing, Image processing, detection, and computing logic in memories.

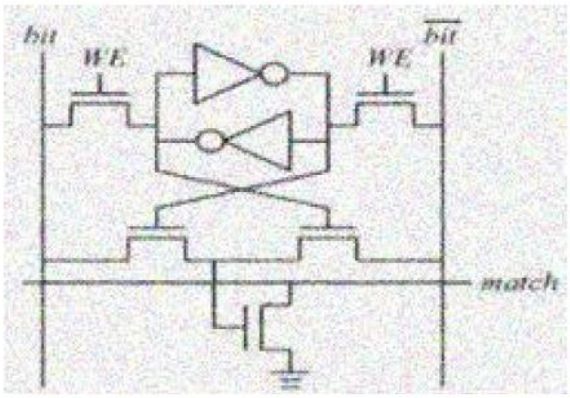

Fig. 3 Existing XOR CAM Cell

Basic 9T BCAM cell using CMOS transistorsconsists a comparing and storageunits discussed here(Consider the picture in figure.1). Here we store the data using 6T SRAM cell. The match and mismatch can be found according to the discharging the data by a pull down transistor. Consider a situation when the cross coupled inverters store the data 1. Now the pull down transistors will be on and other is switched off. Thus there is a discharge path for logic as M3 is in on state, so it remains in low impedance state. This indicates that the data is matched. Basically in this operation, first the match line has to be charged to logic 1 by using pre-charge transistor and then the matching operation can be done. Matching and mismatching of stored data and searched data can be shown in the following truth table:

Search Data (BL)	Stored Data(Q)	Resultant Transistor(M3)	Match – Line(ML)	Comparison Result
0	0	OFF	Floating	Match
0	1	ON	VSS	Mismatch
1	0	ON	VSS	Mismatch
1	1	OFF	Floating	Match

Fig. 4 XOR CAM Cell Truth Table

1.2 Memristor Based CAM Cell Structure

As discussed above, we can design a CAM cell using CMOS transistors. But CAM cell designs based on CMOS devices show some disadvantage such as second order effects, the probability of having mismatch between CMOS devices used and CMOS scaling.Among new devises which came into existence Memristors show prominent advantage over CMOS devices as they have lower power utilization, very low switching time. Nevertheless, this device shows a disadvantage of low endurance due to fast switching in its circuitry. As shown in the figure each cell contains more than one Memristor. In which one of the Memristor is used to keep stored data and the other Memristors are used for comparing stored bit and key bit (input search bit) producing match signals.

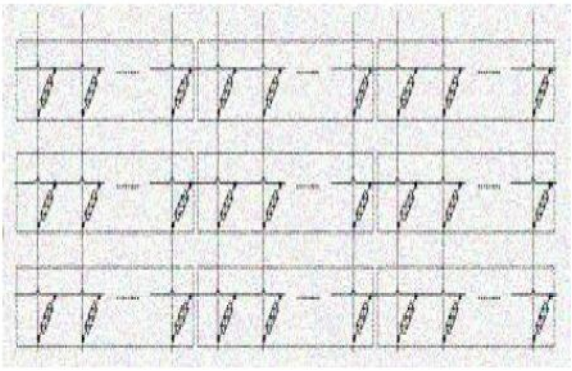

Fig. 5 MemCAM Structure Overview

These types of memories have applications in digital signal based systems, computers and many more.As new technologies are invented beyond CMOS, Memristors devices, new devices are considered for applying these in different memory devices [7].But CAM cell designs based on Memristor technology, shows some disadvantage in terms of endurance. Thus, we move on to Magnetic Tunneling Junctions.

1.3 MTJ Based CAM Cell Structure

Lately, magnetic content addressable memory architecture has been implemented using magnetic tunneling junctions (MTJs) [2][10]. This can handle both storage and comparison between bits using logical XOR operation function. The main advantage of magnetic tunneling junction is it has the capability of replacing 10 CMOS transistors in implementation a CAM cell. This has greatly increased the challenges faced in the fabrication of CMOS devices and Memristors in manufacturing. Here we study new CAM implementation using MTJ's.

A new MRAM architecture was proposed where both the bottom and top magnets were programmed for searching and data storing purposes [10]. Here the spin orientation in the top and bottom magnets determines the resistance in MTJ's. Thus, using a single MTJ we can construct a CAM cell where the bottom magnet represents the search bit and top

magnet the bit stored. The resistance in MTJ is the representation of the match or mismatch.

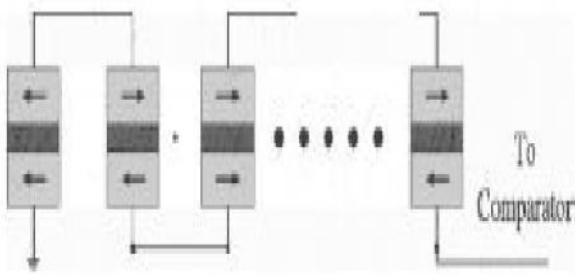

Fig. 6Connection of CAM cells to yield match/mismatch using single MTJ's

As the search word is same for all rows in the bottom magnet no word line required to change the magnetic orientation in the bottom magnet. Here the top magnet is programmed using word and bit lines as in conventional way. In order to induce the search bit into the bottom magnet a vertical ring-shaped magnet is used where the bit line is enclosed inside the ring-shaped magnet. Hence, using this we can program the top magnet and bottom magnet separately without any disturbances.

II. ANALYSIS OF NANO – CAMS

Table 1 shows the comparison of CAMs in terms of delay, power and area.

Table 1

Nano-CAM Type	Search delay	Area	Power		Endurance
			(Search/ Update)	Leakage	
CMOS-CAM[54]	1.077X	2.27X	1.33X	0.15X	10^{16}
MTJ-CAM [55]	2.24X	2.34X	1.49X	5.7	10^{16}

From the Table 1, we can see that CMOS CAM architecture has poor scalability.

III. FUTURE SCOPE

From the CAM structures mentioned above, a new architecture was proposed which increases the speed of the searching operation. As mentioned above, we are not using a word line in the bottom magnet as the search word is same for all rows and for inducing the search bit, we are using a vertical ring-shaped bottom magnet. The new proposed architecture has the same structural arrangement, but we here we introduce a top magnet under the vertical ring-shaped bottom magnet with different word lines and bit lines lying under the existing architecture. According to my view, this type of architecture increases the searching capacity of the structure where the searching of the bit takes place by the top magnet and underlying magnet (which is under vertical ring-shaped magnet).

So the searching the bit is done by two magnets having separate word lines and bit lines. This type of architecture can be shown below:

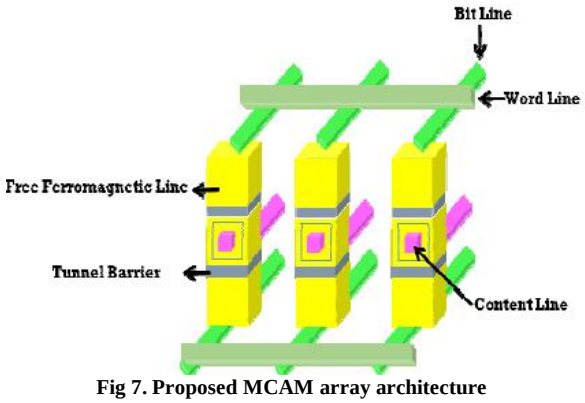

Fig 7. Proposed MCAM array architecture

CONCLUSION

We know that a large amount of data is created every year and we can see an increase in the data size day by day. As data increases various applications, which depend on searching and storing become more difficult to implement. This paper gives the brief explanation of how MRAM based CAM cell design work using magnetic tunneling junctions (MTJs) and how these designs of magnetic content addressable memory can replace the other CAM structures. Searching and storage of memory has become the main concern searching the required data and as well as storing the data at the same time. By using the content addressable memory using magnetic tunneling junctions, we can compute the searching operation as well storing the required data which can reduce the implementation challenge engaging the CMOS and Memristor based device CAM structures.

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