Here are the list of questions, ideas which were provided by previous batch PD guys at their interviews.

Questions asked @ whizchip

Pnr flow
Pd inputs
Blockages types
Congestion numbers in my blocks
Module splitting
Module
Qualifying placement before cts
How much was utilizaion after placement
CTS spec
Synchronoys,Asynchronous clock with waveform
What is skew?global ,IoCal skew .why global skew doesn't consider logic while minimzing skew?
Exclude pin.why do you exclude data pin during CTS?
Have you tried to build clk tree through d pin
Timing opt techniques
How lvt cells reduces delays
Explain Cross talk with waveforms
Setup & hold calculations
Eco flow
When do use eco flow

1. What was the shape of the block?
2. What was the allowed layers for use to you?
3. How the macros were placed?
4. How the cells were clustered?
5. How u placed the modules?
6. What is congestion? Was there any congestion in your block?
7. What are the inputs for pt ?
8. What all things u define while cts (input constraints)?
9. What is eco flow?
10. How u fix timing in eco?
11. What is setup and hold?
12. What is the arrival time when calculating setup and hold, explain separately?
13. What is global cell ?
14. Steps in routing?
15. What happens in CTS?
16. Inputs for pd ?

17. Checks and what all you look of in those checks?
18. What was flow from beginning for PNR?

Smartplay interview's-

1. list of all inputs to start PD flow and whats inside. In which file standard cells height and row information's mentioned.
2. Sanity checks- whats the effects with input floating nets in netlist and what do you do ?
3. My project blocks size and no. of metals used in blocks and macro's.
4. channel length calculation and where is the information's of macros given.
5. basics STA, setup and hold time definitions with diagram.
6. why clock period is not required in hold time calculation.
7. basics of latchup and remedies
8. how does tools do placement optimizations (He wanted to hear path grouping concepts)
9. crosstalk and remedies.
10. Antenna and remedies
11. time borrowing concepts in latches.

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1. Draw INV, AND and OR gate using 2 inputs mux.
2. why we need setup and hold time for flops.
3. define meta-stable state and Noise margins.
4. inter gate clocking (IGT) why do we use it? (what is static and dynamic power consumption's).
5. define CMOS operating modes with drain current equation.
6. what is crosstalk window concepts.
7. Antenna effects and remedies.

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1. who is your client?, what are the tools did you used?
2. what are the inputs did you get form synthesis guy?
3, how did you validate that?
4. some questions on SDC check
5. pick any one of block and expalin PD flow.how did you place macros?
6. what is the minimum space did you follow in your design?
7. present technologies not using straps for macros, then what is the use to give VDD and VSS in between two macros
8. what are the metal layers did you used in your design?

9. M1 is used for standard cells, so which layer did you connected this M1 - means did you connected to M9 or M8?
10. what are the checks you have done after placement
11. what are the inputs required to start CTS?
12. what is the spec file consists of: he is expecting each and every statements in the spec file
13. how did you analyse setup reports?
14. what is the reasons for set up (by seeing the report we should give the answer-not theoretically
15. how did you overcome that?
16. what is DRV, what are those?
17. how did you fixed tran violation?
18. Do you know IR drop, did you work on IR drop tool?
19. what is the important of clock gating?
20. where will you place the clock gating cells-near to source or sync?
21. what are the DRC's did you faced?
22. list out any 10 DRC.
23. insertion and skew delay for your design.
24. Out of all paths how did you know which cell is giving setup violation and how did you overcome that.
25. How did you overcome the congestion?

Tell about yourself (I **was not** started with this question)
1: with one of your project explain complete flow
2: how did you start? (Expectation was to mention all inputs and from whom we get, sanity checks and why we do it)
3: Floorplan (expectation was to explain wrt one block)

- How floorplan was done for the design ?
- Macro placement
  - Deciding spacing between macros which has pins
  - Do we need to keep spacing between macro if it doesn't have pins facing each other.(expectation was to justify our answer)
- In the flow there were many questions , like why macros were placed only at the bottom
- How do we Qualify floorplan

4: placement

- Before starting placement what we do?
- Congestion and solution
- Checks after placement
- Qualifying placement

5: CTS

Before starting cts what we need to do (analyze the quality of placement)

Inputs to CTS

What we analyze after CTS

0: How we can tell CTS is build properly

Clock path (why do we set transition limit) If library has max tran limit of 1ns and you are getting 900ps as transition value, can you take it further (No as clock tree has a chain of buffer we will see min pulse width violation "**clock absorption**")

6: Routing

What you did in routing

Steps in routing

7: Physical verification for your block

Have you run caliber (inputs to DRC and LVS)

List some DRC's and LVS issues

1: timing problem to calculate setup and hold slack
2: explain vth (on what it depends)
3: explain latchup(how do you reduce)
4: why are fillers used
5: what are end cap cells ?
6: what are decap cells ?

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1. Face to Face became a conference call due to internal mis-communication.

2. **Special Case:** Tell me about your family (???), school, college, % of marks in engg.

3. What kind of project you worked?

4. Questions only on 1st page of ChipEdge's FloorPlan. Nothing else. My questions were such that I had to co-relate frontend Design/Verification and backend Physical Design!

5. How do you estimate die size?

6. How do you calculate Aspect Ratio?

AR = Hor Routing Res/Ver Routing Res theory will not help. He was expecting **how did you get/calc** Horizontal and Vertical Resource estimation? I said as we did in lab:

Sq_rt(die_area) = L, W. Nope. It isn't correct.

Later, he dug on. If DA=M + 0.6*S + IO + Blkg, then why std cell util=60%?

If I move from 45nm to 28nm or lower, will this value (60%) change? If yes, why? If no, why? If so, Util = 65% or 55%? Numbers depend on what you answer.

7. How you place macros? For my exp, 10-15 Macros was not sufficient. He was expecting 100/150+ M

Here when you say dataflow – be specific(like power, pll, data, addr, ctrl, etc). That's what I learned from him. There are 10-15 ways of placing Macros!!!

8. Do you know test mode? How do you insert scan chains? How it is done?

9. STA: Do you know about set_false_path, clock_groups, mutually_exclusive, asynchronous, case_analysis? God blessed me. Didn't dig deep.

10. A beautiful question: I liked it.

Case 1: there is a 2:1 mux. set_case_analysis is set to '0'.

Case 2: there is another 2:1 mux. set_disable_timing is set on B->Y

What is the difference? Explain w.r.t timing arcs.

11. What is the difference b/w Exclude pin and Ignore Pin?

12. Have you done PV?

I clearly said NO. He said PV is difficult than PD. My mouth didn't shut. I said I wanted quality work, not quantity work (Hey, indirectly yaar!)

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1. Command to spread the cells.

2. During Placement if more cells are added(utilization increases) by the tool, what could be the reason?

3. How setup/hold analysis are done on CGCs?

4. Why ENDCAP and WELLTAP are added before Placement only?

5. During FloorPlan, if IO info is not given, then how will you proceed? Say, you cant ask the manager(he too doesn't know) nor you can assume and add.

6. Let's say after Placement there is setup violation. What will you do? How will you analyze? How will you validate the violation?

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1. What will you do to reduce static power and dynamic power from physical design perspective?
2. After routing you see there is IR drop what will you do?
3. Explain floorplan steps.
4. Types of physical-only cells?
5. What is latchup and how will tap cells reduce latchup effect?
6. What is lef file, explain some contents, what is difference between technology lef and physical lef
7. Why do you need standard cell blockages to be defined in LEF file?
7. What version of synopsys are you using, how many macros in your design?
8. What is FRAM view, why do you use that in P & R?
9. Explain MOS working using a PMOS
10. Layout of an inverter
11. Why do you need filler cells, how does it help avoid base layer DRCs, what happens if there are spaces?
12. What is punch-through effect, channel length modulation.

- Role of following cells in latest technologies: Endcap/Endrow cells, decaps, Core fillers, metal fillers, tie-hi/tie-lo cells, Well tap cells?
- What are the corners used in previous projects and explain how they work.
- Why via sizes are increasing in lower technologies
- What is ICG and how it works
- What are the types of flip chip design?
- Schematic diagram and truth table on Isolation cells and retention flops. And switch cell schematic structure
- how clock buffer different from normal buffer
- why well taps and endcaps?
- how will u say constraints u r getting from frontend areok
- what are the problems of decoupling cap.

- Given a power budget number, how to come up with full power grid design –decide on number of pwr/gnd pads on each side, core ring width, space (highest layers), mesh width & spacing per Metal layer from top to M3?

- For gated clocks, can gating elements be sized for timing? Are there any EM, slew or cap limits on clock repeaters in library?
- Clock Tree Synthesis targets –minimum Insertion delay & min max skew? Importance of both being minimum? If minimum I.D. Target is met, is minimum skew still important?
- How STA takes OCV & crosstalk effects into SU and Hold time violations? (Pls refer if anyone has a good doc on this)?
- Fixes to Antenna violations: Layer Hoping (jumper/Bridging) and diode insertion (reverse-biased), upsize gate (increase gate area).
- DW-DS for CLK Non –default Routing? Why?
    - -DW :less Resistance, helps Electro migration & Insertion delay,
    - -DS: coupling cap reduces, helps crosstalk
- How shielding exactly reduces crosstalk?
- How buffer insertion to a victim net reduces crosstalk effects?
- Which is preferred in CTS: clock buffer or clk inverter?
- Pulse width violations: How is it imp & fixes?
- How to solve Electro migration violations?-
- DFM techniques specially added in 28nm technology?
- How to come up with CTS specs: max delay values & max skew values?
- Optimal Padring Design –Concept, calculations, design strategies & challenges: Any good doc to share?
- How extraction is taking OCV & crosstalk effects? How timing is taking both these effects?
- Is mix Vt possible in CTS? Why? Why SVT cells are preferred in CTS?
- How to decide optimum H & W of core, given Aspect Ratio & utilization? Implications if H> W & vice-versa?

- CRPR concept and how it works
- What is the difference between low VT and high VT cells in fabrication
- What are the issues in 45 and 65nm technologies
- Explain challenges in previous design
- What will be the feedback to designer to avoid issues which you faced in prvious project
- Why net delays are more in lower technologies
- What are the low power concepts
- To cut down routing violations in a specific module, what suggestions you will suggest to designer
- what is timing derates concept and why it is required
- Explain how timing derates and CRPR on timing path
- What is OCV and how it works
- If you are lead for a project, how you handle your team and how you track the status
- If you and your team are working in new technology(ex: 45nm), what are the ways to escalate issues
- Where will be the IR drop more in case of flip chip designs and why?
- How is the pitch calculated for bump placement?
- Challenge face in the project (referred to one project).
- What are the pros and cons of up sizing and downsizing a cell?
- How will cell sizing affect dynamic, leakage and short circuit power?
- Explain the above answer with cmos structure.
- How will clock gating help in reducing dynamic power?
- Explain the above answer by writing flip-flop circuit.
- What are the challenges, moving from node 90 to 45

- What is the cross talk? how it will effect
- Switching transitions effects the cross talk
- Design Frequency will affect the cross talk? If yes... why
- Which type of violations will get .. due to cross talk
- What is the cross talk effect between 1MHz design to 1GHz design
- What will happen will cross talk goes high
- While comparing 1MHz to 1GHz, which design having more hold violations ? why..?
- What is the clock gate..? explain with diagram and operation
- What are the uses of clock gate
- How many types of clock gate will be available in design
- Advantage of clock gate
- Lookup tables in .libs (input transitions and output load).
- HFN requirement and linked to .libs (lookup tables).
- RC network and transistor level NOT and current source concepts.
- (Falcon à CORTEX-A9MP) Multi power domain floorplan (i-catch and d-catch macro placements) and power plan.

- Xtalk noise on static signals and glitch effects on static signals.
- Timing windows effect on xtalk noise.
- What the difference between synthesis and High Fan-out synthesis
- why more corners at 65 compared to 90
- What's the need of derates
- What the timing issues when big memory macro is there. What happens to timing when It is partitioned in to different sizes

- What does Top level CTS and Block level CTS need to look before setting the input delay parameters.
- What is OCV, explain
- How OCV effects setup and hold
- What do we check for during netlist sanity checks?
- Will P & R tool reject synthesis netlist with unconnected Input ports?
- How do unconnected (or) floating Input ports impact PD flow?
- Explain two ways of fixing min area drc violation because of unconnected I/O ports.
- Explain effects of clock domain crossing?
- When do you constrain a failing timing path with false path? Why not multicycle path?
- What type of paths failing zero RC timing check can be fixed during placement?
- What type of paths failing zero RC timing check cannot be fixed during placement?
- What is power aware CTS?
- How do you minimize clock dynamic power ?
- same path setup and hold
- what all are the tweakings u did in the flow apart from normal flow
- If two buffers are added in the common path (timing path) ,then what will be the effect on hold in PTSI
- same path setup and hold
- tie high and tie low cells
- what is the purpose of via enclosure drc and thin fat wire drc
- set_load , set_driving_cell, report_clock in PT what they do
- in antenna fixing where to add diode.
- softcheck errors in LVS
- ERCs power and signal

- CTS done with what all constraints.
- cell nad net delay graph
- how much cap. And tran values u shud specify in the design
- what is the difference in the setup in OCV and best case /worst case
- in uncertaininty how much is IR drop margin
- how well tap prevents from latchup
- why inverter is preffered in CTS over buffer
- If typical is 1 volt , then what will be the corners for worst and best and why ?
- No. of levels in CTS , can we specify in the clocktree file.
- in hirarachical block , how will we do the I/O budgeting .
- where to place the gater towards the flop or towards the root and why ?
- test chip timingclosure from one block to another block
- in CTS what is preffered first to fix .. logical drcs , skew ,ID
- what are the disadvantages of having good skew.
- if noise height is fix, does the width matter ..why and why not
- flip flop arcs
- How to resolve congestion during placement?
- How to apply timing derates for hold?
- Steps involved in IR drop analysis?
- Dynamic IR drop flow and its inputs
- How would you constrain a port of a subchip if it is timed with diff clocks?
- Have you faced hold violation of magnitude of one clock period? And why it is?
- What are the practical possibilities of hold violations?
- Timing report deference b/w PT and PT-SI?
- How to check unconstrained path in design? (rpt_anlys_covrge, check_timing –clk_not_reaching)
- What are the different constraints and Exceptions?
- What is multicycle path and how will you define it in primetime?

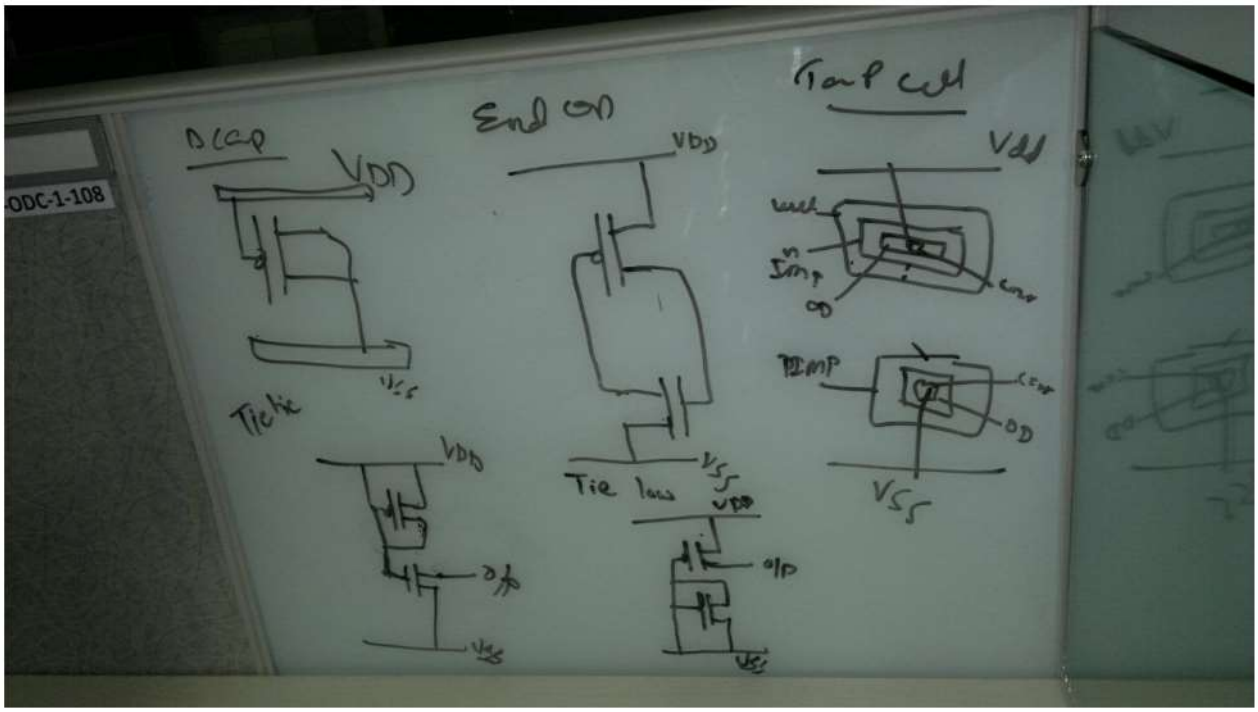
- What are setup and hold timing checks? Explain with a diagram.
- Calculate the maximum frequency of operation of the given circuit ?
- What are virtual clocks and why are they used?
- What is on chip variation ?
- What is Clock re-convergence pessimism removal?
- Why so many timing analysis corners and OCV on top of it?
- What is temperature inversion?
- Which are the timing corners analysed for your chip? explain each
- What does ss or ff in the corner name specifies?
- Draw the circuit of a basic CMOS inverter.
- How are you fixing transition violation ?
- When you increase the drive strength, explain in terms of transistor, how it is getting fixed ?
- How is clock uncertainty calculated in your flow? Based on which all parameters ?
- What are the contents of a .lib?
- How will you constrain a source synchronous interface?
- What is meta stability?
- Why is clock skew constraint specified as 250 ps or a specific value ? Why not it is 0 ?
- What is useful skew ?
- What is AOCV/Advanced On Chip Variation?
- Draw a simple clock divider which divided clock by 2. (A flip flop where D is getting an inverted feedback from Q. Input clock is fed as clock to the flip flop. Output divided clock can be taken from Q output)
- What is Antenna effect? And how we can fix them in detail.

- Why we need to do Cell padding. How it will reduce congestion.
- Will you place the memories touching the core where there are IOs?
    - There was a scenario where in they gave a chip size of 10mm X 10mm, with three partitions P1,P2&P3 each of which having a block insertion delay of 5ns,8ns & 1ns and out of which P2&P3 is frozen. P2 & P3 of size 4mm sitting on top in middle with channels on both the sides and P1 at the bottom left. PLL is on right middle. The design size is approx. 8M instances.[Need to estimate the % of flops from that]. There is a single PLL and a single clock domain for the whole chip. Also they gave the channel spacing of 0.5u and there were logic placed in all the channels and the placement is frozen. How will I plan the clock tree for the top? I need to build the cts both manually and using the tool. Based on the above scenario below questions were asked
    - What is the first step to do clock tree synthesis?
    - Which part of the chip will you manually build the cts for?
    - What considerations will u take while building the cts?
    - What will be the insertion delay for the top?
    - What settings will you use for the cts on the hierarchical block P1, P2& P3?
    - Should we build a clock tree with increasing order of drive strength of buffers from root or decreasing order?
    - At the PLL, which drive strength should be used for clock buffer and why?
- Which clock tree is better, the one with shielding on a single spacing or the one with double spacing?
- How will you set the constraints for the clock input pin in the SDC?
- There is path from the launch clock at 2ns and capture clock at 3ns, where the tool checks the setup and hold? Write the command for hold check in PT?

- Given a path from clock port to two sink flops, one path is direct and other path has clock divider circuit in between. In this case how do you build the clock, what are the things to take care?
- If you move a flop after the CTS, what effects do you find. If there are no setup and hold issues what else timing issue do you find? (expecting clock gating timing violations)
- Given a flop to flop path with clock time period 2ns and 4ns respectively, what are the things to take care, at what edges setup and hold checks done.
- If you have a flop to flop path with asynchronous clocks, how do you handle it?
- What are initial checks you do and what will happen if you have any issues.Reasons for why design should not have these. example (What will happen if you have floating input pins).
- Is it ok to have floating output pins. And is it ok if you have a cell which is not connected to input or output.
- Before going to floorplan what will you check.
- If you have a 1000 macros how will start floorplanning.
- What you will do exactly in CTS. he is asking about scenarios like if you build a clock tree whose frequency is 500Mhz. after postCTS clk freq is 1GHz, will you continue with same clock tree or rebuild it.
- How will you know that two clocks are synchronous?
- Where we place ICG cell at the port or sink and why? you have 10 clocks in your design frequency ranging from 100Mhz to 1GHz, for these clocks where you place ICG?
- What are the considerations and proper way to partition a multi-voltage design, identifying proper power domains?

- What all are the way to minimize STA corners in the top level for a hierarchical design (one ans he is looking for to push pipeline flops inside blocks to reduce top level timing paths)
- SI Prevention in the flow from Placement to Routing .Steps need to take care
- What is the difference between MMMC & normal flow.If a design is given to implement what are the pros & cons of it .
- What is temperature inversion corner? How do we come up with derate values for a particular corner (factors deciding the derates like 6% or 10%)
- What are the criteria's for Scan stitching in synthesis .If we reorder scan chain during P & R does it disturb the Testability vectors
- What are DFM issues & how do we attack it during the flow .Can you name some which was not there in 90nm but was seen in 45nm to great extent (He was expecting well proximity check & Latch up)
- How do we pick up MCMM corners during P & R for Setup & hold corners. Factors deciding the corners
- How do you debug LVS error?
- What kind of LVS errors do you have seen.
- Any significant change from 90nm to 65nm in terms of library configuration.
- Discussion regarding nwell latch-up and hot nwell drc.
- What is ICG and its pros and cons?
- What is temp inversion? And what is it dependent on?
- What are different corners in ur design?
- What are the checks you do after the placement?
- What are all you take care while building clock tree
- If clock net in common path is affected by noise then will the delay be subtracted by CRPR?

- When scenarios are comes in your flow?
- What input will you give for scenario creation?
- What is multicycle path? If there is a design with launch 5ns and capture 10ns then how will it work?
- What is a Clock gating violation? How to fix them?
- You had a crosstalk problem , if you were to redo the floorplan then what changes would you make?
- What is the difference between a normal buffer and clock buffer?



PrimeTime RELATED ISSUES AND ERRORS

- How do setting the clock group relationship affect the crosstalk analysis in PrimeTimeSI?

- Constrain the below circuit for timing analysis. What all additional information is needed to time it correctly?
- ETM generation:

  extract_model -output <module_name> -format lib -remove_internal_arcs -library_cell

  - If we have multiple clock definitions at the same source, ETM .lib generation will not proceed. We need to remove the extra clock declarations with the command remove_clock. ie, Keep only one clock definitions per source.
  - Max delays or min delays if specified, needs to be removed.
- **PTE-060**:
  - When the variable timing_disable_clock_gating_checks is false, which is the default behaviour, Primetime infers "Clock Gating check" in all combinational clock tree cells. But in muxes and complex combinational cells, it is not able to infer clock gating checks, due to the lack of information. Hence it gives PTE-060 to these cells. When you see a PTE-060 warning, check whether the output of this cell is consumed as a clock, down stream. If no, we can ignore this warning. Else we need to enable clock gating checks, with set_clock_gating_check command for these cells.

  - set_clock_gating_check -high [get_pins U5/B]

- **PTE-075** : This is a clock related warning. It informs us that a particular generated clock is not having path to its defined master clock. The reasons can be
- set_clock_group
    - These are asynchronous, physically_exclusive and logically_exclusive. Physically exclusive means that particular clocks will never be present physically at the same time. Logically exclusive means that particular clocks can be present at the same time, but will never be used at the same time.

  set_clock_group -asynchronous -group {clk_1, clk_2, clk_3} -group {clk_4, clk_5, clk_6}

- Codec (LBIST) is a compressor decompressor logic (XOR – MUX) which DFTMAX inserts which helps greatly to reduce tester time.
    - Suppose say 16,000 registers are there in a partition. We have 16 scan chains too. Then one scan chain will be having 1000 registers each. So total shift cycle will be 1000. So if codec is present which will convert 16 scan chains to 160, then each scan chain will be having only 100 registers and the shift cycle is reduced to 100 cycles.

- Scan mode timing checks
    - First check whether the timing path is to the test input pin of the flip-flop.
    - If the timing violation is to the functional input of the flop, check whether the register is scaneable.
    - If it is a scaneable flip-flop, then check whether test input of the flip-flop is getting a case analysis of 1. Ideally in scan mode it should get a case value 1 to enable the scan path alone.
    - Check whether it is a non scan flop which is present in the non scan cell list. If yes, we can put a false path to this register.
    - Cross clock paths through LOCKUP latches are valid paths in scan shift.
    - Ensure whether the timing path is with the intended clock itself. If multiple clocks are not there to the registers, this issue should not come.

- PBA Based Timing Analysis

    - By default, primetime takes worst slew amongst the inputs as the cell delay. Suppose in the case of a two input AND gate the rise time delay of A input is 20 ps and that of B input is 25 ps, primetime considers A to Z delay also as 25 ps in worst slew mode. But when recalculated timing mode is enabled for a particular timing path this delay is substituted by the actual rise time delay of that input. For setup if lot of combinational path is there, with recalculated timing we gets lot of advantage. Usually this is enabled at the final ECO stage when all the ECOs are tapered down.

- Why can't we define the input/output delay w.r.t the real clock itself?
    - If we define so, tool cannot calculate any propagated clock latency to the output port, since it does not have any physical path. Propagated clock latency will be there for the flop anyways. So the analysis will be pessimistic for setup and optimistic for hold since capture clock delay is not there at all. Same explanations hold good for input paths too.

Power Mesh Width Calculation

$$\boldsymbol{Pads\ per\ side} = \frac{\boldsymbol{TotalCorePower}}{(\boldsymbol{\#side} * \boldsymbol{Vworst} * \boldsymbol{MaxAllowableCcurrentofPad})}$$

$$Total\ Dynamic\ Core\ Current = \frac{TotalDynamicCorePower}{CoreVoltage}$$

Core current splits into two branches. So

$$Core\ PG\ ring\ Width = \frac{TotalDynamicCoreCurrent}{2 * Jmax * CurrentSourcePerSide}$$

$$Itop = Ibottom = \frac{I * \frac{W}{W+H}}{2}$$

$$Ileft = Iright = \frac{I * \frac{H}{W+H}}{2}$$

$$Width\ of\ Vertical\ Mesh = \frac{Itop}{MaxCurrentDensityOfMetalLayer}$$

$$Width\ of\ Vertical\ Mesh = \frac{Ileft}{MaxCurrentDensityOfMetalLayer}$$

1> Go through the steps of PD flow ?

Now within the flow only - it will start with what inputs you will give and why and their contents ?

(What is HFNS, difference between LVT and HVT cells, contents of lef file, .lib file.)

2> As I reached Placement, and started about physical cells - boom ,there the question was on What are filler cells and why are they used ?

3> Next After placement - how will you qualify your placement. How will you relive the congestion at that time, what is the minimal number of congestion ?? Do you relive congestion at placement ? What was the utilization number after placement ?

4> What are the inputs to CTS? How do you come to conclusion on using drive strength of the clocks ? (Like what is the decision you make on deciding the number of clock buffers drive strength to be taken as 4, 8, 12, 16 or 32 - why we cannot take up 32X as the drive strength)

5> When does crosstalk occurs ? How can we make crosstalk occur in our design ? (Like what is the criteria on which we can make crosstalk occur)

6> What are we trying to achieve during CTS or after CTS ? (Basically he wanted to ask what the targets of CTS step) (What are NDR's, Why do we apply on clock nets)

7> Questions on latest project - how many corners, how w many instances in the design, what was the target skew , target latency, insertion delay, clock frequency , no. of clocks in design.

8> What are DRC issues.? What is metal hopping ?

What are Physical DRC issues.? - i guess same as DRC

9> Have you ever fixed the DRC issues

10 > Did you do any STA ? - put a answer no, or else he will stretch you in STA

11> Have you done any IR drop analysis - put a answer "no "

12> What is skew balancing ?

13> One tricky question

Suppose we take one of the three paths - reg2reg, reg2out or in2reg. Next we take 10 paths, group them in any of the 3 groups and over constraint them. Suppose the timing of the block to be met was 1.2ns but we over constraint only those paths and the timing we have to achieve for only those particular path is 0.8ns.

Now, What will be the effect in physical design by trying to achieve the above.

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1.brief introduction.

2."RTL" to GDS flow.

3.What happens in synthesis?

4.What is synthesis output format?

5.Why should we do synthesis?

6.How can u differentiate RTL verilog file from Netlist Verilog file?

7.If you know the circuit hardware schematic, can u skip RTL and directly code for netlist file?

8.Which libraries do you use in synthesis?

9.Constraint file used in synthesis? What if constraint file is unavailable during synthesis?

10.typical description of AND gate in netlist file?

11.Contents of SDC file? What are all did u have in your file?

12.Asked about drive strength specification of gates is SDC file. (How this is useful during synthesis)

13.Again flow from Netlist to GDS.

14.Sanity checks? commands used and appropriate description.

15.What is the outcome of report_timing during sanity checks?

16.Floorplan: steps for placing macros.

17.How do you qualify floorplan?

18.Why won't you check timing after floorplan?

19.tell me some thing about check_legality command?

20.placement steps: tell me in tool perspective

21.How do you qualify placement?

22.What is congestion? Horizontal congestion vs vertical congestion?

23.How do you reduce congestion?

24.Discuss about cell padding?

25.What is IR drop? During placement which IR drop do you check?(static IR drop or dynamic IR drop).

26.static IR drop and Dynamic IR drop discussion.

27.How do you reduce IR drop?(where do you increase power stripe width)

28.CTS: Steps in CTS.

29.Which layers are used for CTS and why?

30.Typical launch and capture flop diagram, asked to find out maximum Combinational delay?

31.How do do you address setup violations, hold violations?

32.Can you tape out chip with a DRC? if not why?

33.what do you mean by DRC, what do you mean by LVS? compare both of them?

34.tell me some DRCs you had faced.

35.Cross talk definition. Reasons for crosstalk?

36.What is effect of timing if both nets are in same direction?

37.What is effect of timing if both nets are in opposite direction?

38.How do you reduce crosstalk?

39.NDR's won't cause DRC's?how do you rectify them?

40.Define electron Migration? In which phase of manufacturing will you face it and why?

41.What is antenna violation? In which layer will you face it?

42.How do you fix antenna violations?

43.How to gate oxide breaks with charge?

44.what is the output file for startRC ? input for the tool?

45.SPEF vs SBPEF.

46.Contents of SPEF.

47.Why PT gives better results compared to ICC tool?

48.DEF vs GDS formats.

49.LVS check vs LEC checks.

50.ECO Flow - steps.

51.Skew effect on setup window?

52.Effects of Electron violations

53.clock buffers vs normal buffers, similarly inverters.

54.clock buffers vs clock inverters.

55.How equal rise time and fall time was achieved in clock buffers?

56.why cannot you use clock buffers in your entire design?

Interview questions with 2yrs exp

1) what are the corners you worked for your design ?

2) what is your die size and initial utilization value ?

3) Say me the physical design flow.

4) Is your design hierarchial or flat ? what is your instance count ?

5) how many metal layers for your design ? explain in detail ?

6) Inputs for physical design ,how do your load ur LEF's in to your design ?

7) what is positive skew and negative skew ?

8) Other than critical nets which nets you take care of and why ?

9) Do you accept larger skew if my insertion delay is met and i am ok with clk tree power also ?

10) If in sdc (from synthesis engineer) uncertainity and latency are mentioned why dont you fix setup and hold at pre CTS stage ?

11) What is signal integrity and how does it effect the design ? (crosstalk)

12) Will you tapeout the design with setup violation (huge),hold violation,max tran and huge max cap violation ?

13) One general question on thevenin equivalent (network theory)

14) why do we need horizontal and vertical power routing ?

15) Do you have any experience in partitioning ?

16) what are types of IR drop and its effects ?

17) what is global and detail routing ?

18) CTS inputs

other than pd

1) what is fibonacci series ?

2) based on archimedes principle (a tricky question)

1) explain .lib file and the contents ?

2) 7x7 lookup table in .lib and what is x axis and y axis ?

3) what does tool do if it exceeds those values?

4) how do you qualify placement ?

1) proj details ,values for utilization at the start and end ? why so much variation ?and clk frequency ? technology ? tool used ?

2) question on icc ; what is command to find sink points from q pin of a flop.

3) command used for running CTS ?

4) difference between 2 commands psynopt and focal_opt ?

5) on what factors does setup time depend upon ? (exclusively from .lib file content)

6) ways to fix setup violations ?

7) If ur data path is optimized (2 flops and a combo logic) and have setup violation,what option you use to fix setup violation ?