

1. Question related to calculation of clock period when all other parameters (setup, skew, combo, c2q) were given.
2. What is OCV and how it affects the clock period.
3. What will you do and reason if during CTS the utilization increases by 1
4. Why macros not placed in center, how to place macros correctly?
5. Why I selected 0.1 for metal pitch and not something else in channels equation? And why effective routing resources were half of total routing
6. What is setup violation and how to fix it?
7. How to fix hold violations?
8. Commands to correct setup and hold violations in ICC.
9. Inputs to build a good clock tree?
10. EM, IR, tap cells, endcap cells. And why can't we use filler cells instead?
11. How to fix congestion?
12. MMMC and CRPR, multicycle path.
13. Why hold is not checked before CTS and if before CTS there is a huge violation, how you consider it.

1. CMOS basics (modes of operation and characteristics along with current
2. Pd flow briefly
3. Sanity checks (why netlist and timing sanity checks are done?)
4. Floorplan in details (What happens if macro is placed in centre)
5. What is Congestion and how to remove it?
6. CTS inputs (like clock transition, clock latency, clock skew, input cell