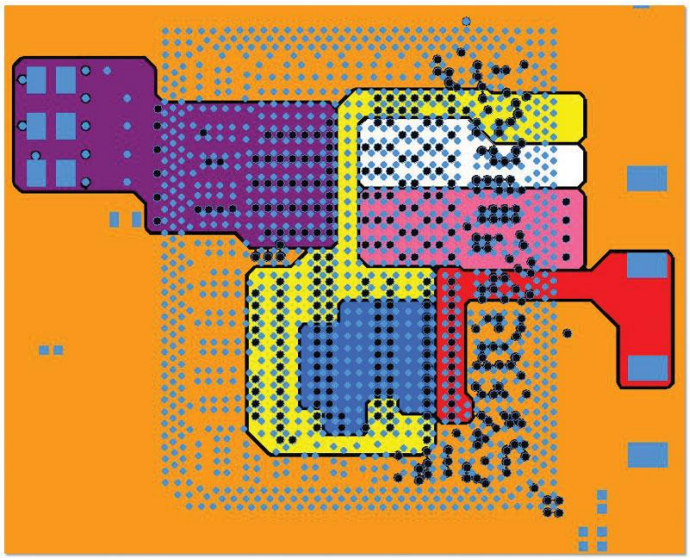
INTRODUCTION TO POWER INTEGRITY



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What is Power Integrity (PI)?

Power integrity can be defined as the assurance that an electrical system and all of its elements have the needed power such that operation can occur adequately or as intended. For design and analysis, this requires not only supplying adequate power to active components but also maintaining power levels and minimizing losses of all signals that your board processes. From the former perspective, your PCB can be viewed as a closed electrical system with a power distribution network (PDN). To achieve power integrity, all components or modules must be supplied with power at the level required for operation, which is not simply making sure that voltages are at, or above, an acceptable level. The major threat to power integrity for your PDN involves line variations or transients from your power supply that may cause fluctuations in the quality of your power profile.

During operation, the latter perspective must be included as the situation is even more complicated by the introduction of input and output signals. Digital circuitry is dependent on your components ability to distinguish between highs and lows (typically near 5V and 0V, respectively) and signal duration. The latter means that transitions or rise and fall times must also be properly recognized. Additionally, analog signals have an inherent frequency component that, in conjunction with amplitude, defines the quality of the signal and must be maintained. For frequency dependent signals, major concerns include external interference or noise and shifts along the transmission path that may result in distortion.

Today, PCBs are typically small and densely packed with components. This closeness of components, especially between signal traces and power paths can be a source of electromagnetic interference (EMI) or noise for your signals and impact power signal stability. In most cases, your boards are comprised of one or more high power components that require power dissipation to prevent adversely affecting other board elements. Optimal management of your power integrity requires that these higher frequency RF signals are isolated from your PDN. To a great extent, the power integrity of your board depends upon your application of design techniques and choices for its manufacture to mitigate these potential issues and promote power and signal integrity.

What is Power Distribution Network (PDN)?

In the early days of Printed Circuit Board (PCB) design, Power Delivery Network (PDN) was not a prominent consideration. With a high-speed design prevalent in the present context, PDN performance should be anticipated early in the PCB design and tailored to satisfy the device specification with lower voltage, higher current, and tighter noise margins. The objective of a PDN is to supply a clean and stable voltage to the core devices in a complex product design.

However, because of the parasitic added by the elements that make up the power network, the PDN analysis isn't perfect. It can be used to gauge and mitigate issues in major power rails at the early stages of the design. The PDN behaviour is estimated by measuring the PCB level parameters such as the overall respective net impedance, DC resistance, and total loop

inductance. To achieve reliable power delivery and low power loss, all PCB designs must have a PDN impedance of near zero.

Power rails on a PCB are part of the structure of the PDN. So, a transient generated on any one load may directly affect the rail and other loads might be impacted from that. The loading of the primary Voltage Regulator Module (VRM) is shown in Figure 1. Switching at Load 1 causes a transient voltage disturbance that is replicated by other loads. In this situation, components draw a large amount of current from the respective power rail with regards to the switching event. During this large amount of current draw, it interacts with the PCB parasitic all over the plane.

Many logic circuits switch at the same time in a practical integrated circuit, resulting in a complicated combination waveform as measured on the power rail.

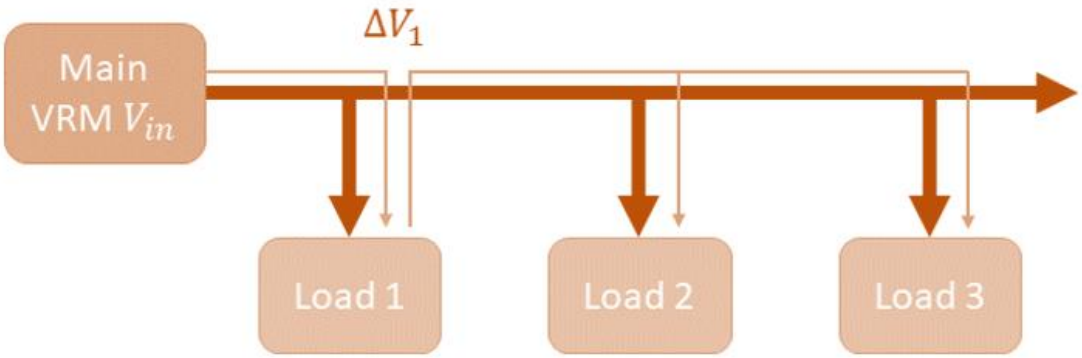

Figure 1 PCB Transient effect on loads

Why do we need a good PDN?

Active components of a PCB require energy from the power supply to operate and a good PDN suffices this need. On a PCB, earlier, integrated circuit devices used to have just one power and ground pin that could be readily linked to a long trace. As circuit density increased, connecting circuits to power and ground planes on a multi-layer board became more challenging. As pin counts rose and IC power needs got more sophisticated, circuit boards began to face some of the following issues:

1. Electromagnetic Interference (EMI)
2. Ground bounce
3. Power ripples

Electromagnetic interference (EMI): The faster the circuitry became, the more sensitive it could be to EMI from both internal and external sources. One way to guard against EMI problems is to configure the power and ground planes to shield against both incoming and outgoing interference.

Ground bounce: Simultaneous switching noise, also known as ground bounce, occurs when a large number of digital signals transition states at the same time. It is observed that in data and memory buses if signals do not return to their respective reference ground plane due to fast switching, they observe a bounce effect. This impact might cause unwanted noise in the circuits that could lead to mistaken switching causing the device to malfunction. When the current is pulled into the PDN, the most typical transient voltage effect is ground bounce. When this happens, the ground reference plane voltage rises while the positive rail on the PDN remains constant. The reference ground level may be controlled with the aid of a well-designed PDN.

Power ripples: When a transient current propagates voltage fluctuation on the positive rail, it creates noise, or ripples, in the circuitry. These are not the same as the rectified AC output signal. These waves can cause crosstalk in other circuitry that can degrade the signal quality in those circuits. The current flow route and the parasitic items present in the current's route separate the two effects. Figure 2 shows the typical use case for ground bounce and power rail ripple.

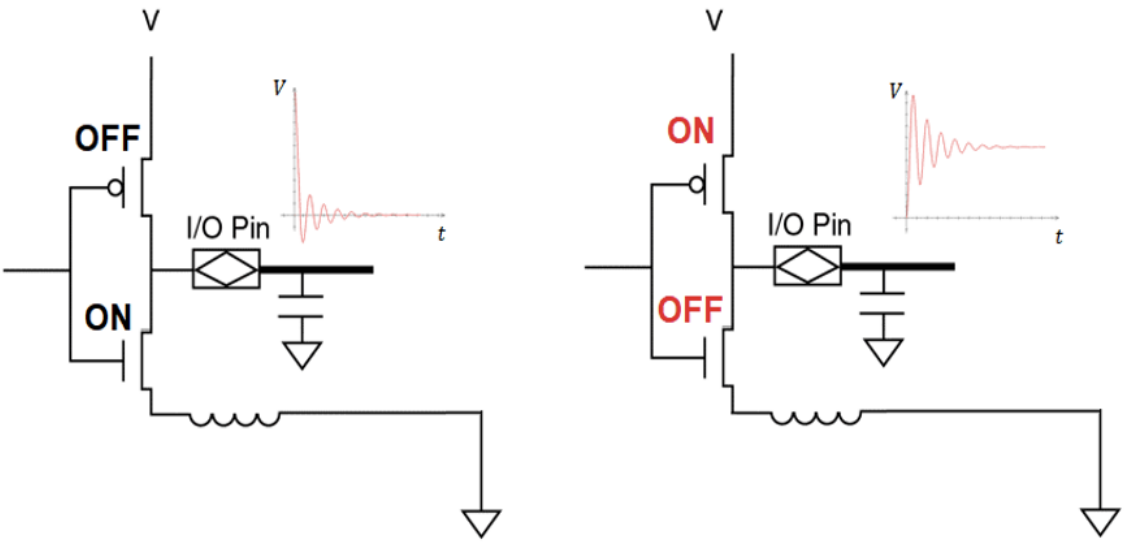

Figure 2 Ground Bounce and Power Ripples

An Integrated Circuit (IC) has many more power and ground connections to handle, in addition to the faster switching speeds of current circuits. On a large processor chip with Ball-Grid Array (BGA) packaging, there are hundreds of power and ground pins with varying reference values. To power the processor, these pins might also consume a lot of current. As a result, ensuring that the power is free of spikes, ripples, and noise necessitates a well-designed PDN.

PDN Fundamentals

The PDN can be represented as an R-L-C network and like any circuitry with some reactance, it can show a transient response that represents damped oscillation. The PDN impedance (Z) can be represented by a combination of resistance, inductance, and capacitance (R-L-C).

1. Inductor: Z = jωL
2. Capacitor: Z = 1/(jωC)
3. Resistor: Z = R

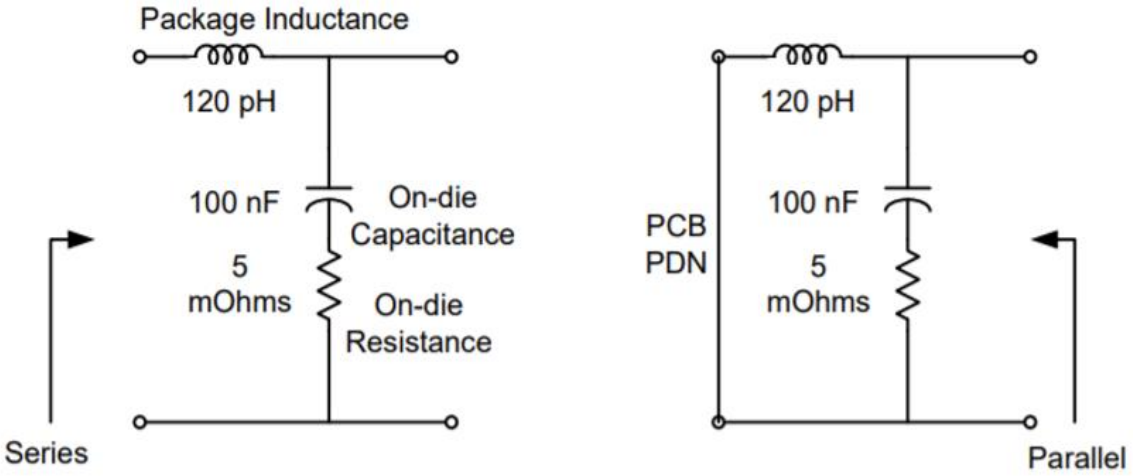

Figure 3 RLC component for PCB PDN

Figure 3 shows the RLC components of a PCB PDN. The complexity of the die structures (field-effect transistor (FET) devices, diffusions, and so on) can be combined with the complexity of the package structures (vias, power planes, balls, and so on) and represented by simple series and parallel circuits for resonance purposes. The RLC circuits are in series from the perspective of component measurement (looking in from the outside). However, because the PCB PDN has a very low impedance, the On-Die Capacitance (ODC) is in parallel with the packaging inductance from the inside looking out (looking out from the inside). When the same circuit components are put in series and in parallel, they behave differently. The frequency response of a typical series and parallel RLC circuit is shown in Figure 4.

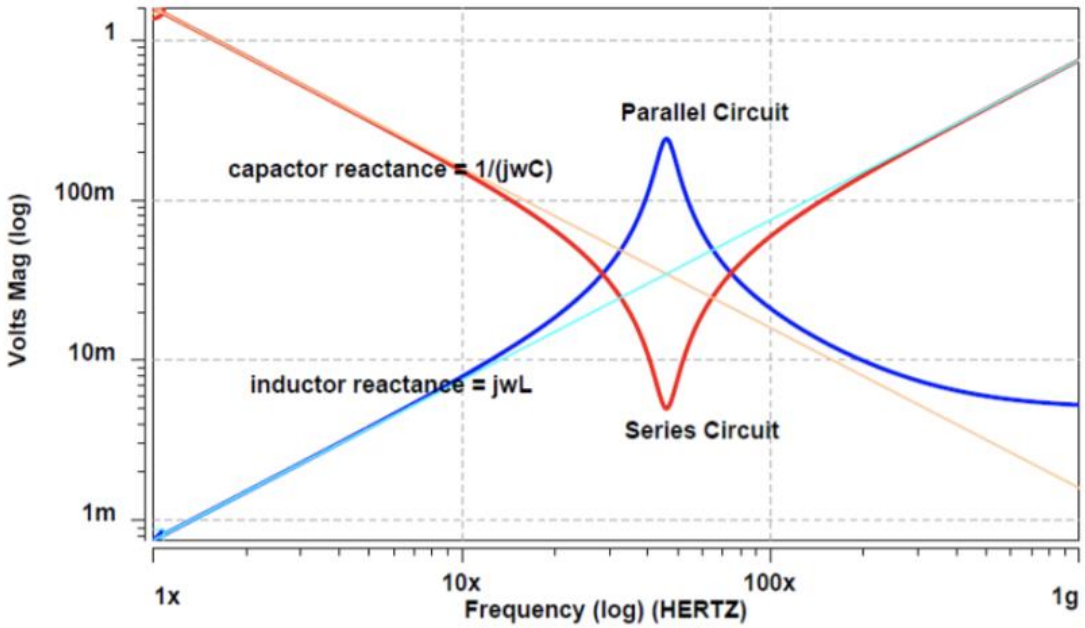

Figure 4 Frequency response for series and parallel RLC

Now, copper traces for power pins and copper planes for ground pins also play a crucial role in PDN performance. A simplified model of PDN can be shown in figure 5.

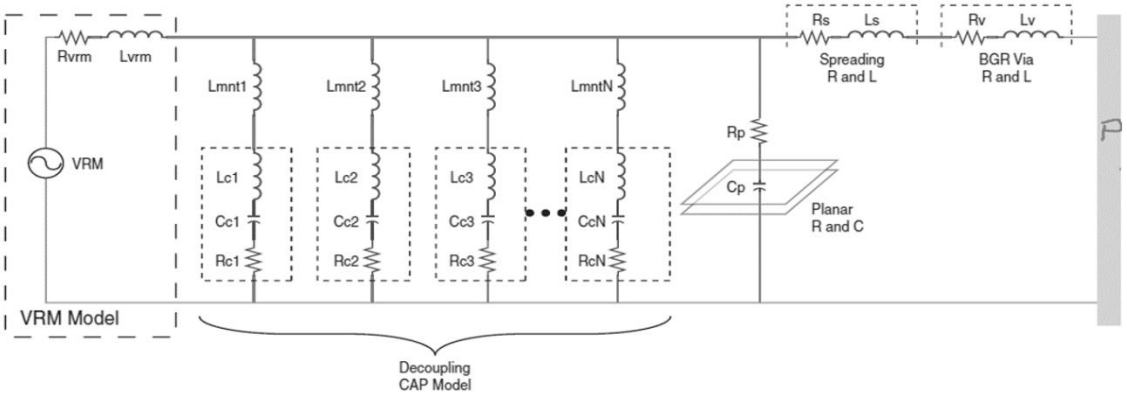

Figure 5 A simplified PDN model

PDN is like a multiport network. The switching component on DC buses can impact the overall DC buses' power distribution. It can cause some variations in the DC power sensed by all components on the PDN. In simulations, Z-parameters are used to benchmark the relationship between impedances seen at various ports. The voltage fluctuation visible at a PDN port in relation to the current drawn into all PDN ports is defined by this parameter matrix.

The target/maximum allowable impedance (PDN) puts a limit on the peak allowable impedance value for the PDN. The waveform of transient ripple on the power lines is determined by the PDN impedance that converts to jitters for a high-speed IC. For switching the IC, it draws current from the power buses that represent the pulse waveform via the PDN. Any capacitors and/or parasitic capacitances in the PDN will offer some reactance,

resulting in a transient response in the PDN. The purpose of the PDN impedance control is to minimize the effect of any transient waveform.

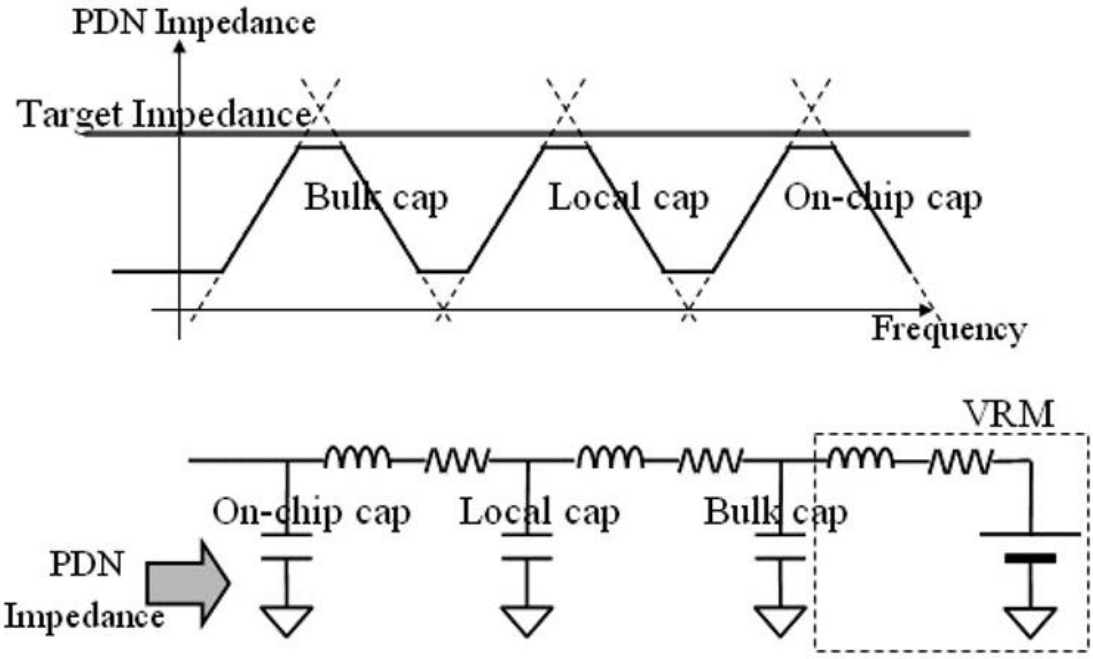

Figure 6 PDN impedance target

The goal is to keep the target spectrum below the target impedance value, from DC to the target frequency. The Frequency Domain method is used for Target Impedance calculation. Due to the predominance of the parasitic planar spreading inductance and package inductances, adding a reasonable number of decoupling capacitors does not lower the power rail impedance |ZEFF| below the target impedance (ZTARGET).

$$Z_{target} = \frac{Voltage\ Rail * \%\ Ripple}{0.5 * I_{max\ transient}}$$

For example - to effectively decouple 0.9 V rail, FTARGET of 50 MHz, 5% ripple (AC Component), and maximum allowable current of 4A (considering 50% as transient current) ZTARGET can be estimated as:

$$Z_{TARGET} = \left[\frac{(0.9)(0.05)}{4X0.5}\right] = 0.0225$$

The PDN utilizes PCB discrete capacitors (decoupling), interplane capacitance, and inductance to provide a very low impedance profile (Zeff) below the target impedance (ZTARGET) up to the desired frequency.

The voltage variations on the power bus are caused by a high PDN impedance. The best method is to reduce the PDN impedance to the lowest level achievable. This is accomplished by carefully selecting decoupling capacitors and strategically arranging neighbouring power or ground planes to achieve high interplane capacitance.

The PDN impedance and transient current determine the amount of transient waveform of ripple on the PDN bus. As impedance can be characterized as the functional domain of frequency, the impedance curve must be below the set target/peak value over the respective signal bandwidth. This relationship can be derived from Ohm's law. Figure 7 shows a typical curve for impedance with respect to frequency.

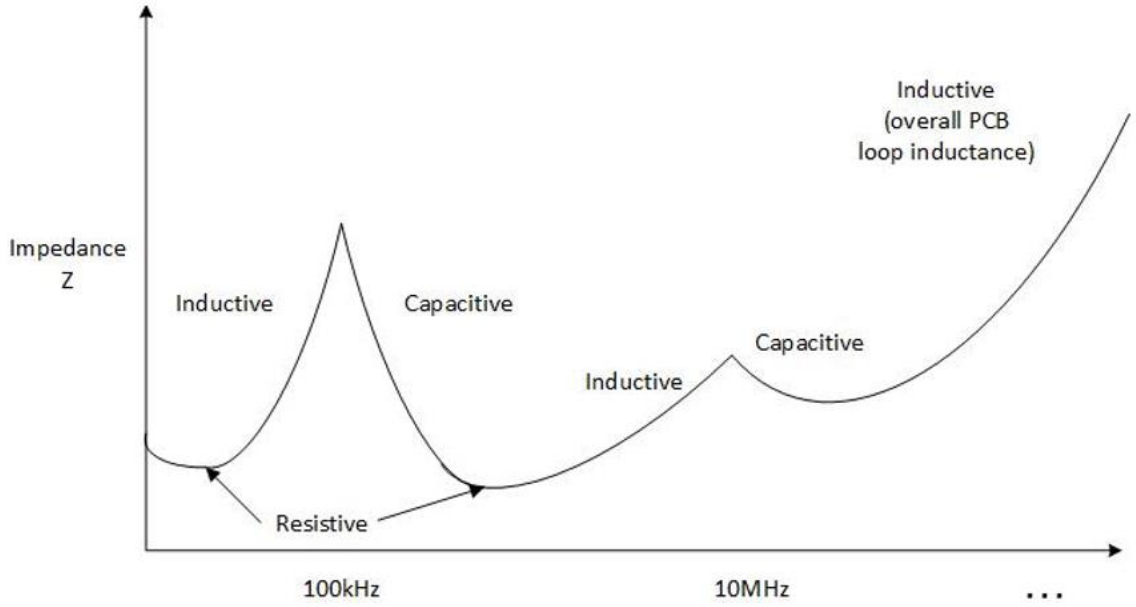

Figure 7 A typical impedance vs frequency curve

In the upcoming power integrity series, we will be discussing on the PDN analysis methods

References

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