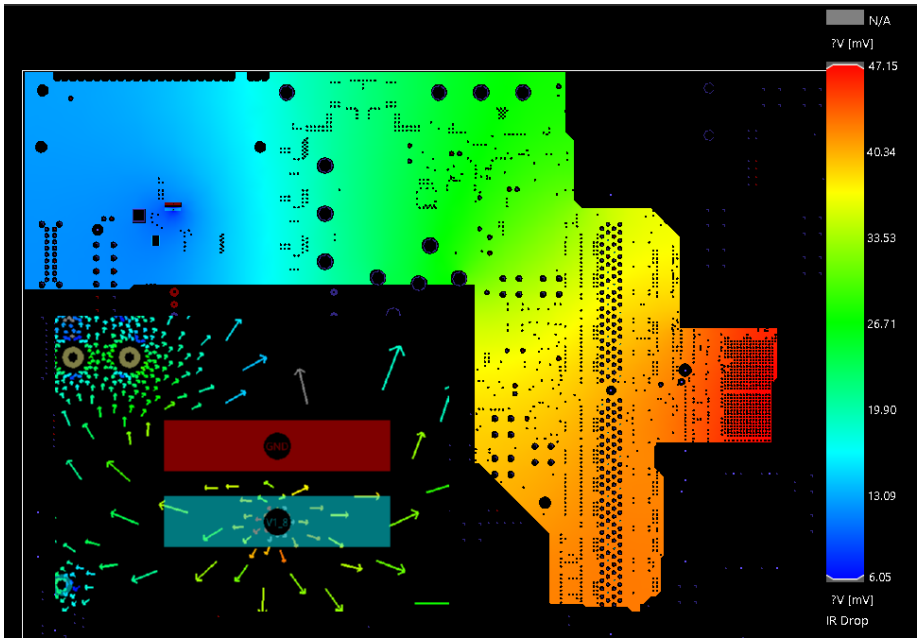
DC -IR DROP ANALYSIS



Source- Cadence

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What is Voltage Drop?

Voltage Drop is the decrease of electrical potential along the path of a current flowing in an electrical circuit. Voltage drops in the internal resistance of the source, across conductors, across contacts, and across connectors are undesirable because some of the energy supplied is dissipated. The voltage drop across the electrical load is proportional to the power available to be converted in that load to some other useful form of energy.

For example, an electric space heater may have a resistance of ten ohms, and the wires that supply it may have a resistance of 0.2 ohms, about 2% of the total circuit resistance. This means that approximately 2% of the supplied voltage is lost in the wire itself. An excessive voltage drop may result in the unsatisfactory performance of a space heater and overheating of the wires and connections.

National and local electrical codes may set guidelines for the maximum voltage drop allowed in electrical wiring to ensure efficiency of distribution and proper operation of electrical equipment. The maximum permitted voltage drop varies from one country to another. In electronic design and power transmission, various techniques are employed to compensate for the effect of the drop on long circuits or where voltage levels must be accurately maintained. The simplest way to reduce voltage drop is to increase the diameter of the conductor between the source and the load, which lowers the overall resistance. In power distribution systems, a given amount of power can be transmitted with less voltage drop if a higher voltage is used. More sophisticated techniques use active elements to compensate for excessive voltage drop.

Voltage Drop in DC Circuits: Resistance

Consider a direct-current circuit with a nine-volt DC source; three resistors of 67 ohms, 100 ohms, and 470 ohms; and a light bulb—all connected in series. The DC source, the conductors (wires), the resistors, and the light bulb (the load) all have resistance; all use and dissipate supplied energy to some degree. Their physical characteristics determine how much energy. For example, the DC resistance of a conductor depends upon the conductor's length, cross-sectional area, type of material, and temperature. If the voltage between the DC source and the first resistor (67 ohms) is measured, the voltage potential at the first resistor will be slightly less than nine volts. The current passes through the conductor (wire) from the DC source to the first resistor; as this occurs, some of the supplied energy is "lost" (unavailable to the load), due to the resistance of the conductor. Voltage drop exists in both the supply and return wires of a circuit. If the drop across each resistor is measured, the measurement will be a significant number. That represents the energy used by the resistor. The larger the resistor, the more energy used by that resistor, and the bigger the drop across that resistor.

Ohm's Law can be used to verify voltage drop. In a DC circuit, voltage equals current multiplied by resistance. V = I R. Also, Kirchhoff's circuit laws state that in any DC circuit, the sum of the drops across each component of the circuit is equal to the supply voltage.

Voltage Drop in AC Circuits: Impedance

In alternating-current circuits, opposition to current flow occurs because of resistance, just as in direct-current (DC) circuits. However, alternating current (AC) circuits also include a second kind of opposition to current flow: reactance. The sum of oppositions to current flow from both resistance and reactance is called impedance.

Electrical impedance is commonly represented by the variable Z and measured in ohms at a specific frequency. Electrical impedance is computed as the vector sum of electrical resistance, capacitive reactance, and inductive reactance.

The amount of impedance in an alternating-current circuit depends on the frequency of the alternating current and the magnetic permeability of electrical conductors and electrically isolated elements (including surrounding elements), which varies with their size and spacing.

Analogous to Ohm's law for direct-current circuits, electrical impedance may be expressed by the formula E = I Z. So, the voltage drop in an AC circuit is the product of the current and the impedance of the circuit.

DC-IR Drop

The difference in electrical potential between the two endpoints of an electrical circuit during current flow is called IR drop. During the current flow, the voltage (V) falling across any resistance (R) is the product of current (I) and resistance (R). IR drop is sometimes referred to as the of Ohms Law and could be written as:

V = I * R

IR drop in circuit is due to several factors, such as a rush current, power straps, insufficient power supply, a high impedance of the power supply network and power supply network architecture, etc.

Types of IR Drop

Local and global IR drops are the two basic types of IR drop. When a group of gates, in close vicinity, switches at the same time, this is known as "local IR drop". The term "global IR drop" refers to a phenomenon that happens when activity in one section of a chip causes an IR decrease in another section

IR Drop Analysis

In IR drop analysis, the power supply in the device is distributed equally in all the metal layers across the complete design. These metal layers have a limited resistance, when a voltage is applied to these metal wires, currents begin to flow through the metal layers, and some voltage is lost as a result of metal wire resistance and current. For IR drop analysis, many tools are utilized, including Apache's Redhawk and Cadence's Voltage Storm.

Redhawk from Apache IR drop analysis is used at different stages of the design flow. When changes are costly and have little influence on the project's timetable, it is preferable to employ Redhawk for IR drop analysis from the beginning of the design cycle. It can detect and correct through power grid design. This also decreases the number of adjustments needed in the sign-off step, where final static and dynamic voltage are conducted. As a result, Redhawk can be used at any point in the design process.

On the other hand, Voltage storm from Cadence used dynamic IR drop for analysing the effect of transient drop. It helps in optimizing the number of decoupling capacitors to reduce leakage in circuit designs. Vector-based and vector fewer methods are used for measuring the consumption in voltage storm tools.

IR Drop Impacts

If the voltage drop is too high, the circuit will not have enough voltage, resulting in timing failure. If IR drop is increasing the clock skew then it will result in a hold time violation otherwise it will be a setup time violation.

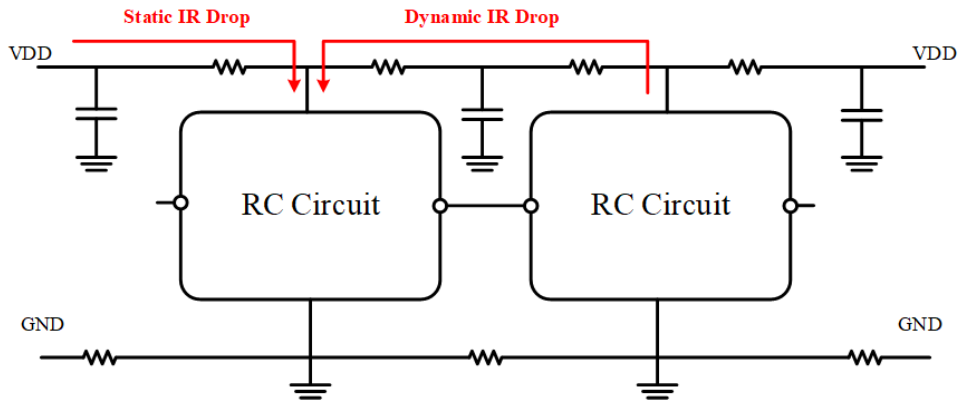
IR Drop in ASIC Design

In ASIC design two types of IR drops are normally occurred i.e. static drop and dynamic drop.

Static IR drop is the average voltage drop for any given design. It is determined by the RC of the power grid that connects the power source to the appropriate standard cells. Static IR decrease is denoted as:

$$Vs = I_{avg} \times R_{wire}$$

Dynamic IR drop refers to a voltage loss caused by the high switching activity of transistors. It is determined by the switching time of the logic and is less affected by the clock period.



IR Drop in Semiconductors

Every transistor in a chip requires power. The metal layers are used to distribute the power around the microprocessor. The size of the wires has shrunk as fabrication processes have been reduced significantly, although the physical chip dimensions have remained nearly the same. The voltage is dropped when the current flows through a resistor, which is referred to as IR drop. When a transistor's voltage lowers, it gets slower, which might affect circuit timing. This can lead to a functional failure if it occurs on a vital path in a design, hence it must be avoided. In Semiconductor design IR drop is a reduction in functional voltage, which means that small variations in supply voltage might account for a growing percentage of the digital swing, potentially resulting in inaccurate logic results.

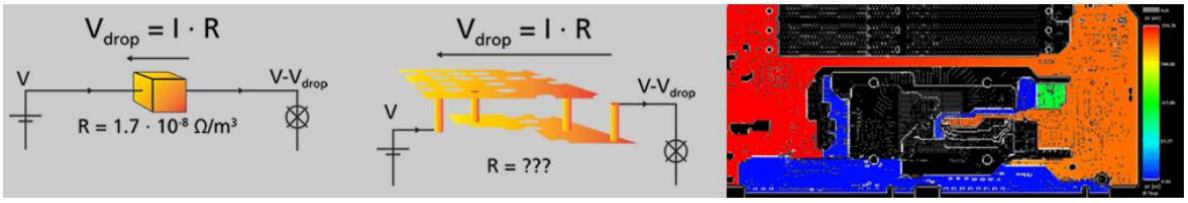
IR Drop on PCBs

Electronic components on printed circuit boards operate with different supply voltages like 5V, 3.3V, 2.5V or less. The components work as specified when the supply voltage is stable within a given tolerance as specified in the datasheet i.e. +/- 10%. A voltage drop is called IR-drop on PCBs and happens, when a voltage is connected to the device pin with a trace or plane, which has an ohm resistance. If the trace or plane is thick and wide the resistance will be low. But when space on a PCB is limited, the track width is often small and supply planes have many holes. In such a case there will be loss of voltage due to Ohm's law. Energy is transformed from electrical energy into thermal energy and the value for the voltage goes down.

$V_{drop} = I * R$ (V_{drop} is called IR-Drop)

$P = I * V_{drop} * R$ (P is the power converted from electrical to thermal energy)

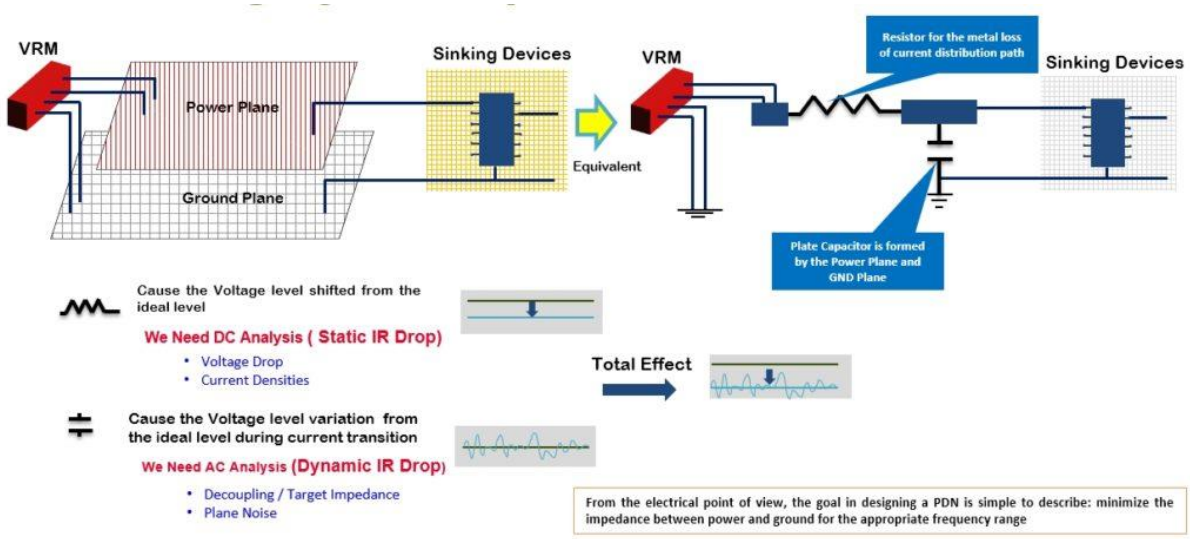
With IR-drop analysis the PCB designer can see where a plane has too many wholes, a trace is to narrow and too long or there are not enough vias placed. In these cases, the voltage drops. The resistance can be calculated with a field solver and a simulation shows the results for current, voltage drop and temperature increase.



Power / ground paths should have low resistance. The goal is to ensure that minimum power is dissipated as heat in the system. Each voltage drop will generate heat and might cause thermal issues with some components close by. When the voltage drops to much, the supply voltage might reach the lower tolerance of the supply voltage and the electronic components fail. Power integrity is an important consideration in advanced devices as it is deeply related to many signal integrity problems.

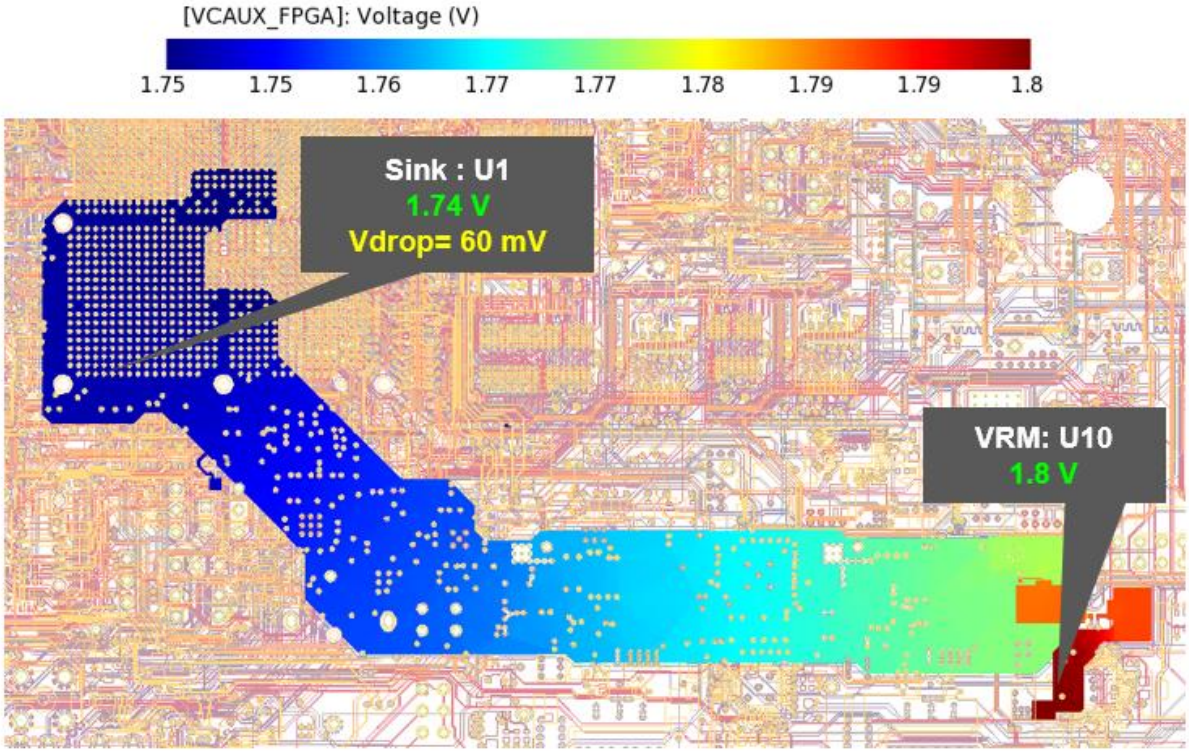
Power Integrity (PI) Analysis

In power integrity analysis, the main types of simulations are dc voltage drop analysis, decoupling analysis, and noise analysis. First, dc voltage drop analysis involves the analysis of complex trace and plane shapes on the PCB to determine how much voltage is being lost due to the resistance of the copper. In the PI analysis, energy is distributed through transmission planes that make the analysis more complex than basic SI, since energy is moving in x and y directions, as opposed to just one direction down the transmission line.



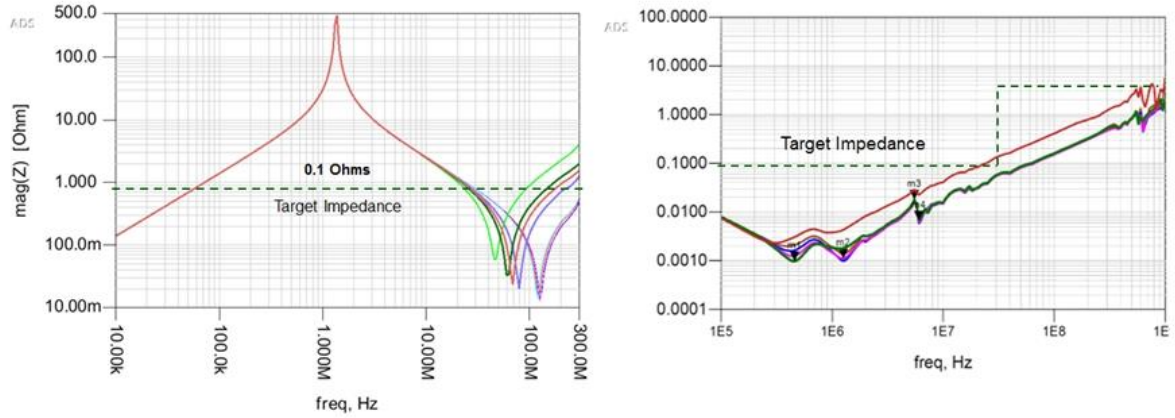
DC Simulation

PI-DC analysis computes the voltage, IR drop (voltage drop), current, and power loss density in the power supply nets. Using this analysis, it is identified how much current is drawn by IC and connector pins or stitching vias at DC operating conditions. Due to excessive voltage drop, the power supply voltage at the IC might fall below the recommended minimum voltage. This can cause malfunctioning of the IC. Excessive current density in the perforated power supply rails can generate excessive heat, which might lead to board failures due to delamination or fusing. Also, excessive current in the stitching vias can lead to failures losing connection. Any number of power supply nets with source and sink models can be simulated together. The simulated DC IR drop result of 1.8 V VCAUX power plane is shown in Fig below. The maximum voltage from VRM to sink (ICs) is 60 mV. Similarly, all PDNs are simulated to get the max voltage drop in power plane.



AC Simulation

At DC, modeling is relatively simple so that the series resistance of traces, plane shapes, and vias need to be calculated. But, for high frequencies, analysing the impedance between power and ground at various locations on the PDN requires complex calculations. PI-AC analysis computes the impedance for the IC current loads over a broad frequency range. It helps to identify whether the PDN provides a low impedance path from the VRM to the IC. AC analysis is carried out to find out the PDN impedance seen from the IC. The VRMs provides 0.9 V to 5 V, the IC pulls 0.1 to 6 A, and a 5% tolerance on the supply voltage is allowed up to around 300 Mhz The result and target impedance is shown for VCAUX power plane in Fig below. Target impedance 0.1 Ω is the green line. At higher frequency, the target impedance specification is more relaxed and rises with frequency. Excessive impedance in a certain frequency range can generate excessive voltage noise, which is also called dynamic IR drop, when the IC power supply pins draw large amounts of transient current required for I/O or core logic switching at rates that fall into that frequency range**.**

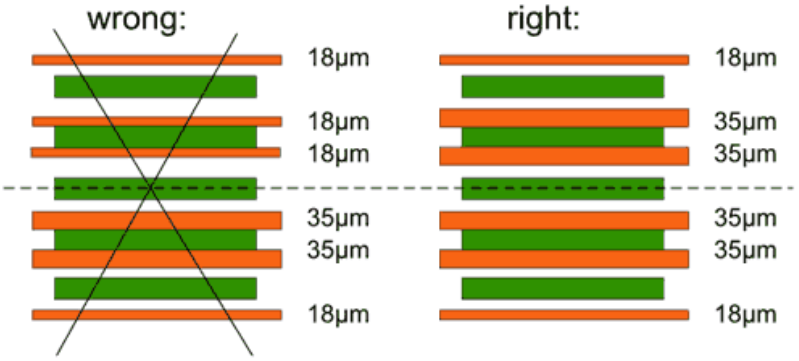


PND impedance profile of 1.8V VCAUX power plane without de-caps with de-caps

PCB Design Guidelines For PDN

Achieving PDN target impedance can be arduous. Using the guidelines mentioned below, you can achieve a PDN close to the target value.

1. Always adapt symmetrical layer stack up (i.e., the top layers must be mirrored in bottom layers). The combination of an uneven layer stack up and high heat and pressures of the manufacturing process might cause the board to distort.



2. Prepreg and core layers are symmetrical in their thickness (throughout the stack up).

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			1.4	7	4	0.31	53.53	98.54		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	5								Core
3	Inner 3	Conductive			1.4	7	4	0.31	50.69	90.13	66.78	Signal
		Dielectric	4.3	5								Prepreg
4	Inner 4	Conductive			1.4	7	4	0.31	50.69	90.13	66.78	Signal
		Dielectric	4.3	5								Core
5	VDD	Conductive			1.4							Plane
		Dielectric	4.3	12								Prepreg
6	GND	Conductive			1.4							Plane
		Dielectric	4.3	5								Core
7	Inner 7	Conductive			1.4	7	4	0.31	50.69	90.13	66.78	Signal
		Dielectric	4.3	5								Prepreg
8	Inner 8	Conductive			1.4	7	4	0.31	50.69	90.13	66.78	Signal
		Dielectric	4.3	5								Core
9	VCC	Conductive			1.4							Plane
		Dielectric	4.3	3								Prepreg
10	Bottom	Conductive			1.4	7	4	0.31	53.53	98.54		Signal
		Dielectric	3.3	0.5								Soldermask

3. Assign power and ground layers first and as close as possible i.e., minimum dielectric thickness between power and ground planes.
4. If possible, keep the power and ground plane layers in the board layer stack symmetrical to maintain signal integrity.
5. Try to maintain the highest density copper layers in the middle of the stack. This must, once again, be done in combination with proper signal integrity procedures.
6. For different plane layers, use the same copper weight. Consider using metal fillers (copper pours) in places where there isn't a lot of metal.
7. Most essential, before committing to suggested board layer stack up, verify with PCB manufacturer to guarantee that process can fabricate it.
8. Confirm with the fabricator the minimum Anti-pad (the void area around a via on internal plane layer) gap that he can do reliably. Follow the same in the design as it helps lower the DC resistance.
9. PCB floor planning should be given the highest priority and shall be considered and worked upon while schematic is 50-60% done. You can speed up the process by leveraging the reference design right from the start.
10. Use decoupling capacitors after major component placement. Inductance is an enemy here and capacitance is a lifesaver. The higher the number of capacitors the lesser number of failures in the PDN.
11. Select a variety of capacitor values so their resulting impedance profile is flat and looks resistive all the way to the frequency.
12. Via on pad should be followed wherever possible in the design. Not only for BGA fanout but for discrete also. Avoid via sharing, it could be disastrous.
13. Placement and orientation of decaps could be optimized using a mix of topside or backside capacitor placement.
14. Do not share power trace for net critical to noise –check design guidelines and layout checklist respective to the device.
15. Larger power loop increases inductance in the path, avoid creating loop inductance paths.
16. Use as many parallel return paths in the power-ground interconnects.

17. Each power rail pin should have decaps. Connect them with the through-hole via if on the other side of the board.
18. Connect the same nets with vias. Blind and buried via should be staggered.
19. Copper planes can be used for thermal improvement.
20. Make small islands for power rails, if not possible then wider traces should be followed depending upon the estimated current requirement.
21. Fanout strategy must be planned to minimize the return path and thus the loop inductance.
22. Place the through-hole vias on the four corners of the IC to provide an easy return path.
23. To reduce the voltage response to a transient current step, increase the capacitance or decrease the inductance

EDA Tools for PI Analysis

- Cadence Sigrity
- Hyperlynx from Siemens
- Ansys SI wave
- ADS from Keysight

References

https://embeddedcomputing.com/

https://www.cadence.com

https://hardwarebee.com