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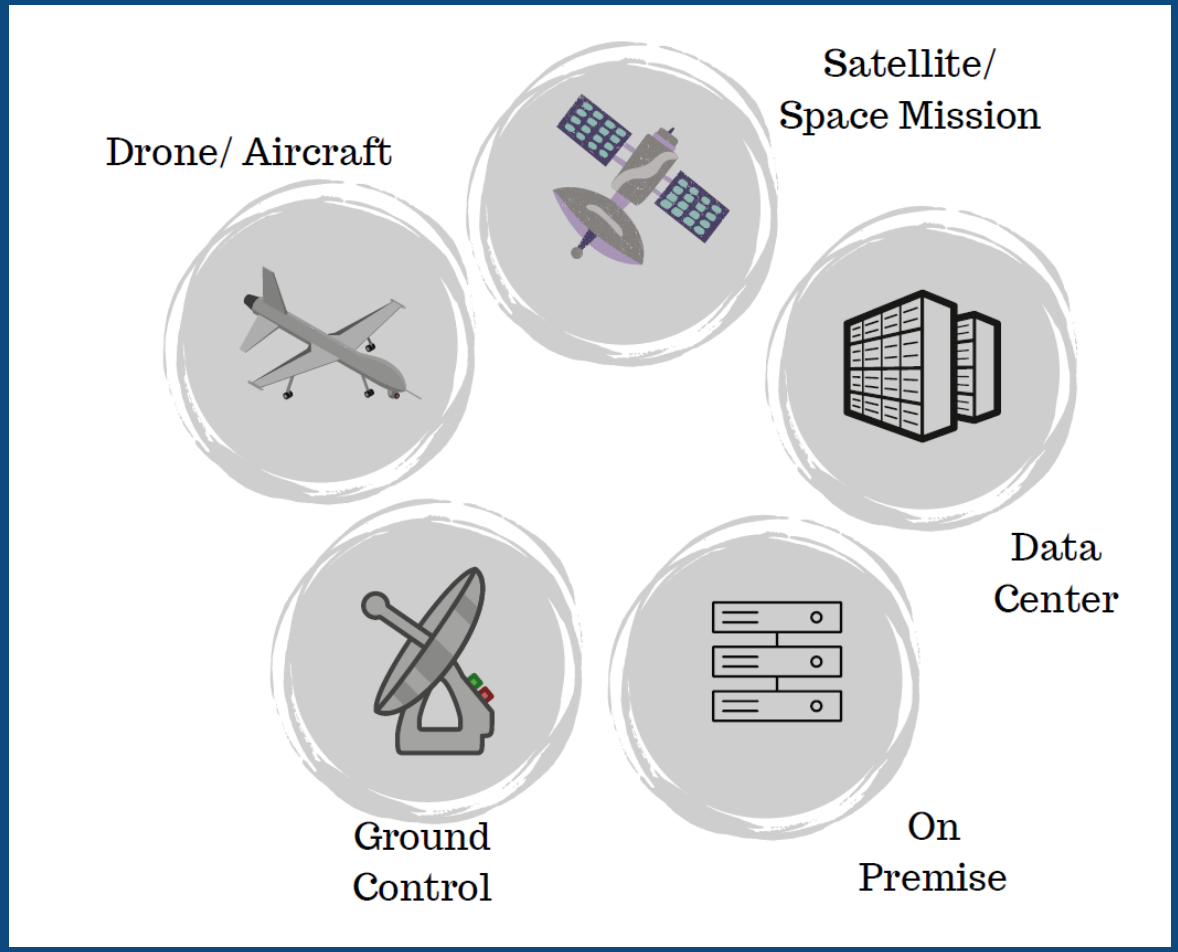
NSF-Crosstalk Phase I Updates

- Mission and objectives:
  - Dual-use AI accelerator/Big data analytics chip design
  - Demonstrate proof-of-concept at 28nm
  - Develop a software interface to communicate with the chip
  - Benchmark against state-of-the-art for computer vision application (i.e., ResNet-50)

- Recent Updates
  - NSF Phase I ended
  - Pending proposals and incubations



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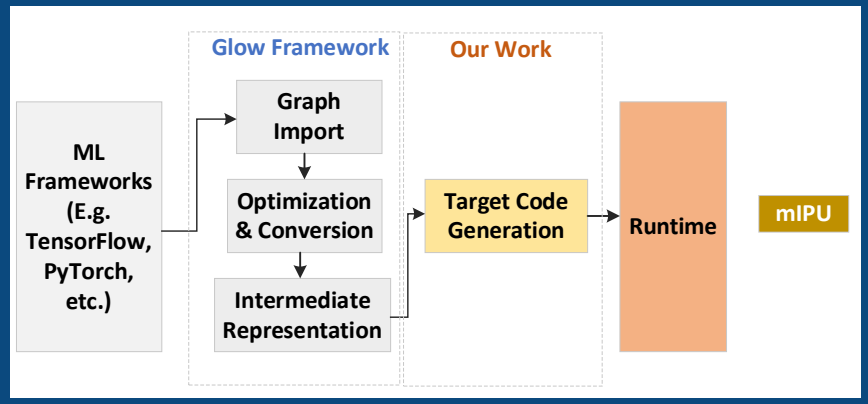
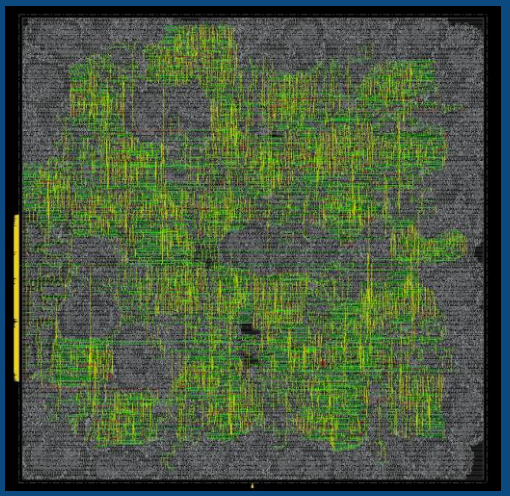
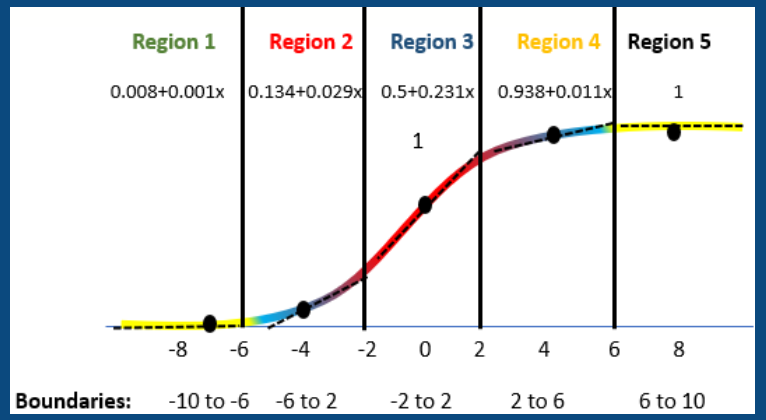
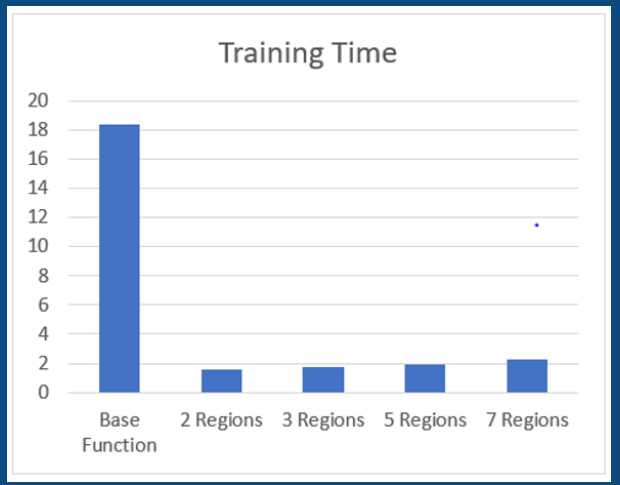
High-Level Overview of the Program:

- Develop chip design flow to go from RTL to GDSII.
- Optimization for Area, Power, and Performance.
- Integrate embedded memory from TSMC.
- Develop software interpreter to interface with Open-Source Compilers.
- Explore commercialization opportunities.
  - NDA: **Qualcomm, TactComputeLab, NAG, HP, InAccel**









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Program Summary

- Sponsor: NSF
- Funding: $256K
- Number of staff/faculty/students:
  - Staff – 1
  - Faculty – 2
  - Students – 1
- Major milestones remaining:
  - Finalize GDS II with optimized power and performance
  - Test the chip
  - Identify customers and commercialization pathway
- Timeline for project: 01FEB21 – 31DEC22

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