Note Title 18-10-2012 Branches: Delayed Branch Delayed Normal Branch. 134 + Higher IPC rif delay slots are filled - Over-emphasis on the compiler.

Predict the direction of the Branch: Taken No? Taken (T) (NT) $(NPC \neq PC+4)$ (NPC = PC+4)ID EX MEM WB Correct branch frediction -> do nothing Wrong branch " -> concel the incorrectly fetched instructions fetch from correct address + compiler independent

How do we fredict branches? Typical program Predict: always taken (mostly corred) Bronch 7/NT Pred. Coon foss -> 50%. always taken -> 70%

```
2-bit saturating counter (c)
(implemented in HW) incl) decl)
               C. inc () {
                   Value = min (value +1, 3):
             C. dec () {
                    value = man (value-1,0);
```

1) Simple Predictor: Branch frediction (\$\$) by = some output as last branch. 1st fred -> X 3NT with fred > x

Fredictor, which does not take exceptions very seriouly.

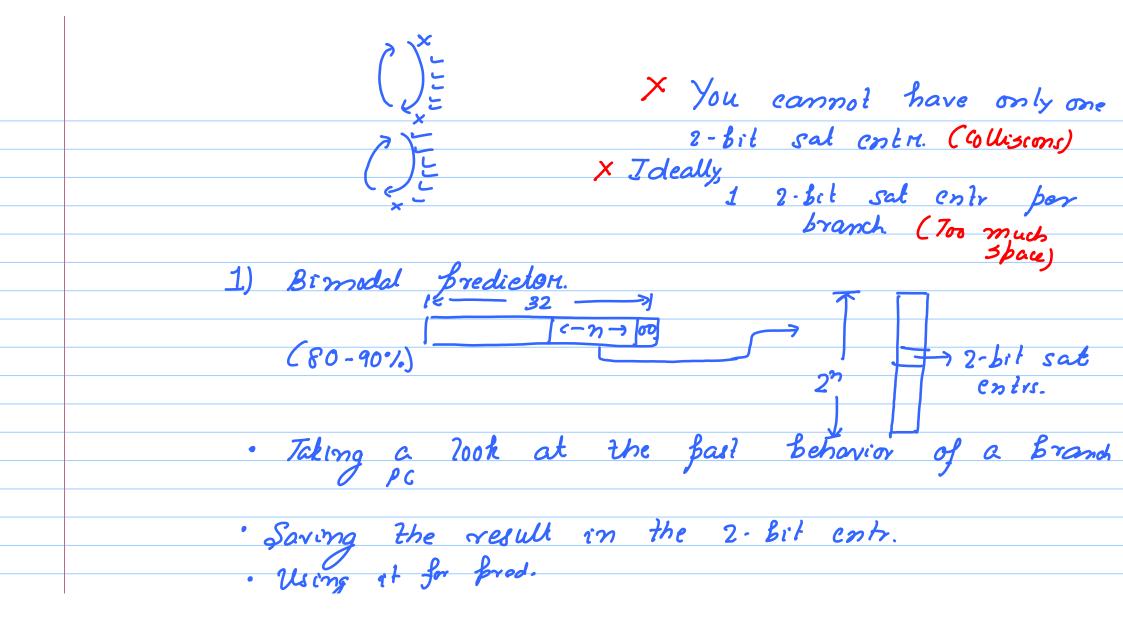
predict NT predict T

Branch Predictor - predict (PC) -> [T,NT] (IF)

Train (PC, [7/NT]) (EX)

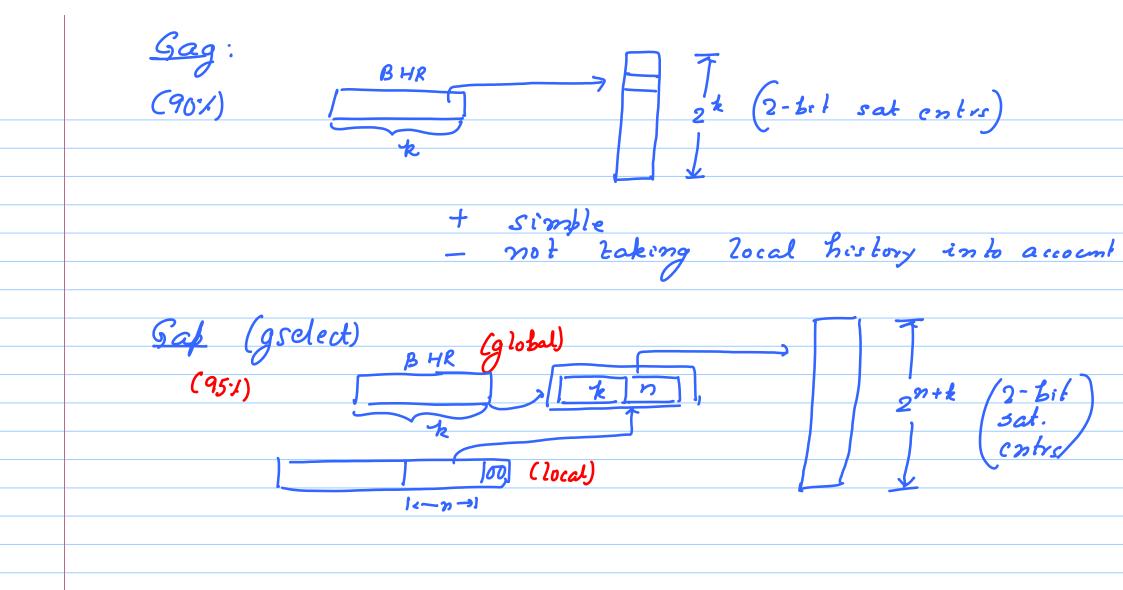
2-bit sat entr. adds some memory to the branch fredictor.

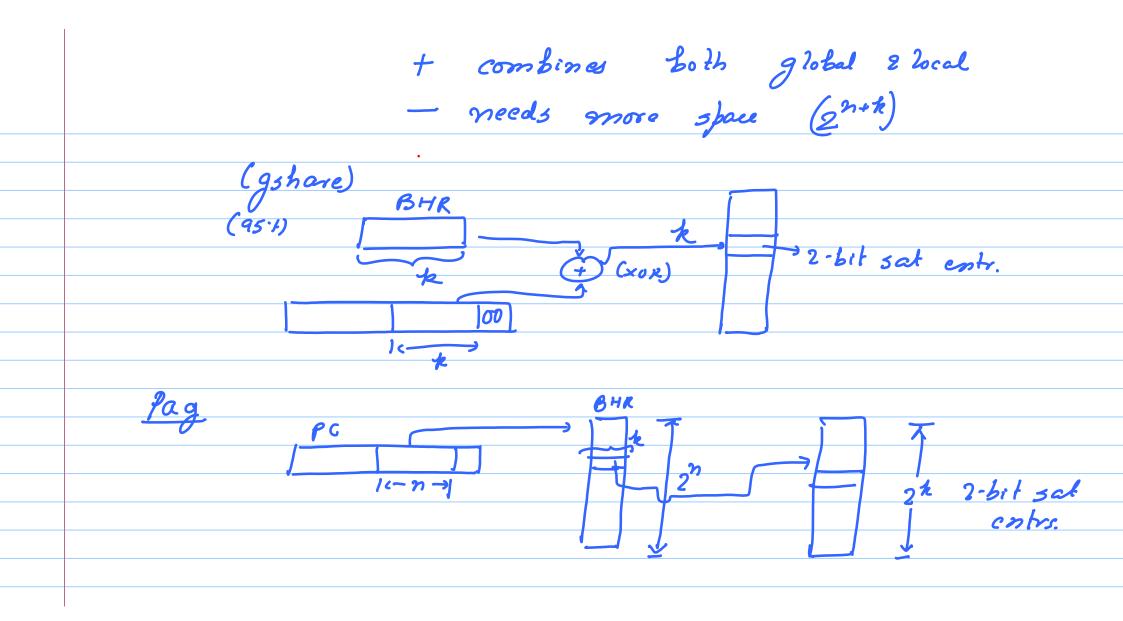
For the example with two loops, makes one less mistake.

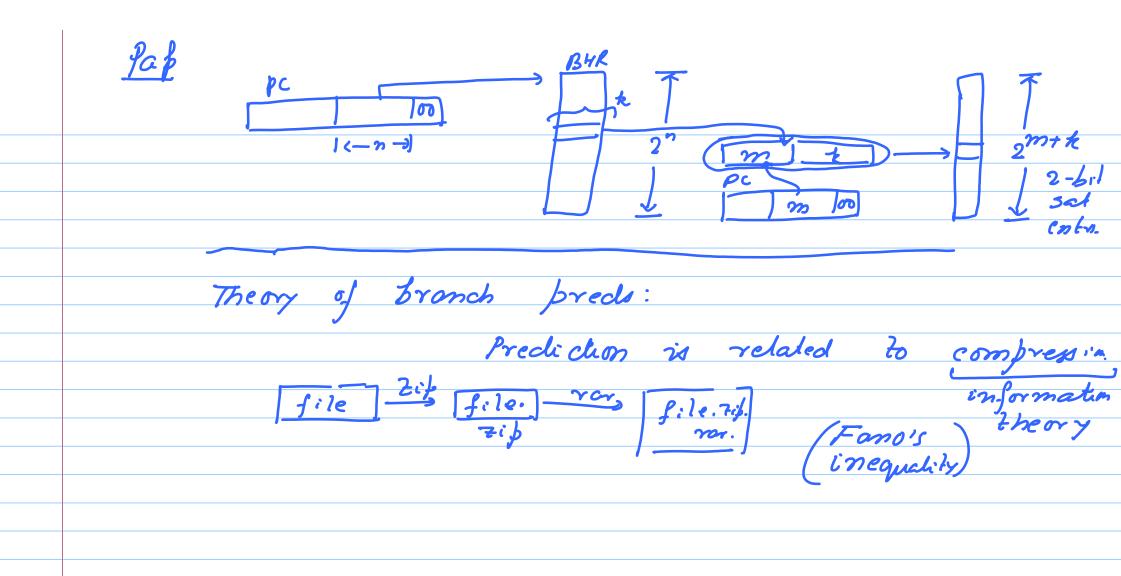


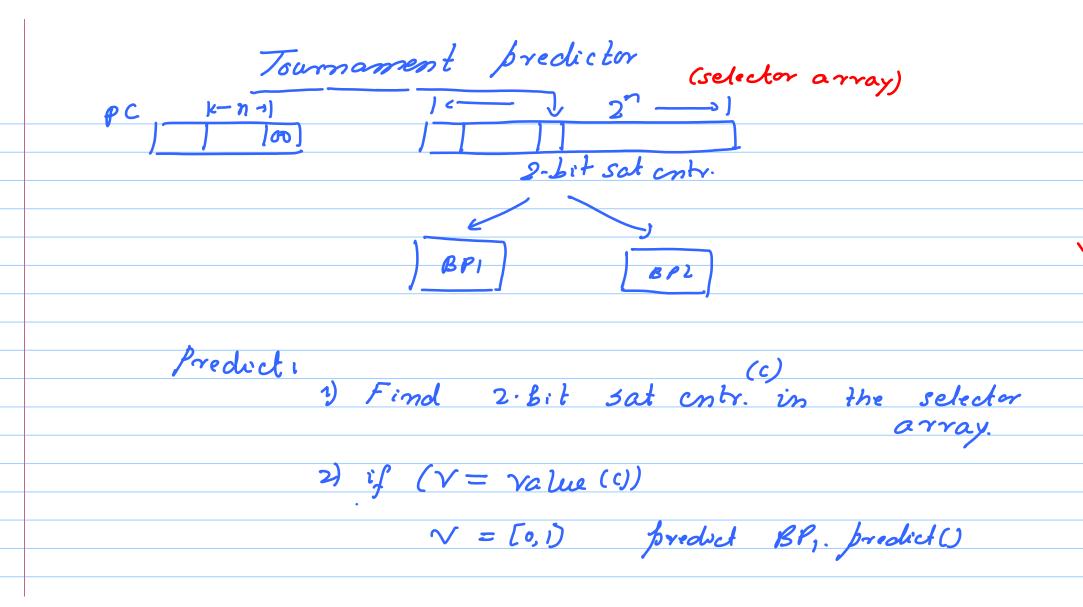
+ reduces collisions. if $(f \log 1 = 0)$ B $f \log 2 = 1$; if $(f \log 2 = 1)$ (B2) frints ("great"); (B, is NT) => (B2 is NT) Branch History Register: BHRR oldest 1-bit per

Branch 20cal History global history Behavior of past executions of the branch PC behavior of last k branches (irrespective BHR 2-bit sat ontr. Family of branch freds. G -> g lobal
P -> pattern (local)









V = [2,3] fredict BP2. predict () Train:

1) Train the selector array. 2) Train BP, and BP2