Aug 18th Note Title 18-08-2011 Assembly Instructions [REFERENCE MANUAL] Data Processing Instructions Arithmetic: ADD, SUB, MUL, UDIV Shift: LSL, LSR, ASR Logical: ORR, AND Pata Movement: MOV, MVN Three formals: Register, Immediate, Shifted

Data Transfer Instructions (DT) ME MORY (DT) Reg is ters LDR, STR LDR (Load Register) 1) Read the value register, γ_2 Memory 2) Let the value be A 3) Read memory at location, A 4) let the value be x

~5) save × in register 71

2DR (destination reg. > [Add ress]
Y2 = 1000	Memory
LDR ~, [~2]	
We are always loading or storing	->(D1 m
we are always loading or storing	15 100
	1001
an integer (4 bytes)	100
4 Int - 4	
Short -2	
Chor - 1	
1 ma / Double - 8	?
Long / Double - 8 Float - 4	

Little Endian Vs. Big Endian $\frac{t = 0x FF AD 34 B2}{mse}$ Little Endian -> LSB is stored in the lowest CARM, INTEL X80 position Big Endian -> MSB is stored in the lowest (spare, 12m, He) position. (BE) 1000 BZ LSB

(1) = OX FE AD 34 B2 Y2 = 1000 1000 - 1003 Reverse of a Load 7 STR Y, [12] MEM [Y] = X Different variants of LDR /STR Instructions Formats / Add ressing Modes. 1) LDR 7, [7.] Register Formet Address = 72

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Cleast count is always bytes)
2) LDK Y_1, [Y_2, #16]

Address = Y_2 + 16 [Immediate Format]
 3) LOR 7, [92, 93]
               Address = 72+73 [Register offset]
  4) LDR 7, [x2, x3, csc#3]
               Add ress = \gamma_2 + \gamma_3 << 2 [Scaled reguster offset]
            Some more addressing modes
            CWe will look at them later)
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LDRB/STRB -> Load 2 Store Integers

LDRB/STRB -> Load/Store 1 by te

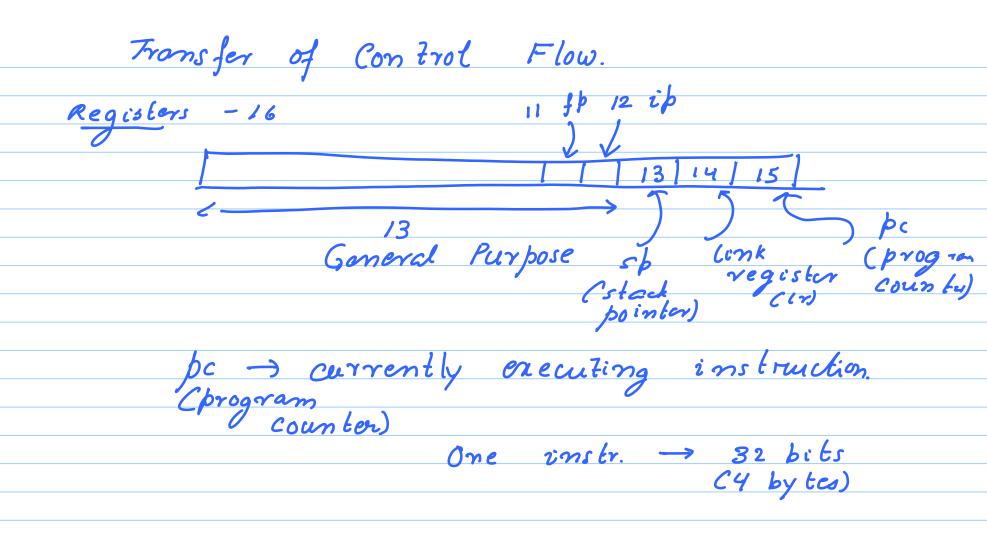
LDRH/STRH -> Load/Store 2 by tes

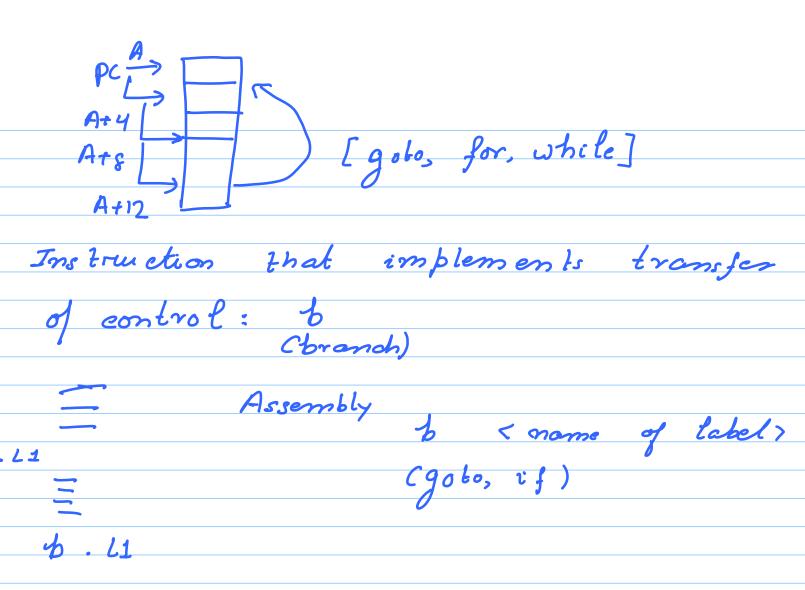
MEMORY WORD -> 4 by te.

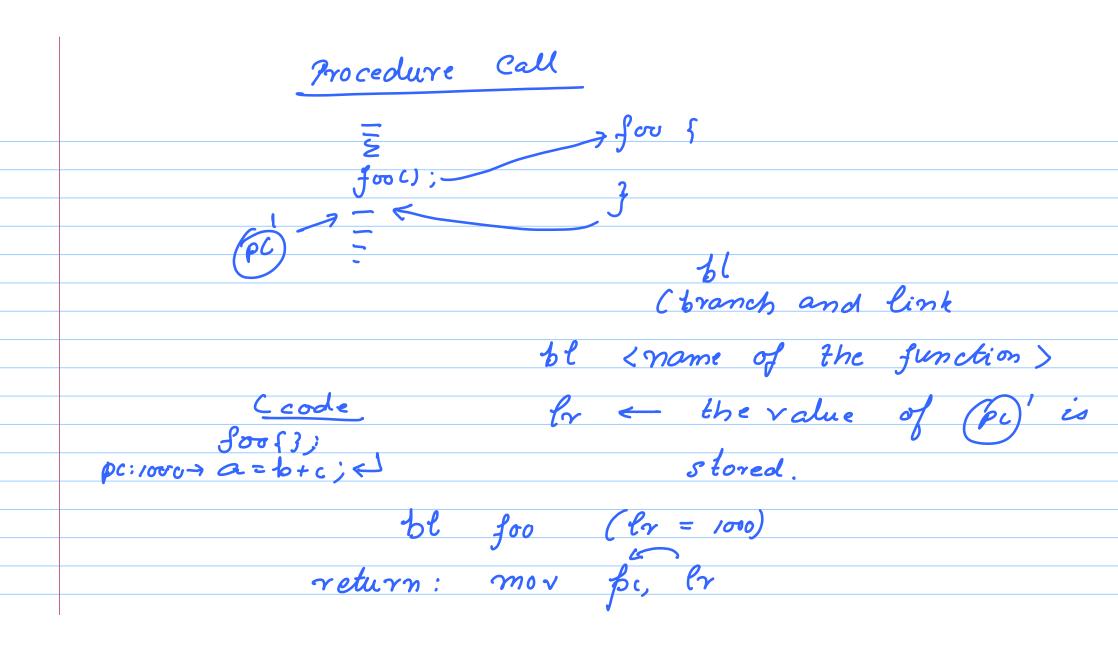
Data Processing & Data Transfer.

* Control Instruction

Branches, Jumps, Procedure calls, Returns







Tutorral: Saturday.

Basic Overview of Assembly Code

[Some examples]

(1) Mini - Homework

TA: Abhishek

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Next Week: Wednesday. 11-12:30

Saturday: 11-12:30