Exam 2 - Part A (multiple choice questions)

Started: Nov 29 at 8:47am

Quiz Instructions

Question 1 **5 pts**

A key feature of pipelining is that it increases the throughput of the system (i.e., the number of customers served per unit time), but it may also slightly increase the latency.

- (●) True
- ( ) False

Question 2 **5 pts**

Conditional data transfers offer an alternative strategy to conditional control transfers for implementing conditional operations. They can only be used in restricted cases.

- (●) True
- ( ) False

Question 3 **5 pts**

DRAM is faster than SRAM, and Disk is much faster than DRAM.

- ( ) True

- (●) False

Question 4 — 5 pts

DRAMs and SRAMs are volatile in the sense that they lose their information if the supply voltage is turned off.

- (●) True
- ( ) False

Question 5 — 5 pts

Usually, SRAM is used for cache memory and DRAM is used for main memory.

- (●) True
- ( ) False

Question 6 — 5 pts

In RISC, "load" and "store" are usually separate instructions.

- (●) True
- ( ) False

Question 7 — 5 pts

RISC has a set of attributes that allows it to have a lower cycle per instruction (CPI) than a complex instruction set computer (CISC).

- (●) True
- ( ) False

Question 8 — 5 pts

Since different instructions may take different amounts of time depending on what they do, CPI (Clock cycles per instruction) is an average of all the instructions executed in the program.

- (●) True
- ( ) False

Question 9 — 5 pts

The term 'clock cycles per instruction', which is the average number of clock cycles each instruction takes to execute, is often abbreviated as CPI.

- ( ) True
- (●) False

Question 10 — 5 pts

The instruction set architecture affects all three aspects of CPU performance, since it affects the instructions needed for a function, the cost in cycles of

each instruction, and the overall clock rate of the processor.

- ○ True
- ○ False

Question 11 — 5 pts

The efficiency of the compiler affects both the instruction count and average cycles per instruction since the compiler determines the translation of the source language instructions into computer instructions.

- ◉ True
- ○ False

Question 12 — 5 pts

Our favorite program runs in 12 seconds on computer P, which has a 2 GHz clock. We are trying to help a computer designer build a computer, Q, which will run this program in 8 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer Q to require 1.2 times as many clock cycles as computer P for this program. What clock rate should we tell the designer to target?

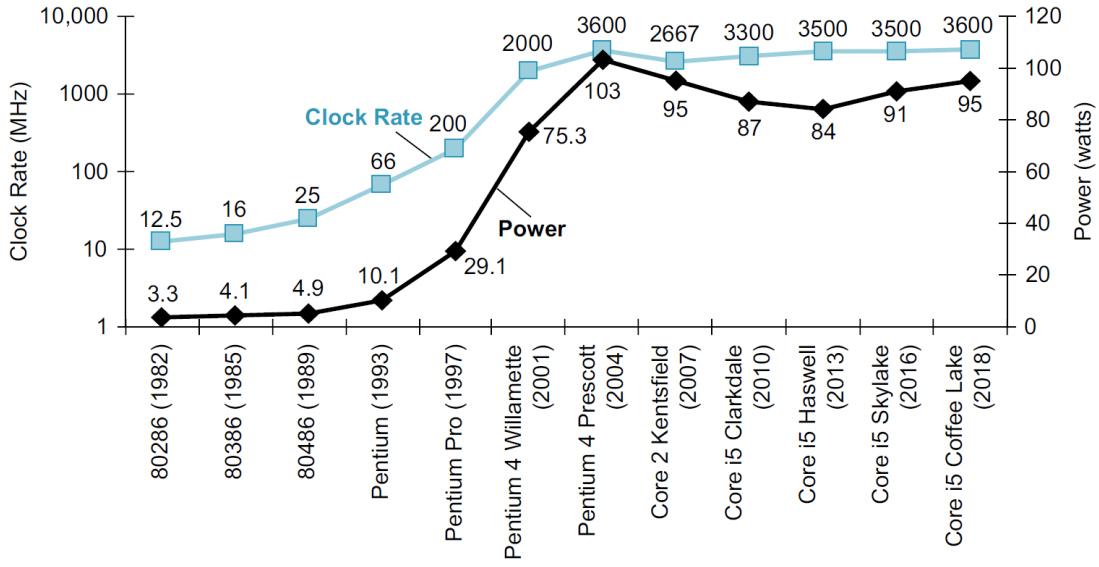
- ◉ 3.6 GHz
- ○ 4 GHz
- ○ 4.2 GHz
- ○ 4.1 GHz

Question 13 — 5 pts

Suppose we have two implementations of the same instruction set architecture.
Computer W has a clock cycle time of 250 ps and a CPI of 3.0 for some program,
and computer X has a clock cycle time of 500 ps and a CPI of 2.0 for the same program. Which computer is faster for this program?

- ○ Computer X
- ○ No correct answer
- ◉ Computer W
- ○ Both

Question 14 — 5 pts



The graph shows the relationship between clock rate and power. Select the correct statement below based on this graph

- ○ This graph is representing the processors over 5 years
- ○ Energy and thus power cannot be reduced by lowering the voltage
- ◉ The clock rate and power are related to each other
- ○ The clock rate and power are not related to each other

Question 15 — 5 pts

Find the best match of the seven great ideas from computer architecture to this real-world example:

Make a copy of your HW and email the HW to yourself fearing a harddisk crash

- ○ parallelism
- ○ pipelining
- ○ make the common case fast
- ◉ reliability via redundancy

Question 16 — 5 pts

Select the correct answer:

- ○ Main memory access time is faster than register access time
- ◉ To maximize performance, we want to minimize response time or execution time for some tasks.
- ○ There is no difference between the User CPU time and the System CPU time
- ○ CPI means one instruction per clock cycle

Question 17 — 5 pts

Do you know there is a part B (short question) part for this exam?

- (●) True
- ( ) False

Question 18 — 5 pts

Which statement is true?

- ( ) Quantum Computing follows the Von Neuman model
- (●) In Von Neuman model, there's a single path, either physically or logically, between the main memory system and the control unit of the CPU, forcing alternation of instruction and execution cycles. This single path is often referred to as the von Neumann bottleneck
- ( ) Neural Networks follows the Von Neuman model
- ( ) Reconfigurable Computing (FPGA) follows the Von Neuman model

Question 19 — 5 pts

Which statement is correct?

- ( ) The Control Unit and Main Memory chip are part of the Central Processing Unit (CPU).
- (●) The performance of a machine is directly affected by the design of the datapath and the control unit.
- ( ) The input/Output systems and the Control Unit are part of the Central Processing Unit (CPU).

- The Hard Disk and Datpath are part of the Central Processing Unit.

Question 20 — 5 pts

Which statement is true?

- Data Path is a network of hard disks and input/output devices connected by buses (capable of moving data from place to place) where the timing is controlled by clocks.
- Data Path is a network of hard disks and arithmetic and logic units (for performing various operations on data) connected by buses (capable of moving data from place to place) where the timing is controlled by clocks.
- **(selected)** Data Path is a network of storage units (registers) and arithmetic and logic units (for performing various operations on data) connected by buses (capable of moving data from place to place) where the timing is controlled by clocks.
- Data Path is a network of hard disks and multiple processors connected by buses (capable of moving data from place to place) where the timing is controlled by clocks.

Question 21 — 5 pts

Which statement is correct?

- Registers are used in computer systems as places to store a wide variety of data, such as addresses, program counters, and data necessary for program execution. Put simply, a register is a hardware device that stores binary data. Registers are located on the main memory chip so information can be accessed very quickly.
- **(selected)** Registers are used in computer systems as places to store a wide variety of data, such as addresses, program counters, and data necessary for program execution. Put simply, a register is a hardware device that stores binary data. Registers are located on the processor so information can be accessed very quickly.
- Registers are used in computer systems as places to store a wide variety of data, such as addresses, program counters, and data necessary for program execution. Put simply, a register is a hardware device that stores binary data. Registers are

located on the hard disks so information can be accessed very quickly.

- Registers are used in computer systems as places to store a wide variety of data, such as addresses, program counters, and data necessary for program execution. Put simply, a register is a hardware device that stores binary data. Registers are located on the input/output systems and buses so information can be accessed very quickly.

Question 22 — 5 pts

Which statement is correct?

- The processor and memory system determines the choice of high-level programming language
- The processor and memory system determines both the number of source-level statements and the number of I/O operations executed
- The processor and memory system determines the number of hard disks in the system.
- **The processor and memory system determines how fast instructions can be executed**

Question 23 — 5 pts

Which statement is correct?

- If the data your program needs are stored in main memory, then they can be accessed in 0 cycles during the execution of the instruction. If stored in a cache, 4 to 75 cycles. If stored in registers, hundreds of cycles. And if stored in disk, tens of millions of cycles
- If the data your program needs are stored in main memory, then they can be accessed in 0 cycles during the execution of the instruction. If stored in a single cache, 4 to 75 cycles. If stored in registers, hundreds of cycles. And if stored in multilevel cache, tens of millions of cycles
- If the data your program needs are stored in the main memory, then they can be

accessed in 0 cycles during the execution of the instruction. If stored in a disk, 4 to 75 cycles. If stored in registers, hundreds of cycles. And if stored in cache, tens of millions of cycles

- (●) If the data your program needs are stored in a CPU register, then they can be accessed in 0 cycles during the execution of the instruction. If stored in a cache, 4 to 75 cycles. If stored in the main memory, hundreds of cycles. And if stored on disk, tens of millions of cycles

Question 24 — 5 pts

Which statement is correct?

- ( ) The main memory chip is a non-volatile memory.
- ( ) ROM, PROM are volatile memory
- (●) SRAM and DRAM are volatile memory
- ( ) SRAM and DRAM are non-volatile memory

Question 25 — 5 pts

Which statement is correct?

- (●) A key feature of pipelining is that it increases the throughput of the system, but it may also slightly increase the latency
- ( ) A key feature of pipelining is that it increases the latency of the system, but it may also slightly increase the throughput
- ( ) The cache memory is built with DRAM cells
- ( ) The hard disk is made with SRAM cells

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