Project 2 - Assignment 1

Digital VLSI Design

Generation of PVT Varied Dataset on a 45nm-HP Node

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1 Introduction

The advancement of semiconductor technology has led to the increasing complexity of integrated circuits (ICs), resulting in higher performance and lower power consumption. However, with shrinking process nodes, the impact of variations in Process, Voltage, and Temperature (PVT) becomes more significant, affecting circuit performance and power consumption. To address this challenge, accurate modeling and prediction of circuit behavior under varying PVT conditions are essential.

The first part of the project focuses on generating datasets for regression-based machine learning models to predict the static leakage power and propagation delay of standard cells on a 45nm High-Performance (HP) node. By simulating circuits under different PVT conditions and sampling from predefined distributions, we aim to create comprehensive datasets that capture the variability inherent in modern semiconductor manufacturing processes.

2 Objectives

1. Develop spice netlists for NOR2, NAND2, and NOT standard gates.
2. Generate PVT distributions within specified bounds for process parameters, voltage, and temperature.
3. Implement a sampling methodology to generate diverse PVT combinations for each standard cell.
4. Configure NGSPICE for circuit simulation using constructed spice netlists and sampled PVT values.
5. Simulate circuits for each PVT combination and record static leakage power and propagation delay measurements.
6. Organize simulated data into structured datasets, including input combinations, corresponding PVT values, and measured leakage power and delay.

3 Methodology

The methodology for generating the PVT varied datasets on a 45nm-HP node comprises the following steps:

1. **Spice Netlist Construction:**
    - Spice netlists for NOR2, NAND2, and NOT standard gates were constructed based on the provided circuit schematics.
    - The netlists are stored in the "netlists" folder, with gate delay and leakage netlists named as <gate name>_delay/leakage.net.

- **NOR2 Netlist:** The spice netlist for the NOR2 gate is constructed by specifying the necessary components and their connections. The netlist typically includes transistor models, voltage sources, and ground connections. This netlist defines the behavior of the NOR2 gate during simulation.
- **NAND2 Netlist:** Similarly, the spice netlist for the NAND2 gate is constructed following the same principles as the NOR2 gate. The components and connections are adjusted to represent the NAND2 gate circuit.
- **NOT Netlist:** The spice netlist for the NOT gate is also constructed in a similar manner, representing the behavior of the NOT gate circuit during simulation.

2. **PVT Distribution Generation:**

   - PVT distributions were generated within predetermined bounds for critical process parameters, voltage, and temperature.
   - Monte Carlo distribution principles were applied to ensure realistic variations reflecting semiconductor manufacturing variability.

   Temperature Parameters:

   ```
   temp_min = -55
   temp_max = 125
   ```

   Voltage Parameters:

   ```
   nominal_voltage = 1.0
   voltage_variation = 0.1
   ```

   Process Parameters:

   ```
   toxe_n = 9e-010
   toxm_n = 9e-010
   toxref_n = 9e-010
   xj_n = 1.4e-008
   ndep_n = 6.5e+018

   toxe_p = 9.2e-010
   toxm_p = 9.2e-010
   toxref_p = 9.2e-010
   xj_p = 1.4e-008
   ndep_p = 2.8e+018

   toxp_par = 6.5e-010
   ```

Delay Parameters:

```
cqload_min = 0.01e-15
cqload_max = 5e-15
```

3. **Sampling Methodology:**
   - A systematic sampling methodology was implemented to generate diverse PVT combinations for each standard cell.
   - PVT values were sampled from the generated distributions, ensuring adequate coverage of the parameter space.
4. **Simulation Setup:**
   - NGSPICE was configured to simulate circuits using the constructed spice netlists and sampled PVT values.
   - Each simulation run considered a specific PVT combination, facilitating the characterization of circuit behavior under varied conditions.
5. **Circuit Simulation and Data Collection:**
   - Circuits were simulated for each PVT combination, and static leakage power and propagation delay measurements were recorded.
   - DC analysis was performed for leakage power estimation, while transient analysis with PWL signals was utilized for delay estimation.
6. **Dataset Generation Script:**
   - The final script for each gate to generate the dataset includes functions for running NGSPICE simulations for leakage and delay.
   - For each gate, the script constructs a spice netlist based on the provided circuit schematics and PVT parameters.
   - The script then runs NGSPICE simulations using the constructed netlists and sampled PVT values, collecting leakage and delay measurements for each PVT combination.
   - The results are stored in a DataFrame and saved to a CSV file for further analysis.

4 Conclusion

We have successfully generated PVT-varied datasets for circuit simulations on a 45nm-HP node. By meticulously constructing spice netlists, generating realistic PVT distributions, and simulating circuits under diverse conditions, we created comprehensive datasets for machine learning model training.