VLSI Design-Course Project

Tips and Trick

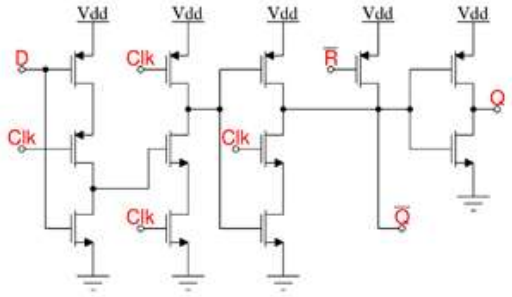
As you guys have completed the pre-requisite for the project, now it's time to step into doing the actual project. The assignment you have done **covers 50% of the work** for the project in terms of complexity, and now you only have to compile all those blocks to make the complete circuit implementation. In this document, we will try to compile all the possible queries you might have and give some tips on how to approach the project.

- Since you guys are new to designing circuits, we won't expect a completely optimized, perfect performance and design with minimal delay. We highly expect you to take a **logical and engineered approach** rather than throwing everything at the sink and hoping that it works. Using the engineered approach, even if the circuits does not work you can still use proper logical reasoning to debug the error and correct those mistakes, whereas if you are going to do without any systematic approach, it will be very tough to track down the error and correct it.
- The first step is to decide which architecture you are using, there are many different designs for CLA which you can refer to online resources. Once you fixate on your design, you need to make the Pre-layout netlist and check its functioning. Since you guys have already created logic gates in assignment 3, you can directly use them as sub-circuits in your netlist. You can give pulses for all the 4-bit inputs and check if you get the correct output for the corresponding inputs. Without completing the Pre-layout, it will not be possible to go further in this project; therefore, make sure your pre-layout netlist is completely working.
- After completing the pre-layout, you must start making the layout in Magic layout tool. This is the toughest step; therefore, you need to put a lot of care and attention while you are making the layout. One wrong step in between and you must do everything all over again. I guess by now you realize the price you must pay once you make mistakes in the layout. Follow the below steps and you can minimize the possibilities of making those mistakes

- Before attempting to make the layout in MAGIC directly, I recommend using a large sized sheet, different coloured pens (your wish) and try to draw the layout of your circuit (stick diagrams) in paper by following the appropriate DRC rules properly (keep DRC rules near-by when you are making the layout).
- Annotate the measurements properly so that you can realize the size of the circuit. This step is primarily important in routing, as there you will face a lot of challenges to connect intermediate nodes. Try to find as efficient routing methods as possible so that your circuit can be as compact as it can be.
- Instead of doing the whole circuit in one layout, I strongly recommend you all to divide the whole circuit into different blocks and design them individually first and then compile them. If you try to make the whole circuit in one single layout file, it will be tough to track the error as you will not be able to identify where exactly the error occurs. Individual blocks are easier to debug for errors than debugging the whole circuit. Use of the Getcell command will be constructive here.
- Use different layers of metal wherever needed. Whenever you get stuck to finding the shortest routing path, using other metals might do the job for you. At the same time, make sure you do the routing as smartly as possible.
- Give Proper labelling to each identified node in your circuit. This will allow you to track down your circuit when you are extracting netlist from the layout.
- Use the gates that you have made for Assignment-3. Using them as block will ease your job.
- Keep saving your layout file frequently while you are making the layout.

- Once you have completed the layout, extract the netlist, and do post layout simulation for the whole circuit. Even if you get errors in the post layout, do not panic. This is where the modular approach is extremely useful. Once you know your individual modules are working properly, the only mistake which is possible in the final layout is the connections in your intermediate blocks, so make sure you have made all the right connections. Keep verifying your post layout netlist repeatedly as this is where we make a lot of silly errors.

- Once you are done with the above parts, if you have time, you can try the bonus part which is not a huge leap in terms of the effort required. You are required to make D-Flip flop and place it for getting the input bits as well as giving the output bits. Below you can find a sample D-flip flop circuit



- To verify the functionality, you can use the below pulse command to get all input combination possible.

```
*****Inputs*****
*A3-A0
va0 a0 GND pulse(0 'supply' 0 0 0 'ckpd' '2*ckpd')
va1 a1 GND pulse(0 'supply' 0 0 0 '2*ckpd' '4*ckpd')
va2 a2 GND pulse(0 'supply' 0 0 0 '4*ckpd' '8*ckpd')
va3 a3 GND pulse(0 'supply' 0 0 0 '8*ckpd' '16*ckpd')

*B3-B0
vb0 b0 GND pulse(0 'supply' 0 0 0 '16*ckpd' '32*ckpd')
vb1 b1 GND pulse(0 'supply' 0 0 0 '32*ckpd' '64*ckpd')
vb2 b2 GND pulse(0 'supply' 0 0 0 '64*ckpd' '128*ckpd')
vb3 b3 GND pulse(0 'supply' 0 0 0 '128*ckpd' '256*ckpd')
```

- After Completing the SPICE part, you can start the HDL part which is easiest component in the circuit. Keep in mind that you have to make structural design not the behavioural model. You can use OYOSYS tool or Xilinx tool to get the circuit that you have implemented.
- Once you are done with the technical task, start writing the report using Word or latex. We will be posting the checklist soon of what all components required in the report.

If you are following these steps mentioned you will save a lot of time and unnecessary effort. Start working as soon as possible as it will be exceedingly difficult to pull everything at the end. The task you are required to do requires bit of calm and patient mind which is very tough to maintain as the deadline approaches. **ALL THE BEST!!**