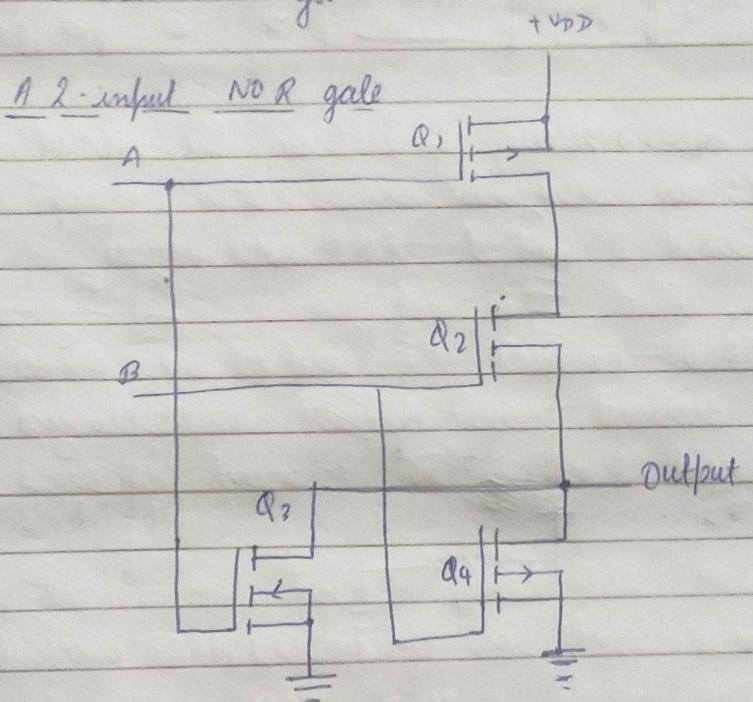


Q. Explain Relation of its input tree

Ans:

- 1) (a) Draw and explain briefly about CMOS NOR gate and TTL NAND gate?

Ans: CMOS NOR gate



~~Ans~~

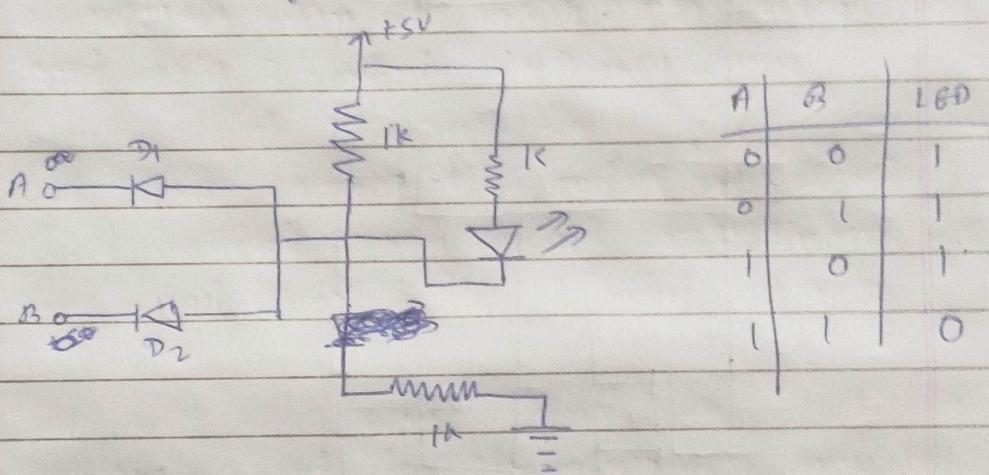
The NMOS transistors are in parallel to pull the output low when either input is high. The PMOS transistors are in series to pull the output high when both inputs are low, as given in the below table. The output is never left floating.

b)

The truth table of the NOR logic gate given in the below table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

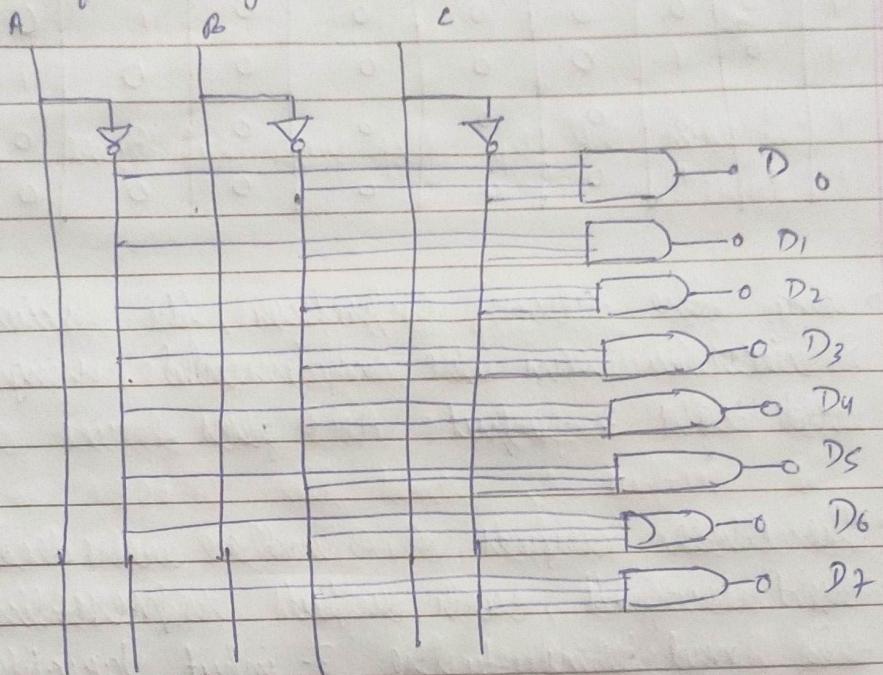
→ DTL NAND gate.



The DTL NAND gate combine the DTL inverter with a simple diode register logic (DRL) AND gate as shown in its circuit diagram. Thus, any number of inputs can be added simply by adding input diodes to the circuit. The problem of signal degradation caused by diode logic is overcome by the transistor, which amplifies the signal while inverting it. This means DTL gates can be cascaded to any required extent, without losing the digital signal.

b) Explain 3x8 decoder with figure and truth table

→ A 3 to 8 decoder has three inputs (A, B, C) and eight outputs (D_0 to D_7). Based on the 3 inputs (A, B, C), one of the eight output is selected.



The truth table for 3 to 8 decoder:

From the truth table, it is seen that only one of eight outputs (D_0 to D_7) is selected based on three select inputs.

From the truth table, the logic expressions for outputs can be written as follows:

Truth table of 3 to 8 decoder.
Inputs	Outputs

$$\begin{aligned}
 D_0 &= \bar{A} \bar{B} \bar{C}, & D_1 &= \bar{A} \bar{B} C, & D_2 &= A \bar{B} \bar{C} \\
 D_3 &= \bar{A} B C, & D_4 &= A \bar{B} C, & D_5 &= A B \bar{C} \\
 D_6 &= A B C, & D_7 &= A B C
 \end{aligned}$$

A	B	C	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

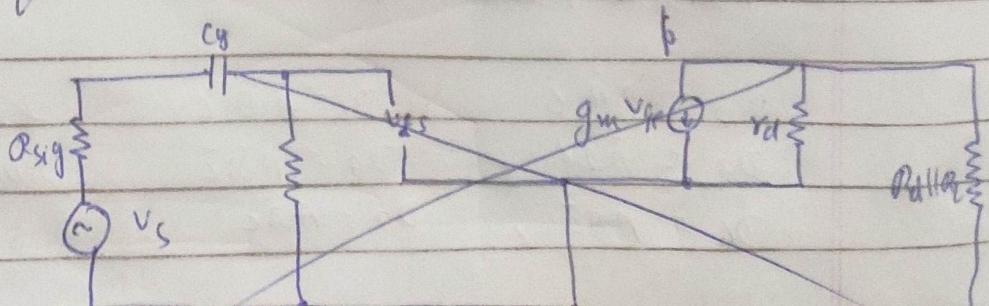
→ Using the above expression, the circuit of a 3 to 8 decoder can be implemented using three NOT and eight 3-input AND gates.

→ The three inputs A, B and C are decoded into eight outputs, each output representing one of the minterms of the 3-input variables.

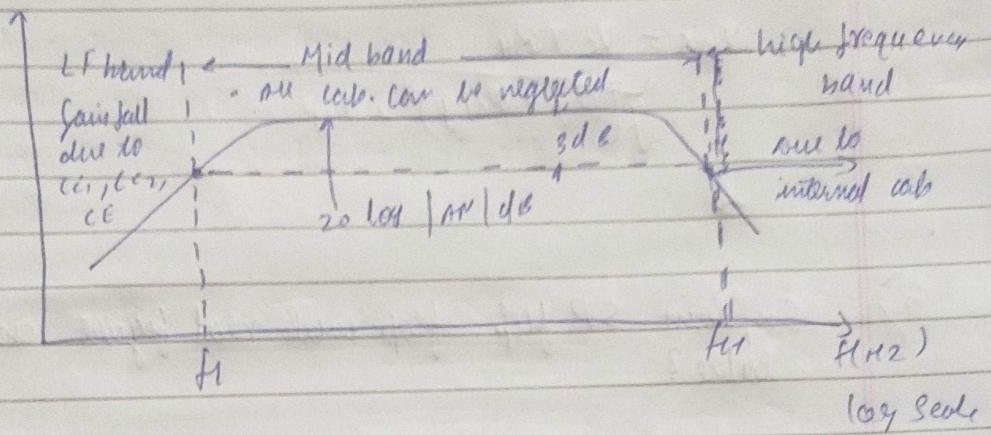
3) (a) Explain about low frequency CS amplifier?

The voltage gain of the amplifier decreases at low frequency. The decrease in gain is due to corner capacitance i.e. $c_g, c_c = c_s$.

Let us consider effect of c_g with $c_c = c_s = \infty$, hence an equivalent circuit,



frequency response :-



- ① Gain falls at lower frequency because -

coupling and bypass cap no longer have low impedance.

$$as \rightarrow f \downarrow \rightarrow \frac{1}{\omega c} \uparrow \rightarrow \text{overall gain } \downarrow$$

\rightarrow These capacitance will set the lower end of the midband - i.e. f1

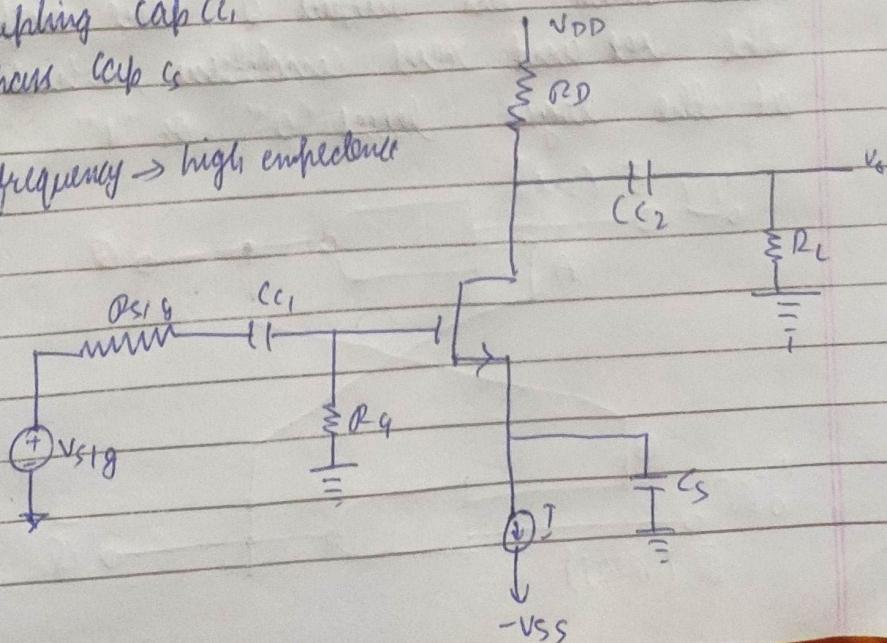
~~f1~~

low frequency response of CS amplifier

\rightarrow coupling cap C_1

\rightarrow bypass cap C_2

low frequency \rightarrow high impedance



V_{GS} - At low frequency X_{CG} is very large

$$V_{GS} = V_C \times R_g$$

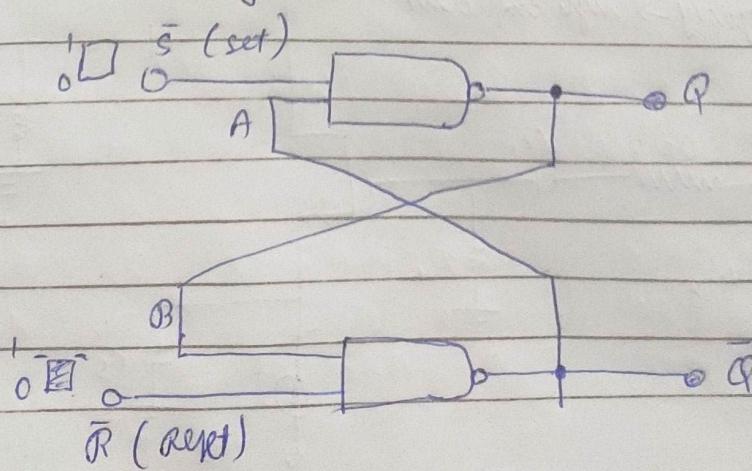
$$\sqrt{(R_g + R_{CIG})^2 + X_{CG}}$$

A

b) Explain SR flip flop with neat figure and truth table?

Ans:- The SR flip flop is a 1-bit memory bistable device having two inputs i.e., SET and RESET. The SET input 'S' set the device or produce the output 1, and the RESET input 'R' reset the device or produce the output 0. The set and reset inputs are labeled as S and R, respectively.

The SR flip flop stand for "Set-Reset" flip flop. The reset input is used to get back the flip-flop to its original state from the current state with an output 'Q'. The output depends on the set and reset conditions, which is either at the logic level "0" or "1".



Truth Table:-

state	S	R	Q	Q'	description
set	1	0	0	1	Set $Q' >> 1$
	1	1	0	1	Not change
reset	0	1	1	0	Reset $Q' >> 0$
	1	1	1	0	Not change
Inverted	0	0	1	1	Inverted condition

From the above truth table, we can see that when set 'S' and reset 'R' inputs are set to 1, the outputs Q and Q' will be either 1 or 0. These outputs depend on the input state S or R before the input condition exist. So, when the inputs are 1, the states of the outputs remain unchanged.