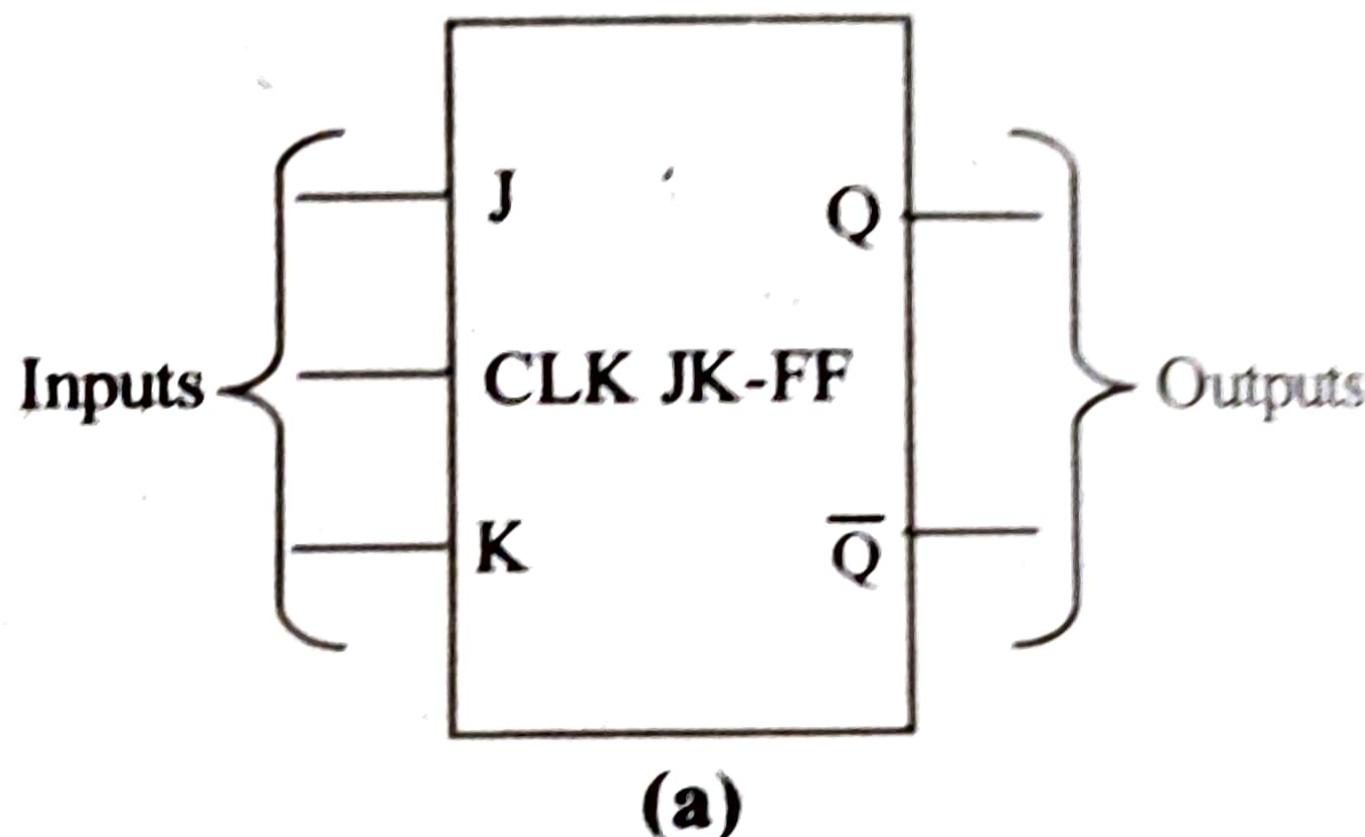


Q25. Explain the operation of JK flip-flop with diagram.

Ans:

Model Paper 1

The logic symbol and circuit diagram of JK-flip-flop as shown in figure (1).



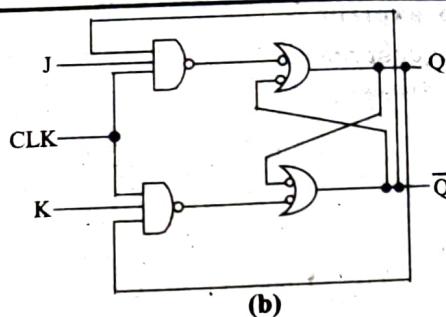


Figure (1)

Where, J, K – Data inputs

CLK – Clock input

Q – Normal output

\bar{Q} – Complementary output.

The truth table of JK-flip flop is as shown in table (1).

Operating modes	Inputs			Output	
	CLK	J	K	Q	Effect on output Q
Hold		0	0	No change	No change/disable
Reset		0	1	0	Reset (i.e., cleared to 0)
Set		1	0	1	Set to 1
Toggle		1	1	Toggle	Changes to opposite state (i.e., from 0 to 1 (or) 1 to 0)

Table (1)

Working: The operation of JK-flip-flop is described as follows,

Case (i)

If both the inputs of JK-flip-flop are '0' (i.e., $J = K = 0$), then the flip-flop enters into hold mode. In this mode, output remains same as that of the previous state (i.e., no change in the output).

Case (ii)

If $J = 0, K = 1$, then the flip flop enters into reset mode. In reset mode, the data inputs reset the output ' Q '. Thus, the outputs are $Q = 0, \bar{Q} = 1$.

Case (iii)

If $J = 1, K = 0$, then the flip flop enters into set mode. In this mode, the data inputs set the output ' Q '. Thus, the outputs are $Q = 1, \bar{Q} = 0$.

Case (iv)

If both the inputs of JK -flip flop are '1' (i.e., $J = K = 1$), then the flip-flop enters into toggle mode, in which output continuously shifts between logic '0' and logic '1' for complete clock pulse. Thus, uncertain output is obtained.

Timing Diagram: The timing diagram of JK-flip-flop is as shown in figure (2).

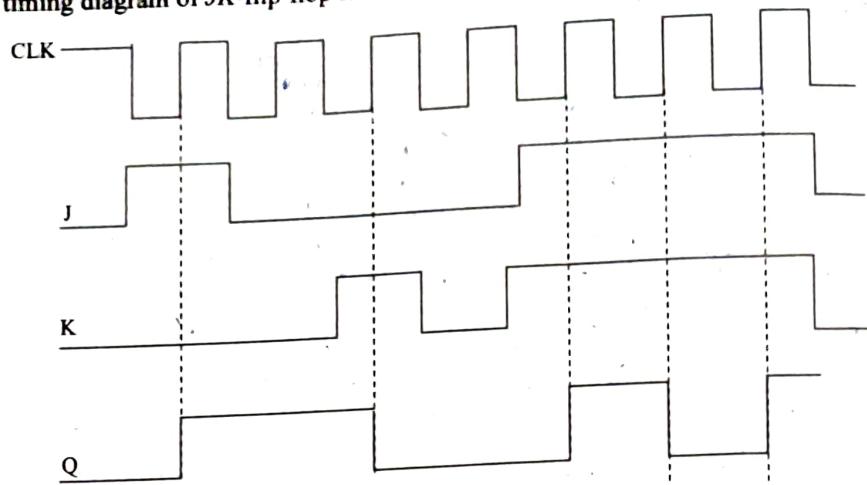


Figure (2): Timing Diagram

Q26. Explain T flip-flop along with its truth table.

Ans:

T-Flip-flop or Toggle Flip-flop can be obtained from JK flip-flop, if both J and K inputs are combined together. The diagram of T flip-flop is as shown in figure (1).

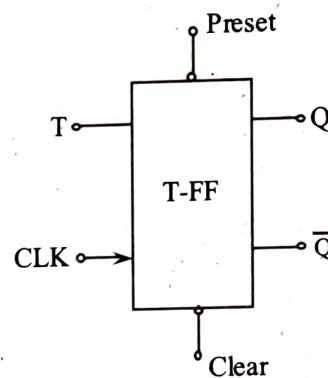


Figure (1)

The circuit diagram of T-flip-flop is as shown in figure (2).

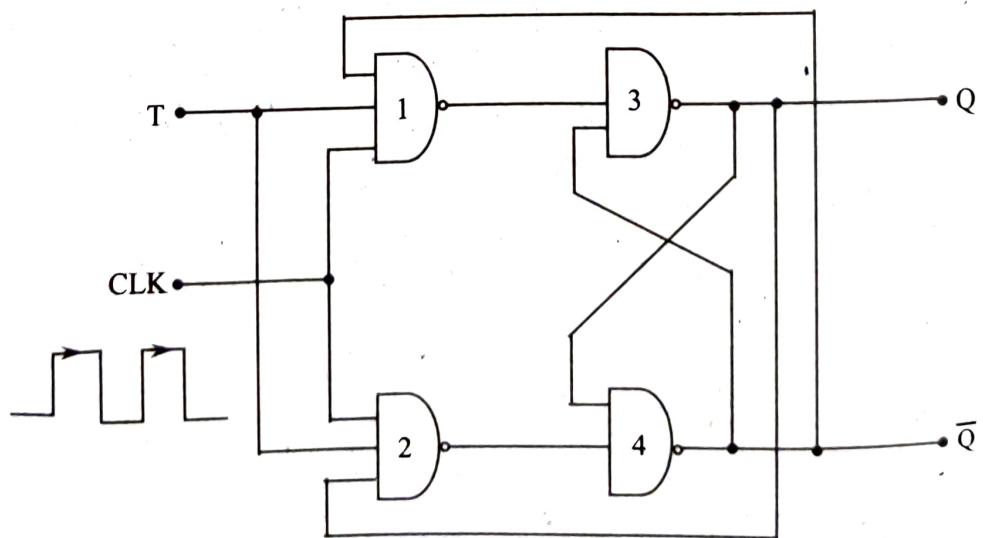


Figure (2): Circuit Diagram

UNIT-5 (Sequential Logic Circuits)

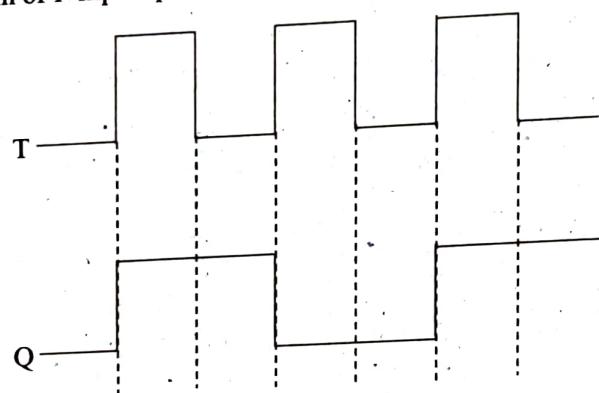
The truth table of T-flip-flop is as shown in table.

Clock	Input (T)	Output (Q)
0	1	No change
0	0	
1	0	Q_n
1	1	\bar{Q}_n

Table

From the above truth table, it is clear that T-flip-flop produces toggled output, when T input and clock signal are high. i.e., if CLK = 1, input (T) = 1, output = \bar{Q}_n . In other case i.e., when T-input is low, there is no change in the output, it maintains the previous state.

Timing Diagram: The timing diagram of T-flip-flop is as shown in figure (3).

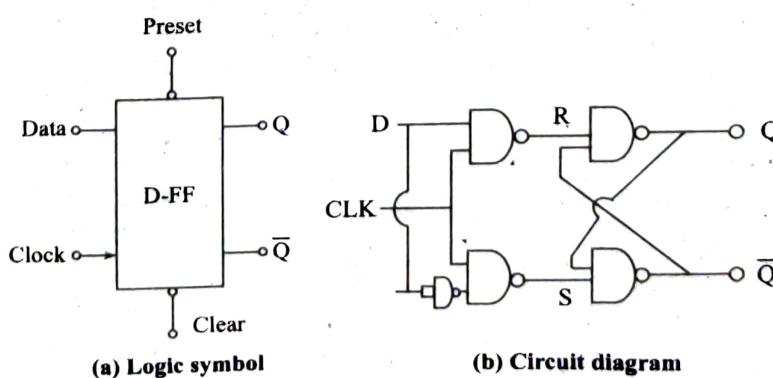
**Figure (3): Timing Diagram****Application**

T-flip-flop is particularly used to construct up-down counters.

Q27. Explain the operation of D-flip flop with the help of truth table.

Ans:

D-flip-flop (or) delay flip-flop is the modified form of SR (or) JK-flip-flop. It has single input (i.e., D) and two outputs (i.e., Q and \bar{Q}). The logic and circuit diagrams of D-flip-flop is as shown in figure (1).

**Figure (1)**

UNIT-5 (Sequential Logic Circuits)

Here, J, K - Data inputs

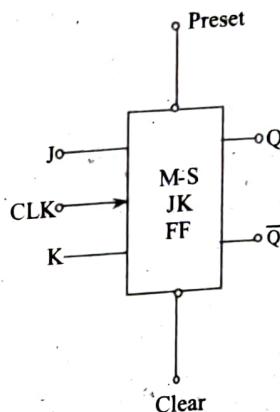
CLK - Clock inputs

 \overline{CLK} - Inverter clock input

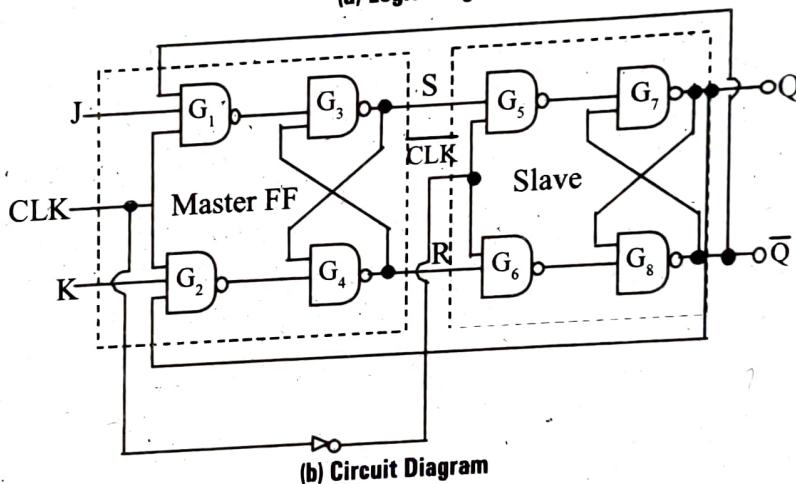
Q - Output

 \overline{Q} - Complementary output.

The logic and circuit diagrams of master slave JK-flip-flop is as shown in figure (2).



(a) Logic Diagram



(b) Circuit Diagram

Figure (2)

The truth table of master slave JK-flip-flop is shown in table.

PR	CLR	CLK	J	K	Q
0	0	x	x	x	x
0	1	x	x	x	1
1	0	x	x	x	0
1	1	x	0	0	NC
1	1		0	1	Reset
1	1		1	0	Set
1	1		1	1	Toggle

Table

The truth table of D -flip-flop is shown in table.

Input		Output	Operation
CLK	D	Q_n	
0	0	Q_{n-1}	No change
0	1	Q_{n-1}	
1	0	0	Data Storage
1	1	1	

Table

Operation: The output of the D -flip-flop depends on the clock signal applied at its input.

Case (i)

When clock signal is low (i.e., clock = 0), there is no change in the output.

Case (ii)

If clock signal is high (i.e., clock = 1), data storage takes place.

For $D = 0$; Reset = High, $Q = 0$

For $D = 1$; Set = High, $Q = 1$

This indicates that the input data appears at the output after some delay i.e., at the end of the clock pulse. Thus, it is referred to as delay flip-flop.

Timing Diagram: The timing diagram of D -flip-flop is as shown in figure (2).

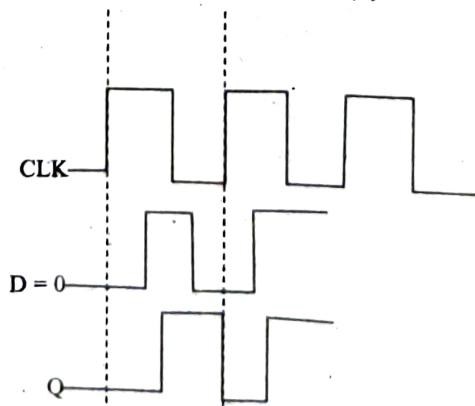


Figure (2): Timing Diagram

Applications

1. It is used as a delay device
2. It is also used as a latch to store 1-bit of binary information.

Q29. Discuss in detail about the pulse triggered S-R flip-flop. Also draw the output waveform of this flip flop and explain it with an example.

Ans:

Model Paper-II, Q11

A master slave (or) a pulse triggered SR-flip-flop is a combination of two SR-flip-flops, with feedback connection from output to input. The first flip-flop is referred as master and second flip-flop is referred as slave. The logic diagram of master-slave SR-flip-flop is as shown in figure (1).

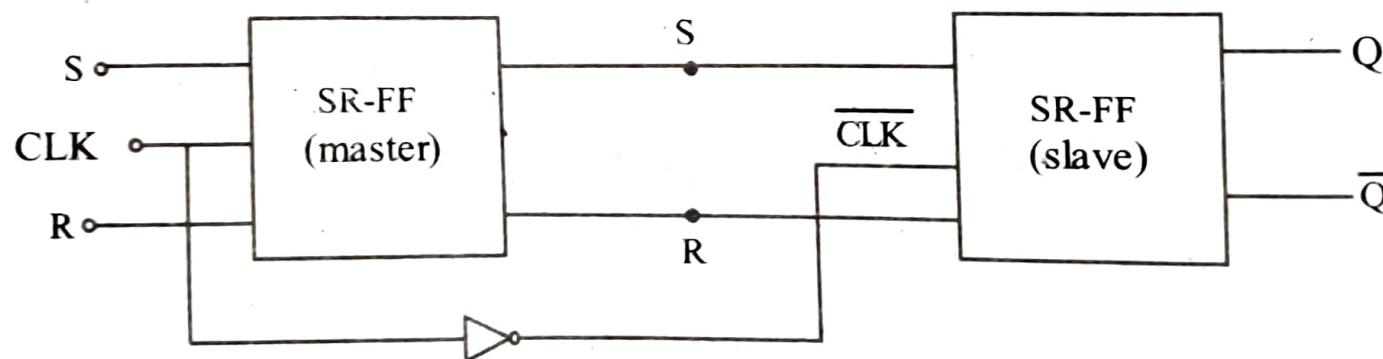


Figure (1)

Here, S , R – Data inputs

CLK – Clock inputs

\overline{CLK} – Inverter clock input

Q – Output

\overline{Q} – Complementary output.

The logic diagram of master slave SR-flip-flop is as shown in figure (2).

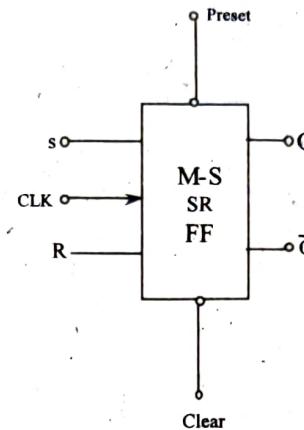


Figure (2)

Design and Operation of Master-slave RS Flip-flop: A master-slave RS flip-flop consists of,

1. A master RS flip-flop
2. A slave RS flip-flop
3. An inverter.

Figure (3) illustrates the circuit diagram of a RS master slave flip-flop.

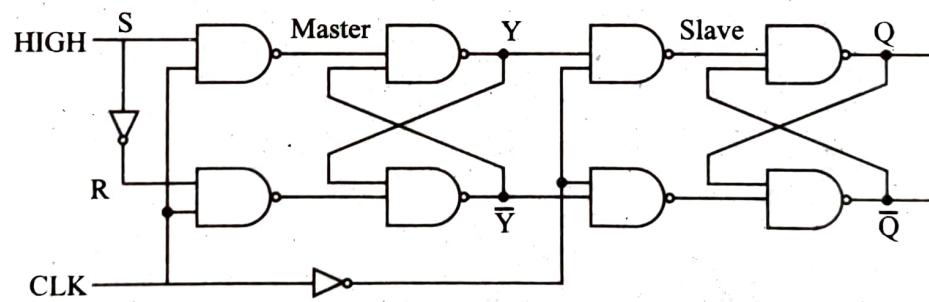


Figure (3)

The slave flip-flop is enabled when the clock pulse 'CLK' is 0 (i.e., when the output of the inverter is 1, it serves as a clock input to the slave flip-flop).

Thus, $Q = Y$ and $\overline{Q} = \overline{Y}$.

When the clock pulse 'CLK' becomes 1, the master flip-flop becomes enabled and the information is passed from the external R and S to the master flip-flop. The slave flip-flop is disabled as long as the clock pulse 'CLK' is 1. As the 'CLK' becomes 0, the master flip-flop gets disabled.

The operation of the master-slave flip-flop can be demonstrated by a truth table as shown below.

R	S	Clk	Q	Comments
0	1	0	0	Clear state
0	1	1	1	Set state

Table

The operation of master slave SR flip-flop is described as follows,

Case (i)

When $R = 0$, $S = 1$ and $CLK = 0$, the master flip flop enters into clear state and produces output $y = 0$ and $\bar{y} = 1$. These outputs are fed to the slave flip-flop when clock signal goes low. The S and R inputs force slave flip-flop to reset and produce outputs $Q = 0$; $\bar{Q} = 1$.

Case (ii)

When $R = 0$, $S = 1$ and $CLK = 1$, the master flip-flop enters into set state and produces output $y = 1$ and $\bar{y} = 0$. But the output remains constant and when the clock signal goes low, slave flip-flop becomes active and set the output to $Q = 1$; $\bar{Q} = 0$.

The timing diagram of master slave SR flip flop is as shown in figure (4).

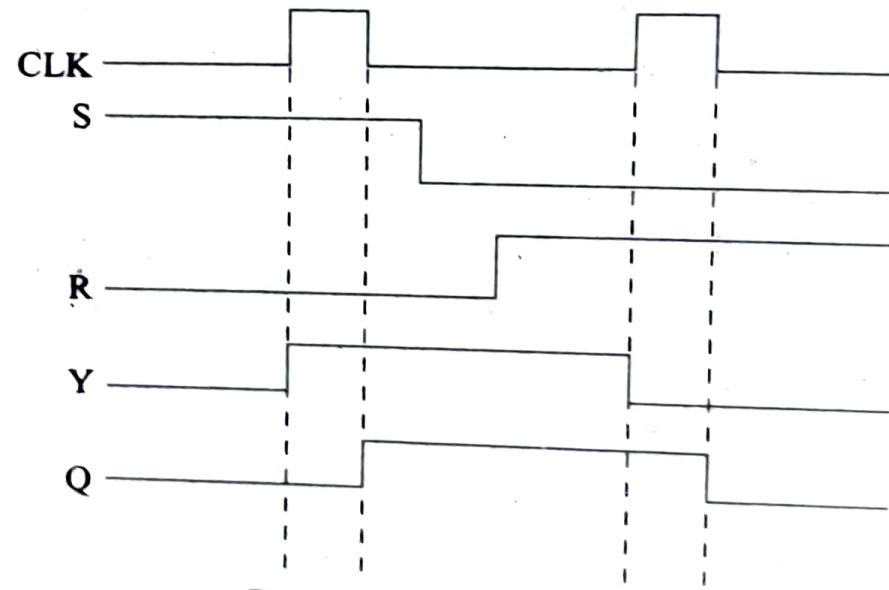


Figure (4) Timing diagram

5.1 SEQUENTIAL CIRCUITS, STORAGE ELEMENTS: LATCHES AND FLIPFLOPS

Q19. What is a sequential circuit? Explain its types.

Ans: A logic circuit whose output at any instant of time not only depends on current input, but also on past output is known as a sequential circuit. This include memory elements and combinational circuits.

Depending on the timing of signals, sequential circuits are classified as two types. They are.

1. Synchronous sequential circuit
2. Asynchronous sequential circuit.

1. Synchronous Sequential Circuit

A circuit is said to be synchronous circuit if its output depends on the input signals only at discrete interval of time i.e., memory device undergoes a change only at a discrete time interval. These circuits use flip-flops as their memory device for storing the binary information. A timing element known as clock generator is needed for synchronization and provides a periodic pulse train signals.

Figure (1) represents the circuit diagram of a synchronous sequential circuit.

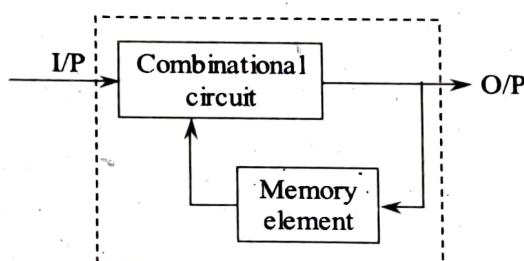


Figure (1): Block Diagram of Synchronous Sequential Circuit

It can be observed from figure (1) that the output can be obtained from combinational circuit or flip flop or both.

As the output is only obtained at discrete instant of time with the input, the state of flip-flop i.e., the memory device changes at active state of clock pulses and remains unaffected when the clock pulse is not active.

Synchronous sequential circuits are also called clocked-sequential circuits. If more than one flip-flop is used, then they have a common clock pulse. These circuits are simple to design and have limited speed of operation due to time delay.

2. Asynchronous Sequential Circuit

A circuit is said to be asynchronous sequential circuit if its output depends on the input signals at all instants of time i.e., the output changes accordingly with the input. Such circuits uses time delay latches, gate devices as their memory element.

Asynchronous sequential circuits does not require clock pulses and are called as combinational circuit with feedback.

At the time of unclock, the change in input is simultaneous for clocked sequential circuits as shown in figure (2).

These circuits are more difficult to design and the speed of operation is high.

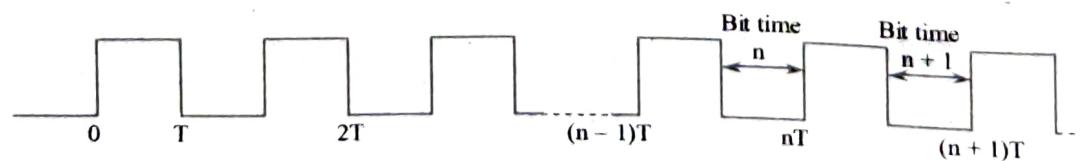


Figure (2): Timing Diagram of Clock Pulse

Q2. Distinguish between combinational logic and sequential logic circuits.

Ans:

Model Paper-I, Q1(i)

The comparison between sequential and combinational circuits is mentioned below.

Combinational Logic Circuits		Sequential Logic Circuits	
1.	Output depends only on the present input.	1.	Output depends on the present input and past output also.
2.	Easier to design.	2.	Comparatively harder to design.
3.	Speed of operation is high.	3.	Speed of operation is comparatively low.
4.	Memory unit is not required.	4.	Memory unit is required to store the past outputs.
5.	Example: Parallel adder.	5.	Example: Serial adder.

Q3. Compare synchronous and asynchronous sequential circuits.

Ans:

The comparison between synchronous and asynchronous sequential circuits is mentioned below:

Comparison of RAM, ROM, PROM, EPROM

Memory Type	Writable	Erasable Length	Speed	Relative Size	Performance	Cost Per Byte
RAM	Possible to write any number of times	Complete data can be erased	Fast to read and write	Small	Volatile	Costly
ROM	Not possible	—	Fast to read	Large	Permanent	Moderate
PROM	Possible to write but only once	—	Fast to read	Large	Permanent	Moderate
EPROM	Possible to write any number of times	Complete data can be erased	Fast to read and write	Very Large	Persistent	Moderate

Q30. Write the characteristic and excitation tables for JK, RS, T and D flip-flops.

Ans:

JK-Flip Flop: The block diagram of a JK flip-flop is as shown in figure (1).

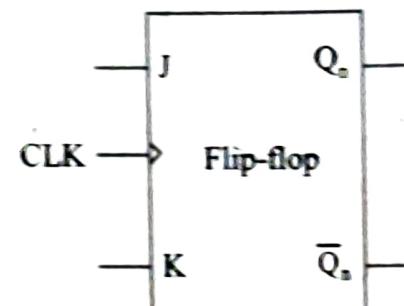


Figure (1)

The characteristic table of a JK flip-flop is given as shown in table (1).

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

Table (1): Characteristic Table

The excitation table of a JK flip-flop is given as shown in table (2).

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Table (2): Excitation Table of JK Flip-flop

UNIT-5 (Sequential Logic Circuits)

From the table (2), characteristic equation can be obtained using k-map as,

JK	00	01	11	10
Q _n	0		(1)	(1)
	1	1		1

$\therefore Q_{n+1} = JQ_n + \bar{K}Q_n$

RS-Flip-flop or SR- Flip-flop: The block diagram of RS flip-flop is as shown in figure (2).

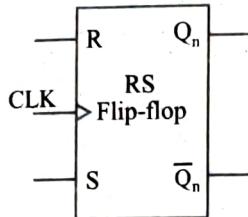


Figure (2): RS Flip-flop

The characteristic table of RS flip-flop is shown in table (3).

S	R	Q _{n+1}
0	0	Q _n
0	1	0
1	0	1
1	1	?

Table (3): Characteristic Table

The excitation table for RS flip-flop is shown in table (4).

Q _n	Q _{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Where, x - don't care

Table (4): Excitation Table of RS Flip-flop

From the table (4), characteristic equation can be obtained by using K-map as,

SR	00	01	11	10
Q _n	0	0	x	1
	1	1	x	1

$$\therefore Q_{n+1} = S + \bar{R}Q_n$$

T-Flip-Flop: The block diagram of T-flip-flop is as shown in figure (3).

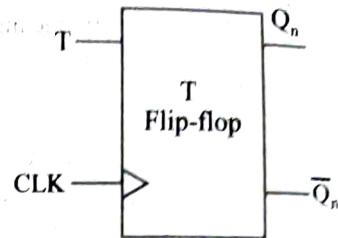


Figure (3)

The characteristic table of T flip-flop is shown in table (5).

T	Q _{n+1}
0	(Q _n)
1	(Q-bar_n)

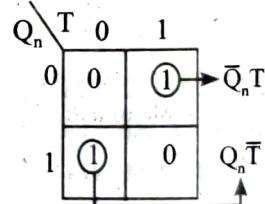
Table (5): Characteristic Table of T Flip-flop

The excitation table for T flip-flop is shown in table (6).

Q _n	Q _{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Table (6): Excitation Table of T Flip-flop

From the table (6), characteristic equation can be obtained by using K-map as,



From the K-map, characteristic equation is obtained as.

$$Q_{n+1} = T\bar{Q}_n + \bar{T}Q_n$$

D Flip-flop: The block diagram of D flip-flop is as shown in figure (4).

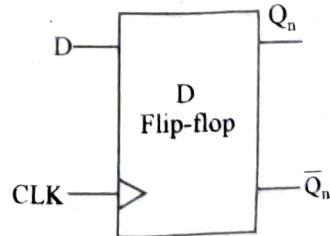


Figure (4): D Flip-flop

The characteristic table of D flip-flop is shown in table (7).

D	Q_{n+1}
0	0
1	1

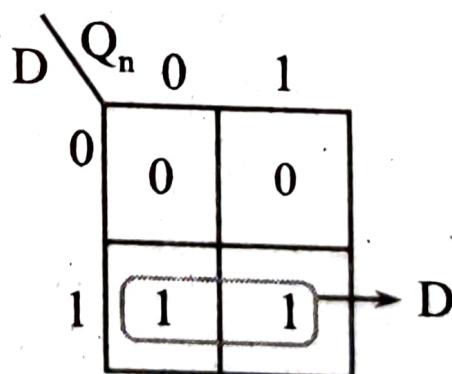
Table (7): Characteristic of D Flip-flop

The excitation table for D flip-flop is shown in table (8).

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Table (8): Excitation Table of D Flip-flop

From the table (8), characteristic equation can be obtained as,



Hence, the characteristic equation is,

$$Q_{n+1} = D$$

Q39. Draw the logic diagram of Mealy model and explain its operation.

Ans:

The logic diagram of a Mealy model is as shown in figure (1).

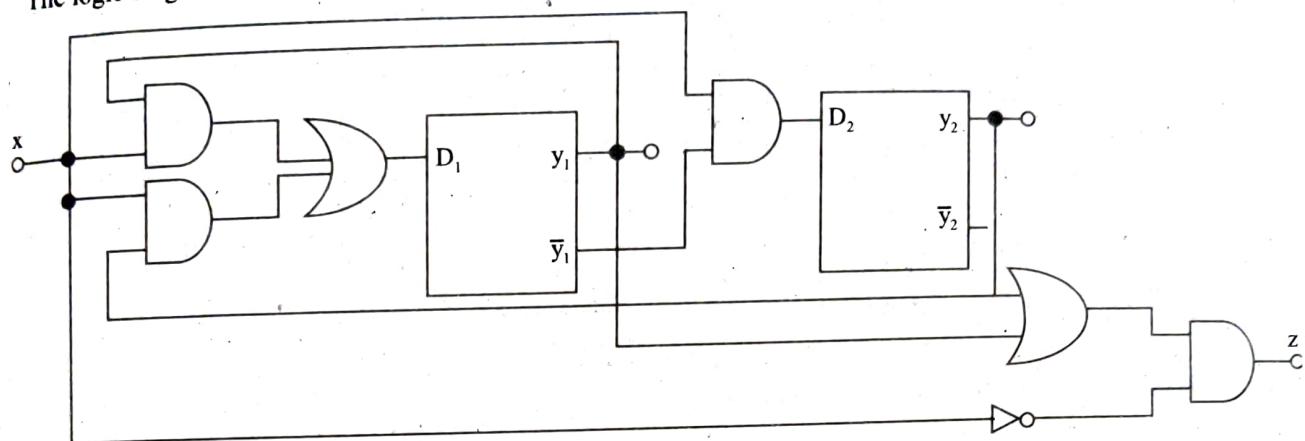


Figure (1): Logic Diagram of a Mealy Model

It consists of two D -flip-flops, an input (x) and an output (z).

During clock pulse, any variations in the input directly affect the output of the circuit. As a result, the input variations and output remains unsynchronized with the clock, thereby producing false outputs.

Generally, state equation helps in determining the behaviour of clocked sequential circuit. Here, input to ' D ' describes the value of next state.

The state equations for Mealy model can be obtained as,

$$y_1(t+1) = y_1(t)x(t) + y_2(t)x(t) \quad \dots (1)$$

$$y_2(t+1) = \bar{y}_1(t)x(t) \quad \dots (2)$$

The output equation (z) is,

$$z(t) = \{y_1(t) + y_2(t)\}\bar{x}(t) \quad \dots (3)$$

Where,

$x(t)$ – Present input

$z(t)$ – Present output.

$y(t+1)$ – Next state of the flip-flop.

Let,

$$Y_1(t) = y_1(t+1) \text{ and}$$

$$Y_2(t) = y_2(t+1)$$

Then equations (1), (2) and (3) can be written as,

$$Y_1 = y_1x + y_2x \quad \dots (4)$$

$$Y_2 = \bar{y}_1x \quad \dots (5)$$

$$z = (y_1 + y_2)\bar{x} \quad \dots (6)$$

The state table for Mealy model can be obtained using equations (4), (5) and (6) as shown in table.

PS		NS				output	
		x = 0		x = 1		x = 0	x = 1
y ₁	y ₂	Y ₁	Y ₂	Y ₁	Y ₂	z	z
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

Table: State Table

Its corresponding state diagram is shown in figure (2).

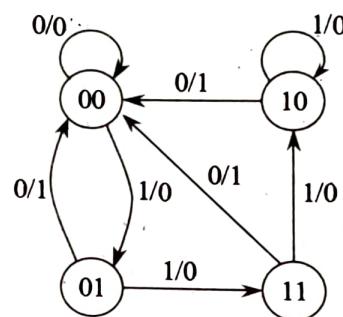


Figure (2): State Diagram

Q40. Draw and explain the logic diagram of Moore model.

Ans:

The logic diagram of Moore model is illustrated as shown in figure (1).

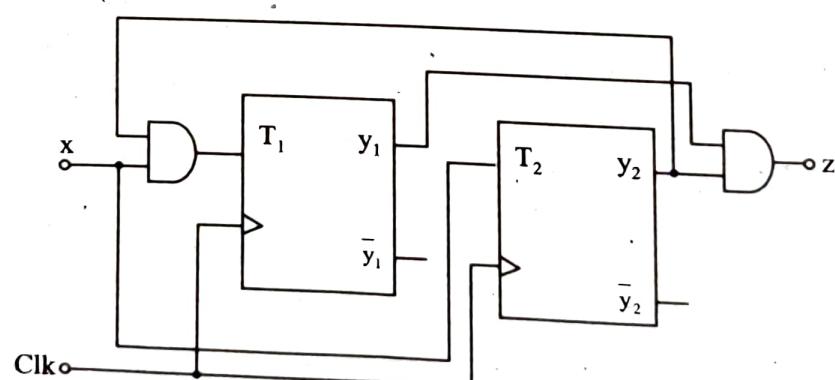


Figure (1): Logic Diagram of a Moore Model

It consists of two T flip-flops, an input (x) and an output (z).

In Moore model, the output depends only on the present state.

From figure (1), the input equations (T_1 and T_2) and output equation (z) are obtained as,

$$T_1 = y_2 x$$

$$T_2 = x$$

$$z = y_1 y_2$$

Generally, the characteristic equation of a T flip-flop can be written as,

$$Q(t+1) = T\bar{Q} + \bar{T}Q \quad \dots (1)$$

On substituting the corresponding values of T_1 and T_2 in equation (1), the state equations for Moore model are obtained as,

$$y_1(t+1) = Y_1 = (y_2x) \oplus y_1 = (\bar{y}_2x)y_1 + (y_2x)\bar{y}_1 = y_1\bar{y}_2 + y_1\bar{x} + \bar{y}_1y_2x. \quad \dots (2)$$

$$y_2(t+1) = Y_2 = x \oplus y_2 = x\bar{y}_2 + \bar{x}y_2 \quad \dots (3)$$

$$\text{Output } z = y_1y_2 \quad \dots (4)$$

The state table for Moore model can be obtained using equations (2), (3) and (4) as shown in table.

NS						
PS		$x = 0$		$x = 1$		O/P
y_1	y_2	Y_1	Y_2	Y_1	Y_2	z
0	0	0	0	0	1	0
0	1	0	1	1	0	0
1	0	1	0	1	1	0
1	1	1	1	0	0	1

Table: State Table

The corresponding state diagram is shown in figure (2).

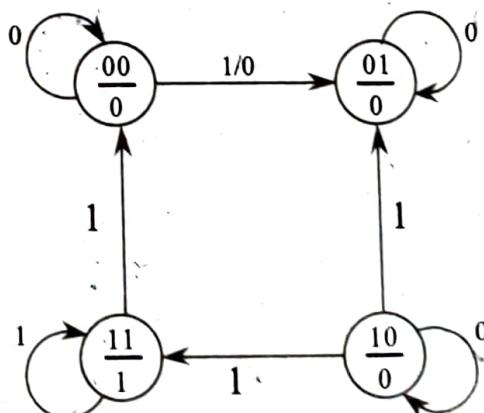


Figure (2): State Diagram

Q48. Design a ripple counter considering one example.

Ans:

Ripple Counter

Ripple counter is an asynchronous counter in which the clocks of all flip-flops are not connected.

Example

BCD Counter

BCD counter is also known as mod-10 counter or decade counter. BCD counter counts binary coded decimal from 0000 to 1001. When the 11th clock pulse is applied, the next state of register becomes 0000 due to external logic gate. Since BCD doesn't have a regular pattern, it becomes all the more important to go through the sequential circuit design procedure to derive a BCD synchronous counter circuit.

The state diagram of a BCD-ripple counter is as shown in figure (1).

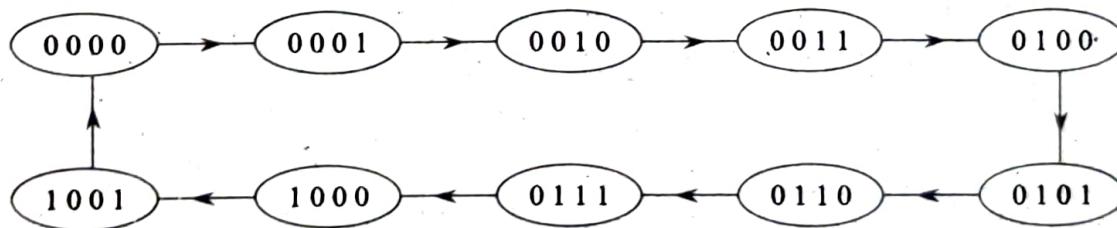


Figure (1): State Diagram

A D-flip-flop is used. The truth table of D-FF is shown in table (1).

Count pulse	D	Q
0	x	x
1	0	0
1	1	1

Table (1)

From this, the function table of the ripple counter is written as shown in table (2).

Count Pulse	Present state				Next state				Output				y
	A	B	C	D	A	B	C	D	D_A	D_B	D_C	D_D	
0	0	0	0	0	0	0	0	1	0	0	0	1	0
1	0	0	0	1	0	0	1	0	0	0	1	0	0
2	0	0	1	0	0	0	1	1	0	0	1	1	0
3	0	0	1	1	0	1	0	0	0	1	0	0	0
4	0	1	0	0	0	1	0	1	0	1	0	1	0
5	0	1	0	1	0	1	1	0	0	1	1	0	0
6	0	1	1	0	0	1	1	1	0	1	1	1	0
7	0	1	1	1	1	0	0	0	1	0	0	0	0
8	1	0	0	0	1	0	0	1	0	0	0	1	0
9	1	0	0	1	0	0	0	0	0	0	0	0	1

Table (2): State Transition Table

The expressions for D_A , D_B , D_C , D_D can be obtained by using the K-map simplification technique as,

For D_A

		CD	00	01	11	10
		AB	00	01	11	10
00	00	0	0	0	0	0
00	01	0	0	1	0	0
01	11	x	x	x	x	x
01	10	0	0	x	x	x

$$\therefore D_A = BCD$$

For D_B

		CD	00	01	11	10
		AB	00	01	11	10
00	00			1		
00	01	1	1			1
01	11	x	x	x	x	x
01	10			x	x	x

$$\therefore D_B = \overline{C}B + \overline{B}\overline{D} = B(\overline{C} + \overline{D})$$

For D_C

		CD	00	01	11	10
		AB	00	01	11	10
00	00	0	1	0	1	0
00	01	0	1	0	1	0
01	11	x	x	x	x	x
01	10	0	0	x	x	x

$$\therefore D_C = \overline{C}\overline{D} + \overline{A}\overline{C}\overline{D}$$

For D_D

CD \ AB	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	x	x	x	x
10	1	0	x	x

$$\therefore D_D = \bar{D}$$

(4)

The implementation of BCD ripple counter using above expressions requires four D -flip-flop as shown in figure (2).

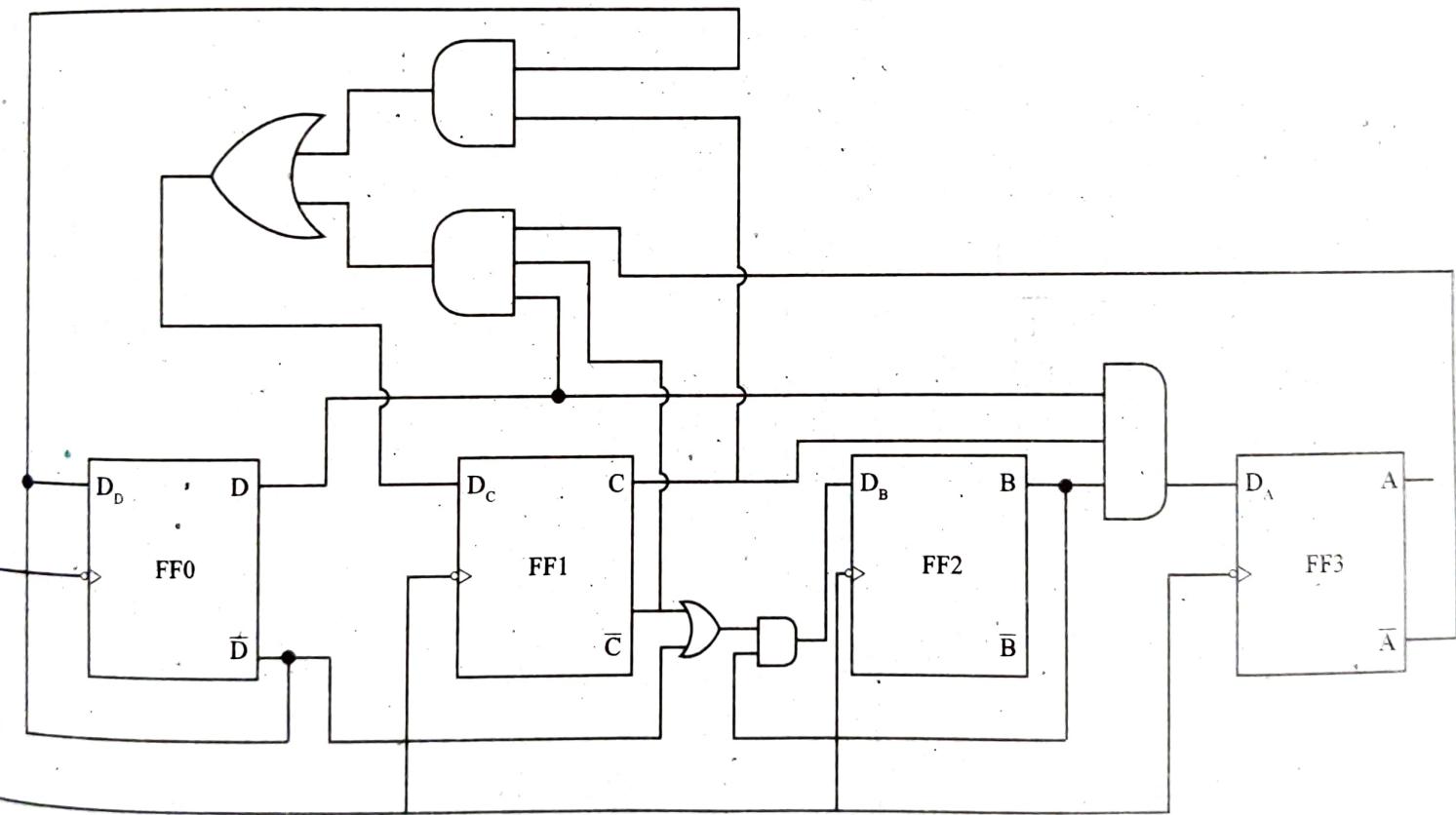


Figure (2): BCD Counter