ESSAY QUESTIONS WITH KEY

UNIT - I

Q1. Explain the components of the computer system. **(Refer Unit-I, Q15)**

Q2. Give the block diagram for registers and explain. Also, discuss about memory transfer operations. **(Refer Unit-I, Q18)**

Q3. Tabulate various symbols used for register transfers. With the help of an example, how register transfer is implemented. **(Refer Unit-I, Q19)**

Q4. What is a logic microoperation? Discuss in detail various types of logic microoperations. Also give the hardware implementation of logic microoperations. **(Refer Unit-I, Q25)**

Q5. Discuss in detail various types of shift microoperations. **(Refer Unit-I, Q27)**

Q6. With the help of a diagram explain one stage of arithmetic logic shift unit. **(Refer Unit-I, Q29)**

Q7. Draw and explain about the instruction cycle state diagram. **(Refer Unit-I, Q35)**

Q8. Explain briefly about input-output configuration. **(Refer Unit-I, Q39)**

UNIT - II

Q1. Explain about the microprogrammed control organization. **(Refer Unit-II, Q13)**

Q2. Diagrammatically explain the process of selection of address for control memory. **(Refer Unit-II, Q15)**

Q3. Describe how mapping from instruction code to microinstruction is done. Also, explain about subroutines. **(Refer Unit-II, Q16)**

Q4. With the help of a block diagram explain the computer configuration. **(Refer Unit-II, Q17)**

Q5. Discuss in detail about all the microinstruction formats. Also explain various microinstruction fields. **(Refer Unit-II, Q18)**

Q6. Discuss the decoding of microoperation fields. **(Refer Unit-II, Q23)**

Q7. With the help of a diagram, explain the organization of microprogram sequencer for a control memory. **(Refer Unit-II, Q24)**

Q8. Describe briefly the general register organization. **(Refer Unit-II, Q25)**

Q9. Write short notes on instruction formats. **(Refer Unit-II, Q26)**

Q10. Illustrate the use of different addressing modes with numerical example. **(Refer Unit-II, Q31)**

Q11. Discuss in brief about program control instructions. **(Refer Unit-II, Q34)**

UNIT - III

Q1. Define each of the following number systems,

(i) Decimal (ii) Binary (iii) Octal (iv) Hexadecimal. **(Refer Unit-III, Q11)**

Q2. Convert $(19.625)_{10}$ into its binary, octal and hexadecimal equivalents. **(Refer Unit-III, Q15)**

Q3. What are the different types of complements? Explain. **(Refer Unit-III, Q19)**

Q4. Explain in detail about fixed-point representation. **(Refer Unit-III, Q22)**

Q5. What is meant by overflow? Also explain how it can be detected. **(Refer Unit-III, Q24)**

Q6. Explain in detail about floating-point representation. Support your answers with examples wherever necessary. **(Refer Unit-III, Q26)**

Q7. How computer arithmetic addition and subtraction can be performed using signed magnitude data? Also provide it's hardware implementation. **(Refer Unit-III, Q30)**

Q8. Draw a flowchart to explain how addition and subtraction of two fixed point numbers can be done. Also, draw a circuit using full adders for the same. **(Refer Unit-III, Q35)**

Q9. What is a Booth's algorithm for 2's complement multiplications? Explain with an example. **(Refer Unit-III, Q37)**

Q10. How is floating point multiplication done? **(Refer Unit-III, Q49)**

UNIT - IV

Q1. What is the need of I/O Interface? Explain. **(Refer Unit-IV, Q10)**

Q2. What are the three modes of data transfer? Explain each mode in detail along with its advantages, disadvantages. **(Refer Unit-IV, Q19)**

Q3. What is priority interrupt? Define polling mechanism. **(Refer Unit-IV, Q21)**

Q4. Describe the organization of DMA. **(Refer Unit-IV, Q28)**

Q5. Show the memory hierarchy and give the brief explanation. **(Refer Unit-IV, Q31)**

Q6. Discuss in detail the two most common auxiliary memory devices used in computer systems. **(Refer Unit-IV, Q36)**

Q7. What do you mean by associative memory? Give the hardware organization of associative memory. **(Refer Unit-IV, Q38)**

Q8. What are the different mapping techniques of cache memory? Describe each technique with suitable diagram. **(Refer Unit-IV, Q43)**

Q9. Describe briefly the following terms,
(i) Cache hits (ii) Cache miss (iii) Hit ratio
(iv) Average memory access time. **(Refer Unit-IV, Q45)**

UNIT - V

Q1. Differentiate between RISC and CISC characteristics. **(Refer Unit-V, Q12)**

Q2. Discuss about Flynn's classification of parallel processor systems. **(Refer Unit-V, Q14)**

Q3. What is pipelining? Explain pipeline processing with an example. **(Refer Unit-V, Q15)**

Q4. What is meant by instruction pipeline? Explain four segment instruction pipeline. **(Refer Unit-V, Q21)**

Q5. Explain three segment instruction pipeline. Show the timing diagram with data conflict. **(Refer Unit-V, Q23)**

Q6. Write short notes on vector processing. **(Refer Unit-V, Q25)**

Q7. Write short notes on superscalar processors. **(Refer Unit-V, Q28)**

Q8. Illustrate in detail various characteristics of multiprocessors. **(Refer Unit-V, Q30)**

Q9. Explain with the help of a neat sketch how a time shared bus interconnection system for multiple processors provides a common communication path connecting all of the functional units. **(Refer Unit-V, Q32)**

Q10. What is a system bus? What are the different signal lines associated with a system bus? Explain. **(Refer Unit-V, Q38)**

Q11. Discuss various dynamic arbitration techniques. **(Refer Unit-V, Q41)**

Q12. What is cache coherence problem? Discuss about different cache coherence approaches. **(Refer Unit-V, Q43)**

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B.Tech. II Year I Semester Examination

MODEL PAPER-I

MODEL PAPER 1

COMPUTER ORGANIZATION AND ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours | Max. Marks: 75

Note: This question paper contains two **Parts A** and **B**

Part A is compulsory which carries **25 marks.** Answer all questions in **Part A.**

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries **10 marks** and may have a, b, c as sub questions.

PART-A (25 Marks)

Solutions

1. (a) Write about memory read and memory write operations. (Unit-I / Q2)

   (b) Draw a diagram that shows the register transfer implementation along with the timing diagram. (Unit-I / Q7)

   (c) Write short notes on interrupt. (Unit-II / Q9)

   (d) Discuss about internal interrupts. (Unit-II / Q12)

   (e) What is the gray code equivalent of the Hex Number 3A7. (Unit-III / Q5)

   (f) Write short notes on overflows. (Unit-III / Q10)

   (g) What are the advantages and disadvantages of handshaking? (Unit-IV / Q1)

   (h) Compare between main memory and auxiliary memory. (Unit-IV / Q6)

   (i) Explain the factors affecting throughput in pipelined processors. (Unit-V / Q3)

   (j) Write in brief about RISC. (Unit-V / Q8)

PART-B (50 Marks)

2. (a) Explain the components of the computer system. (Unit-I / Q15)

   (b) Give the block diagram for registers and explain. Also, discuss about memory transfer operations. (Unit-I / Q18)

OR

3. Discuss in detail various types of shift microoperations. (Unit-I / Q27)

4. (a) Describe how mapping from instruction code to microinstruction is done. Also, explain about subroutines. (Unit-II / Q16)

   (b) Discuss the decoding of microoperation fields. (Unit-II / Q23)

OR

5. Discuss in detail about all the microinstruction formats. Also explain various microinstruction fields. (Unit-II / Q18)

6. (a) Convert $(19.625)_{10}$ into its binary, octal and hexadecimal equivalents. (Unit-III
(b) What are the different types of complements? Explain. (Unit-III

OR

7. (a) What is meant by overflow? Also explain how it can be detected. (Unit-III
(b) Draw a flowchart to explain how addition and subtraction of two fixed point numbers can be done. Also, draw a circuit using full adders for the same. (Unit-III

8. Describe the organization of DMA. (Unit-IV

OR

9. (a) What do you mean by associative memory? Give the hardware organization of associative memory.
(b) Describe briefly the following terms, (Unit-IV
(i) Cache hits
(ii) Cache miss
(iii) Hit ratio
(iv) Average memory access time.

10. (a) Discuss about Flynn's classification of parallel processor systems. (Unit-IV
(b) Explain three segment instruction pipeline. Show the timing diagram with data conflict. (Unit-V

OR

11. (a) Illustrate in detail various characteristics of multiprocessors. (Unit-V
(b) Explain with the help of a neat sketch how a time shared bus interconnection system for multiple processors provides a common communication path connecting all of the functional units. (Unit-V

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MODEL PAPER 2

B.Tech. II Year I Semester Examination

MODEL PAPER-II

COMPUTER ORGANIZATION AND ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours Max. Marks: 75

Note: This question paper contains two **Parts A** and **B**

Part A is compulsory which carries **25 marks**. Answer all questions in **Part A**.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries **10 marks** and may have a, b, c as sub questions.

PART-A (25 Marks)

Solutions

1. (a) Write substraction microoperation of 4-bit arithmetic circuit with the help of function table. (Unit-I / Q5)
   (b) Write about timing signal. (Unit-I / Q10)
   (c) Discuss in brief about microinstruction format. (Unit-II / Q2)
   (d) Distinguish between hardwired control unit and microprgrammed control unit. (Unit-II / Q6)
   (e) Write about decimal number system. (Unit-III / Q1)
   (f) Obtain divide operation on $\frac{110}{111}$. (Unit-III / Q8)
   (g) Give the disadvantages of programmed I/O. (Unit-IV / Q3)
   (h) What do you mean by associative memory? (Unit-IV / Q7)
   (i) What is vector processing? (Unit-V / Q4)
   (j) Write a short note on cache coherence. (Unit-V / Q9)

PART-B (50 Marks)

2. (a) With the help of a diagram explain one stage of arithmetic logic shift unit. (Unit-I / Q29)
   (b) Explain briefly about input-output configuration. (Unit-I / Q39)

OR

3. What is a logic microoperation? Discuss in detail various types of logic microoperations. Also give the hardware implementation of logic microoperations. (Unit-I / Q25)

4. (a) Write short notes on instruction formats. (Unit-II / Q26)
   (b) Illustrate the use of different addressing modes with numerical example. (Unit-II / Q31)

OR

5. (a) Describe briefly the general register organization. (Unit-II / Q25)
   (b) Discuss in brief about program control instructions. (Unit-II / Q34)

6. (a) Define each of the following number systems,

(i) Decimal

(ii) Binary

(iii) Octal

(iv) Hexadecimal. (Unit-

(b) How is floating point multiplication done? (Unit-

OR

7. How computer arithmetic addition and subtraction can be performed using signed magnitude data? Also provide it's hardware implementation. (Unit-II

8. What are the three modes of data transfer? Explain each mode in detail along with its advantages, disadvantages. (Unit-IV

OR

9. (a) What is priority interrupt? Define polling mechanism. (Unit-IV

(b) Discuss in detail the two most common auxiliary memory devices used in computer systems.

10. (a) Write short notes on vector processing. (Unit-IV /

(b) Discuss various dynamic arbitration techniques. (Unit-V /

OR (Unit-V /

11. (a) What is a system bus? What are the different signal lines associated with a system bus? Explain.

(b) What is cache coherence problem? Discuss about different cache coherence approaches. (Unit-V / 0

(Unit-V / 0

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MODEL PAPER 3

B.Tech. II Year I Semester Examination

MODEL PAPER-III

COMPUTER ORGANIZATION AND ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours

Max. Marks: 75

Note: This question paper contains two Parts A and B

Part A is compulsory which carries **25 marks**. Answer all questions in **Part A**.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries **10 marks** and may have a, b, c as sub questions.

PART-A (25 Marks)

Solutions

1. (a) Define digital computer. (Unit-I / Q1)
   (b) Discuss in brief about microinstruction. (Unit-I / Q6)
   (c) Describe stack organization. (Unit-II / Q5)
   (d) What are the three basic fields present in an instruction? (Unit-II / Q7)
   (e) What is 10's complement. (Unit-III / Q3)
   (f) Write short notes on underflows. (Unit-III / Q9)
   (g) Differentiate cycle stealing and burst transfers of DMA. (Unit-IV / Q4)
   (h) List the characteristics of memory devices. (Unit-IV / Q8)
   (i) How MIMD computer differs from SISD computer? (Unit-V / Q1)
   (j) Discuss in brief about snooping protocol. (Unit-V / Q10)

PART-B (50 Marks)

2. Tabulate various symbols used for register transfers. With the help of an example, how register transfer is implemented. (Unit-I / Q19)

OR

3. Draw and explain about the instruction cycle state diagram. (Unit-I / Q35)

4. (a) Explain about the microprogrammed control organization. (Unit-II / Q13)
   (b) Diagrammatically explain the process of selection of address for control memory. (Unit-II / Q15)

OR

5. (a) With the help of a block diagram explain the computer configuration. (Unit-II / Q17)
   (b) With the help of a diagram, explain the organization of microprogram sequencer for a control memory. (Unit-II / Q24)

6. (a) Explain in detail about fixed-point representation. (Unit-III / Q22)
   (b) Explain in detail about floating-point representation. Support your answers with examples wherever necessary. (Unit-III / Q26)

OR

7. What is a Booth's algorithm for 2's complement multiplications? Explain with an example. (Unit-III / Q3

8. (a) What is the need of I/O Interface? Explain. (Unit-IV / Q1

(b) Show the memory hierarchy and give the brief explanation. (Unit-IV / Q3

OR

9. What are the different mapping techniques of cache memory? Describe each technique with suitable diagram. (Unit-IV / Q4

10. (a) Differentiate between RISC and CISC characteristics. (Unit-V / Q1

(b) What is pipelining? Explain pipeline processing with an example. (Unit-V / Q1

OR

11. (a) What is meant by instruction pipeline? Explain four segment instruction pipeline. (Unit-V / Q2

(b) Write short notes on superscalar processors. (Unit-V / Q2