AN EFFICIENT AND LOW POWER 45NM CMOS BASED R-2R DAC

Dr. S.Rajendra Prasad[1]
Prof., Dept. of ECE
VNRVJIET
Hyderabad, India
Rajendraprasad_s@vnrvjiet.in

Namani kavya sree[2]
Dept. of ECE
VNRVJIET
Hyderabad, India
Namanikavya73@gmail.com

Kondra omkumar[3]
Dept. of ECE
VNRVJIET
Hyderabad, India
Kondraom17@gmail.com

Kothapalli srujana[4]
Dept. of ECE
VNRVJIET
Hyderabad, India
Srujanaone8@gmail.com

***Abstract*— The main purpose of the Digital to Analog converter (DAC) is to act as an interface between the digital device and the analog device. Which converts the binary digital values(0,1) into a series of analog voltages. Each type of DAC has its own set of advantages and disadvantages, It is not possible to attain all positive aspects in one circuit. By considering different parameters like power, resolution etc., we have designed a 4-bit CMOS based R-2R DAC in 45nm technology. In this paper, we are using two stage operational amplifier(opamp) in order to enhance the performance of the R-2R DAC. A differential amplifier stage and a gain stage form the two stage opamp, and two values of resistors R and 2R are invoked to form the R-2R ladder network. This two stage opamp and 4-bit R-2R ladder network are used together to design a 4-bit R-2R DAC. Then This DAC is simulated using the Synopsys H-spice tool and based on the simulation results, analysis is performed by considering various parameters like accuracy-Integral nonlinearity (INL) and Differential nonlinearity(DNL) errors, resolution, average, static, and dynamic powers, and settling time. The proposed R-2R DAC has low power and less INL, and DNL errors which are efficient when compared with the related work.**

***Keywords* – Digital to analog converter, 45nm CMOS technology, Opamp, R-2R ladder, INL and DNL.**

I. INTRODUCTION

Complementary Symmetrical Metal-Oxide Semiconductor is another name for CMOS (COS-MOS). The phrase "complementary symmetric" refers to a form of CMOS analytical design that employs complementary, metal oxide semiconductor field effect transistors (MOSFETs) in symmetrical pairs for logic functions. ADCs convert analog signals in the form of physical variables to digital values in any communication system. For further processing, this digital signal is transformed back into an analog signal. Analog signals, for example, are required to power motors, temperature controls, and other devices. In order to handle analog signals, a digital input signal must be converted into the analog voltage or current required by a digital-to-analog converter (DAC). A digital signal is represented by a binary code, which is an arrangement of bits 0 and 1. A converter from digital to analog (DAC) is used to convert pulse value to a sine wave. The DACs are used in transfiguring the digital data of video signals and audio signals into analog signals By and large, Nowadays these DACs are used on numerous gadgets. [1].

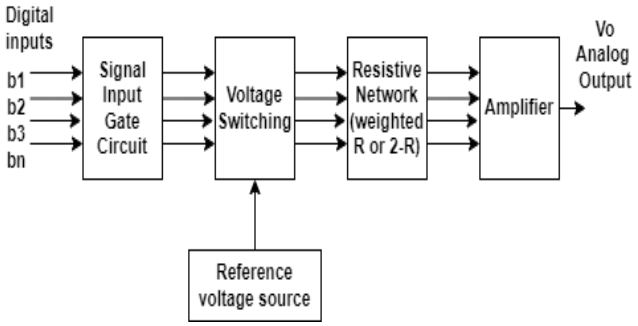

Fig. 1. A simple digital to analog converter

All but the most specialized DACs are built as IC's due to their complexity and requirement for perfectly matched components. They often take the form of mixed-signal IC chips made of metal oxide semiconductors (MOS) that merge analog and digital circuitry.

The R-2R DAC utilizes an R and 2R stepping stool network in a transformed viper circuit to give a simple result that approximates a computerized (two-fold) input. The R-2R DAC is named the way that it is comprised of exclusively R and 2R resistors. It likewise doesn't require the utilization of higher-worth resistors. At the point when the significant info bit is set to '0,' the computerized switches in the picture are connected to the ground. While the matching information bit is '1', the advanced switch in the outline above is connected to the negative reference voltage – V_R. The operation amp's transforming input wire is connected to the ground. As such, zero volts are applied to the opamp's non-reversing input terminal. It consists of an Operational Amplifier, here we are using a two-stage opamp schematic as a non-inverting summing amplifier which amplifies the sum of applied input voltages through a resistive network[1].

The R-2R DAC architecture's functionality can be implemented in a variety of ways, and it is easy to construct with a higher conversion rate. The simplicity of the architecture facilitates the design of higher DACs which is having high resolution for use in several applications where sensors or else control feedback systems are required. Moreover, R-2R DACs have less power consumption, making them perfect for low power applications. The design has a lower production cost since it only needs two resistor values instead of the three required by binary-weighted DACs. It is also possible to attain great linearity. The design's Opamp is essential for enhancing the DAC's performance.

A. OPAMP

DAC systems commonly use differential amplifiers or op amps. This not only amplifies the signal but also differentiates the signal and includes process signals such as signal and summation. The opamp is a multistage amplifier, Differential amplifier is the input stage of the opamp with two inputs and a balanced output. This stage generally sets the opamp's input resistance and provides a higher voltage gain for the amplifier. Another stage is driven by the output of the first stage of the opamp(ie., a differential amplifier) which is known as the middle stage. Mostly the middle stage of the opamp has dual input and unbalanced output also called single-ended output. The intermediate stage output DC voltage will also be greater than the ground potential as the direct coupling is used.

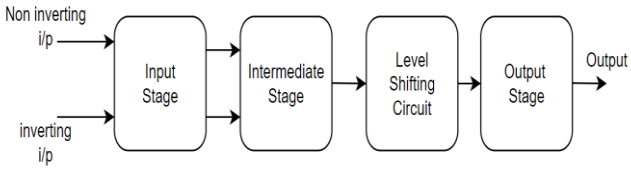

Fig. 2. Basic opamp structure

The DC Voltage level of the intermediate stage output is shifted to zero voltage with regard to the ground by using a level shifter circuit at the output of the intermediate stage. Always the output stage of a push-pull amplifier is used as the final stage in opamp. To increase the current capability of the opamp and also to increase the voltage swing of the output this final stage is used. The low output resistance is also provided by the proper output stage.

II. RELATED WORK

P. Whig et al., [3] Designed a 4-bit R-2R DAC in several topologies such as CMOS, opamp and Transmission gates(TG) in TANNER-EDA T-SPICE. In CMOS based R-2R DAC, CMOS inverters are used i.e., for one bit CMOS inverter is connected in cascade with the next CMOS inverter and it is connected with the R-2R ladder and then it outputs the same bit that was input. Then for all bits same process is repeated. After that this design is simulated and observed maximum and average power dissipation.

In the Transmission gate(TG) based R-2R DAC where a transmission gate acts as a switch that is formed by connecting PMOS and NMOS in parallel. The input signal is passed to the output by TG when S is high. For DAC all the bits are given with digital input then TG is connected to each of the inputs acts as a good switch and the digital pulse is converted to a corresponding analog signal.

In the opamp based R-2R DAC, using gates the data is converted to digital form which are on or off based on the value of input signal. Then the analog signal is obtained from this digital input by using the summing amplifier which is designed using opamp. Like this 4 bit DAC is designed using opamp then inputs are binary format, for zero it is grounded whereas for 1 TTL voltages are assigned. Then these three types of topologies R-2R DAC is simulated by using TANNER EDA tool and observed that Average power and maximum power are high for opamp based R-2R DAC when compared to CMOS and TG based DAC's.

III. DESIGN OF R-2R DAC

In the existing model, they are using a single-stage opamp with less gain so DAC is less accurate in terms of INL and DNL errors. And average power is also higher in this existing opamp based R-2R DAC. To overcome these disadvantages two-stage opamp is used. Where the differential amplifier is one stage of the opamp and the common source amplifier is known as the second stage.

A. DESIGN OF TWO STAGE OPAMP

A differential amplifier stage, a gain stage, and a bias stage are the three different sections of a two-stage operational amplifier. The first stage of the circuit, referred to as the differential stage, offers more gain, and the second stage, referred to as the gain stage, adds additional gain for achieving greater output swings. The differential amplifier stage of the opamp is constructed using the connections indicated in fig. 4 between the transistors M11, M12, M13, and M14. Differential input of the amplifier is provided through two NMOS transistors M_{11}, and M_{12} i.e., The Gate terminals of M_{12} and M_{11} transistors are applied with non-inverting and inverting inputs respectively. The main resistance which is contributing for the output is the input transistors M_{11}, M_{12} resistance and active load transistors M_{13}, and M_{14}.

These M_{11}, M_{12}, M_{13} and M_{14} forms the basic differential amplifier where as biasing is needed for perfect operation of this differential amplifier which can be achieved by using either a current source or else two transistors connected with a resistor R_b of 1k ohm which is given with a supply voltage of 3.5V in this design i.e., V_{DD} of the circuit. Then this M_{18}, M_{19}, and R_b forms the baising of the opamp.

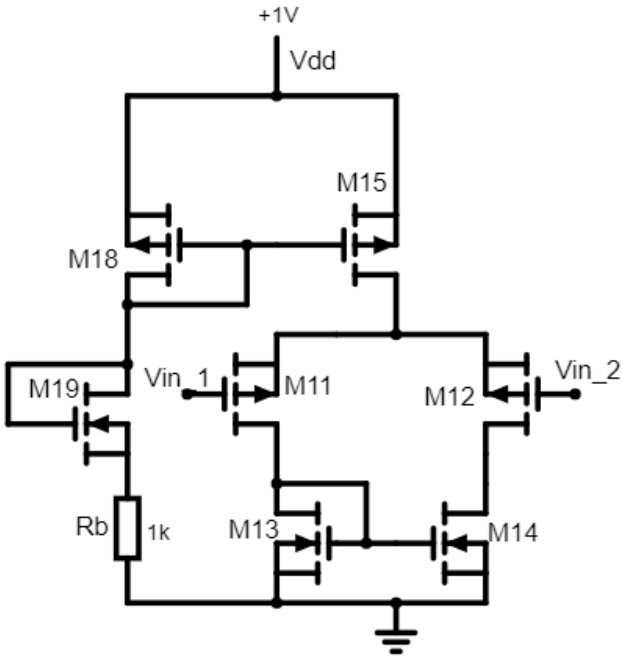

Fig. 3. Differential amplifier

The Current mirror helps in converting the input signal of dual input i.e., differential to a single output signal which is the main advantage of using the current mirror that is formed through connecting M_{13} and M_{14} (active load transistors), and common mode rejection is achieved by the load. M_{11} and M_{13} are current mirrors to each other, so M_{11} and M_{13} have equal currents and the current in M_{14} is subtracted from the current in the M_{12} transistor so that M_{12} and M_{14} transistors are also having equal currents. [4].

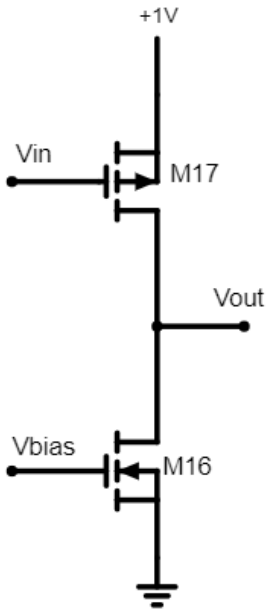

Fig. 4. Common source amplifier

The current sink load inverter is formed by the transistors M_{16} and M_{17}. Through the common source configuration output from the drain of a transistor, M_{12} is amplified by the transistor M_{16}. The four transistors also work to implement the opamp biasing. In order to sink a particular amount of current dependent on the gate to source voltage of transistors M15 and M18, a bias chain is employed. To reduce the frequency of the dominating pole and move the output pole of the amplifier away from the centre (i.e., origin) a compensation capacitor (CC) is used which is connected to the output of the differential stage. And at the output of the opamp, a load capacitor is connected. [4]. These two stages together form a two stage opamp as shown in fig. 6.

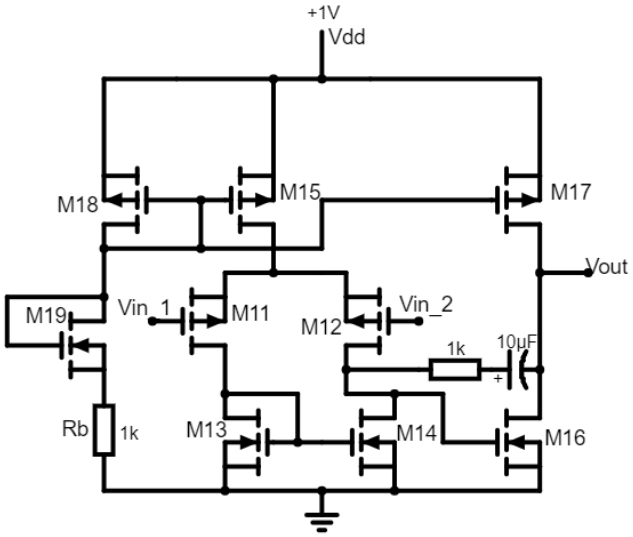

Fig. 5. Schematic view of two stage Opamp

Design Equations:

$$I_{ds} = \frac{\mu C_{ox} W}{2L(V_d - V_s)^2} \tag{4}$$

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{5}$$

$$Gain * Bandwidth = \frac{g_m}{2\pi f C l} \tag{6}$$

$$\frac{W}{L} = \frac{g_m^2}{2I_{ds}\mu C_{ox}} \tag{7}$$

$$I_{bias} = slewrate * C_C \tag{8}$$

Assuming slew rate=80V/microseconds, Coupling capacitance is 0.08pF. Then we get I_{bias}as 7μs, but we have to consider the higher value of I_{bias} as 15μs. And μC_{ox} is 20μ then as per the equation 4, we get $(W/L)_{15}$ is 50. And this bias current(I_{bias}) is divided in differential amplifier circuit, and as per current mirror technique both M_{13} and M_{11} are equal i.e., half of the bias current (7.5μs) and then W/L ratio of M_{13} and M_{14} are equal i.e., 16.6. Like this we have designed two-stage opamp by using these design equations, to achieve different specifications like gain, bandwidth, etc.,

TABLE I

Width to length ratios of opamp

W/L Ratios	Values
M_{11} , M_{12}	10
M_{13} , M_{14}	16.6
M_{15}	50
M_{16}	20
M_{17}	120
M_{18}	150
M_{19}	33.32

B. DESIGN OF CMOS R-2R DAC

For the 4-bit R-2R DAC which is shown in the below figure, there are 4 binary inputs B_0(LSB), B_1, B_2, and B_3(MSB). The binary inputs are realized by using the pulse inputs connecting in series with the resistors, for the least significant bit (B_0) the pulse values of 1V are given in the period of 32us and a pulse width of 16us. Similarly, for the next most significant bit (B_1) the pulse values of 1V with period and width of the pulse are double of the previous lower significant bit (B_0), and for the (MSB) most significant bit (B_3) the pulse values is 1V with the period 256us and pulse width 128u which is 2^3 times time period and pulse width of the least significant bit(LSB) i.e., B_0.

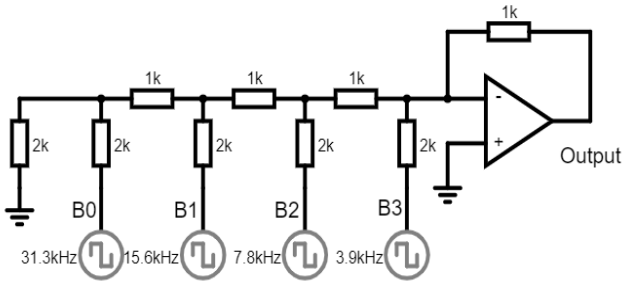

Fig. 6. Design of 4 bit R-2R DAC

In the R-2R DAC, R and 2R are the only two resistor values present. The 1K ohm resistor is taken as the feedback resistor, and the two resistor values considered in the circuit are 1k and 2k ohms. The resistor 2R (2k) is connected in series with all four binary input pulses (B0, B1, B2, and B_3) . The resistor values of R (1k) ohms are connected in between the networks of the two binary bit inputs resistors and one extra resistor of 2R(2k) is connected in series with the whole resister network and the ground.

C. Simulation Results of Opamp

By simulating two-stage opamp using H-spice, observed transient and ac analysis as shown in fig. 8 and 9 respectively. And we get a maximum gain of 42.9dB and a phase margin of 50.6 degrees.

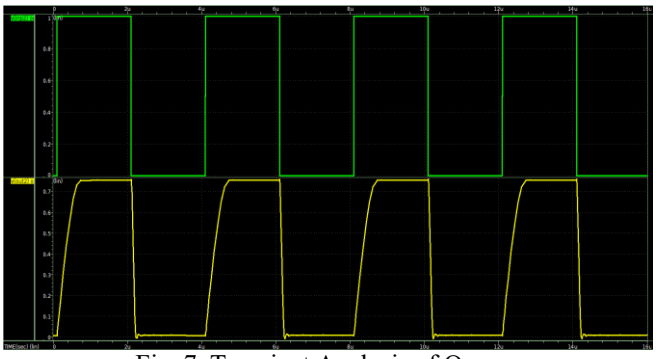

Fig. 7. Transient Analysis of Opamp

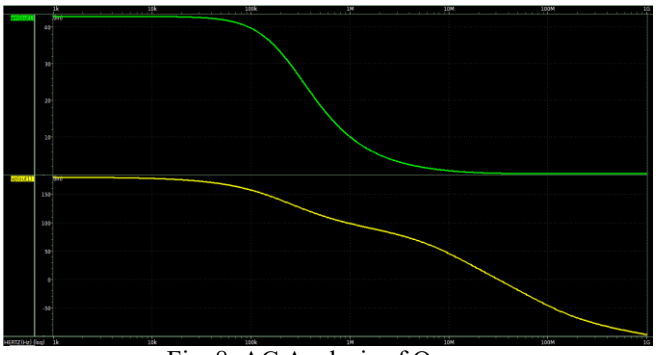

Fig. 8. AC Analysis of Opamp

D. Simulation Results of R-2R DAC

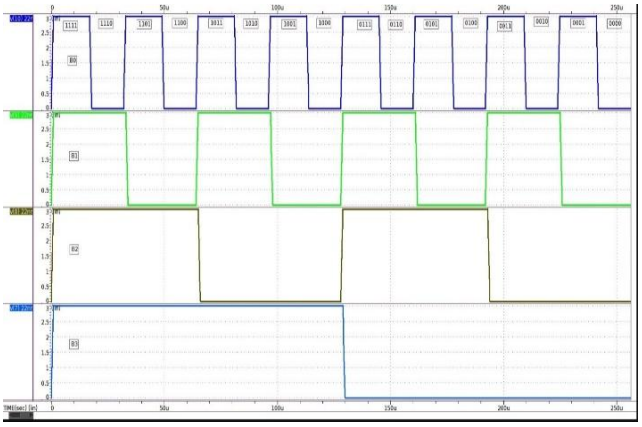

Fig. 9. Digital input

The digital input varying from 1111 to 0000 consisting of total 16 combinations is applied and observed transient analysis as shown in fig. 9.

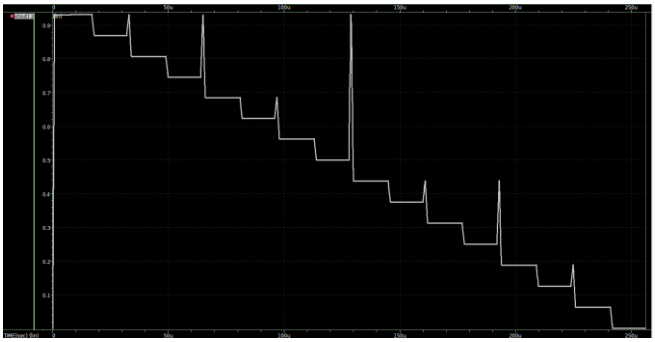

Fig. 10. Simulation output of 4-bit R-2R DAC

Analysis of R-2R DAC is done by implementing the design in H-spice by using 45nm CMOS technology by calculating different parameters like Average power, Static power, Dynamic power, Resolution and settling time, INL, and DNL errors.

TABLE II

Calculation of different parameters of proposed R-2R DAC

Parameters	**Proposed R-2R DAC**
Technology	45nm
Resolution	0.1853V
INL	-0.104 to +0.128
DNL	-0.312 to +0.323
Settling time	1.25us

Calculated INL and DNL errors by observing simulation results of 4-bit R-2R DAC as shown in fig.7, where INL errors are in a range between -0.104 to +0.128 and DNL errors are in a range between -0.312 to +0.323 as shown in table III. and concluded that both INL and DNL errors are less than ±0.5LSB.

TABLE III

INL & DNL errors of proposed R-2R DAC

Bit	**Actual Values**	**R-2R**	**DNL(LSB)**	**INL(LSB)**
0	0	0.0522	0.27875	0.0222
1	0.1875	0.1434	-0.235	-0.0384
2	0.375	0.316	-0.3125	-0.016
3	0.5625	0.5981	0.19	0.008
4	0.75	0.699	-0.26875	-0.016
5	0.9375	0.9691	0.16875	0.04
6	1.125	1.076	-0.2575	-0.032
7	1.3125	1.2787	-0.18	-0.056
8	1.5	1.5607	0.32375	0
9	1.6875	1.7085	0.1125	0.008
10	1.875	1.925	0.26875	0.032
11	2.0625	2.0329	-0.1575	-0.088
12	2.25	2.199	-0.26875	-0.064
13	2.4375	2.410	-0.14625	-0.104
14	2.625	2.679	0.29	0.128
15	2.8125	2.8232	0.0575	0.104

Through the simulation of R-2R DAC, INL and DNL errors have been calculated manually and then based on those values shown in table III, INL and DNL graph is drawn as shown in the fig. 11. And through that we have concluded that INL & DNL values of the proposed R-2R DAC are less than ±0.5LSB (maximum range of INL and DNL errors).

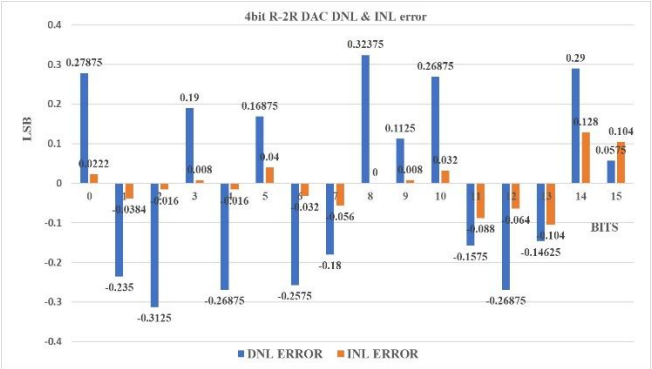

Fig. 11. DNL and INL errors of 4-bit R-2R DAC

E. Comparative Analysis

Comparison of Proposed and existing R-2R DAC is performed by calculating different parameters and then observed some parameters like average, static, and dynamic powers are better in the proposed DAC when compared to the existing opamp based DAC.

TABLE IV

Comparison of existing and proposed R-2R DAC

S.NO	**PARAMETERS**	**Opamp based R-2R DAC[3]**	**Proposed R-2R DAC**
1.	Technology	45nm	45nm
2.	Average Power	29.4mW	7.86mW
3.	Dynamic Power	23.22mW	6.429mW
4.	Static Power	5.18mW	1mW
5.	Supply Voltage	3.5V	3.5V

IV. CONCLUSION

A Low power 45nm CMOS based 4-bit R-2R DAC is designed and simulated using Synopsys H-Spice. In this proposed R-2R DAC as two stage opamp is used, achieved better performance in terms of some parameters when compared to an existing model. i.e., Average power is reduced from 29.4mW to 7.86mW and also static, and dynamic powers are less 1mW, 6.429mW respectively. And observed low INL, and DNL errors in range of ±0.13 and ±0.32 respectively. Hence proposed 4bit R-2R DAC is efficient in terms of power and INL, DNL errors when compared to the existing opamp based R-2R DAC.

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