Design and Analysis of Various CMOS based Binary Scaled Digital to Analog Converter

Dr. S.Rajendra Prasad[1]
Dept. of ECE
VNRVJIET
Hyderabad, India
Rajendraprasad_s@vnrvjiet.in

Namani kavya sree[2]
Dept. of ECE
VNRVJIET
Hyderabad, India
Namanikavya73@gmail.com

Kondra omkumar[3]
Dept. of ECE
VNRVJIET
Hyderabad, India
Kondraom17@gmail.com

Kothapalli srujana[4]
Dept. of ECE
VNRVJIET
Hyderabad, India
Srujanaone8@gmail.com

***Abstract*— Digital-to-analog converters are critical in connecting digital device interfaces to analog devices and vice versa. A digital-to-analog converter (DAC) is a device that transforms binary information into a collection of continuous analog voltages. Binary-scaled D/A converters are one of various DAC realizations that integrate binary-weighted circuit quantities (currents, resistors, capacitors, etc.) under digital control to realize an analog quantity. Binary scaled digital to analog converters are constructed in 22nm CMOS technology (which dissipates little power) and compared in terms of conversion accuracy, conversion speed, settling time, power, and resolution. The H-Spice software is used to simulate and analyze various binary-scaled digital to-analog converters.**

***Keywords* - Binary scaled digital to analog converters, 22nm CMOS, Synopsys H- Spice tool.**

I. INTRODUCTION

Complementary Symmetrical Metal-Oxide Semiconductor is another name for CMOS (COS-MOS). The phrase "complementary symmetric" refers to a form of CMOS analytical design that employs complementary, symmetrical pairings of p-type and n-type metal-oxide-semiconductor field-effect transistors (MOSFETs) for logic operations. ADCs convert analog signals in the form of physical variables to digital values in any communication system. For further processing, this digital signal is transformed back into an analog signal. Analog signals, for example, are required to power motors, temperature controls, and other devices. A digital-to-analog converter (DAC) is a device that transforms a digital input signal into the analog voltage or current needed for analog signal processing. A binary code, which is a combination of bits 0 and 1, is used to represent a digital signal. A converter from digital to analog (DAC) is used to convert pulse value to a sine wave. The DACs are used in transfiguring the digital data of video signals and audio signals into analog signals By and large, these DACs are worn on numerous gadgets in this day and age.

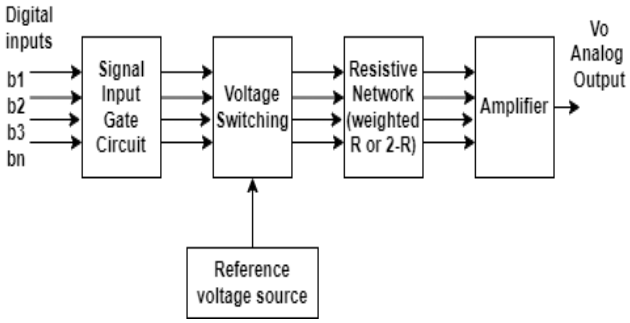

Fig. 1. A simple digital-to-analog converter

All but the most specialized DACs are built as IC's due to their complexity and requirement for perfectly matched components. They often take the form of mixed-signal IC chips made of metal oxide semiconductors (MOS) that merge analog and digital circuitry.Discrete DACs (circuits built from multiple discrete electronic components rather than encapsulated ICs) are the high-speed, low-resolution, high-power consumption type typically used in military radar systems. Very high-speed test equipment, especially sampling oscilloscopes, can also use discrete DACs.

A weighted resistor DAC produces a simple result that approximates a computerized (twofold) contribution by involving binary-weighted resistors in a modified inverter circuit. Subsequently, a parallel weighted obstruction DAC is alluded to as a weighted opposition DAC. At the point when the significant information bit is set to '0,' the advanced switches in the picture are connected to the ground. While the matching info bit is '1', the advanced switch in the graph above is connected to the negative reference voltage - VR. The operation amp's modifying input wire is connected to the ground. At the end of the day, zero volts are applied to the opamp's non-upsetting info terminal. It is comprised of a functional enhancer, for this situation a two-stage opamp circuit as a non-rearranging adding intensifier that enhances

For an n-bit DAC, the relationship between V_{OUT} and the binary input is as follows:

$$V_{OUT} = -\frac{V_{ref}R_f}{R}\sum_{i=1}^{n}\frac{a_i}{2^i}$$

The R-2R DAC utilizes a R and 2R stepping stool network in a transformed viper circuit to give a simple result

that approximates a computerized (twofold) input. The R-2R DAC is named the way that it is comprised of exclusively R and 2R resistors. It likewise doesn't require the utilization of higher-worth resistors. At the point when the significant info bit is set to '0,' the computerized switches in the picture are connected to the ground. While the matching information bit is '1', the advanced switch in the outline above is connected to the negative reference voltage - VR. The operation amp's transforming input wire is connected to the ground. As such, zero volts are applied to the opamp's non-reversing input terminal. [2]. It contains a functional enhancer, of which two are utilized here.

Switched capacitor DAC is similar to binary weighted resistor DAC, as there are binary weighted resistors in binary weighted DAC switched capacitor DAC also having binary weighted capacitors in terms of the power of two the values of capacitors are used. Output is the combination of all inputs given through capacitors where the current is divided based on the weights of the capacitor.

*A. **Op-amp***

DAC systems commonly use differential amplifiers or op amps. This not only amplifies the signal but also differentiates the signal and includes process signals such as signal and summation. The op-amp is a multistage amplifier, Differential amplifier is the input stage of the opamp with two inputs and a balanced output. This stage generally sets the opamp's input resistance and provides a higher voltage gain for the amplifier. Another stage that is driven by the output of the first stage is a differential amplifier which is known as the middle stage. Mostly the middle stage of the opamp has dual input and unbalanced output also called single-ended output. The intermediate stage output DC voltage will also be greater than the ground potential as the direct coupling is used.

The DC Voltage level of the intermediate stage output is shifted to zero volts with respect to the ground by using a level-shifting circuit at the output of the intermediate stage. Always the output stage of a push-pull amplifier is used as the final stage in opamp. To increase the current capability of the opamp and also to increase the voltage swing of the output this final stage is used. The low output resistance is also provided by the proper output stage.

II. DIFFERENT CMOS BASED BINARY WEIGHTED DAC

DAC consists of two blocks one is an opamp the other one is a switching network either with resistor or capacitors based on the requirement. To get better accuracy and gain a two stage opamp is used and designed various types DACC's and then compare the performance of all types of DAC

*A. **DESIGN OF TWO STAGE OPAMP***

A two-stage operational amplifier consists of three different sections: a differential amplifier stage, a gain stage, and a bias stage. The first stage is the differential stage of the circuit, which provides higher gain, whereas the second stage is known as the gain stage, which serves as an additional gain for getting larger output swings. Transistors M11, M12, M13, and M14 form the differential amplifier stage of the opamp. Differential input of the amplifier is provided through two NMOS transistors M11 and M12 i.e., inverting and non-inverting inputs to the Gates of M11 and M12 transistors respectively. The main resistance which is contributing to the output is the resistance of the input transistors M11, M12, and active load transistors M13 and M14. The Current mirror helps in converting the input signal of differential form to a single-ended signal which is the main advantage of using the current mirror of active load transistors M13 and M14, and common mode rejection is achieved by the load. [9].

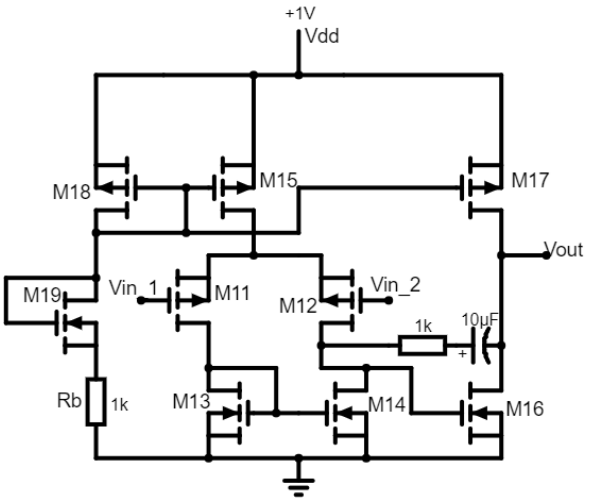

Fig. 4. Design of Opamp

M11 and M13 are current mirrors to each other, so M11 and M13 have equal currents and the current in M14 is subtracted from the current in the M12 transistor so that M12 and M14 transistors are also having equal currents. The current sink load inverter is formed by the transistors M16 and M17. Through the common source configuration output from the drain of a transistor, M12 is amplified by the transistor M16 (Verma et al., 2013). And also, the biasing of the opamp is implemented by the four transistors. A bias chain is used for sinking a specific amount of current based on the gate-to-source voltage of transistors M15 and M18. To lower the frequency of the dominant pole and to move the output pole of the amplifier away from the origin a compensation capacitor (CC) is used which is connected to the output of the differential stage. And at the output of the opamp, a load capacitor is connected. [9].

Design Considerations:

$$I_{ds} = \frac{\mu C_{ox} W}{2L(V_d - V_s)^2} \tag{4}$$

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{5}$$

$$Gain * Bandwidth = \frac{g_m}{2\pi f Cl} \quad (6)$$

$$\frac{W}{L} = \frac{g_m^2}{2I_{ds}\mu C_{ox}} \quad (7)$$

Using these Design considerations we have designed two-stage opamp to achieve different specifications like gain, bandwidth, etc.,

B. DESIGN OF CMOS BINARY WEIGHTED DAC

For the 4-bit binary weighted resistor DAC shown in fig there are 4 binary inputs B_0(LSB), B_1, B_2, and B_3(MSB). The binary inputs are realized by using the pulse inputs connecting in series with the resistors, for the least significant bit (B_0) the pulse values of 1V are given with a period of 32us and a pulse width of 16us. Similarly, for the next most significant bit (B_1) the pulse value is 1V with the period and width of the pulse double of the previous lower significant bit (B_0), and for the (MSB) most significant bit (B_3) the pulse values is 1V with the time period 256us and pulse width 128us, which is 2^3 times time period and pulse width of the (LSB) least significant bit (B_0).

The 1k resistor is connected in series with the MSB bit(B_3) and for the next lower significant bit (b2) the resistor value is 2^1 times the MSB bit, likewise, the resistor values are increased in the binary-weighted fashion, the least significant (b0) has the resistor value of 8k (2^3 times of the MSB bit resistor value). The least significant bit (b0) has the highest resistor value passing the lowest current and the d highest significant bit (B3) has the lowest resistor value which allows the highest current. The feedback resistor has a value of 1k which is equal to the resistor value across the most significant bit(B3).

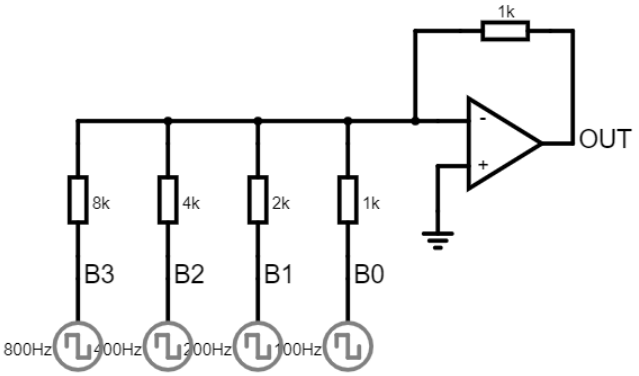

Fig 3: Schematic of binary-weighted DAC

C. DESIGN OF CMOS R-2R DAC

For the 4-bit R-2R DAC which is shown in the below figure, there are 4 binary inputs B_0(LSB), B_1, B_2, and B_3(MSB). The binary inputs are realized by using the pulse inputs connecting in series with the resistors, for the least significant bit (B_0) the pulse values of 1V are given in the period of 32us and a pulse width of 16us. Similarly, for the next most significant bit (B_1) the pulse values of 1V with period and width of the pulse are double of the previous lower significant bit (B_0), and for the (MSB) most significant bit (B_3) the pulse values is 1V with the period 256us and pulse width 128u which is 2^3 times time period and pulse width of the (LSB) least significant bit (B_0).

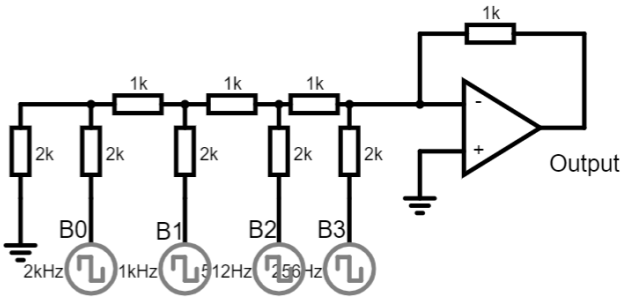

Fig. 5. Design of 4 bit R-2R DAC

In the R-2R DAC, R and 2R are the only two resistor values present. The 1K ohm resistor is taken as the feedback resistor, and the two resistor values considered in the circuit are 100 and 200 ohms. The resistor 2R (200) is connected in series with all four binary input pulses (B0, B1, B2, and B_3) . the resistor values of R (100) ohms are connected in between the networks of the two binary bit inputs resistors and one extra resistor of 2R(200) is connected in series with the whole resister network and the ground.

D. DESIGN OF CMOS SWITCHED CAPACITOR DAC

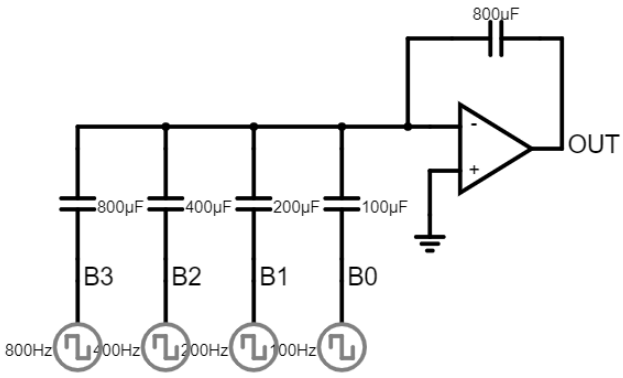

Fig 5: Schematic of Switched Capacitor DAC

For the 4-bit Switched Capacitor DAC shown in fig 5 there are 4 binary inputs B_0(LSB), B_1, B_2, and B_3(MSB). The binary inputs are realized by using the pulse inputs connecting in series with the resistors, for the least significant bit (B_0) the pulse values of 1V are given with a period of 32us and a pulse width of 16us. Similarly, for the next most significant bit (B_1) the pulse value is 1V with the period and width of the pulse double of the previous lower significant bit (B_0), and for the (MSB) most significant bit (B_3) the pulse values is 1V with the time period 256us and pulse width 128us, which is 2^3 times time period and pulse width of the (LSB) least significant bit (B_0).

III. RESULTS AND COMPARISON

A. Results of binary-weighted DAC

Modern CMOS design is very much based on reducing power consumption. By increasing the number of bits of input we can get better resolution in binary-weighted DAC and weare implementing DAC in Hspice by using 22nm technology through which we get low power consumption, better resolution, and accuracy.

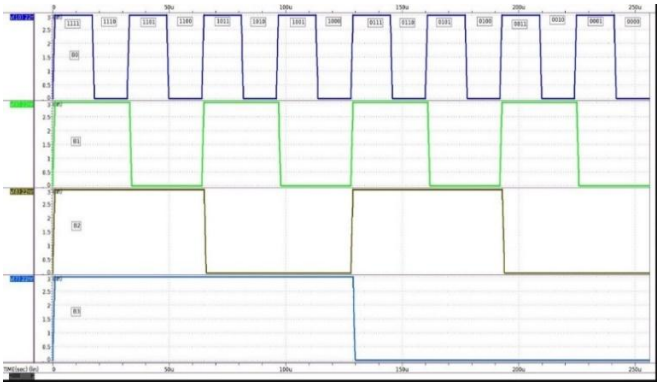

Figure 6: Digital Input

The digital input is given in form of pulses of the voltage value of 1V, the pulse width for the single bit change is 16us, the digital input is given for the duration of 256us, the digital input varying from 1111 to 0000 consisting of total of 16 combinations.

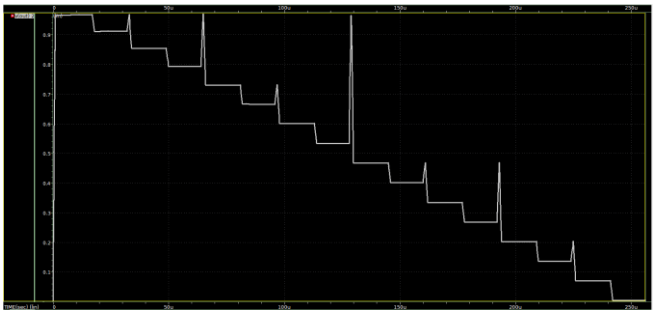

Figure 7: Output Waveform of Binary weighted DAC

B. Results of R-2R DAC

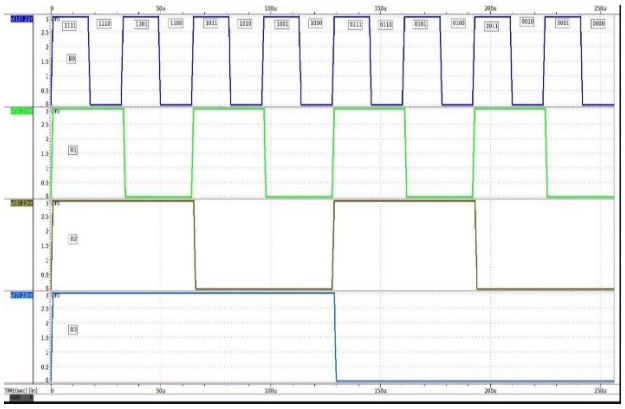

Figure 8: Digital Input

The digital input is given in form of pulses of the voltage value of 1V, the pulse width for the single bit change is 16us, the digital input is given for the duration of 256us, the digital input varying from 1111 to 0000 consisting of a total of 16 combinations.

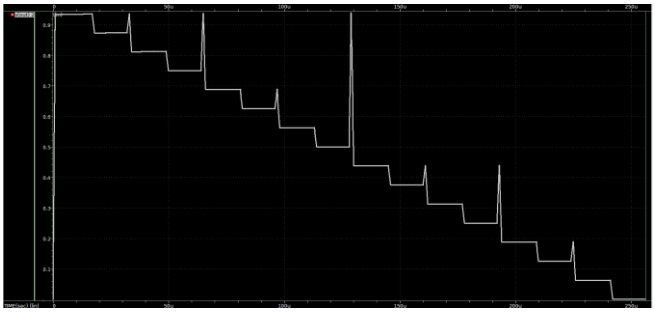

Figure 9: Output Waveform of R-2R DAC

C. Results of Switched Capacitor DAC

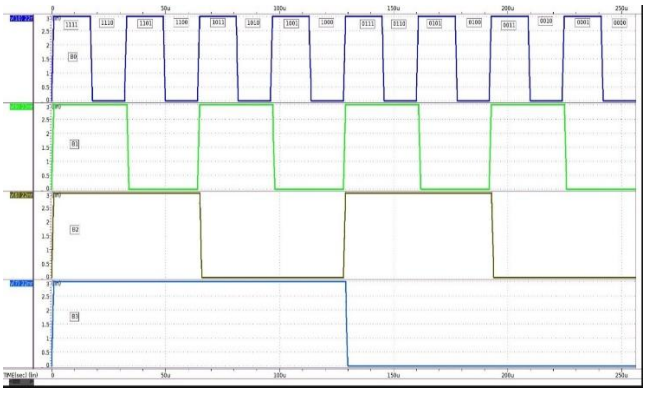

Figure 10: Digital Input

The digital input is given in form of pulses of the voltage value of 1V, the pulse width for the single bit change is 16us, the digital input is given for the duration of 256us, the digital input varying from 1111 to 0000 consisting of total of 16 combinations.

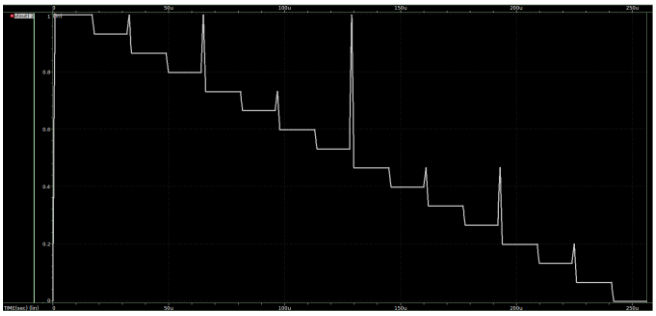

Figure 11: Output Waveform of Switched Capacitor DAC

For the CMOS Binary weighted resistor DAC, R-2R DAC, and Switched Capacitor DAC different parameters like rise delay, fall delay, average power, dynamic power, static power, resolution, and settling time are measured and noted in the table

TABLE I

Comparison of different parameters of DAC's

S.NO	PARAMETERS	Binary Weighted Resistor DAC	R-2R DAC	Switched Capacitor DAC
1.	Technology	22nm	22nm	22nm
2.	Rise delay	1.19us	1.26us	1.144us
3.	Fall delay	8.17ns	1.25ns	7.44ns
4.	Average Power	2.6932mW	3.594 mW	7.4856mW
5.	Dynamic Power	2.449mW	3.1121 mW	6.6193mW
6.	Static Power	0.2442mW	0.4819 mW	0.8719mW
7.	Resolution	0.1786V	0.1853 V	0.1757V
8.	Settling time	1.33us	1.25us	1.23us

IV. CONCLUSION

Each and every DAC has supremacy and drawbacks on different parameters over others. It is not possible to have all the useful aspects in only one circuit, Designed and simulated different binary scaled DAC's with a supply voltage of 1V. As we compared Binary weighted, R-2R DAC, and Switched Capacitor DAC performance with different parameters, Binary weighted DAC has low static and dynamic powers consumption than R-2R and Switched Capacitor DAC i.e., 0.2442mW, 2.449mW respectively. The average power of binary-weighted DAC is 2.6932, R-2R DAC and Switched Capacitor DAC are 2.6932mW, 3.594mW, and 7.4856mW respectively, where binary weighted DAC has less average power. Resolution is high for R-2R DAC(0.1853) than Binary weighted and Switched Capacitor DAC. And Binary weighted DAC has lower accuracy as INL and DNL errors are more when compared to Switched Capacitor and R-2R DAC. By considering all the above parameters, We can conclude that when compared to a binary-weighted resistor and Switched Capacitor DAC, R-2R DAC has more advantages like high accuracy, High resolution, and lesser INL & DNL errors. Whereas Binary weighted DAC has lower Average, static and dynamic powers, and Switched capacitor has a low settling time.

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