VALLURUPALLI NAGESWARA RAO VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

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NBA Accreditation for B.Tech. CE, EEE, ME, ECE, CSE, EIE, IT Programmes
Approved by AICTE, New Delhi, Affiliated to JNTUH, NIRF 135th Rank in Engineering Category
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Vignana Jyothi Nagar, Pragati Nagar, Nizampet (S.O), Hyderabad – 500090, TS, India

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Estd: 1995

THE SEVEN HABITS OF HIGHLY EFFECTIVE PEOPLE

- **Be Proactive**
- **Begin with the End in Mind**
- **Put First Things in Mind**
- **Think Win-Win**
- **First Understand, then be Understood**
- **Synergize**
- **Sharpen Your Saw**

I have followed the above seven steps during the course of my project work

K. SRUJANA **(19071A04M1)**

DESIGN AND ANALYSIS OF LOW POWER CMOS BASED R-2R DAC

A PROJECT REPORT SUBMITTED IN THE PARTIAL FULFILMENT OF REQUIREMENTS FOR THE AWARD OF

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING(ECE)

UNDER THE GUIDANCE OF

Dr. S. RAJENDRA PRASAD

Professor and Head,

Department of ECE, VNR VJIET

Submitted by

K. SRUJANA (19071A04M1)

Estd: 1995

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May 2023

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TAMASŌMA JYOTIRGAMAYA

Estd: 1995

CERTIFICATE

This is to certify that the Project Report entitled "**DESIGN AND ANALYSIS OF LOW POWER CMOS BASED R-2R DAC**", that is being submitted by **K. Srujana (19071A04M1)** in partial fulfillment for the award of the degree of "**Bachelor of Technology in Electronics and Communication Engineering** " of the VNRVJIET, Hyderabad during the academic year **2022-2023** is a record of bonafide research works carried out by her under my supervision and guidance. The contents embodied in the report have not been submitted for the award of any other degree or diploma in this or any other university.

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SIGNATURE OF THE EXTERNAL EXAMINER

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Estd: 1995

DECLARATION

I hereby declare that work contained in the project work entitled "**DESIGN AND ANALYSIS OF LOW POWER CMOS BASED R-2R DAC**", submitted in the department of Electronics and Communication Engineering (ECE), Vallurupalli Nageswara Rao Vignana Jyothi Institute of Engineering and Technology, Hyderabad, in partial fulfilment of the requirement for the award of the degree of **Bachelor of technology in department of Electronics and Communication Engineering** during the academic year 2022-2023 is a bonafide record of my work carried out under the supervision of **Dr. S. Rajendra prasad** (Professor and Head).

Also, I declare that the matter embodied in this report has not been submitted in full or in any part for the award of any degree/diploma of any other institution or university previously.

Place: Hyderabad **Date:** 12-05-2023

K. SRUJANA

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It's my pleasure to add heartfelt words for the people who gave me support right from the stage the idea was conceived. The success of this project is attributed to the intensity, drive, and technical competence of many individuals, who contributed to make this project a reality despite of all odds.

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K. SRUJANA

ABSTRACT

The main purpose of the Digital to Analog converter (DAC) is to act as an interface between the digital device and the analog device. Which converts the binary digital values(0,1) into a series of analog voltages. Each type of DAC has its own set of advantages and disadvantages, It is not possible to attain all positive aspects in one circuit. By considering different parameters like power, resolution etc., we have designed a 4-bit CMOS based R-2R DAC in 45nm technology. In this paper, we are using two stage operational amplifier(op-amp) in order to enhance the performance of the R-2R DAC. A differential amplifier stage and a gain stage form the two stage op-amp, and two values of resistors R and 2R are used to form the R-2R ladder. This two stage op-amp and 4-bit R-2R ladder network are used together to design a 4-bit R-2R DAC. Then This DAC is simulated using the Synopsys H-spice tool and based on the simulation results, analysis is performed by considering various parameters like accuracy-Integral nonlinearity (INL) and Differential nonlinearity(DNL) errors, resolution, average, static, and dynamic powers, and settling time. The proposed R-2R DAC has low power and less INL, and DNL errors which are efficient when compared with the related work.

INDEX

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

Abbreviations	Full form
CMOS	Complementary Metal Oxide Semiconductor
NMOS	N-Type Metal Oxide Semiconductor
PMOS	P-Type Metal Oxide Semiconductor
DAC	Digital to Analog Converter
DNL	Differential non-linearity
INL	Integral non-linearity

CHAPTER 1
INTRODUCTION

Complementary Symmetrical Metal-Oxide Semiconductor is another name for CMOS (COS-MOS). The phrase "complementary symmetric" refers to a form of CMOS analytical design that employs complementary, metal oxide semiconductor field effect transistors (MOSFETs) in symmetrical pairs for logic functions. ADCs convert analog signals in the form of physical variables to digital values in any communication system. For further processing, this digital signal is transformed back into an analog signal. Analog signals, for example, are required to power motors, temperature controls, and other devices.

In order to handle analog signals, a digital input signal must be converted into the analog voltage or current required by a digital-to-analog converter (DAC). A digital signal is represented by a binary code, which is an arrangement of bits 0 and 1. A converter from digital to analog (DAC) is used to convert pulse value to a sine wave. The DACs are used in transfiguring the digital data of video signals and audio signals into analog signals By and large, Nowadays these DACs are used on numerous gadgets. All but the most specialized DACs are built as IC's due to their complexity and requirement for perfectly matched components. They often take the form of mixed-signal IC chips made of metal oxide semiconductors (MOS) that merge analog and digital circuitry.

The R-2R DAC utilizes an R and 2R stepping stool network in a transformed viper circuit to give a simple result that approximates a computerized (two-fold) input. The R-2R DAC is named the way that it is comprised of exclusively R and 2R resistors. It likewise doesn't require the utilization of higher-worth resistors. At the point when the significant info bit is set to '0,' the computerized switches in the picture are connected to the ground. While the matching information bit is '1', the advanced switch in the outline above is connected to the negative reference voltage – V_R. The operation amp's transforming input wire is connected to the ground. As such, zero volts are applied to the op-amp's non-reversing input terminal. It consists of an Operational Amplifier, here we are using a two-stage op-amp schematic as a non-inverting summing amplifier which amplifies the sum of applied input voltages through a resistive network. The R-2R DAC architecture's functionality can be implemented in a variety of ways, and it is easy to construct with a higher conversion rate. The simplicity of the

architecture facilitates the design of higher DACs which is having high resolution for use in several applications where sensors or else control feedback systems are required. Moreover, R-2R DACs have less power consumption, making them perfect for low power applications. The design has a lower production cost since it only needs two resistor values instead of the three required by binary-weighted DACs. It is also possible to attain great linearity. The design's Op-amp is essential for enhancing the DAC's performance.

1.1 Problem statement

The main challenges of conventional digital-to-analog converters (DACs) are to achieve high accuracy - (INL and DNL), low offset error, low settling time, high resolution, and low power. Audio and video encoders, televisions, mobile phones, motor speed controllers, data acquisition systems, and digital potentiometers require conversion speed, high resolution, and low power consumption. DAC architectures such as binary-weighted DACs, redistributed switched-capacitor converters, and R-2R DAC's are widely used and suitable for many applications. In that R-2R DAC is chosen due to its simple structure, fast settling time, and low power consumption, low INL and DNL errors.

1.2 Scope of the project

The conversion of the digital to analog signal (and vice versa) is used in many systems.It is a bridge between the analog and digital world. Two very separate worlds with lots of advantages and disadvantages. To connect these two together we need data conversions from digital to analog and vice versa. The main applications for data conversion are related to communication and data collection from sensors.

To make communication faster and more efficient the data converters should be operating at higher rates. Different types of DAC's have their advantages and disadvantages over others. It is not possible to have all the positive aspects in only one circuit. So for getting better performance in different parameters a type of DAC is chosen. R-2R DAC has low power and better accuracy in terms of INL and DNL. Our research will be continued to get a better conversion rate, resolution, and improvement in some performance parameters.

1.3 Objective of the project

There are different types of Digital to Analog converters like binary weighted resistor, Switched Capacitor and R-2R DAC etc., DAC should have good accuracy, low settling time, low power, and high resolution in order to get that R-2R DAC is chosen. Our main objective is to design a 4-bit R-2R DAC using 45nm CMOS technology in Synopsys H-Spice tool. Which is designed by using two stage op-amp in order to enhance the performance of the DAC. And based on the simulation results, analyze the performance of R-2R DAC by calculating different parameters and then compare with the existing DAC.

CHAPTER 2
LITERATURE SURVEY

In this chapter, various topologies and techniques are described and the work done on them is evaluated. For various applications, we need robust and high-performance DAC's. Foran ideal digital to analog converter, we require low power consumption, low power supply, high speed, high conversion speed, and minimal area.

P. Whig et al., [3] Designed a 4-bit R-2R DAC in several topologies such as CMOS, op-amp, and Transmission gates(TG) in TANNER-EDA T-SPICE. In the op-amp based R-2R DAC, using gates the data is converted to digital form which is on or off based on the value of the input signal. Then the analog signal is obtained from this digital input by using the summing amplifier which is designed using op-amp. Like this 4-bit DAC is designed using op-amp then inputs are in binary format, for zero it is grounded whereas for 1 TTL voltages are assigned. Then these three types of topologies R-2R DAC is simulated by using the TANNER EDA tool and observed that Average power and maximum power are high for op-amp based R-2R DAC when compared to CMOS and TG based DAC's.

A. Noorwali et al., [4] Designed a 16-bit 4MSPS DAC for a lock-in amplifier in 65nm CMOS. Based on the R-2R topology, both INL and DNL can be driven with high resolution and high power, but linearity is reduced due to voltage drop due to wire resistance and for achieving better performance in terms resolution and power and area there is a usage of a current compensation circuit. It is basically a segmented DAC.

D. Arbet et al., [5] Designed an 8-bit R-2R digital to analog converter (DAC) on basis of a digitally controlled operational amplifier's (OPAMP) input offset. To enhance the DAC's overall performance. To compensate for the variations in input offset voltage of the opamp which are caused by variations in the process a digital offset cancellation technique is used. The entire circuitry of DAC and offset compensation were designed using a standard 45nm CMOS process.

Jangra, Payal et al., [6] Designed an 8 bit DAC of type R-2R and fabricated it in 600nm CMOS technology. And after implementation calculated voltage and also current were in order

to know the characteristics of the R-2R ladder network. INL errors are calculated for each bit to know what are the sources of errors in DAC, and in this design INL of the resistive network is 1.2LSB. And in this type of DAC, the components used are fewer in number and simple in construction.

L. Wang et al., [7] Implemented an R-2R DAC of 12 bits in cadence virtuoso tool. Where they have used CMOS technology of 180nm. And after the simulation observed several parameters and concluded that in comparison with previous work done this design has more advantages like lesser consumption of power, chip area is less, and DNL error is also less i.e., 0.03 which is very less than the previous design. And also when compared to the design implemented in 130nm CMOS technology this design of 12 bit DAC has lesser DNL that is errors are less.

CHAPTER 3
BASICS OF DAC

Designing is done step by step, we know DAC is used for conversion of digital to analogsignal, there are several types of dac's like binary weighted resistor dac, switched capacitor dac, current steering dac and R-2R ladder. It is not possible to achieveall good parameters in one type of circuit, we are designing R-2R DAC using H-Spice tool in 45nm CMOS technology and compare the performance with existing DAC.

3.1 Block diagram of Digital to Analog converter

Digital-to-analog conversion is more complex than analog-to-digital conversion. Analog-to-digital conversion involves separating signals or removing power, while digital-to-analog conversion involves adding signals or power. Generally, a D/A converter or DAC can have multiple inputs and one output. It basically converts a discrete-time amplitude signal to a continuous-time amplitude signal.

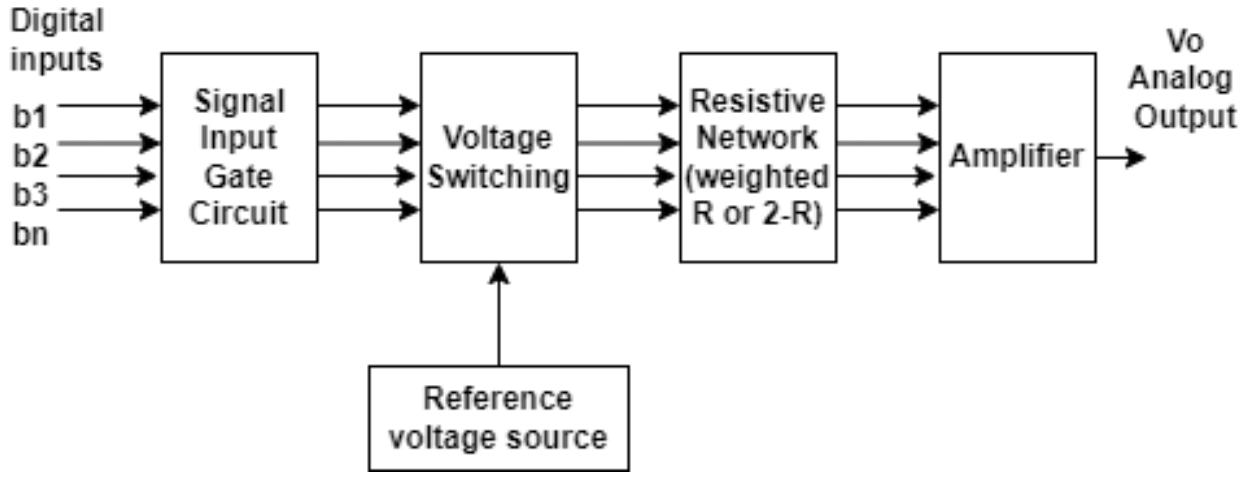

Fig 3.1: Block diagram of Digital to analog converter

3.2 Input circuit

It receives the binary digital inputs safely and does some process or filtration if required. It does not have any important role in the whole circuit. For an n-bit DAC, n number of inputs are applied through this input circuit. It is basically an interface between voltage switching

network and digital inputs (binary bits b0,b1,b2…...bn).

3.3 Voltage switching circuit

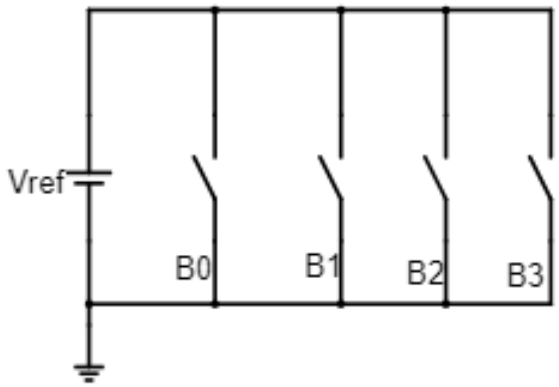

Fig 3.2: Voltage Switching Circuit

It switches voltages between input digital signals and reference voltage sources and passes to the main resistive circuit. It also makes connection or isolation with the ground.

3.4 Resistive network

It is the main part of the digital to analog conversion circuit. Basically, it helps to process multiple digital input before the amplifier circuit. Depending on your resistor network, we can use these two types of DACs binary weighted resistor networks and R-2R networks.

3.5 Amplifier

DAC systems commonly use differential amplifiers or op amps. This not only amplifies the signal but also differentiates the signal and includes process signals such as signal and summation. The op-amp is a multistage amplifier, Differential amplifier is the input stage of the op-amp with two inputs and a balanced output. This stage generally sets the op-amp's input resistance and provides a higher voltage gain for the amplifier. Another stage is driven by the output of the first stage of the op-amp(ie., a differential amplifier) which is known as the middle stage. Mostly the middle stage of the op-amp has dual input and unbalanced output also called single-ended output. The intermediate stage output DC voltage will also be greater than the ground potential as the direct coupling is used.

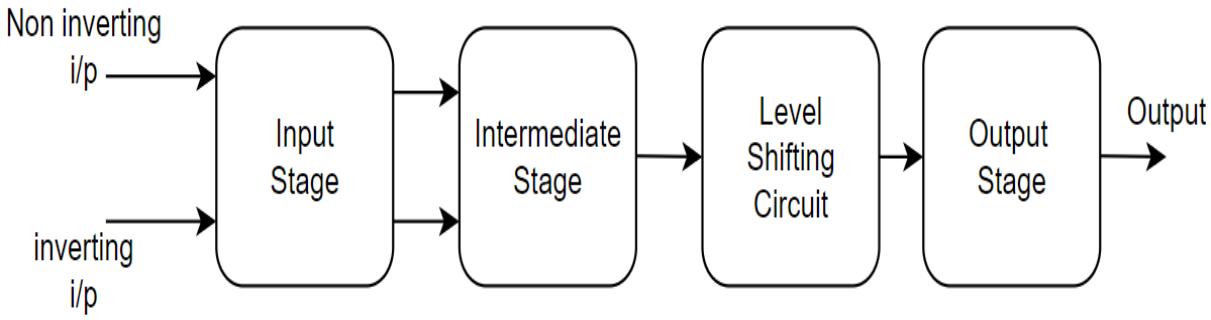

Fig 3.3: Basic op-amp structure

The DC Voltage level of the intermediate stage output is shifted to zero voltage with regard to the ground by using a level shifter circuit at the output of the intermediate stage. Always the output stage of a push-pull amplifier is used as the final stage in the op-amp. To increase the current capability of the op-amp and also to increase the voltage swing of the output this final stage is used. The low output resistance is also provided by the proper output stage.

3.6 R-2R DAC

At various points of the R-2R ladder network input voltages are applied, and the number of input voltages corresponds to the number of bits. To get a better resolution of the R-2R ladder more inputs are applied. At the end of the R-2R ladder inverting terminal of the opamp is connected so this ladder network is used to drive the opamp by combining all these input voltages as a resulting output signal.

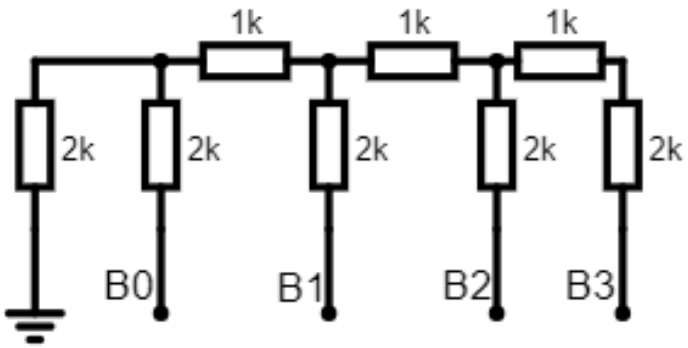

Fig 3.4: R-2R Resistive Network

This four-bit resistor ladder network may appear complex, but it just involves the connection of resistors in series and parallel arrangements and the application of basic circuit principles to determine the output's proportionality to the source of its input. By assuming that all the inputs(binary) are connected to the ground i.e., 0 volts. Resistor R_{13} is in series with R11 and R_{12} which are connected in parallel. Then R_{AA} is the equivalent resistance of the resistors R11, R_{12}, and R_{13}.

$$R_{AA} = R_{13} + \frac{R_{11} \times R_{12}}{R_{11} \times R_{12}} = R + \frac{2R \times 2R}{2R \times 2R} = R + R = 2R \quad (1)$$

Resistor R_{15} is in series with R_{14} and R_{AA} which are connected in parallel. Again the equivalent resistance of these resistors is denoted with R_{BB}, whereas resistance R_{AA} is equivalent to "2R".

$$R_{BB} = R_{15} + \frac{R_{AA} \times R_{14}}{R_{AA} \times R_{14}} = R + \frac{2R \times 2R}{2R \times 2R} = R + R = 2R \quad (2)$$

As stated above R_{BB} is also equivalent to "2R". And Resistor R_{17} is in series with R_{16} and R_{BB} which are connected in parallel. Then again the equivalent resistance calculated from these resistors is represented with R_{CC}.

$$R_{CC} = R_{17} + \frac{R_{BB} \times R_{16}}{R_{BB} \times R_{16}} = R + \frac{2R \times 2R}{2R \times 2R} = R + R = 2R \quad (3)$$

As we know before the parallel combination of two equal resistance values resulting halved resistance value. As the parallel combination of two 2R resistors gives an equivalent resistance of R. Each resistor in the 4-bit R-2R resistor ladder network is linked in parallel. The series combination is identical to "R" when the binary code "0000" is applied to the four inputs. Which is denoted by the resistance(REQ).

CHAPTER 4
DESIGN OF R-2R DAC

In the existing model, they are using a single-stage opamp with less gain so DAC is less accurate in terms of INL and DNL errors. To overcome this disadvantage two-stage opamp is used. Where the differential amplifier is one stage of the opamp and the common source amplifier is known as the second stage.

4.1 Design of two stage op-amp

A differential amplifier stage, a gain stage, and a bias stage are the three different sections of a two-stage operational amplifier. The first stage of the circuit, referred to as the differential stage, offers more gain, and the second stage, referred to as the gain stage, adds additional gain for achieving greater output swings. The differential amplifier stage of the op-amp is constructed using the connections indicated in Fig. 4 between the transistors M_{11}, M_{12}, M_{13}, and M_{14}. Differential input of the amplifier is provided through two NMOS transistors M_{11}, and M_{12} i.e., The Gate terminals of M_{12} and M_{11} transistors are applied with non-inverting and inverting inputs respectively. The main resistance which is contributing for the output is the input transistors M_{11}, M_{12} resistance and active load transistors M_{13}, and M_{14}.

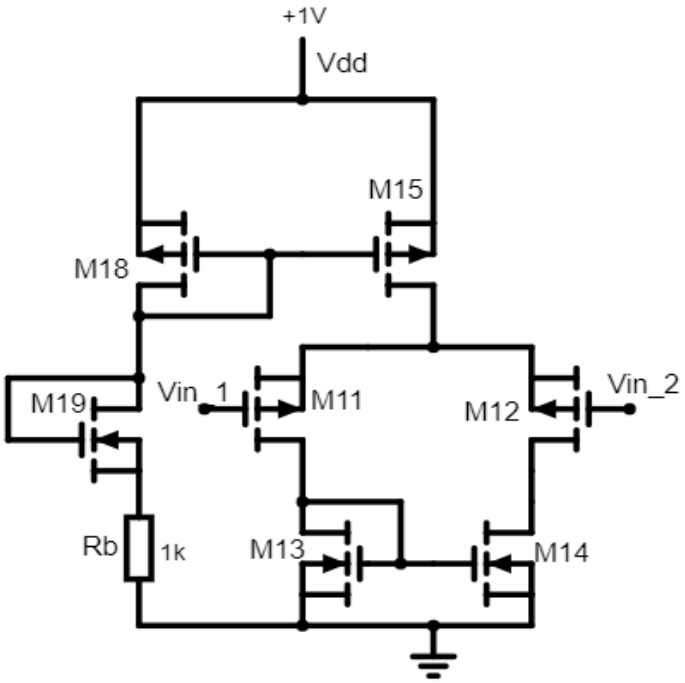

Fig 4.1: Differential amplifier

These M_{11}, M_{12}, M_{13} and M_{14} forms the basic differential amplifier where as biasing is needed for perfect operation of this differential amplifier which can be achieved by using either a current source or else two transistors connected with a resistor R_b of 1k ohm which is given with a supply voltage of 3.5V in this design i.e., V_{DD} of the circuit. Then this M_{18}, M_{19}, and R_b forms the biasing of the op-amp. The Current mirror helps in converting the input signal of dual input i.e., differential to a single output signal which is the main advantage of using the current mirror that is formed through connecting M_{13} and M_{14} (active load transistors), and common mode rejection is achieved by the load. M_{11} and M_{13} are current mirrors to each other, so M_{11} and M_{13} have equal currents and the current in M_{14} is subtracted from the current in the M_{12} transistor so that M_{12} and M_{14} transistors are also having equal currents.

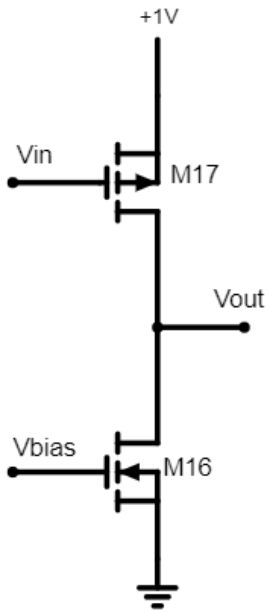

Fig 4.2: Common source amplifier

The current sink load inverter is formed by the transistors M_{16} and M_{17}. Through the common source configuration output from the drain of a transistor, M_{12} is amplified by the transistor M_{16}. The four transistors also work to implement the op-amp biasing. In order to sink a particular amount of current dependent on the gate to source voltage of transistors M_{15} and M_{18}, a bias chain is employed. To reduce the frequency of the dominating pole and move the output pole of the amplifier away from the centre (i.e., origin) a compensation capacitor (CC) is used which is connected to the output of the differential stage. And at the output of the op-amp, a load capacitor is connected. These two stages together form a two stage op-amp as shown in

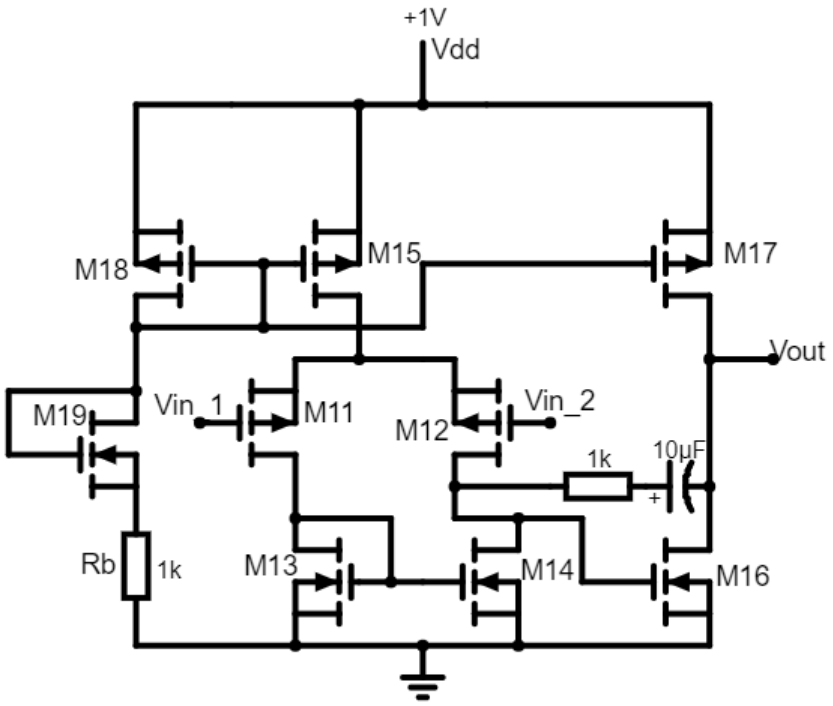

Fig 4.3: Schematic view of two stage op-amp

Design Equations:

$$I_{ds} = \frac{\mu C_{ox} W}{2L(V_d - V_s)^2} \tag{3}$$

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{4}$$

$$Gain * Bandwidth = \frac{g_m}{2\pi f Cl} \tag{5}$$

$$\frac{W}{L} = \frac{g_m^2}{2I_{ds}\mu C_{ox}} \tag{6}$$

$$I_{bias} = slewrate * C_C \tag{7}$$

Assuming slew rate=80V/microseconds, Coupling capacitance is 0.08pF. Then we get I_{bias}as 7μs, but we have to consider the higher value of I_{bias} as 15μs. And μC$_{ox}$ is 20μ then as per the equation 4, we get $(W/L)_{15}$ is 50. And this bias current(I_{bias}) is divided in differential amplifier circuit, and as per current mirror technique both M_{13} and M_{11} are equal i.e., half of

the bias current (7.5μs) and then W/L ratio of M_{13} and M_{14} are equal i.e., 16.6. and calculated W/L ratios of all transistors as shown in table 4.1. Like this we have designed two-stage op-amp by using these design equations, to achieve different specifications like gain, bandwidth, etc.,

Table 4.1: W/L ratios of CMOS in two stage op-amp

S. No.	W/L Ratios	Values
1.	M_{11} , M_{12}	10
2.	M_{13} , M_{14}	16.6
3.	M_{15}	50
4.	M_{16}	20
5.	M_{17}	120
6.	M_{18}	150
7.	M_{19}	33.32

4.2 Design of 4-bit R-2R DAC

For the 4-bit R-2R DAC which is shown in the below figure, there are 4 binary inputs B_0(LSB), B_1, B_2, and B_3(MSB). The binary inputs are realized by using the pulse inputs connecting in series with the resistors, for the least significant bit (B_0) the pulse values of 1V are given in the period of 32us and a pulse width of 16us. Similarly, for the next most significant bit (B_1) the pulse values of 1V with period and width of the pulse are double of the previous lower significant bit (B_0), and for the (MSB) most significant bit (B_3) the pulse values is 1V with the period 256us and pulse width 128u which is 2^3 times time period and pulse width of the least significant bit(LSB) i.e., B_0.

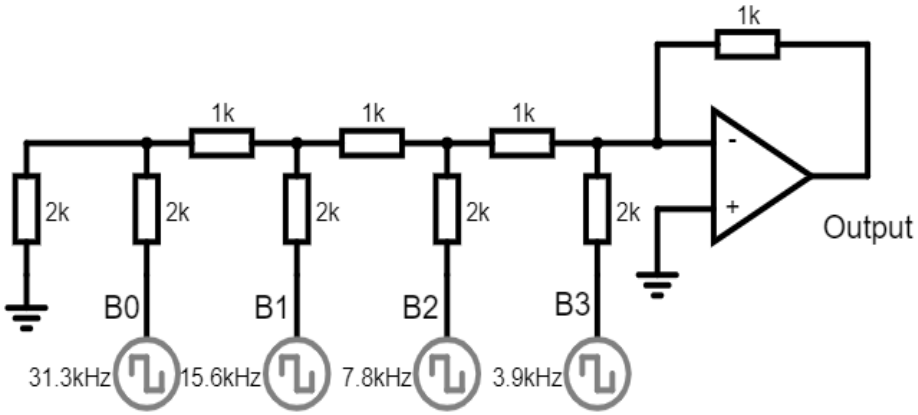

Fig 4.3: Schematic of 4-bit R-2R DAC

In the R-2R DAC, R and 2R are the only two resistor values present. The 1K ohm resistor is taken as the feedback resistor, and the two resistor values considered in the circuit are 1k and 2k ohms. The resistor 2R (2k) is connected in series with all four binary input pulses (B0, B1, B2, and B_3) . The resistor values of R (1k) ohms are connected in between the networks of the two binary bit inputs resistors and one extra resistor of 2R(2k) is connected in series with the whole resister network and the ground.

4.3 H-Spice code for R-2R DAC

```
**R-2R dac**
.include D:\project\45nm.lib
.param IRef=1.5E-6
VDD  VDD  GND   DC  3.5V
VSS  VSS  GND   DC  0V

.SUBCKT OPAMP VDD VSS INP INM OUT gnd
* Your OPAMP Circuit will be here  *
I1 1 VSS IRef
RB 6 gnd 81K
M1 4 INM 2 VDD pmos w= 180n l= 45n
M2 3 INP 2 VDD pmos w= 180n l= 45n
M3 4 4 VSS VSS nmos w= 90n l= 45n
M4 3 4 VSS VSS nmos w= 90n l= 45n
M6 OUT 3 VSS VSS nmos w=90n l= 45n
M8 1 1 VDD VDD pmos w= 180n l= 45n
M7 OUT 1 VDD VDD pmos w= 180n l= 45n
M5 2 1 VDD VDD pmos w= 180n l= 45n
M9 1 1 6 6  nmos w= 90n l= 45n
Rc 3 5 10K
CC 5 OUT 0.08p
.ENDS OPAMP

x1 VDD VSS INP INM OUT gnd OPAMP
```

```
R9 INM OUT 0.5k
R1 7 INM 1k
R2 8 11 1k
R3 9 12 1k
R4 10 13 1k
R5 GND 13 1k
R6 11 INM 0.5k
R7 12 11 0.5k
R8 12 13 0.5k

V4 7 GND pulse(0 3 0 1n 1n 128u 256u)
V3 8 GND pulse(0 3 0 1n 1n 64u 128u)
V2 9 GND pulse(0 3 0 1n 1n 32u 64u)
V1 10 GND pulse(0 3 0 1n 1n 16u 32u)

.tran 1u 256u
.MEAS TRAN avgpow AVG POWER FROM=1u TO=256u
.MEASURE TRAN avg_static_power AVG POWER FROM=1u TO=16u
.print v(OUT)
.end
```

CHAPTER 5
RESULTS AND ANALYSIS

5.1 Simulation results of two stage op-amp

Two stage op-amp is designed using 45nm CMOS technology in Synopsys H-Spice tool and simulated and observed transient and AC analysis and noted down some parameters like gain that is of 42.9dB. as shown in Figure. 5.2.

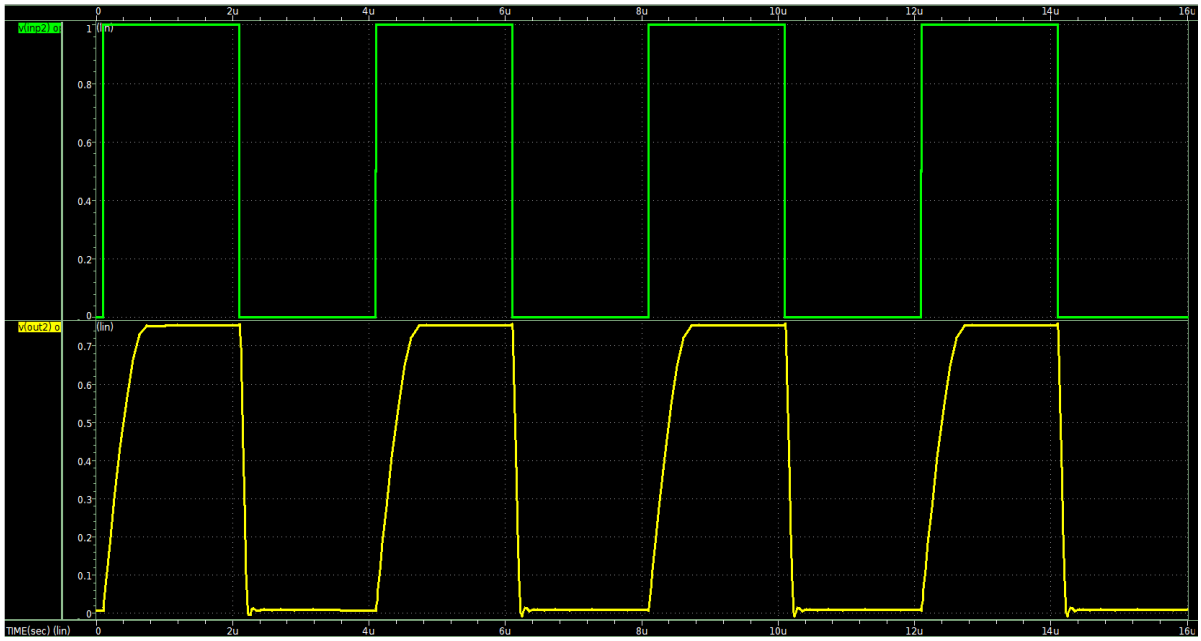

Fig 5.1: Transient Analysis of two stage Op-amp

As we can observe the input and output waveforms of this two stage op-amp are same in phase in the above Figure. 5.1. as we have given input to the non inverting terminal of the op-amp. And also by observing the AC analysis of the two stage op-amp we get a maximum gain of 42.9dB and phase margin of 50.6 degrees as measured at unity gain. This two stage op-amp is used in our main design i.e., R-2R DAC.

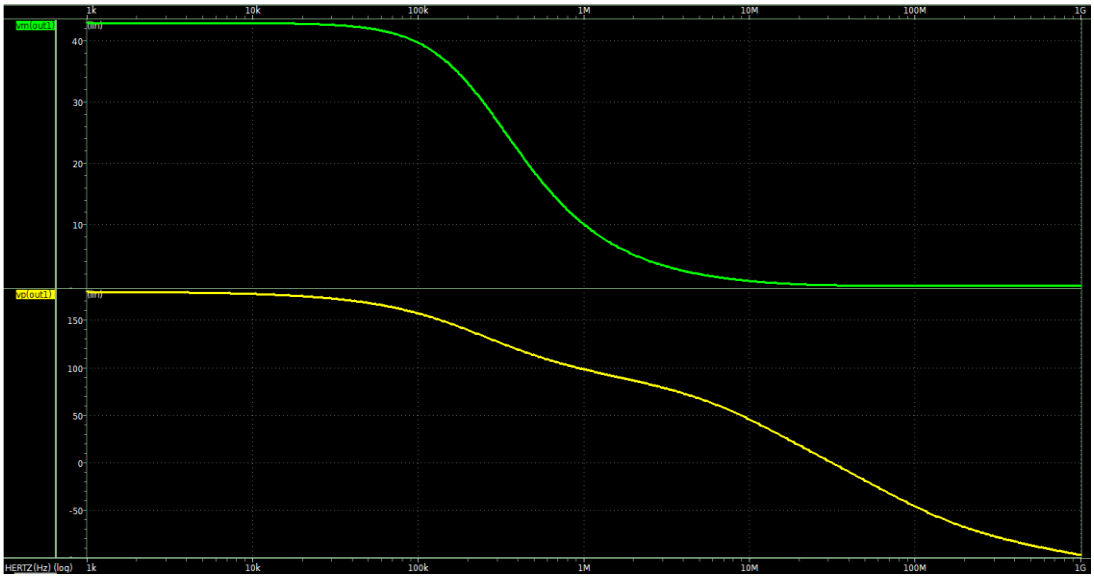

Fig 5.2: AC Analysis of two stage Op-amp

5.2 Simulation results of 4-bit R-2R DAC

Modern CMOS designing is very much based upon reducing power consumption. By increasing the number of bits of input we can get better resolution in R-2R DAC and were implementing DAC in H-Spice by using 45nm technology through which we get low power consumption, better resolution and accuracy.

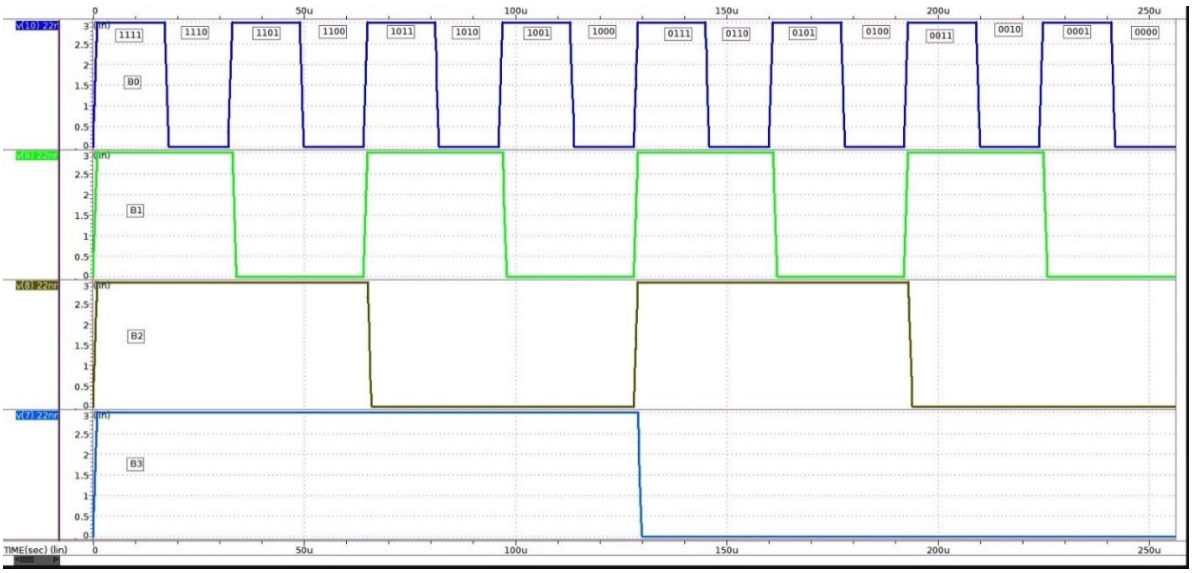

Fig 5.3: Digital Input

The digital input is given in form of pulses of voltage value of 3V, the pulse width for the single bit change is 16us, the digital input given for the duration of 256us, the digital input varying from 1111 to 0000 consisting total of 16 combinations.

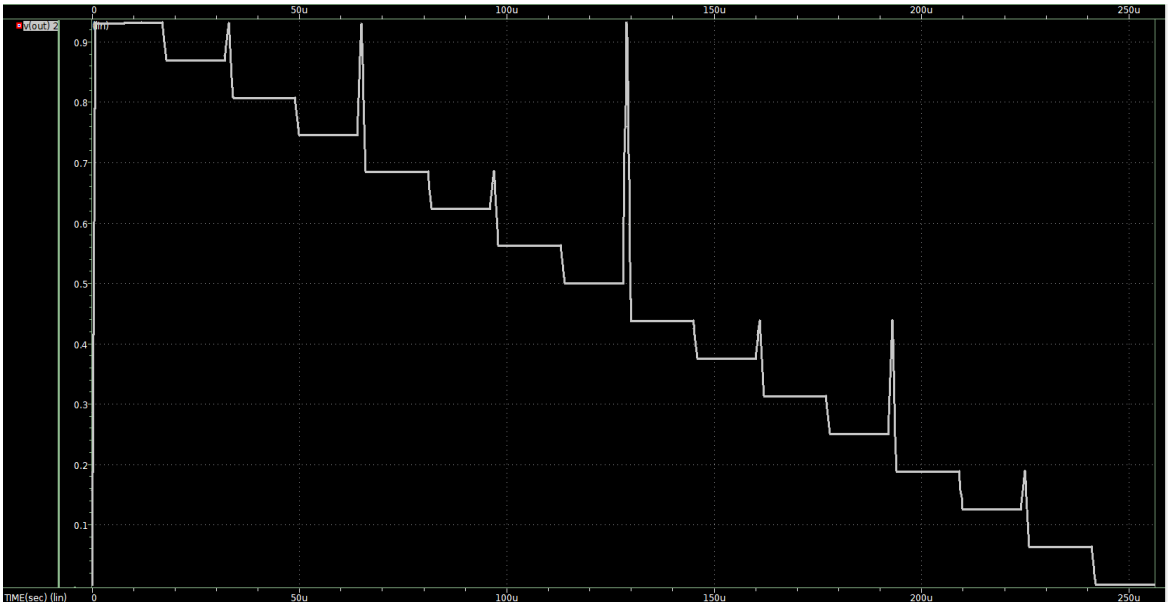

Fig 5.4: Output Waveform of R-2R DAC

Analysis of R-2R DAC is done by implementing the design in H-spice by using 45nm CMOS technology by calculating different parameters like Average power, Static power, Dynamic power, Resolution and settling time, INL, and DNL errors as shown in table 5.1.

Table 5.1: Parametric analysis of R-2R DAC

S. No.	Parameters	Proposed R-2R DAC
1.	Technology	45nm
2.	Resolution	0.1853V
3.	INL	-0.104 to +0.128
4.	DNL	-0.312 to +0.323
5.	Settling time	1.25us
6.	Average Power	7.86mW
7.	Dynamic Power	6.429mW
8.	Static Power	1mW

From the above table we can conclude that proposed R-2R DAC has less settling time (i.e., 1.25us), high resolution (0.1853V), and low INL and DNL errors which is less than range of ±0.5 LSB that tends to high accuracy and also observed low Average, Static and Dynamic powers i.e., 7.86mW, 1mW, 6.429mW respectively.

5.3 Analysis of 4-bit R-2R DAC

Analysis of 4-bit R-2R DAC is performed by calculating different parameters and then by comparing those values with the existed DAC to know in which parameters the proposed DAC is better than the existed. For this manual calculation of some parameters like INL and DNL errors, Resolution are done by observing simulation results of 4-bit R-2R DAC in H-Spice tool as shown in Figure 5.2.

5.4 Calculation of INL and DNL errors

Integral nonlinearity error (INL) is deviation from a straight line after both offset and gain errors have been removed. INL is a measure of the converter's accuracy only at low input signal frequencies since it involves slowly sweeping the converter input throughout its full-scale range. Each analogue step size in a perfect converter is 1 LSB. In other words, in an A/D converter, the transition values are precisely 1 LSB apart, but in a D/A converter, each output level is 1 LSB from neighbouring levels. The difference between analogue step sizes close and far from 1 LSB is known as differential nonlinearity (DNL).

Table 5.2: INL & DNL errors of R-2R DAC

Bit	Ideal values	Practical Values	DNL(LSB)	INL(LSB)
0	0	0.222	0.509	0.14
1	0.1875	0.358	0.49	0.068
2	0.375	0.507	0.48	0.143
3	0.5625	0.668	0.496	0.0937
4	0.75	0.843	0.34	0.14
5	0.9375	1.03	0.493	0.068
6	1.125	1.22	0.506	0.137
7	1.3125	1.41	0.38	0.081

8	1.5	1.61	0.5	0.137
9	1.6875	1.81	0.48	0.081
10	1.875	1.99	0.49	0.168
11	2.0625	2.18	0.5	0.1
12	2.25	2.37	0.3	0.14
13	2.4375	2.54	0.498	0.068
14	2.625	2.69	0.346	0.14
15	2.8125	2.78	0.1733	0

Calculated INL and DNL errors by observing simulation results of 4-bit R-2R DAC as shown in fig.7, where INL errors are in a range between -0.104 to +0.128 and DNL errors are in a range between -0.312 to +0.323 as we see in table 5.2. and concluded that both INL and DNL errors are less than ±0.5LSB.

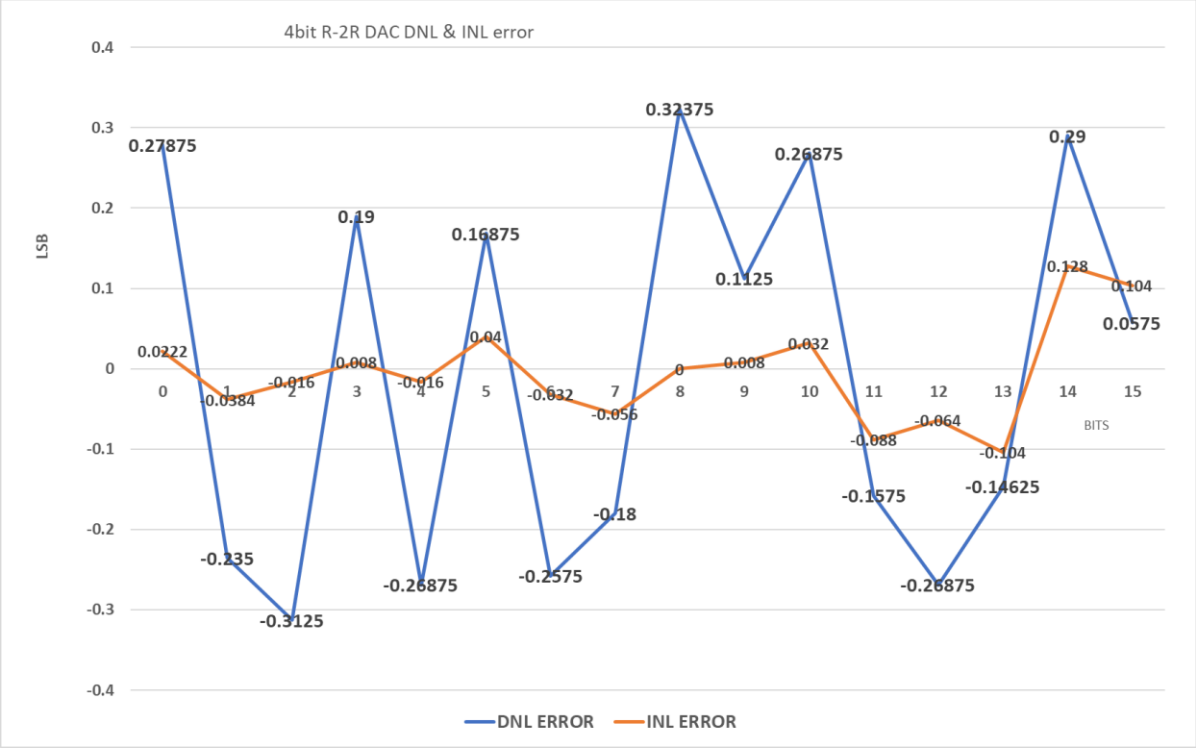

Figure 5.5: INL & DNL Graph of R-2R DAC

5.5 Comparison Analysis

Comparison of Proposed and existing R-2R DAC is performed by calculating different parameters and then observed some parameters like average, static, and dynamic powers are better in the proposed DAC when compared to the existing op-amp based DAC.

Table 5.3: Comparison of existed and proposed R-2R DAC

S.NO	PARAMETERS	Op-amp based R-2R DAC	Proposed R-2R DAC
1.	Technology	45nm	45nm
2.	Average Power	29.4mW	7.86mW
3.	Dynamic Power	23.22mW	6.429mW
4.	Static Power	5.18mW	1mW
5.	Supply Voltage	3.5V	3.5V

The proposed 4-bit R-2R DAC has low Average, Static and Dynamic powers i.e., 7.86mW, 1mW, 6.429mW respectively when compared to the existed DAC.

CHAPTER 6
CONCLUSION

A Low power 45nm CMOS based 4-bit R-2R DAC is designed and simulated using Synopsys H-Spice. In this proposed R-2R DAC as two stage op-amp is used, achieved better performance in terms of some parameters when compared to an existing model. i.e., Average power is reduced from 29.4mW to 7.86mW and also static, and dynamic powers are less 1mW, 6.429mW respectively. And observed high accuracy as there are low INL, and DNL errors in range of ±0.13 and ±0.32 respectively, low settling time that is of 1.25us and high resolution i.e., 0.1853V. Hence proposed 4bit R-2R DAC is efficient in terms of power and INL, DNL errors when compared to the existing op-amp based R-2R DAC.

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