No. of Pages: 3

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SECOND SEMESTER M.TECH DEGREE EXAMINATION, APRIL/MAY 2018

Branch: ***COMPUTER SCIENCE & ENGINEERING***

Stream(s): ***Computer Science & Engineering***

01CS6102:PARALLEL COMPUTER ARCHITECTURE

Answer *any two full* questions from *each* part.
Limit answers to the required points.

Max. Marks: 60 Duration: 3 hours

PART A

1. a. Determine the number of clock cycles required to process a program with 300 instructions in a five stage pipeline. [2]
   b. Explain about the seven dimensions of Instruction Set Architecture. [4]
   c. Suppose that we want to enhance the processor used for web processing. The new processor is 15 times faster on computation in the web serving application than the original processor. Assuming that the original processor is busy with computation 40% of the time and is waiting for I/O 60% of the time, what is the overall speed up gained by incorporating the enhancement? [3]
2. a. Explain about three data hazards with proper examples. [3]
   b. Illustrate the concept of loop-unrolling. [3]
   c. How many bits are there in the (2,2) branch predictor with 8K entries? How many entries are there in a (1,2) predictor with the same number of bits. [3]
3. a. State Amdahl's law and derive an expression for overall speedup. [4]
   b. Find the CPU time needed for executing 100K program with a processor of speed 200 MIPS. [2]
   c. Write the dependencies existing between the various instructions in the following code. [3]

```
ADD.D    F1,F2,F4
MUL.D    F6,F1,F8
S.D      F6,0(R1)
SUB.D    F8,F10,F14
MUL.D    F14,F1,F10
```

PART B

4. a. Explain how the three hazards are avoided in Tomasulo's approach. [3]
   b. Write the difference in how stores are handled in a speculative processor versus in Tomosulo's approach. [2]

c. What are the different steps involved in instruction execution in a system which supports hardware based speculation. [4]

5. a. Describe the Intel core i7 pipeline structure. [4]

b. Show how the following code sequence lays out in convoys, assuming a single copy of each vector functional unit. How many chimes will this vector sequence take? [3]

```
LV        V1,Rx      ;load vector X
MULVS.D   V2,V1,F0   ;vector-scalar multiply
LV        V3,Ry
ADDVV.D   V4,V2,V3   ;add two vectors
SV        V4,Ry      ;store the sum
```

c. What do you understand by flexible chaining in vector processing? [2]

6. a. What are the two different approaches used to issue multiple instructions per clock in a dynamically scheduled processor? [3]

b. The largest configuration of a Cray T90 has 32 processors, each capable of generating 4 loads and 2 stores per clock cycle. The processor clock cycle is 2.167 ns, while the cycle time of the SRAMs used in the memory system is 15 ns. Calculate the minimum number of memory banks required to allow all processors to run at full memory bandwidth. [3]

c. Explain the C-Access vector memory scheme. [3]

PART C

7. a. Explain the concept of multiport memory organization for a multiprocessor system. [5]

b. What do you understand by hierarchical bus system? [2]

c. Draw an 8x8 Omega network built with 2x2 switches. Check whether the permutation (0,6,4,7,3)(1,5)(2) is blocking or non-blocking. Explain the routing of a message from 111 to 011. [5]

8. a. What is multiprocessor cache coherence? Point out the reasons which cause the cache inconsistencies. [6]

b. Assume that words x1 and x2 are in the same cache block, which is in the shared state in the caches of both P1 and P2. Assuming the following sequence of events, identify each miss as a true sharing miss, a false sharing miss, or a hit. Any miss that would occur if the block size were one word is designated a true sharing miss. [6]

Time	P1	P2
1	Write x1	
2		Read x2
3	Write x1	
4		Write x2
5	Read x2	

9. a. Explain the Snooping coherence protocols. [6]

b. Explain the different types of directory structures used in case of a directory based cache coherence scheme. [6]