Program:

Course Number	2005
Course Title	EMBEDDED SYSTEMS ARCHITECTURE 1
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Lab No.	**2**

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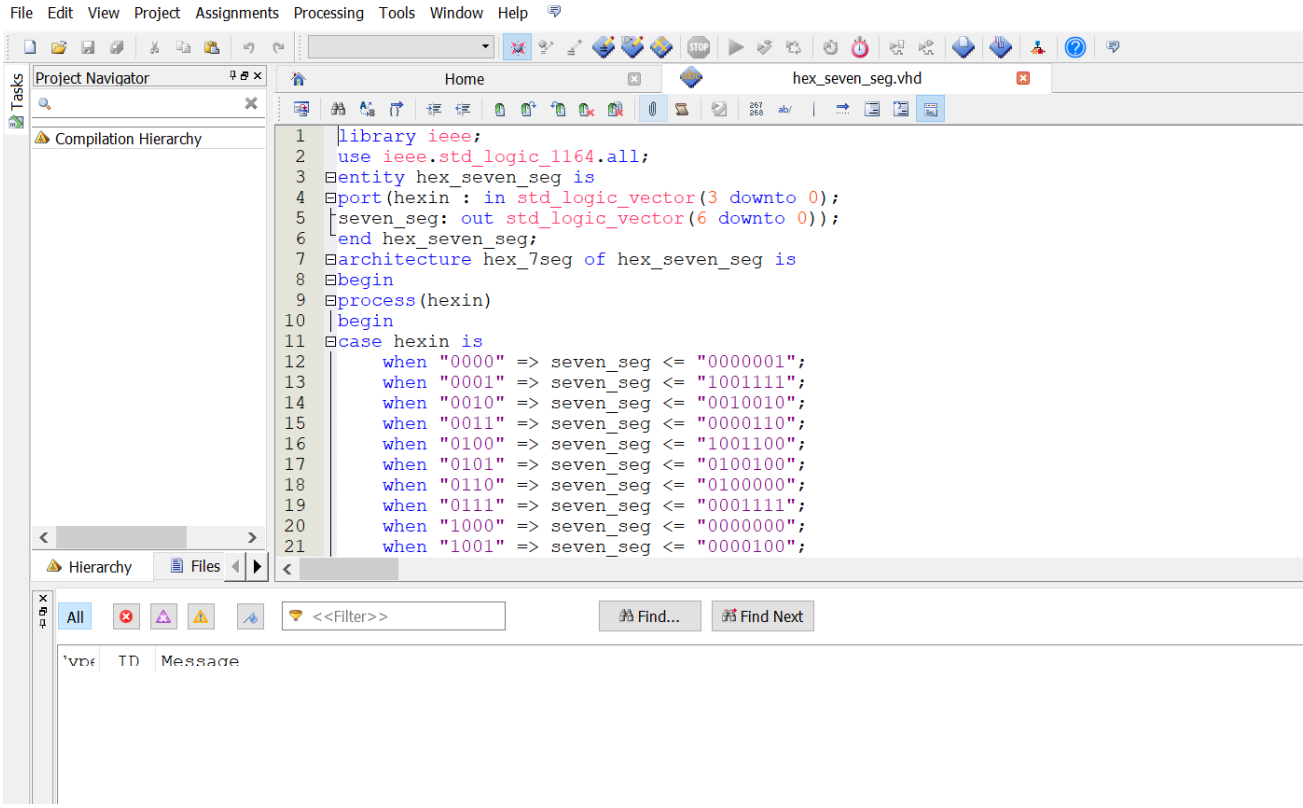
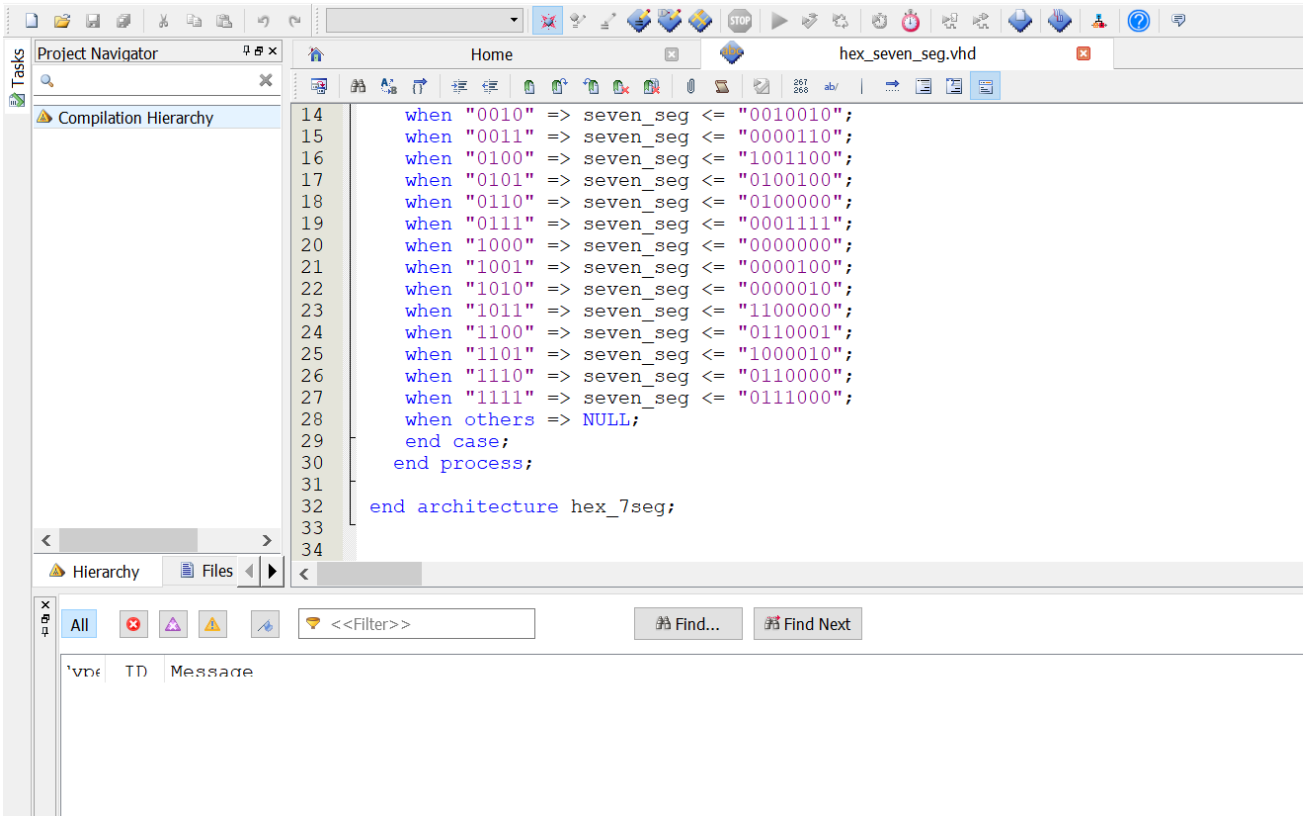
SEVEN SEGMENT DISPLAY

1. PROGRAMMING VHDL



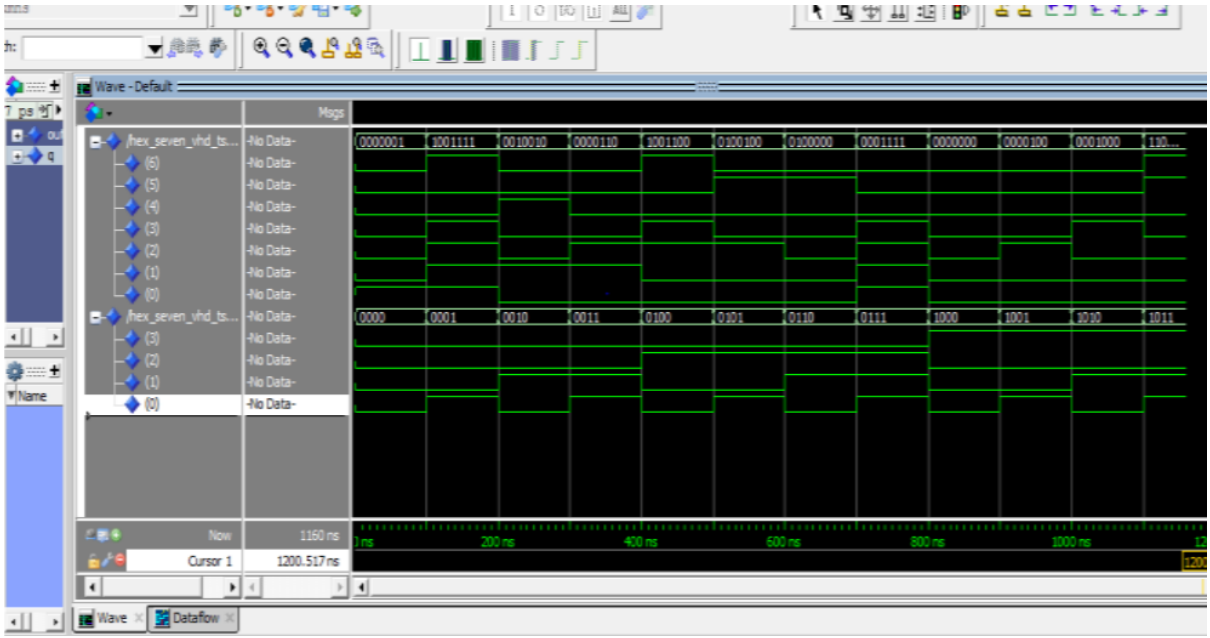


2. TEST BENCH

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY hex_seven_seg_vhd_tst IS
END hex_seven_seg_vhd_tst;
ARCHITECTURE hex_seven_seg_arch OF hex_seven_seg_vhd_tst IS
-- constants
-- signals
SIGNAL hexin : STD_LOGIC_VECTOR(3 DOWNTO 0);
SIGNAL seven_seg : STD_LOGIC_VECTOR(6 DOWNTO 0);
COMPONENT hex_seven_seg
        PORT (
        hexin : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
        seven_seg : BUFFER STD_LOGIC_VECTOR(6 DOWNTO 0)
        );
END COMPONENT;
BEGIN
        i1 : hex_seven_seg
        PORT MAP (
-- list connections between master ports and signals
        hexin => hexin,
        seven_seg => seven_seg
        );
init : PROCESS
-- variable declarations
BEGIN
      -- code that executes only once

WAIT;
END PROCESS init;
always : PROCESS
-- optional sensitivity list
-- (       )
-- variable declarations
BEGIN
       -- code executes for every event on sensitivity list
                hexin <="0000";
      wait for 100 ns;
      hexin <="0001";
      wait for 100 ns;
      hexin <="0010";
      wait for 100 ns;
      hexin <="0011";
      wait for 100 ns;
      hexin <="0100";
      wait for 100 ns;
      hexin <="0101";
      wait for 100 ns;
      hexin <="0110";
```

```
        wait for 100 ns;
        hexin <="0111";
        wait for 100 ns;
        hexin <="1000";
        wait for 100 ns;
        hexin <="1001";
        wait for 100 ns;
        hexin <="1010";
        wait for 100 ns;
        hexin <="1011";
        wait for 100 ns;
        hexin <="1100";
        wait for 100 ns;
        hexin <="1101";
        wait for 100 ns;
        hexin <="1110";
        wait for 100 ns;
        hexin <="1111";
        wait for 100 ns;

    WAIT;
    END PROCESS always;
    END hex_seven_seg_arch;
```

3. WAVEFORM



4. TRUTH TABLE

HEXADECIMAL	BINARY	SEVEN SEGMENT
0	0000	0000001
1	0001	1001111
2	0010	0010010
3	0011	0000110
4	0100	1001100
5	0101	0100100
6	0110	0100000
7	0111	0001111
8	1000	0000000
9	1001	0000100
a	1010	0000010
b	1011	1100000
c	1100	0110001
d	1101	1000010
e	1110	0110000
f	1111	0111000