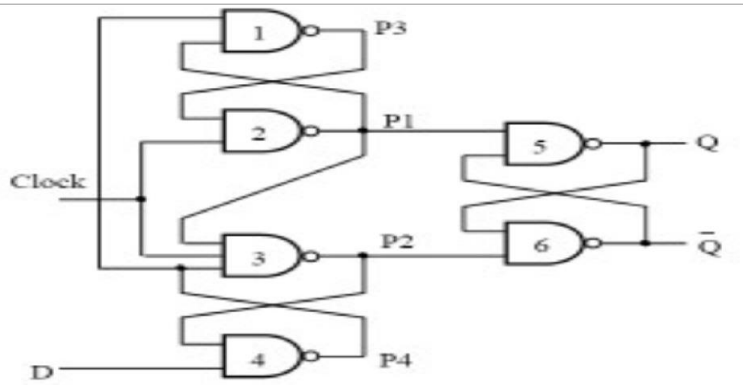
DFF (NAND GATE):



Main verilog code:

```
21 module Main(input A,input B,input CLK, output Y,output Z);
22
23     wire S , DFFInput1 , DFFInput2;
24     wire QDff1,QDff2; // First and second (Q`)outputs
25     wire tempDffOutput; // for second DFF
26     Wire R ; // R wire will help us for Z output
27
28    //FIRST DFF
29    #10 and(S,QDff2,B);
30    #10 or(DFFInput1,S,A); // DFFInput1 --> input D for first Dff
31    #10 DFF DFF1(DFFInput1,CLK,Y,QDff1); //Y --> Q output of first DFF , Y is the first output of this circuit
32
33    //Seconnd DFF
34    #10 nor(DFFInput2,DFFInput1,QDff1); // DFFInput2 --> input D for second Dff
35    #10 DFF DFF2(DFFInput2,CLK,tempDffOutput,QDff2); //QDff2 --> Q` (we will need it forr Z)
36
37    //Wire R
38    #10 and(R,B,QDff2);
39
40    //Zoutput
41    #10 or(Z,QDff1,R);
42
43 endmodule
44
```

DFF verilog code:

```
22 //D flip flap with nand gates
23 module DFF(input D,input CLK,output Q1,output Q2);
24
25 wire P1,P2,P3,P4; // P wires will help us to connect nand gates
26 wire temp;//THIS WIRE WILL HELP US IN P2 NAND WITH 3 INPUTS ...
27
28 //P1 WIRE
29 #10 nand(P1,P3,CLK);
30 //P2 WIRE
31 #10 and(temp,P1,P4);
32 #10 nand(P2,temp,CLK);
33 //P3 WIRE
34 #10 nand(P3,P1,P4);
35 //P4 WIRE
36 #10 nand(P4,P2,D);
37
38 //Q1 OUTPUT
39 #10 nand(Q1,Q2,P1);
40 //Q2 OUTPUT
41 #10 nand(Q2,Q1,P2);
42
43
44 endmodule
```