4th Semester

Course Title	Course Structure			Pre-Requisite
SE 204 Computer System Architecture	**L**	**T**	**P**	Digital Electronics
	3	**0**	**2**	

Course Objective:
To provide knowledge about the principles, concepts and applications of Computer Architecture.

Course Outcome (CO):
1. Describe the functionalities of various units of a computer
2. Illustrate the logic design of Control Unit
3. Understand the architecture and functionality of central processing unit.
4. Learn the different types of serial communication techniques.
5. Illustrate various memory components and memory mapping techniques

S.No.	Content	Contact Hours
Unit 1	Introduction: Digital computer generation, computer types and classifications, functional units and their interconnections, bus architecture, types of buses and bus arbitration. Register, bus and memory transfer. REGISTER TRANSFER LANGUAGE: Data movement around registers. Data transfer from/to memory, arithmetic, logic and shift micro operations. Concept of bus and timing in register transfer.	8
Unit 2	Control Unit: Instruction types, Instruction formats, Instruction cycles and sub-cycles (fetch and execute etc.), micro-operations, execution of a complete instruction. Hardwired Control Unit and Microprogrammed Control Unt: microprogrammed sequencing, wide branch addressing, and micro-instruction with next address field, pre-fetching microinstructions, concept of horizontal and vertical microprogramming.	8
Unit 3	Central Processing Unit: Processor organization, general register organization, stack organization and addressing modes. Computer Arithmetic: Addition and subtraction of signed numbers, Signed operand multiplication, Booth's algorithm and array multiplier. Division	9

	and logic operations. Floating point arithmetic operation	
Unit 4	Input/Output organization: Peripheral devices, I/O interface, I/O ports, Interrupts: interrupt hardware, types of interrupts and exceptions. Modes of Data Transfer: Programmed I/O, interrupt initiated I/O and Direct Memory Access. I/O channels and processors. Serial Communication: Synchronous & asynchronous communication, standard communication interfaces.	9
Unit 5	Memory: Basic concept and hierarchy, Main memory, Auxiliary memory, Associative memory, Cache memories: concept and design issues, associative mapping, direct mapping, set-associative mapping, cache writing and initialization.	8
	Total	42

Books:-

S.No.	**Name of Books/Authors/Publisher**
1)	Patterson, Computer Organization and Design, Elsevier Pub. 2009
2)	Morris Mano, Computer System Architecture, PHI 1992
3)	William Stalling, Computer Organization, PHI 2012
4)	Vravice, Hamacher&Zaky, Computer Organization, TMH 2009
5)	Tannenbaum, Structured Computer Organization, PHI 2006