5. Credits: 4

6. Semester: VII

7. Subject Area: DCC

8. Pre-requisite: NIL

9. Objective: To familiarize the students to work in group and develop an independent understanding of engineering and analysis of engineering systems. He should also be able to write and present the work done during the course.

1. Subject Code: **EP403** Course Title: **Training Seminar**

2. Contact Hours: L: 0 T:0 P:0
3. Examination Duration (Hrs.): Theory: 0 Practical: 0

4. Relative Weight**:** CWS: 0 PRS: 0 MTE: 0 ETE: 0 PRE: 0

5. Credits: 2

6. Semester: VII

7. Subject Area: DCC

8. Pre-requisite: NIL

9. Objective: To familiarize the students to work in industry and working culture of the industrial system. He should also be able to write and present the work done during the course.

1. Subject Code: EP 405 Course Title: VLSI and FPGA Design
2. Contact Hours: L: 3 T: 0 P: 2
3. Examination Duration (Hrs.) Theory: 3 Practical: 0
4. Relative Weight: CWS: 15 PRS:15 MTE: 30 ETE: 40 PRE: 0
5. Credits: 4
6. Semester: ODD
7. Subject Area: DCC
8. Pre-requisite: NIL
9. Objective: To familiarize the student with the concept of MOSFET, VLSI circuits, RAM, ROM and implementation of FPGA.
10. Details of Course:

S. No.	Contents	Contact Hours
1.	Enhancement mode & Depletion mode MOSFETs	**2**
2.	Basic MOS inverter design, transfer characteristics, logic threshold	**1**
3.	NAND \ NOR logic	**1**
4.	Transit time and inverter time delay, CMOS inverter	**2**
5.	Inverting and non-inverting type super buffers, noise margins.	**2**
6.	MOS design rules: Lamda based design rules and MOS layers.	**2**
7.	Stick diagrams, NMOS design layout diagrams	**1**
8.	Scaling of MOS Circuits. Functional limitations to scaling	**2**
9.	Failure mechanism in VLSI, Fault finding in VLSI chips.	**2**
10.	Packaging of VLSI devices, packaging types. Packaging design consideration	**2**
11.	VLSI assembly technology and fabrication technologies.	**2**
12.	Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture	**3**