Course code: Course Title	Course Structure			Pre-Requisite
	L	T	P	
SE310: Parallel Computer Architecture	3	1	0	Computer Architecture

	Course Objective: To introduce fundamentals of parallel, pipelines and superscalar architecture.

S. NO	Course Outcomes (CO)
CO1	Understand the fundamentals of parallel computing, architectural classifications, and performance evaluation techniques.
CO2	Apply multi-core programming techniques, optimization strategies, and parallel processing libraries.
CO3	Analyze and understand multi-threaded architectures, cache coherence mechanisms, and memory consistency models.
CO4	Understand and analyze compiler optimization and operating system issues for multiprocessing and approaches to resolve these issues.
CO5	Analyze and implement parallel computing techniques in real-world applications

S.No.	Contents	Contact Hours
UNIT 1	**Introduction**: Introduction to parallel computing, need for parallel computing, parallel architectural classification schemes, Flynn's, Fang's classification, performance of parallel processors, distributed processing, processor and memory hierarchy, bus, cache & shared memory, introduction to super scalar architectures, quantitative evaluation of performance gain using memory, cache miss/hits.	6
UNIT 2	**Multi-core Architectures**: Introduction to multi-core architectures, issues involved into writing code for multi-core architectures, development of programs for these architectures, program optimizations techniques, building of some of these techniques in compilers, Open MP and other message passing libraries, threads, mutex etc.	6
UNIT 3	**Multi-threaded Architectures:** Parallel computers, Instruction level parallelism (ILP) vs. thread level parallelism (TLP), Performance issues: Brief introduction to cache hierarchy and communication latency, Shared memory multiprocessors, General architectures and the problem of cache coherence, Synchronization primitives: Atomic primitives; locks: TTS, ticket, array; barriers: central and tree; performance implications in shared memory programs; Chip multiprocessors: Why CMP (Moore's law, wire delay); shared L2 vs. tiled CMP; core complexity; power/performance; Snoopy coherence: invalidate vs. update, MSI, MESI, MOESI, MOSI; performance trade-offs; pipelined snoopy bus design; Memory consistency models: SC, PC, TSO, PSO, WO/WC, RC; Chip multiprocessor case studies: Intel Montecito and dual-core, Pentium4, IBM Power4, Sun Niagara	10
UNIT 4	**Compiler Optimization Issues:** Introduction to optimization, overview of parallelization; Shared memory programming, introduction to Open MP; Dataflow analysis, pointer analysis, alias analysis; Data dependence analysis, solving data dependence equations (integer linear programming problem); Loop optimizations; Memory hierarchy issues in code optimization.	8

UNIT 5		**Operating System Issues:** Operating System issues for multiprocessing, Need for pre-emptive OS; Scheduling Techniques, Usual OS scheduling techniques, Threads, Distributed scheduler, Multiprocessor scheduling, Gang scheduling; Communication between processes, Message boxes, Shared memory; Sharing issues and Synchronization, sharing memory and other structures, Sharing I/O devices, Distributed Semaphores, monitors, spin-locks, Implementation techniques on multi-cores; Open MP, MPI and case studies	**8**
UNIT 6		**Applications** Case studies from Applications: Digital Signal Processing, Image processing, Speech processing.	**4**
		TOTAL	**42**

REFERENCES

S.No.		Name of Books/Authors/Publishers	Year of Publication / Reprint
1.		Kai Hwang, Naresh Jotwani, "Advanced Computer Architecture: Parallelism, Scalability, Programmability", TMH, 3rd Edition.	**2003**
2.		John P. Hayes, "Computer Architecture and Organization", McGraw Hill, 3rd Edition.	**2017**
3.		Michael. J. Flynn, "Computer Architecture, Pipelined and Parallel Processor Design", Narosa Publishing.	**1998**
4.		John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative approach", Morgan Kauffmann, 6th Edition	**2017**
5.		Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH.	**2000**