EC405: System on Chip Design

Details of course:-

Course Title	Course Structure			Pre-Requisite
	L	T	P	
System on Chip Design	3	1	0	Microprocessor and embedded systems

Course Objective:To develop fundamental concepts to design, verify, and optimize a System-on-Chip using modern methodologies and tools, enabling students to contribute effectively to cutting-edge developments in the semiconductor and embedded systems industries.

Course Outcomes:

CO1Describe the fundamental principles of SoC design Methodology for Logic and Analog Cores.
CO2Analyze the design of different embedded memories.
CO3 Interpret various state-of-the-art languages and tools used in the creation of SoCs.
CO4Explainthe concepts of System on Chip Design Validation.
CO5Classify testing methodologies to develop Debugging and Testing Skills

S. No.	Content	Contact Hours
Unit 1	Introduction- System tradeoffs and evolution of ASIC Technology- System on chip concepts and methodology – SoC design issues -SoC challenges and components.	8
Unit 2	Design Methodologyfor Logic Cores- SoC Design Flow – On-chip buses –Design process for hard cores – Soft and firm cores – Core and SoC design examples.	8
Unit 3	Design Methodology for Memory and Analog Cores- Embedded memories –Simulation modes Specification of analog circuits.	8
Unit 4	Design Validation- Core level validation –Test benches –SoC design validation – Co simulation – hardware/ Software co-verification.	10
Unit 5	Introduction to SoC Testing- SoC Test Issues –Cores with boundary scan –Test methodology for design reuse– Testing of microprocessor cores – Built in self-method –testing of embedded memories.	8
	Total	42

Books:-

S. No	Name of Books/Authors/Publisher
1	System-on-a-chip:DesignandTest/ Rochit Rajsunah/ArtechHouse,2007.
2	System-on-a-chip verification: Methodology and Techniques, Prakash Raslinkar, Peter Paterson & Leena Singh/ Kluwer Academic Publishers,2000.
3	Low Power Methodology Manual for System-on- Chip Design Series: Integrated Circuits and Systems/M.Keating, D.Flynn, R.Aitken, A, GibbonsShi/ Springer,2007.
4	Integrating BIST techniques for on-line SoC testing / A.Manzone, P.Bernardi, M.Grosso, M. Rebaudengo, E. Sanchez, M.SReorda, Centro Ricerche Fiat/ IEEE Symposium on On-Line testing, 2000.