EC408: Low-Power VLSI Design

Details of course:-

Course Title	Course Structure			Pre-Requisite
	L	T	P	
Low-Power VLSI Design	3	0	2	Digital CMOS IC, VLSI Design

Course Objective: To introduce different low-power techniques to carry out a low-power IC (Integrated Circuit) in silicon.

Course Outcomes:
CO1: Identify the sources of power dissipation in digital ICs and Compute power consumption and apply logical effort theory to size transistors
CO2: Apply Voltage Scaling power for Low power at different abstraction levels of VLSI
CO3: Apply switching and leakage power techniques at different abstraction levels of VLSI
CO4: Design and Analyse arithmetic circuits and evaluate timing parameters
CO5: Explain timing issues in synchronous circuits and design asynchronous circuits

S. No.	Content	Contact Hours
Unit 1	Need for Low Power VLSI Chips, Charging and Discharging Capacitance, CMOS Leakage Current, Static Current, BasicPrinciples of Low Power Design, Low Power Figure of MeritsSimulation Power Analysis: SPICE Circuit simulation, DiscreteTransistor Modelling, and Analysis, Gate-level Logic Simulation,Architecture-level Analysis, Data Correlation Analysis in DSPSystems, Monte Carlo SimulationRandom Logic Signals, Probabilistic Power AnalysisTechniques, Propagation of Static Probability in Logic Circuits,Transition Density Signal Model, Gate Level Power Analysis Using Transition Density	8
Unit 2	Circuit: Logical effort and transistor sizing, RC delay models,Sizing an Inverter Chain, Transistor, and Gate Sizing forDynamic Power Reduction, Transistor Sizing for Leakage PowerReduction, Equivalent Pin Ordering, Network Restructuring andReorganization, Special Latches and Flip-flops, Low Power Digital Cell Library	8
Unit 3	Supply Voltage Scaling for Low Power, Architectural-LevelApproaches, Voltage Scaling Using High-LevelTransformations, Multilevel Voltage Scaling (MVS), DynamicVoltage and Frequency Scaling, Adaptive Voltage ScalingSwitched Capacitance Minimization, System-Level	8

	Approach:Hardware–Software Codesign, Transmeta's Crusoe Processor,Bus Encoding, Clock Gating, Gated-Clock FSMs, FSM StateEncoding,FSM Partitioning, Operand Isolation, Precomputation, Glitching Power Minimization	
Unit 4	Leakage Power Minimization: Fabrication of Multiple ThresholdVoltages, VTCMOS Approach, Transistor Stacking, MTCMOSApproach, Power Gating, Clock, Isolation Strategy, StateRetention Strategy, Power-Gating Controller, PowerManagement, Combining DVFS and Power Management,Dual-Threshold Assignment Approach (DTCMOS)Low power clocked tree design, Low voltage and low power arithmetic circuits.	10
Unit 5	Adiabatic logic: Adiabatic Charging, Adiabatic Amplification,Adiabatic Logic Gates, Pulsed Power Supply, Stepwise ChargingCircuits, Partially Adiabatic Circuits, Efficient Charge RecoveryLogic, Positive Feedback Adiabatic Logic Circuits, 2N−2N2P Inverter/Buffer.Timing issues in synchronous circuits (clock skew and clock jitter), Asynchronous circuit Design	8
	Total	42

Books:-

S. No	Name of Books/Authors/Publisher
1	Practical Low Power Digital VLSI Design/G. K. Yeap/Kluwer Academic Publishers, 2002.
2	Low-Power VLSI circuits and systems/A. Pal/Springer
3	Digital integrated circuits a design perspective/Jan M Rabaey, Anantha Chadrakasan, Borivoje Nikolic/Pearson education.
4	Principle of CMOS VLSI Design/Neil E Weste and Kamran, Eshraghian/Pearson Education.
5	CMOS digital integrated circuits/Sung MO Kang Yusuf Leblebici,/Tata McGraw Hill Publication.
6	Low-Power CMOS VLSI Circuit Design/K. Roy and S. Prasad/Wiley