CS206: Computer System Architecture and Organization	L	T	P	Digital Logic Design
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Course Objective: To provide in depth knowledge of Computer system architecture and organization covering design of processor, memory and I/O systems**.**

S. No	Course Outcomes (CO)
CO1	To get familiar with basic architecture of computer systems, its sub-systems and concept of register based architecture.
CO2	To understand design of various types of control units and design of instructions.
CO3	To understand design of CPU and arithmetic and logic unit (ALU)
CO4	To understand concept of main memory and its interaction with cache memory
CO5	To understand architecture of Input and Output, and various data transfer modes and techniques.

S. No	Contents	Contact Hours
UNIT 1	Introduction: REGISTER TRANSFER LANGUAGE: Data movement around registers. Data movement from/to memory, arithmetic and logic micro operations. Concept of bus and timing in register transfer. Functional units and their interconnections, bus architecture, types of buses and bus arbitration. Register, bus and memory transfer.	6
UNIT 2	Control Unit: Instruction types, formats, instruction cycles and sub-cycles (fetch and execute etc), micro-operations, execution of a complete instruction. Hardwired and microprogrammed control: microprogramme sequencing, wide branch addressing, and micro-instruction with next address field, pre-fetching microinstructions, concept of horizontal and vertical microprogramming	10
UNIT 3	Central Processing Unit: Computer Arithmetic: Addition and subtraction of signed numbers look ahead carry adders. Multiplication: Signed operand multiplication, Booths algorithm and array multiplier. Division and logic operations. Floating point arithmetic operation, Processor organization, general register organization, stack organization and addressing modes.	10
UNIT 4	Memory: Basic concept and hierarchy, Main memory, Auxiliary memory, Associative memory, Cache memories: concept and design issues, associative mapping, direct mapping, set-associative mapping, cache writing and initialization.	8
UNIT 5	Input/Output organization: Peripheral devices, I/O interface, I/O ports, Interrupts: interrupt hardware, types of interrupts and exceptions.	6
UNIT 6	Modes of Data Transfer: Programmed I/O, interrupt initiated I/O and Direct Memory Access. I/O channels and processors. Serial Communication: Synchronous & asynchronous communication, standard communication interfaces.	8
	Total	**48**