DEPARTMENT CORE COURSE-6 (DCC)
EC204- DIGITAL DESIGN - II

Details of course: -

Course Title	Course Structure			Pre-Requisite
	L	T	P	
Digital Design - II	3	-	1	Digital Design - I

Course Objective: To prepare the students for accomplishing design of finite state machines and VHDL/Verilog coding for digital circuits.

Course Outcomes (CO):

1. Realize the combinational and sequential digital circuits using VHDL/Verilog.
2. Design Mealy/Moore Finite state machine, state table conversion and reduction.
3. Illustrate asynchronous sequential machines and minimization.
4. Simplify races, hazards, and faults for digital circuits.
5. Implement the expression using programmable logic devices and algorithm state machine.

S. No.	Content	Contact Hours
Unit 1	**VHDL/ Verilog-** Introduction to FPGAs, Basics of HDLs, Entity declaration, Architecture modelling: Data Flow, Behavioral, structural, Data Types, Operators, Attributes, Signals and Variables, Coding of combinational and sequential circuits, Generic coding.	8
Unit 2	**Synchronous Finite State Machine-** Introduction to synchronous sequential circuits and finite state machine, realization of state table and state diagram from verbal description, complete design and coding of Mealy and Moore machines, Conversion of Moore to Mealy and Mealy to Moore, Minimization of completely and incompletely specified sequential machines.	8
Unit 3	**Asynchronous Finite State Machine-** Introduction to Asynchronous FSM, General Model and Classification of Asynchronous Sequential Circuit, Fundamental mode Analysis, Design of Asynchronous sequential circuits, completely and incompletely specified state machines and reduction of flow tables.	10
Unit 4	**Hazard, Races and Fault Detection-** Introduction to hazards, static, dynamic, functional, and essential hazards, hazards in combinational circuits and their elimination, hazard in sequential circuits, design of hazard-free switching circuits, Races and cycles in Asynchronous sequential machine, concept of secondary state assignment, fault and fault models: stuck-at faults, fault detection methods.	8
Unit 5	**PLDs and Algorithmic State Machine** - Introduction and classification of PLDs, ROM, Implementation of combinational logic circuits using ROM, PLA, PAL. Basics of CPLD, FPGA, ASIC. Introduction	8

	to ASM, ASM Chart: state box, decision box, conditional box, conversion of state diagram into ASM, representation of sequential circuits using ASM, synthesis of ASM chart.	
Total		**42**

Books:-

S. No.	Name of Books/Authors/ Publishers
1.	A Verilog HDL Primer by J. Bhaskar; BS Publication, 3rd edition
2.	Verilog Digital Systems Design by Z. Navabi; Tata McGraw Hill, 1st edition
3.	Switching and Finite Automata Theory by Z. Kohavi; TMH, 3rd edition
4.	Fundamental of Logic Design by Roth; Cengage learning, 6th edition
5.	Advanced Digital design with Verilog HDL by Michael D Ciletti, 2nd edition
6.	Digital Logic State Machine Design" by D. J. Comer; Oxford University Press, 3rd edition
7.	Contemporary Logic Design by R. H. Katz, G. Borriello; PHI, 3rd edition