III Year: SIXTH SEMESTER (EVEN)

Department Core Course-13 (DCC)

EC302: VLSI Design

Details of course:-

Course Title	Course Structure			Pre-Requisite
	L	T	P	
VLSI Design	3	0	2	-

Course Objective:To give the student an understanding of the different design steps required to carry out a complete digital VLSI (Very-Large-Scale Integration) design in silicon.

Course Outcomes:

CO 1. Describe the technology, design concepts, electrical properties and modelling of MOS device.
CO2. Analyze static and timing parameters of inverters and design inverters as per specification
CO3. Design static combinational logic circuits using CMOS, Transmission gates and complementary pass transistor logic
CO4. Apply dynamic circuit techniques to combinational circuit design
CO5. Design and analyze Static and Dynamic Sequential logic circuit and evaluate timing parameters
CO6. Describe design process of memory, design methodologies and apply concept of hierarchy, modularity and locality in designs

S. No.	Content	Contact Hours
Unit 1	Introduction to VLSI, Manufacturing process of CMOS integrated circuits, CMOS n-well process design rules packaging integrated circuits, stick diagram, IC layout and design tools, trends in process technology MOS transistor, Energy band diagram of MOS system, MOS under external bias, derivation of threshold voltage equation, gradual channel approximation, MOS I V characteristics secondary effects in MOSFETS MOSFET scaling and small geometry effects, MOS capacitances, MOS C-V characteristics	8
Unit 2	MOS inverters: Resistive load inverter, inverter with n-type MOSFET	8

	load, CMOS inverter: Switching Threshold, Noise Margin, Dynamic behaviour of CMOS inverter,computing capacitances, Propagation delay,Inverter design with delay constraint, Estimation of interconnect Parasitics, Calculation of interconnect delay Static and Dynamic power consumption, energy, and energy delay product calculations	
Unit 3	Designing Combinational Logic Gates in MOS and CMOS: MOS logic circuits with depletion MOS load. Static CMOS Design: Complementary CMOS, Ratioed logic, Pass transistor logic, pseudo nMOS logic, DCVSL logic Dynamic CMOS logic, clocked CMOS logic CMOS domino logic, NP domino logic, speed and power dissipation of Dynamic logic, cascading dynamic gates.	8
Unit 4	Designing sequential logic circuits: Timing matrices for sequential circuits, classification of memory elements, static latches and registers, the bistability principle, multiplexer based latches , Master slave Edge triggered register, static SR flip flops,dynamic latches and registers, dynamic transmission gate edge triggered register, the C2MOS register, TSPC register Pulse registers, sense amplifier based registers, Pipelining, Latch verses Register based pipelines, NORA-CMOS. Two-phase logic structure	10
Unit 5	Semiconductor memories, DRAM, SRAM, Nonvolatile memory, Flash memory, Introduction to memory peripheral circuits VLSI designing methodology –Introduction, VLSI designs flow, Computer aided design technology: Design capture and verification toolsDesign Hierarchy Concept of regularity, Modularity & Locality, VLSI design style, Design quality	8
	Total	42

Books:-

S. No	Name of Books/Authors/Publisher
1	CMOS digital integrated circuits by Sung MO Kang Yusuf Leblebici, Tata McGraw Hill Publication.
2	Digital integrated circuits a design perspective by Jan M Rabaey, Anantha Chadrakasan Borivoje Nikolic, Pearson education.
3	Principle of CMOS VLSI Design by Neil E Weste and Kamran, Eshraghian, Pearson education.