EC310: Testing and Diagnosis of Digital System Design

Details of course:-

Course Title	Course Structure			Pre-Requisite
	L	T	P	
Testing and Diagnosis of Digital System Design	3	1	0	NIL

Course Objective: To provide students with a comprehensive understanding of digital system testing techniques, fault detection methods, fault tolerance mechanisms, and design for testability concepts.

Course Outcomes:
CO1: Analyze combinational and sequential digital circuits for various types of faults.
CO2: Generate test vectors for faults in digital circuits.
CO3: Identify machines from the input-output sequence.
CO4: Design the fault-tolerant digital systems.
CO5: Describe the methods of design for testability.

S. No.	Content	Contact Hours
Unit 1	Defect, Fault, Error and Failure, fault modelling, fault detection, fault equivalence, fault dominance. Types of faults: stuck at faults, bridging faults, stuck open faults, transient faults, permanent faults.	6
Unit 2	Controllability and Observability: SCOAP, test generation for combinational logic circuits: Path sensitization, Boolean difference method, D-algorithm, PODEM.	8
Unit 3	Testing of sequential circuits: Successor tree, homing tree, distinguishing tree, synchronizing tree, machine identification experiments, checking experiments. Types of faults in RAM, Fault detection in memories: MARCH algorithms.	10
Unit 4	Self-checking circuits, Self-checking in Programmable Logic Arrays. Fault tolerance techniques for combinational and sequential circuits.	8

Unit 5	Design for testability: Random test generation, transition count testing, signature analysis, syndrome testable design, Built In Self Test, Level sensitive scans design, BILBO, BIDCO, Boundary Scan Standard.	10
	Total	42

Books:-

S. No	Name of Books/Authors/Publisher
1	Essentials of Electronic Testing for Digital Memory and mixed-signal VLSI Circuits/ Michael L Bushnell and Vishwani D Agrawal, /Springer
2	An Introduction to Logic Circuit Testing/ PK Lala/ Springer Nature, 2008.