Analysis of Temperature Effect on SRAM PUF For Low Cost Applications

Sayan Samanta*, Biswajit Ray†, Aleksandar Milenkovic*
*Department of Electrical and Computer Engineering, University of Alabama in Huntsville, USA
†Dept. of Electrical and Computer Engineering, Colorado State University, USA
Email: *{ss0443, milenka}@uah.edu, †biswajit.ray@colostate.edu

This is the author's accepted version of the paper. The final published version will be available on IEEE Xplore.

***Abstract*—This paper presents a detailed analysis of temperature effects on Static Random Access Memory (SRAM)–based Physical Unclonable Functions (PUFs) for low-cost embedded applications. We first characterize the power-up behavior of SRAM bitcells at room temperature and evaluate their stability across a temperature range from -15°C to 75°C. Experimental results show that approximately 87% of SRAM cells maintain stable power-up states across all temperatures. While intra-Hamming Distance vary with temperature, inter-Hamming Distance remains largely unchanged, ensuring that device responses remain distinct. These findings suggest that, when the proportion of marginally stable SRAM cells is small, room temperature characterization is sufficient to estimate PUF stability across a wide temperature range, reducing characterization overhead for low-cost embedded systems.**

***Index Terms*—SRAM, PUF, Hamming Distance.**

I. Introduction

Physical Unclonable Functions (PUFs) provide a cost-effective, hardware-rooted approach for device authentication by leveraging inherent manufacturing variations in silicon. Among various PUF architectures, SRAM-based PUFs are widely adopted in resource-constrained platforms such as IoT devices due to their ease of integration, low cost, and the ability to generate device-unique identifiers without requiring additional circuitry.

A strong PUF exhibits three fundamental properties: uniqueness (each device produces a distinct response), reproducibility (stable responses under consistent conditions), and unclonability (impracticality of replicating the response, even with advanced fabrication techniques). In SRAM PUFs, these properties arise from the random power-up state of memory cells, determined by process variations affecting the threshold voltages of transistors in each bitcell.

SRAM PUFs have found applications in device authentication [1], secure key generation and storage [2], [3], and hardware-rooted security solutions. A typical PUF-based authentication system, shown in Figure 1, involves an enrollment phase, where device fingerprints (Gold PUFs or gPUFs) are characterized and stored, and an authentication phase, where a freshly extracted fingerprint (authentication PUF or aPUF) is compared against the stored gPUF using statistical metrics such as Hamming Distance (HD).

The reliability of SRAM PUFs is affected by environmental and operational factors, including temperature [4]–[6], power supply variations [7], power supply ramp, [8], radiation [9], and device aging [10]–[12]. Prior studies have evaluated the impact of temperature on SRAM PUF stability [4]–[6], often focusing on aggregate reliability across limited temperature points. However, these studies have not systematically explored per-bitcell behavior across a broad temperature range or investigated whether room-temperature characterization can reliably predict behavior at other temperatures.

This work addresses this gap by conducting a fine-grained, per-bitcell analysis of SRAM power-up stability across eight temperature points ranging from -15°C to 75°C. Using embedded SRAM in MSP430 microcontrollers, we quantify the power-up stability of each bitcell and analyze intra- and inter-device Hamming Distances across temperature variations. Our results show that in devices where marginally stable cells constitute a small proportion of the memory, room-temperature characterization provides a practical estimate of temperature-dependent stability, thereby reducing the need for extensive environmental testing.

The main contributions of this work are as follows.

- We conduct a detailed, per-bitcell analysis of SRAM PUF stability across a wide temperature range, providing insights beyond aggregate-level measurements presented in prior work.
- We present experimental evidence that room temperature characterization is sufficient to predict the stability of SRAM PUF responses under temperature variation, specifically in devices with a small fraction of marginally stable cells ($\sim$ 6% in our study).
- We demonstrate that intra- and inter-device HD distributions remain well-separated across temperatures, confirming the viability of SRAM PUFs for device authentication without complex post-processing.
- We discuss practical implications for reducing the characterization overhead in low-cost embedded systems where extensive environmental testing may be impractical.

The remainder of this paper is organized as follows. Section II provides background on PUF-based authentication, SRAM power-up mechanisms, and prior work on temperature effects. Section III describes the experimental setup and methodology. Section IV presents the results and discusses their implications

for SRAM PUF stability. Finally, Section V concludes the paper.

II. Background

A. PUF-Based Authentication Process

A typical PUF-based authentication system, illustrated in Figure 1, consists of two distinct phases: enrollment and authentication [13]. During enrollment, typically conducted by the device manufacturer, one or more PUF responses are extracted from the device under controlled conditions. These responses, collectively referred to as Gold PUFs or gPUFs, are securely stored in a database before the device is shipped to customers.

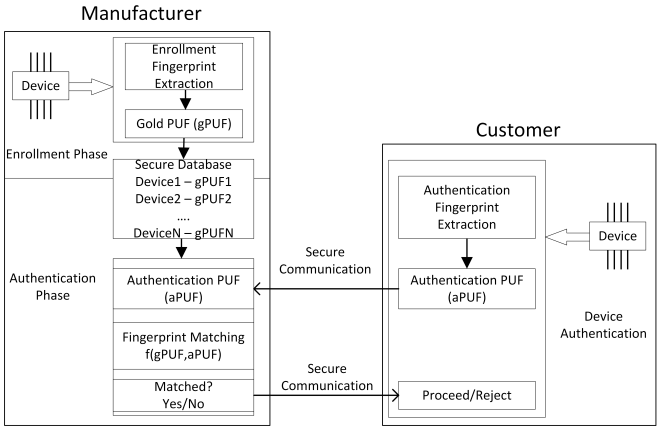

Fig. 1: System View of PUF based Authentication

During authentication, a customer extracts PUF responses, often referred to as authentication PUFs or aPUFs, using the same controlled process. The extracted aPUFs are securely transmitted to the manufacturer, which determines their authenticity by comparing them to the stored gPUF responses. The authenticity check is performed using statistical distance metrics such as Hamming Distance, Jaccard Index, Jaccard Distance or Correlation Value. Based on the matching results, the manufacturer confirms or denies the authenticity of the customer's device via a secure communication channel.

B. Overview of PUF Implementations

Silicon-based PUF architectures, introduced by Gassend et al. [14] in 2002, leverage a variety of physical phenomena that reflect process-induced variations in integrated circuits. Since then, various PUF implementations have been explored, such as Arbiter PUFs [14], Ring Oscillator based PUFs [15], and many other techniques [13]. Arbiter PUFs [14] use race conditions in identically designed paths to produce unique responses, while Ring Oscillator PUFs [15] measure frequency differences in identically structured oscillators. SRAM-based PUFs are memory-based and leverage the unpredictable power-up state of SRAM cells, which arises from mismatches in the threshold voltages of transistors forming each cell. SRAM PUFs [16]–[18] require no additional circuitry, making them highly attractive for resource-constrained applications, such as embedded systems and IoT devices.

C. SRAM Bitcell Power-Up Mechanism

This work focuses on widely used 6-transistor (6T) SRAM bitcell architecture, commonly employed in microcontrollers and other digital systems. A 6T SRAM bitcell includes two cross-coupled inverters acting as a latch and two NMOS access transistors, as shown in Figure 2a. The latch holds data in its true and complementary forms at two internal nodes, Q and $\overline{Q}$, while the access transistors enable read and write operations by connecting these nodes to the bitlines, BL and $\overline{BL}$ [17].

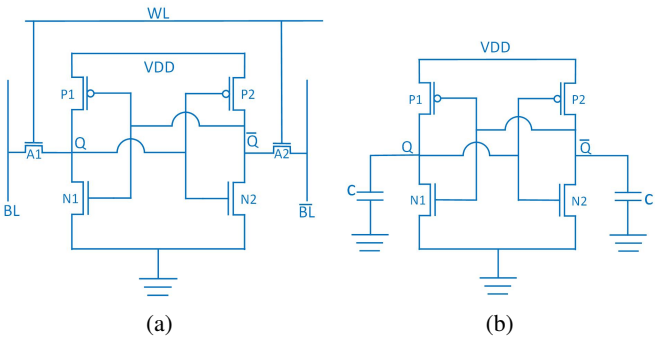

Fig. 2: (a) 6T SRAM Bitcell (b) SRAM PU with two possible state $Q/\overline{Q}$ = 0/1 or 1/0

When the device powers up, before any read or write operations, each bitcell spontaneously settles into either a logic '0' or '1' state. This state is determined by inherent mismatches in the threshold voltages of the transistors within the inverters. For example, if one NMOS or PMOS transistor has a slightly lower threshold voltage, it will switch on more readily, causing the corresponding side of the cell to drive its node toward a preferred state. Table I summarizes the conditions for stable state formation. Figure 2b illustrates the equivalent circuit of a bitcell during power-up.

TABLE I: NMOS and PMOS V_t Mismatch Conditions

$Q/\overline{Q}$	NMOS mismatch	PMOS mismatch
0/1	$V_t^{N_1} < V_t^{N_2}$	$\lvert V_t^{P_1} \rvert > \lvert V_t^{P_2} \rvert$
1/0	$V_t^{N_1} > V_t^{N_2}$	$\lvert V_t^{P_1} \rvert < \lvert V_t^{P_2} \rvert$

The manufacturing process introduces random variations in transistor threshold voltages, leading to unique but repeatable power-up states in each cell. This reproducible behavior forms the basis for generating the SRAM PUF response [18]. However, the power-up behavior of SRAM cells is not solely determined by manufacturing variations; environmental factors, particularly temperature, can influence transistor characteristics and potentially alter the stable power-up state of marginally biased cells.

D. Temperature Effects on MOSFETs and SRAM Cells

The electrical characteristics of MOSFETs and, by extension, SRAM cells exhibit well-known dependencies on temperature. Several prior works [4]–[6], [19] have shown that temperature affects reproducibility and reliability of SRAM

PUFs. Three primary temperature-dependent mechanisms, relevant to SRAM cell behavior, are as follows.

Carrier Mobility Degradation. Carrier mobility decreases with increasing temperature due to enhanced lattice scattering. This in turn lowers the drive strength of transistors, affecting switching dynamics. The relationship between mobility and temperature follows a power-law dependence, given by Equation 1, typically with k_μ greater than 1.

Threshold Voltage Shift. The magnitude of the threshold voltage of both NMOS and PMOS transistors decreases approximately linearly with temperature. This shift is described by process-specific temperature coefficients (λ_N for NMOS and λ_P for PMOS) as shown in Equations 2 and 3. As temperature rises, lower threshold voltages cause transistors to turn on more easily, modifying the balance between the pull-up and pull-down strengths in the SRAM bitcell.

Negative Bias Temperature Instability (NBTI). NBTI is a long-term aging effect that increases the threshold voltage of PMOS transistors subjected to negative gate bias at elevated temperatures. In SRAM bitcells, the PMOS that stays ON longer degrades more than the other PMOS, leading to imbalance and potential reverse data-pattern imprinting, as recently shown by researchers [10]–[12]. However, it does not affect the short-term power-up behavior investigated in this study.

$$\mu(T) = \mu(T_r)\left(\frac{T}{T_r}\right)^{-k_\mu} \tag{1}$$

$$V_t^N(T) = V_t^N(T_r) - \lambda_N(T - T_r) \tag{2}$$

$$|V_t^P(T)| = |V_t^P(T_r)| - \lambda_P(T - T_r) \tag{3}$$

These temperature-dependent shifts influence the relative strength of the transistors in each SRAM cell. As a result, cells with marginal threshold mismatches may exhibit power-up state changes when temperature varies, while strongly biased cells remain stable.

E. Prior Work on Temperature Impact in SRAM PUFs

Previous studies have investigated the impact of temperature on the stability and reliability of SRAM PUFs, focusing primarily on aggregate PUF responses. Holcomb et al. [18] examined SRAM power-up behavior at three temperatures (273°K, 293°K, 323°K), showing that temperature shifts could flip the power-up state of marginally stable cells. Herrewege et al. [4] and Masoumian et al. [5] conducted further reliability analyses across various process nodes, identifying temperature as one of the main factors affecting reproducibility. Hosey et al. [6] analyzed the stability SRAM cells and interactions between neighboring SRAM cells at different temperatures. More recently, Zeinzinger et al. [19] explored the temperature sensitivity of embedded SRAM PUFs, but their work focused on overall PUF response stability rather than analyzing behavior of individual bitcells.

While these works provide valuable insights into the environmental sensitivity of SRAM PUFs, they primarily evaluated aggregated measures such as the overall intra and inter HD across a few temperature points. To the best of our knowledge, prior work has not systematically investigated whether the power-up behavior of individual SRAM bitcells at room temperature can predict their stability across a wide temperature range. This paper addresses this gap by presenting a fine-grained, per-bitcell analysis across multiple temperatures, highlighting practical implications for reducing PUF characterization efforts in resource-constrained systems.

III. Experimental Setup and Methodology

We conducted experiments on the embedded SRAM of the `MSP430F5529`, a low-power microcontroller from Texas Instruments, to characterize its power-up behavior across a wide temperature range. The embedded SRAM in `MSP430F5529` is organized into 2 KB sectors; each sector can be independently turned on or off by toggling specific control bits in the SRAM memory controller. We use **Sector-7** of SRAM that is typically reserved for a USB peripheral.

Figure 3 provides an overview of the experimental setup and flow. The experiments were carried out on five different `MSP-EXP430F5529LP` Launchpad boards, referred to as **Set-1** through **Set-5**. The SRAM power-up data are collected on a workstation connected to the Launchpads via a serial link.

The study includes three key stages:

1. **Baseline Characterization** establishes a reference PUF response at room temperature (25°C).
2. **Temperature Characterization** captures power-up behavior at multiple temperature points ranging from -15°C to 75°C.
3. **SRAM PUF Evaluation** analyzes intra- and inter-device HD across temperature variations.

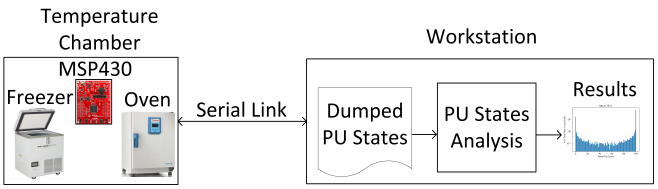

Fig. 3: Experimental Setup and Flow

Baseline Characterization. During the baseline characterization phase, the SRAM was powered up repeatedly at 25°C, and the power-up state of each bitcell was recorded. A total of 100 power cycles were performed, with each cycle consisting of the following steps:

1. Power off the SRAM.
2. Wait 5 seconds to clear remanence effects.
3. Power on the SRAM.
4. Read and store the SRAM contents.

The gPUF was generated using majority voting across 100 power-up measurements of each bit cell.

Temperature Characterization. Temperature experiments are conducted across eight temperature points: $-15°C$, $0°C$, $25°C$, $35°C$, $45°C$, $55°C$, $65°C$, and $75°C$. High-temperature experiments ($35°C$ and above) were conducted using a

Heratherm Heating and Drying Oven, and low-temperature experiments ($-15°$C and $0°$C) were performed using a *SO-LOW FDC-4000 Ultralow Cooling Chamber*. For each temperature point, the following procedure is followed:

1. Stabilize the test environment at the target temperature.
2. Perform 100 power-up cycles, following the same sequence as the baseline characterization.
3. Capture and store the SRAM power-up states for analysis.

SRAM PUF Evaluation. The gold PUF responses generated at room temperature were used as references. The power-up states collected during the temperature characterization formed the authentication PUF (aPUF) responses. To increase the number of comparisons and evaluate response randomness at a finer granularity, the 16,384-bit memory block is divided into 16 logical devices, each 1,024 bits in size. Given that there are 5 sets, each containing 16 logical devices, the total number of logical devices included in this analysis is 80.

Two primary metrics were used to evaluate SRAM PUF stability: HD and Entropy. HD quantifies the bit-level difference between two responses (see Equation 4 where A_i and B_i represent the i-th bit of bitstrings A and B, respectively). Intra-device HD was computed by comparing the aPUF responses at each temperature with the corresponding gPUF (see Equation 5). Inter-device HD was computed by comparing gPUF responses across different logical devices to assess uniqueness (see Equation 6).

Entropy measures the randomness of the PUF response. Entropy was calculated for each logical device and used to assess the unpredictability of the bit patterns. It is given by the equation 7 where P_0 is the probability of zeros and P_1 is the probability of ones in a given bitstring. High entropy indicates strong randomness, a desirable property in security applications.

$$HD(A,B) = \frac{\sum_{i=1}^{n}(A_i \oplus B_i)}{Number\ of\ Total\ Bits} \times 100\% \quad (4)$$

$$HD_{\text{intra}} = HD(aPUF_{\text{LogicalDevice-}i}, gPUF_{\text{LogicalDevice-}i}) \quad (5)$$

$$HD_{\text{inter}} = HD(aPUF_{\text{LogicalDevice-}i}, gPUF_{\text{LogicalDevice-}j}) \quad \text{where } i \neq j \quad (6)$$

$$Entropy = -P_0 \times \log_2 P_0 - P_1 \times \log_2 P_1 \quad (7)$$

IV. Results and Discussion

A. Baseline Characterization

We first measured the power-up behavior of each SRAM bitcell at room temperature by counting how often each cell initialized to logic '1' over 100 power-up cycles. We refer to this metric as the power-up count (PUC). This measurement characterizes the bias of each cell during power-up at $25°$C.

Figure 4 shows the distribution of the PUC values for all bitcells in Set-1, plotted on a logarithmic scale. The x-axis represents the PUC values (0-100), while the y-axis shows the proportion of bitcells that exhibit each PUC value. The distribution is bimodal, indicating that most cells consistently power up as either '0' or '1.' An asymmetric bias toward the '1' state is observed, with approximately 71% of cells favoring that state when majority voting is used. Specifically, ($\sim$ 63%) of bitcells consistently powered up as '1' and ($\sim$ 20%) consistently power up as '0', while only about only $\sim$1% of bitcells showed no strong preference. The results suggest that the power up SRAM state in MSP430 is not balanced between '0' and '1.' The circuit design and process variations favor the logic '1' power-up state. This finding is consistent across all evaluated sets.

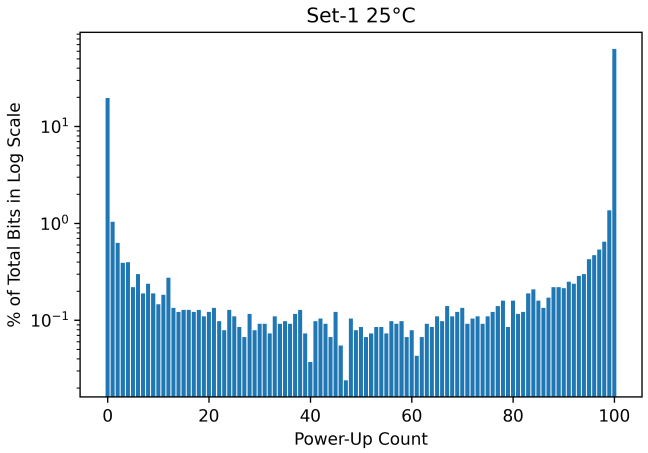

Fig. 4: SRAM Bitcell Power-Up Probability Distribution (Log Scale, 25°C) for Set-1

To better interpret this behavior, we categorized the bitcells into five groups based on their PUC values::

- **Strong '1' (S1)**: PUC = 81–100.
- **Weak '1' (W1):** PUC = 61–80.
- **Unstable (U):** PUC = 41–60.
- **Weak '0' (W0):** PUC = 21–40.
- **Strong '0' (S0):** PUC = 0–20.

Table II summarizes the distribution of these categories across all bitcells in all sets, by reporting the maximum, median, and minimum. The majority of bitcells fall into the strongly biased categories, with approximately ($\sim$69.5%) in S1 and ($\sim$25%) in S0. The remaining cells are distributed among W0, U, and W1, representing a small fraction of the array.

TABLE II: Categorized SRAM Power-Up State Distribution at 25°C

Bit-cell Category	Percentage of Total Bits		
	Max (%)	Median (%)	Min (%)
S0	27.11	24.81	24.20
W0	2.07	1.92	1.81
U	1.76	1.69	1.65
W1	2.27	2.16	2.09
S1	70.13	69.47	66.86

To visualize spatial distribution, Figure 5 shows a bitmap of the categorized bitcells, arranged in a 128x128 grid. Localized clusters of S1 and S0 cells are apparent, suggesting some

spatial correlation in process variations. In contrast, cells in the W0, U, and W1 categories appear randomly distributed, forming a 'salt and pepper' pattern with no apparent structure. These marginally stable cells contribute to the overall unpredictability of the SRAM power-up state.

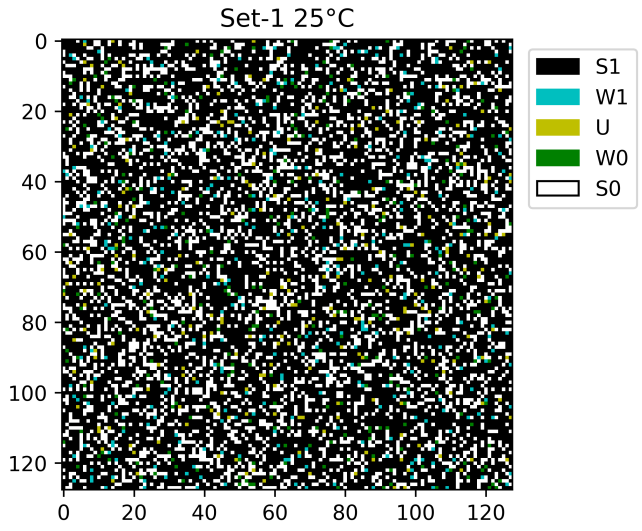

Fig. 5: SRAM Bitcell Categorization Bitmap for Set-1 at $25°C$

B. Temperature Characterization

PUC was measured and bitcells were categorized at each temperature point using the same methodology described in the baseline characterization. Table III shows the percentage distribution of SRAM bitcell categories for Set-1 across the full temperature range ($-15°C$, $75°C$). These results demonstrate that the SRAM power-up state is highly deterministic, with most cells consistently favoring either '0' or '1.' Temperature variations have only a minor effect on the overall category distribution. The proportion of W0, W1, and U cells remains relatively small and constant at all temperatures.

We observe slight temperature-dependent behavior, as follows. As temperature increases, the percentage of cells in the S0 category gradually decreases and in the S1 category gradually increases. This trend likely reflects the influence of temperature on threshold voltage asymmetry. The same characterization was performed on Sets 2 through 5, and the results were consistent with those observed in Set-1.

TABLE III: Categorized SRAM Power-Up State Distribution at all temperatures for Set-1

Categories	-15°C	0°C	25°C	35°C	45°C	55°C	65°C	75°C
S0	26.71	25.93	24.81	24.43	24.13	23.82	23.60	23.46
W0	1.78	1.78	1.90	2.06	2.08	2.02	2.06	2.20
U	1.48	1.78	1.65	1.71	1.83	2.06	2.12	2.01
W1	2.12	2.13	2.17	2.14	2.15	2.12	2.25	2.35
S1	67.91	68.38	69.47	69.67	69.82	69.97	69.97	69.98

Approximately 87% bitcells retain their original category across all temperature points and devices, indicating strong temperature immunity. Table IV summarizes the proportion of bitcells in each category that experience a state change relative to their room-temperature classification. The most significant shifts occur in marginal categories (W0, U, W1), which are more sensitive to temperature due to their weaker threshold voltage mismatches. In contrast, strongly biased S1 and S0 cells exhibit minimal variation.

These results confirm that temperature effects primarily impact marginally stable cells, while the majority of bitcells maintain consistent power-up states. The small proportion of temperature-sensitive cells suggests that temperature-induced variability in SRAM PUF responses is predictable and limited in scope.

TABLE IV: Categorical SRAM Power-Up State Impact with Temperature Variations

Bit-cell Category	**Change w.r.t. Room Temperature**		
	Max (%)	**Median (%)**	**Min (%)**
S0	14.84	14.20	12.90
W0	99.12	98.65	98.07
U	99.63	99.28	98.24
W1	99.19	97.46	96.82
S1	6.98	6.19	4.99

C. SRAM PUF Evaluation

We first analyzed the entropy of the collected PUF responses using Equation 7, since the power-up states exhibit a bias towards logic '1'. The entropy across all logical devices ranged from approximately 0.7 to 0.95, with a peak near 0.85. These results confirm that the raw power-up data maintain a strong level of randomness without applying any debiasing techniques.

We evaluated the reproducibility and uniqueness of SRAM PUF responses by comparing gPUFs and aPUFs captured at room temperature across all five sets. Intra HD (Equation 5) measured the similarity between responses from the same logical device, while inter HD (Equation 6) quantified the difference between responses from different logical devices. Ideally, intra HD is 0% and inter HD is near 50%, but marginally stable bitcells introduce some mismatch at room temperature.

Figure 6 shows a clear separation between intra and inter HD distributions. Intra HD is tightly clustered near 0%, indicating strong reproducibility, while inter HD centers around 40%, confirming device-level uniqueness. This separation supports reliable threshold-based authentication.

We further investigated how temperature affects intra and inter HD. For intra HD analysis, 100 aPUFs were captured at each temperature point and compared to the room-temperature gPUF. Across 80 logical devices in five different boards, this produced 8,000 comparisons per temperature point. For inter HD, comparisons were made as follows. Each gPUF from Logical Device-1 on a given board was compared against all aPUFs from other logical devices on the same board and from all logical devices on the other four boards. Each gPUF was

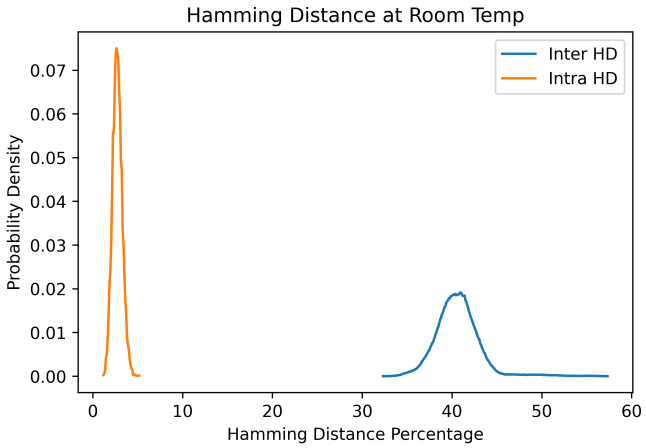

Fig. 6: Inter and Intra HD at Room Temperature

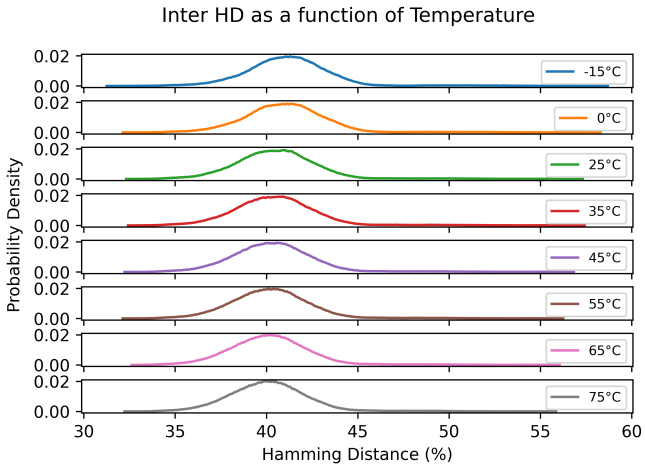

Fig. 8: Inter HD as a Function of Temperature

thus compared against (15 × 100 + 4 × 16 × 100) aPUFs, ensuring comprehensive evaluation.

Figure 7 shows that intra HD slightly increases with temperature deviations, with the most significant shift and broadening occurring at $-15°\mathrm{C}$, indicating greater instability in marginally stable cells.

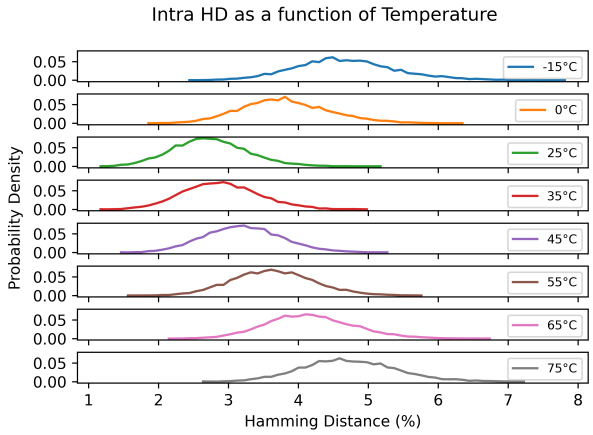

Fig. 7: Intra HD as a Function of Temperature

In contrast, Figure 8 demonstrates that inter HD remains largely consistent across temperatures. Notably, its peak shifts rightward $0°\mathrm{C}$ and $-15°\mathrm{C}$, enhancing distinctiveness between logical devices, though the left tail broadens slightly.

In summary, the highest intra HD value remains below 8%, while the lowest inter HD exceeds 30% across all temperatures, maintaining a clear and distinguishable gap. These results demonstrate that room-temperature power-up characterization of this SRAM PUF implementation is sufficient to maintain reliable authentication performance across a wide temperature range.

D. Discussion

Our baseline characterization shows that most SRAM bitcells exhibit a strong bias toward either '0' or '1' state. This suggests substantial threshold voltage mismatches between transistors in each cell, as outlined in Table I. Bitcells categorized as W0, U and W1 have weaker threshold voltage mismatches, leading to less stable power-up behavior. These marginally stable cells represent a small fraction of the total SRAM array and primarily contribute to the intra HD observed at room temperature.

Temperature characterization further supports these observations. Across the tested temperature range, approximately 87% of the bitcells retained their initial power-up category, with most of these cells belong to strongly biased S1 or S0 categories. This aligns with the baseline results, indicating that temperature variations do not significantly impact cells with strong threshold voltage mismatches.

The primary mechanism driving temperature-induced changes in SRAM power-up states is the temperature dependence of threshold voltage described in Equations 2 and 3. Carrier mobility degradation, which affects PMOS and NMOS transistors similarly, contributes minimally to power-up state changes. NBTI is a long-term aging effect and was not a factor in our short-term experiments.

In most strongly-biased bitcells, the threshold voltage temperature coefficients (λ_N in Equation 2 and λ_P in Equation 3) remain closely matched between the paired transistor in the cross-coupled inverters (Figure 2b). This matching preserves the cells' preferred power-up state across temperatures. The state of strongly-biased bitcells can be flipped only if λ_{N1} and λ_{N2} or λ_{P1} and λ_{P2} pairs have significant differences. However, in marginally stable bitcells, even small differences in these coefficients can shift the balance, causing occasional state flips.

The intra HD variations observed at different temperatures correlate with the proportion of W0, U and W1 bitcells identified in the baseline characterization (Table II). These categories are most susceptible to temperature-driven threshold voltage shifts, explaining their contribution to power-up instability.

The inter HD remains relatively stable across all temperatures because logical devices within same physical devices are independent of one another because of within-die process variations and logical devices between different physical devices are independent because of die-to-die process variations. Temperature variations will have little or no impact on their hamming distances.

E. Limitation and Future Work

We acknowledge the limitation that our study did not involve other family of devices or stand-alone SRAM chips other than embedded SRAM of `MSP430F5529`.

Future work should explore how the impact of temperature changes with technology node and should involve broader range of devices or stand-alone SRAM chips. Expanding the study will help us further investigate whether the impact of temperature on SRAM PUF follows the same pattern as observed here.

V. Conclusion

The extensive characterization of SRAM power-up behavior across temperatures provides key insights into its stability and implications for PUF applications. By quantifying per-bitcell PU stability, this study establishes a framework for inferring the expected behavior of SRAM PUFs under temperature variations from baseline characterization alone. The consistency observed across all five device sets, suggests that devices from the same family exhibit similar stability characteristics, regardless of lot number. This finding indicates that a reduced number of sample devices may be sufficient for characterization without compromising overall conclusions.

The analysis confirms that only a small fraction of bitcells exhibit random or unstable behavior. Approximately 92% of S1 bitcells and 87% of S0 bitcells maintained their state across all tested temperatures. Since S1 and S0 categories together represent roughly 94% of the total bitcells, the overall repeatability of power-up states is high. This conclusion is further supported by the low intra Hamming Distances observed between gPUFs and aPUFs.

These findings demonstrate that characterizing a single device at room temperature is sufficient to infer broader stability trends across a wide temperature range. Furthermore, the results suggest that room-temperature power-up states can be used directly as PUF responses without applying post-processing techniques such as hashing or debiasing, enabling practical, low-cost device authentication schemes.

References

[1] F. Wilde, "Large scale characterization of SRAM on Infineon XMC microcontrollers as PUF," in *Proceedings of the Fourth Workshop on Cryptography and Security in Computing Systems*. New York, NY, USA: Association for Computing Machinery, 2017, p. 13–18. [Online]. Available: https://doi.org/10.1145/3031836.3031839

[2] H. Handschuh, "Hardware-Anchored Security Based on SRAM PUFs, Part 1," *IEEE Security and Privacy*, vol. 10, no. 3, pp. 80–83, 2012.

[3] ——, "Hardware-Anchored Security Based on SRAM PUFs, Part 2," *IEEE Security and Privacy*, vol. 10, no. 4, pp. 80–81, 2012.

[4] A. Van Herrewege, V. van der Leest, A. Schaller, S. Katzenbeisser, and I. Verbauwhede, "Secure PRNG seeding on commercial off-the-shelf microcontrollers," in *Proceedings of the 3rd International Workshop on Trustworthy Embedded Devices*. New York, NY, USA: Association for Computing Machinery, 2013, p. 55–64. [Online]. Available: https://doi.org/10.1145/2517300.2517306

[5] S. Masoumian, G. Selimis, R. Wang, G.-J. Schrijen, S. Hamdioui, and M. Taouil, "Reliability Analysis of FinFET-Based SRAM PUFs for 16nm, 14nm, and 7nm Technology Nodes," in *2022 Design, Automation and Test in Europe Conference and Exhibition (DATE)*, 2022, pp. 1189–1192.

[6] A. Hosey, M. T. Rahman, K. Xiao, D. Forte, and M. Tehranipoor, "Advanced Analysis of Cell Stability for Reliable SRAM PUFs," in *2014 IEEE 23rd Asian Test Symposium*, 2014, pp. 348–353.

[7] P. Urien, "Innovative ATMEGA8 Microcontroler Static Authentication Based on SRAM PUF," in *2020 IEEE 17th Annual Consumer Communications and Networking Conference (CCNC)*, 2020, pp. 1–2.

[8] A. T. Elshafiey, P. Zarkesh-Ha, and J. Trujillo, "The effect of power supply ramp time on SRAM PUFs," in *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2017, pp. 946–949.

[9] U. Surendranathan, H. Wilson, L. R. Cao, A. Milenkovic, and B. Ray, "Analysis of SRAM PUF Integrity Under Ionizing Radiation: Effects of Stored Data and Technology Node," *IEEE Transactions on Nuclear Science*, vol. 71, no. 4, pp. 485–491, 2024.

[10] J. Hovanes, Y. Zhong, and U. Guin, "Beware of Discarding Used SRAMs: Information is Stored Permanently," in *2022 IEEE Physical Assurance and Inspection of Electronics (PAINE)*, 2022, pp. 1–7.

[11] A. Santana-Andreo, P. Saraza-Canflanca, H. Carrasco-Lopez, R. Castro-Lopez, E. Roca, and F. V. Fernandez, "A detailed, cell-by-cell look into the effects of aging on an SRAM PUF using a specialized test array," in *2023 19th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, 2023, pp. 1–4.

[12] Z. Guo, X. Xu, M. T. Rahman, M. M. Tehranipoor, and D. Forte, "SCARe: An SRAM-Based Countermeasure Against IC Recycling," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 4, pp. 744–755, 2018.

[13] C. Herder, M.-D. Yu, F. Koushanfar, and S. Devadas, "Physical Unclonable Functions and Applications: A Tutorial," *Proceedings of the IEEE*, vol. 102, no. 8, pp. 1126–1141, 2014.

[14] B. Gassend, D. Clarke, M. van Dijk, and S. Devadas, "Silicon physical random functions," in *Proceedings of the 9th ACM Conference on Computer and Communications Security*. New York, NY, USA: Association for Computing Machinery, 2002, p. 148–160. [Online]. Available: https://doi.org/10.1145/586110.586132

[15] G. E. Suh and S. Devadas, "Physical unclonable functions for device authentication and secret key generation," in *Proceedings of the 44th Annual Design Automation Conference*. New York, NY, USA: Association for Computing Machinery, 2007, p. 9–14. [Online]. Available: https://doi.org/10.1145/1278480.1278484

[16] P. A. Layman, S. Chaudhry, J. G. Norman, and J. R. Thomson, "ELECTRONIC FINGERPRINTING OF SEMICONDUCTOR INTEGRATED CIRCUITS, Patent 6,738,294," *United States Patent*, 2004.

[17] D. E. Holcomb, W. P. Burleson, K. Fu *et al.*, "Initial SRAM state as a fingerprint and source of true random numbers for RFID tags," in *Proceedings of the Conference on RFID Security*, vol. 7, no. 2, 2007, p. 01.

[18] D. E. Holcomb, W. P. Burleson, and K. Fu, "Power-Up SRAM State as an Identifying Fingerprint and Source of True Random Numbers," *IEEE Transactions on Computers*, vol. 58, no. 9, pp. 1198–1210, 2009.

[19] M. Zeinzinger, J. Langer, F. Eibensteiner, P. Petz, L. Drack, D. Dorfmeister, and R. Ramler, "Comparative Analysis of SRAM PUF Temperature Susceptibility on Embedded Systems," in *2023 International Conference on Electrical, Computer and Energy Technologies (ICECET)*, 2023, pp. 1–8.