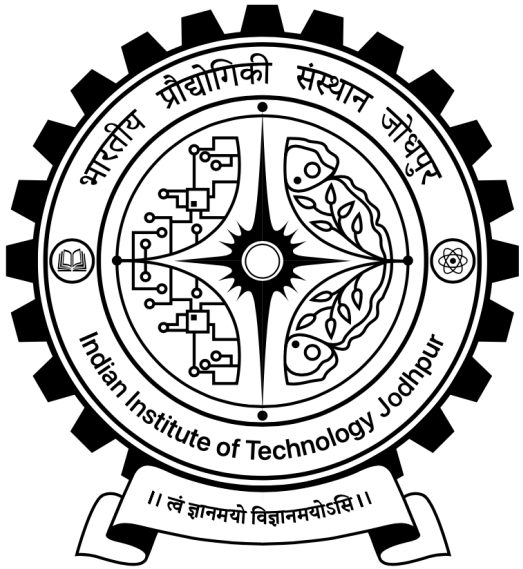


# Computer Architecture
# CSL3020

Deepak Mishra

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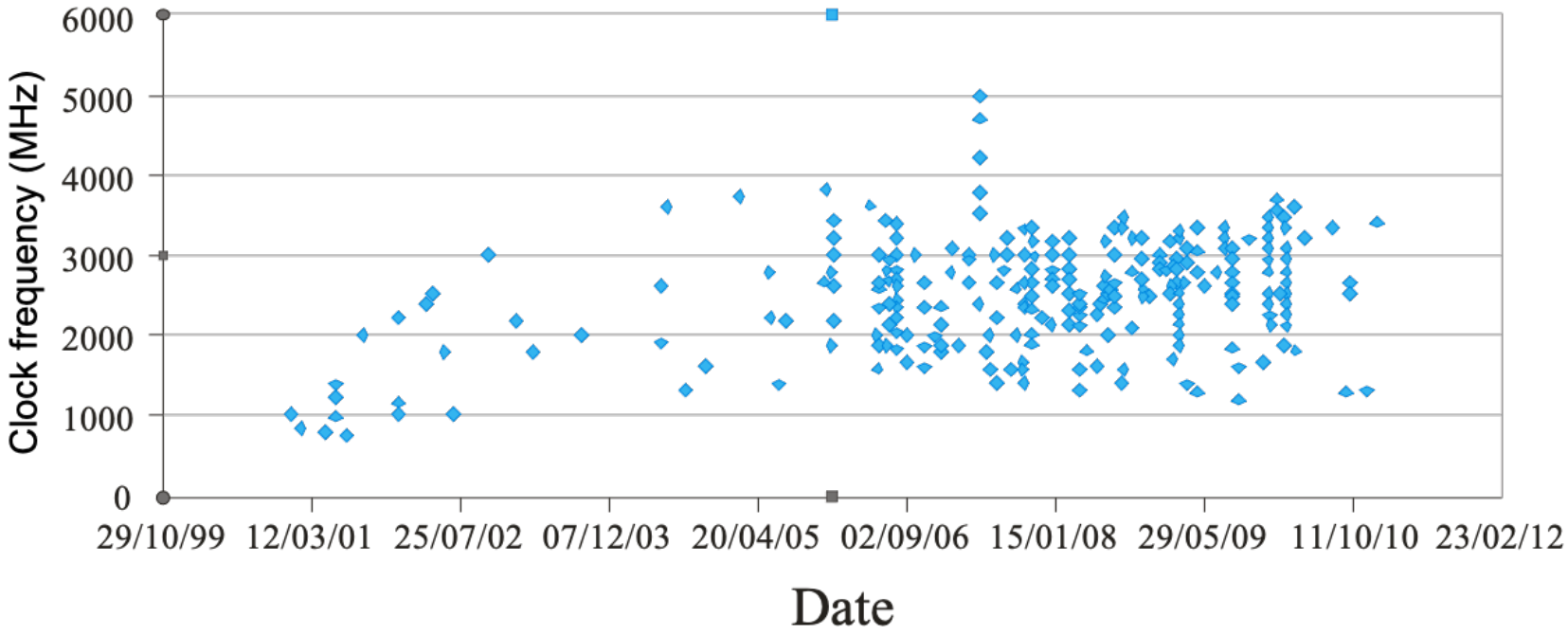
Department of Computer Science and Engineering
Indian Institute of Technology Jodhpur

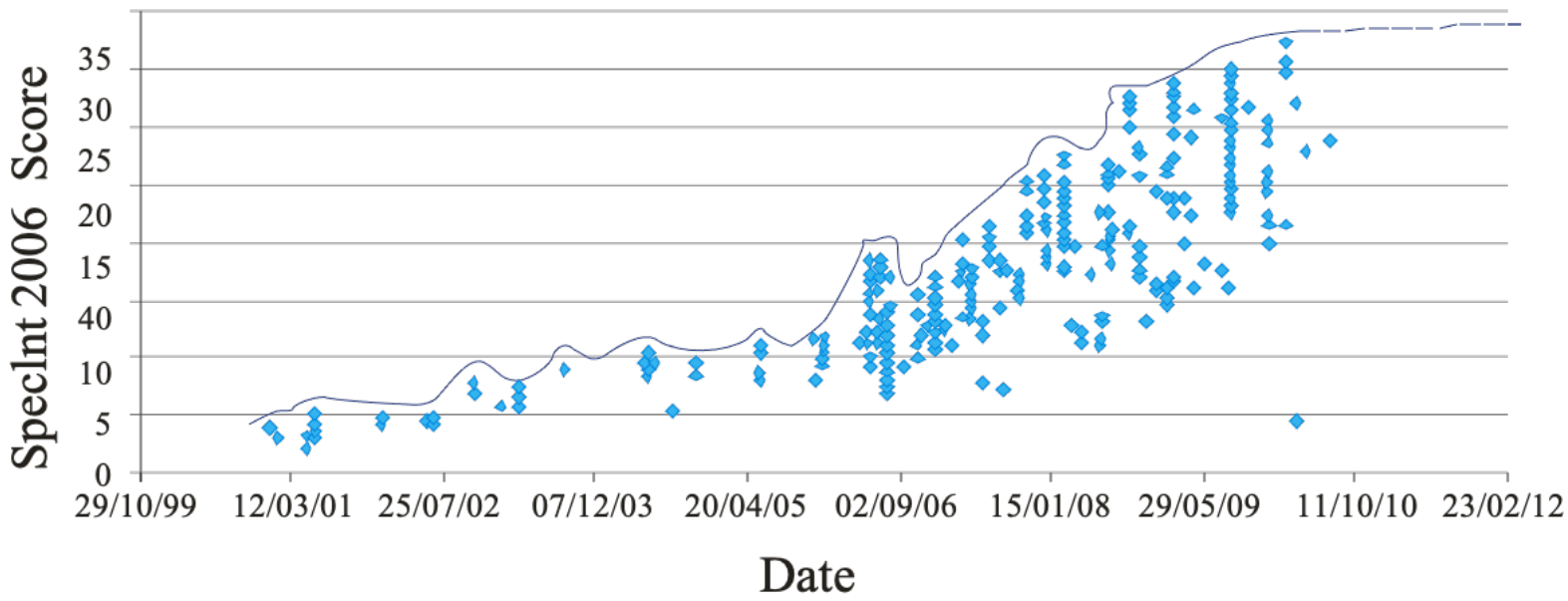
# Multicore Architecture




Clock frequency saturation.

Source: Basic Computer Architecture by SR Sarangi

# Multicore Architecture




Performance saturation.

Source: Basic Computer Architecture by SR Sarangi

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- This is a generic definition, and it can refer to multiple processors in the same chip, or processors across different chips.

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- This is a generic definition, and it can refer to multiple processors in the same chip, or processors across different chips.
- A multicore processor is a specific type of multiprocessor that contains all of its constituent processors in the same chip. Each such processor is known as a **core**.

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Ans. 5.5, 10

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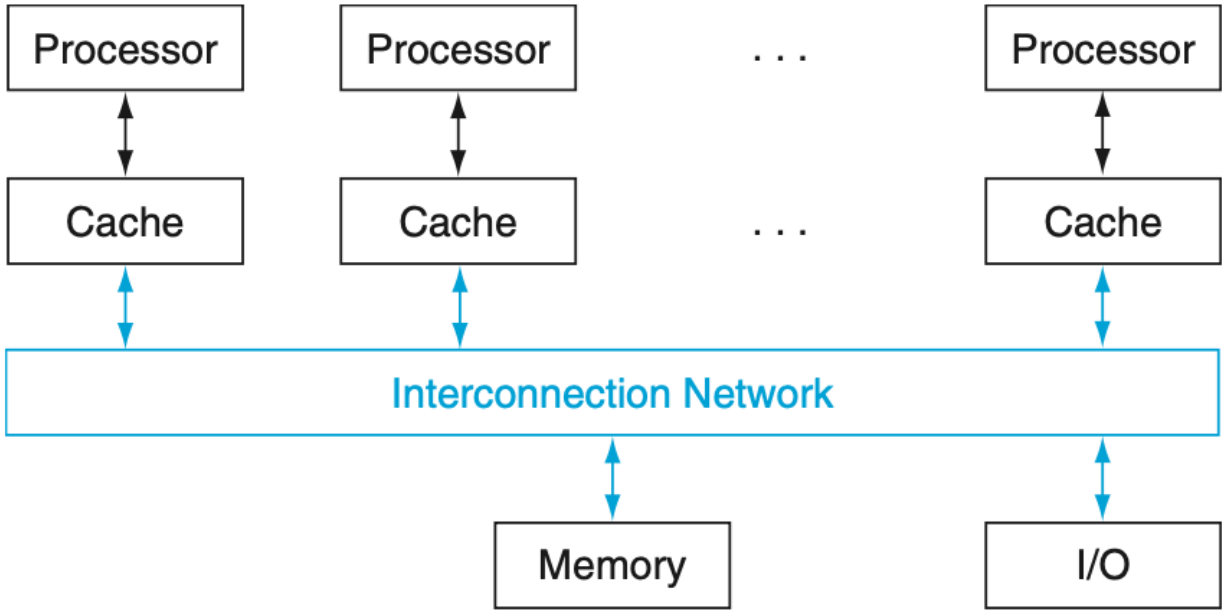
A shared memory multiprocessor (SMP) is one that offers the programmer a single physical address space across all processors.



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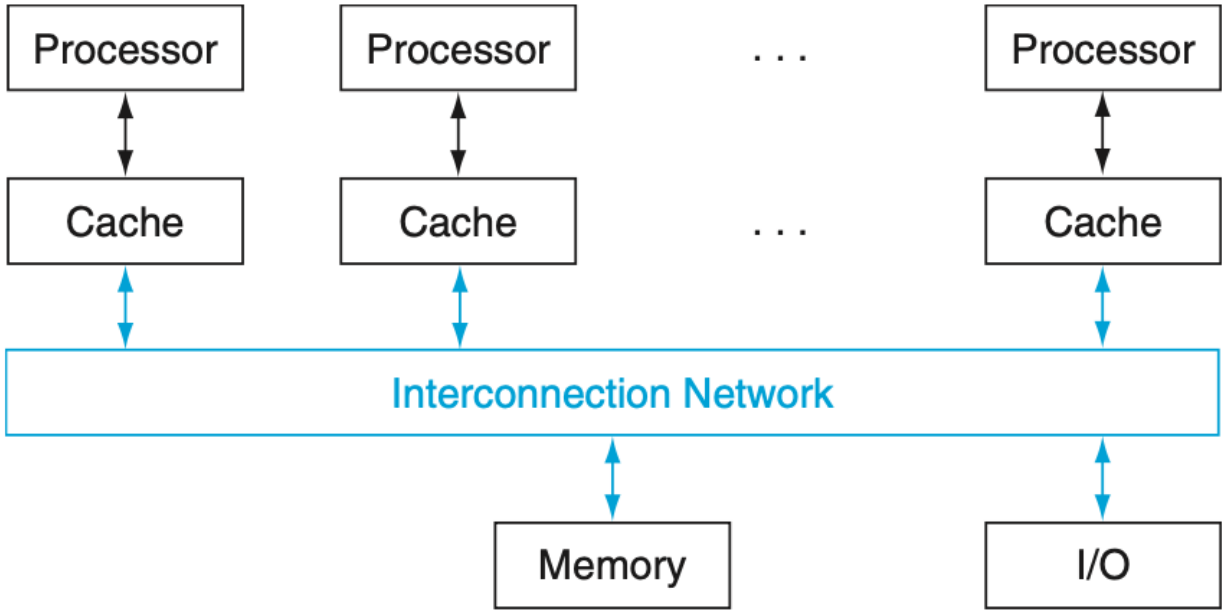


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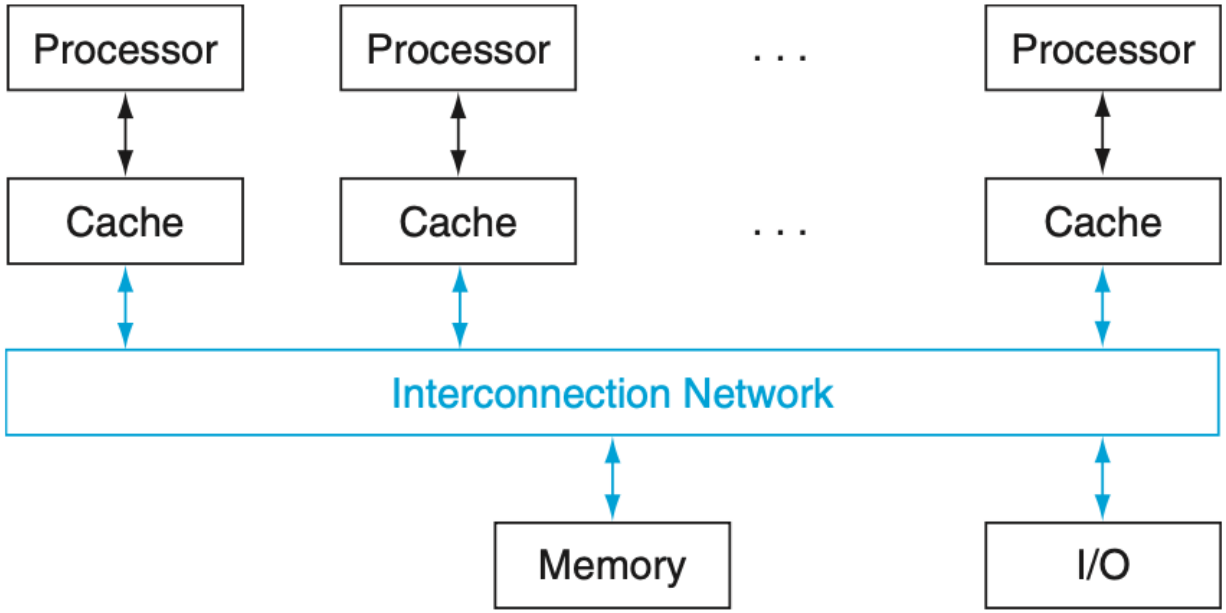
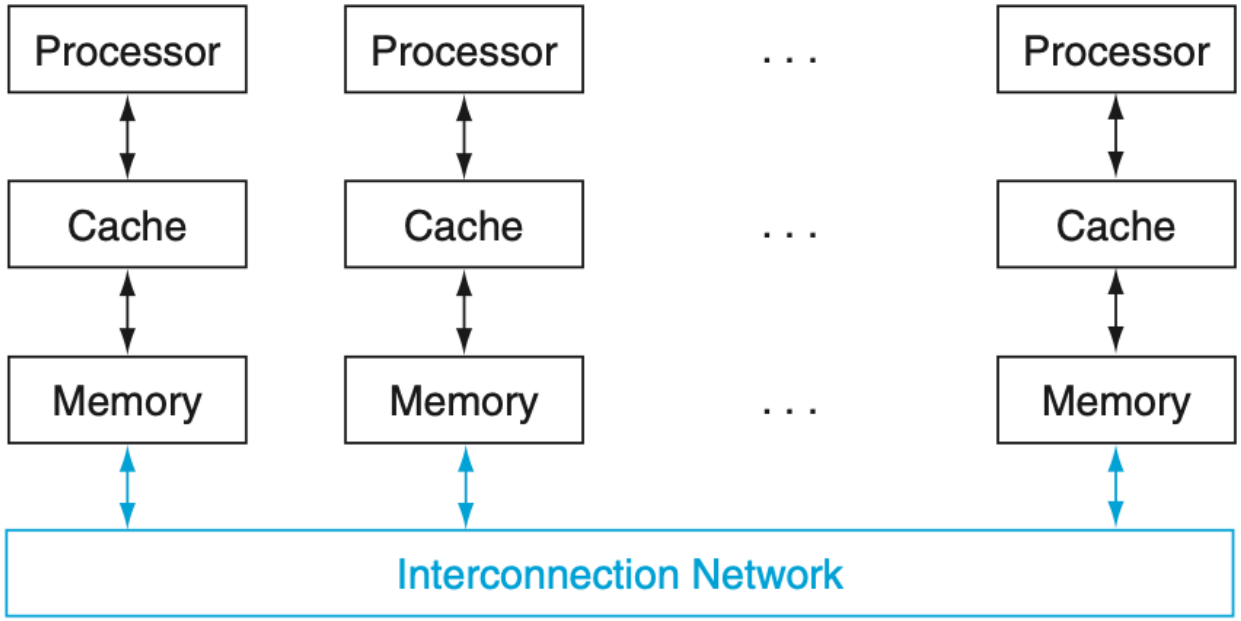



Processors communicate through shared variables in memory.

Uniform Memory Access (UMA) vs. Nonuniform Memory Access (NUMA)

# Message-Passing Multiprocessors

Each processor has its own private physical address space.

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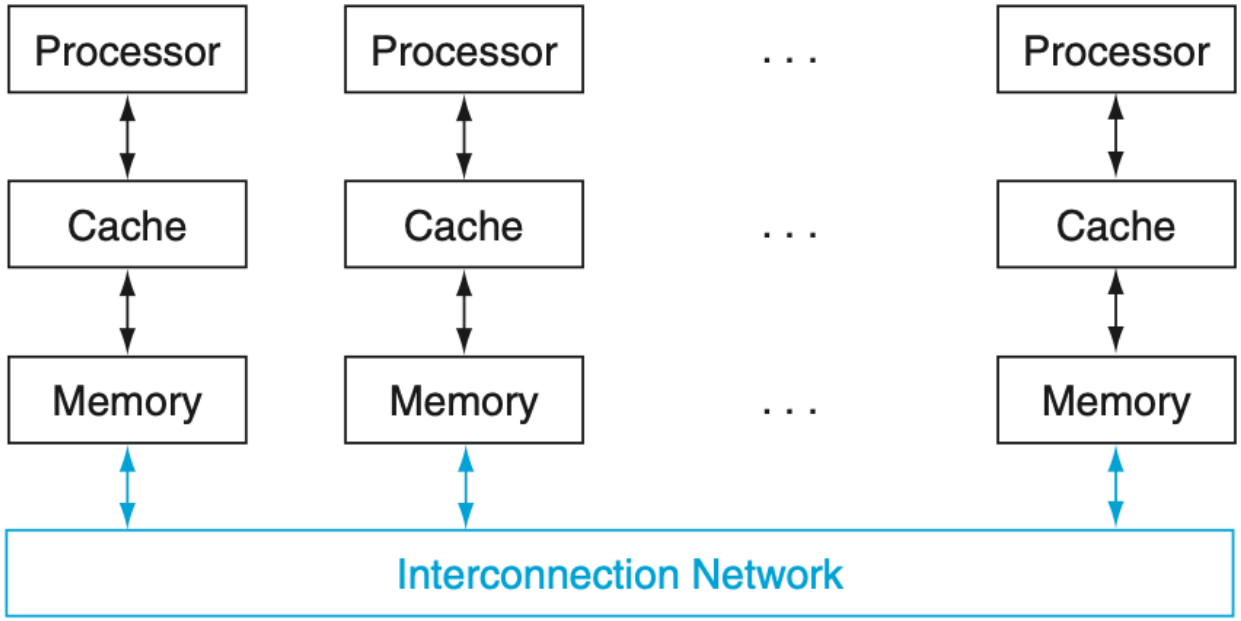


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High-performance computing (HPC) clusters commonly use message passing.

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The next step is to get the sum of each subset.

```
sum = 0;
for (i = 0; i<1000; i = i + 1) /* loop over each array */
 sum = sum + AN[i];  /* sum the local arrays */
```

The last step is the reduction that adds these 100 partial sums.

```
limit = 100; half = 100;/* 100 processors */
repeat
  half = (half+1)/2; /* send vs. receive dividing line*/
  if (Pn >= half && Pn < limit) send(Pn - half, sum);
  if (Pn < (limit/2)) sum = sum + receive();
  limit = half; /* upper limit of senders */
until (half == 1); /* exit with final sum */
```

# Multiple Instruction and Data Streams

- **SISD:** A standard uniprocessor.
- **SIMD:** Single Instruction, Multiple Data. Vector processor.
- **MISD:** Multiple Instruction, Single Data. Rarely used.
- **MIMD:** Multiple Instruction, Multiple Data. Generally used in Single Program Multiple Data (SPMD) form.

# Vector Processors

- A vector instruction operates on arrays of data.

Source: Basic Computer Architecture by SR Sarangi

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- MMX, SSE1, SSE2, SSE3, SSE4, and AVX instruction sets for x86 processors.

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# Vector Processors

MIPS code for $Y = a \times X + Y$

```
l.d      $f0,a($sp)      ;load scalar a
lv       $v1,0($s0)      ;load vector x
mulvs.d  $v2,$v1,$f0     ;vector-scalar multiply
lv       $v3,0($s1)      ;load vector y
addv.d   $v4,$v2,$v3     ;add y to product
sv       $v4,0($s1)      ;store the result
```