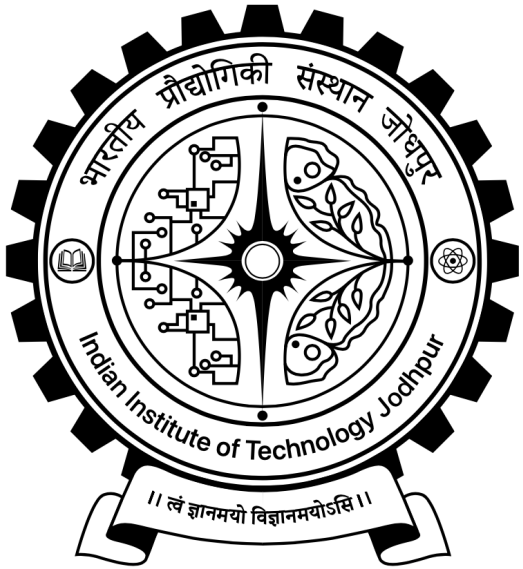

Computer Architecture
CSL3020

Deepak Mishra

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Department of Computer Science and Engineering
Indian Institute of Technology Jodhpur

Overview of Memory System

Story so far –

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All our programs take less than 4 GB of space.

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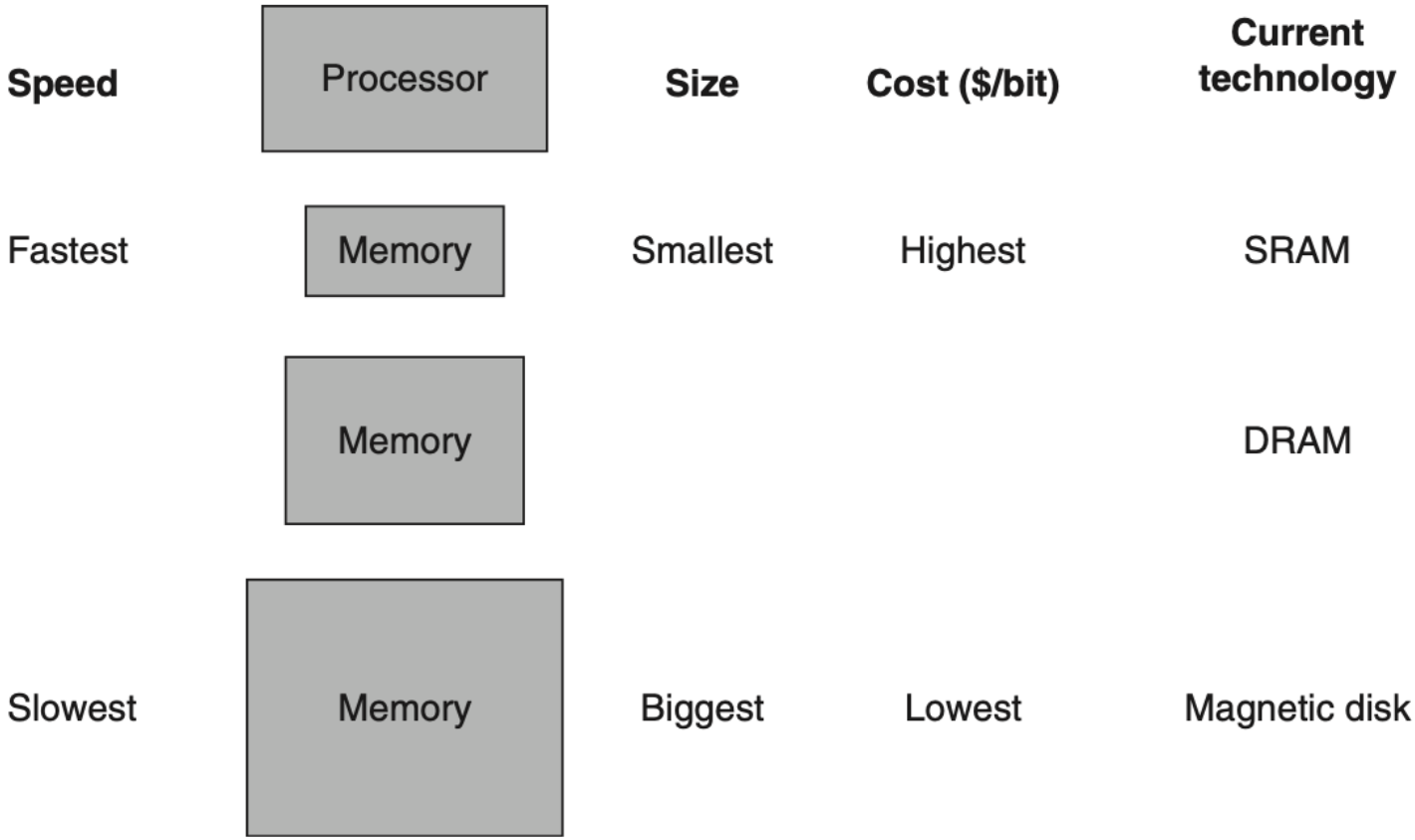

Area, power, latency trade-off

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Spatial locality: The principle stating that if a data location is referenced, data locations with nearby addresses will tend to be referenced soon.

Overview of Memory System

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- Hit rate: The fraction of memory accesses found in the upper level.
- Miss rate = 1 - hit rate
- Miss penalty: It is the time taken to transfer data from lower level to upper level, plus the hit time.

How to take the advantage of spatial locality?

Overview of Memory System

How to take the advantage of spatial locality?

Group memory addresses into blocks and transfer blocks between the levels in memory hierarchy instead of transferring single byte.

- Block: The minimum unit of information that can be either present or not present in the two-level hierarchy is called a block or a line.

Basics of Cache

Using main memory (RAM) for the IM and DM units of the processor we design is inefficient.

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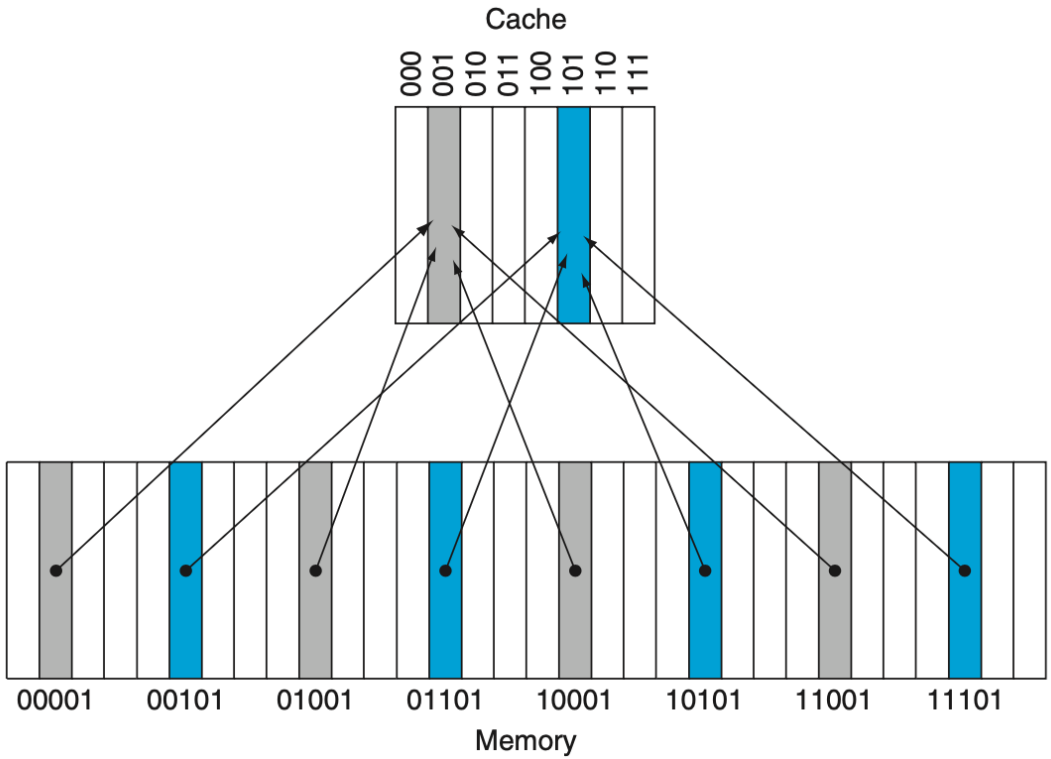
We need a mapping scheme to answer these questions.

Basics of Cache

Direct mapping: Each (main) memory location is mapped to exactly one location in the cache.

Cache location = (Block address) modulo (Number of blocks in the cache)



Basics of Cache

As multiple addresses are mapped to a single cache location, the referenced address is divided into two fields:

- *Tag:* contains the address information required to identify associated block
- *Cache index:* used to select the block

The index of a cache block, together with the tag, uniquely specifies the corresponding memory address.

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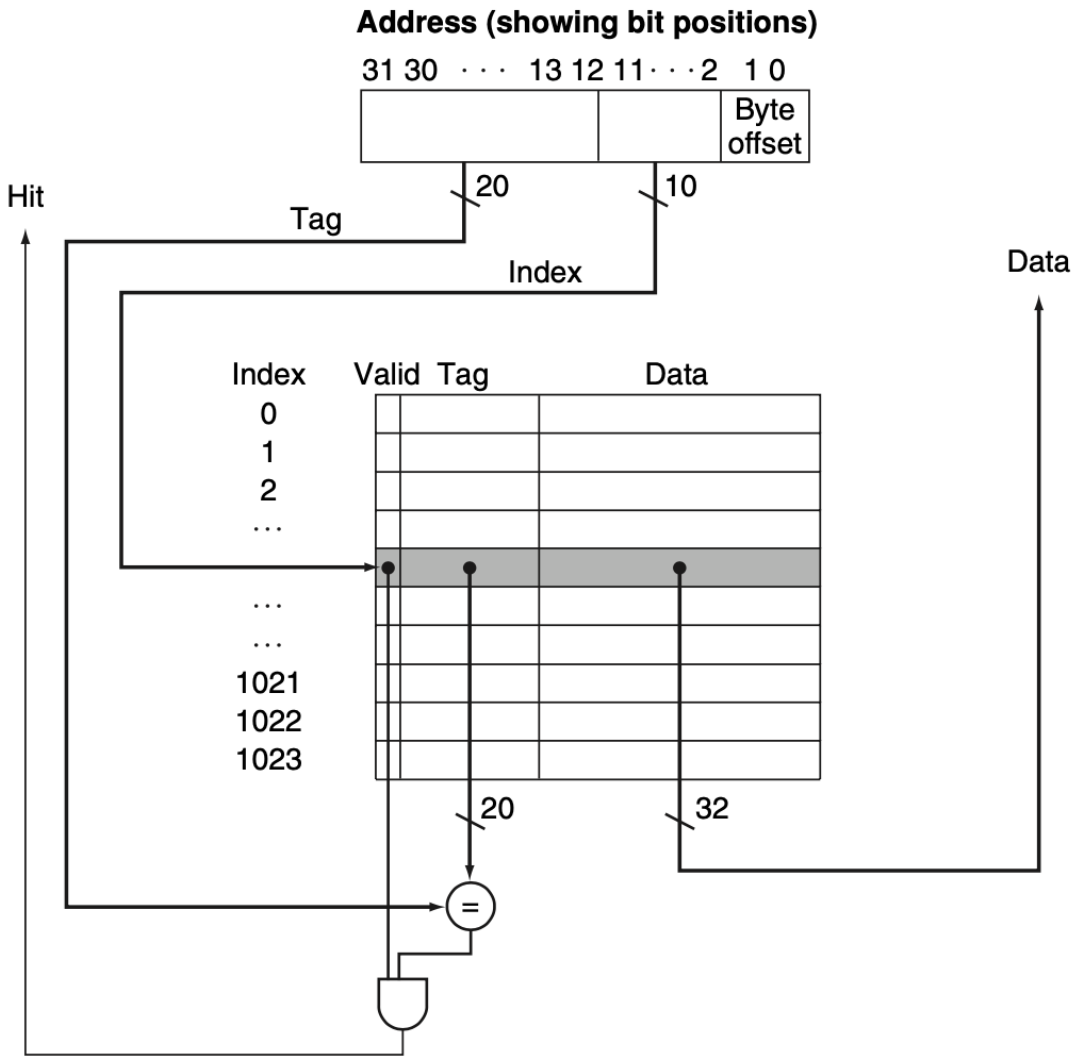
Valid bit: A field in the tables of a memory hierarchy that indicates that the associated block in the hierarchy contains valid data.

Example:

Binary address of reference	Hit or miss in cache	Assigned cache block (where found or placed)
10110_{two}	miss (5.6b)	$(10110_{two} \bmod 8) = 110_{two}$
11010_{two}	miss (5.6c)	$(11010_{two} \bmod 8) = 010_{two}$
10110_{two}	hit	$(10110_{two} \bmod 8) = 110_{two}$
11010_{two}	hit	$(11010_{two} \bmod 8) = 010_{two}$
10000_{two}	miss (5.6d)	$(10000_{two} \bmod 8) = 000_{two}$
00011_{two}	miss (5.6e)	$(00011_{two} \bmod 8) = 011_{two}$
10000_{two}	hit	$(10000_{two} \bmod 8) = 000_{two}$
10010_{two}	miss (5.6f)	$(10010_{two} \bmod 8) = 010_{two}$
10000_{two}	hit	$(10000_{two} \bmod 8) = 000_{two}$

Index	V	Tag	Data
000	N		
001	N		
010	N		
011	N		
100	N		
101	N		
110	N		
111	N		

Cache Misses



Assuming that the block size is one word and address is 32 bit long

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Ans: 147 Kbits

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4. Restart the instruction execution at the first step.

Cache Misses

The control of the cache on a data access is essentially identical: on a miss, we simply stall the processor until the memory responds with the data.

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- *Write buffer:* A queue that holds data while the data is waiting to be written to memory.
- *Write-back:* Updating values only to the block in the cache, then writing the modified block to the lower level of the hierarchy when the block is replaced.

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Example: Assume the miss rate of an instruction cache is 2% and the miss rate of the data cache is 4%. If a processor has a CPI of 2 without any memory stalls and the miss penalty is 100 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. Assume the frequency of all loads and stores is 36%.

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Ans: 2.72 times

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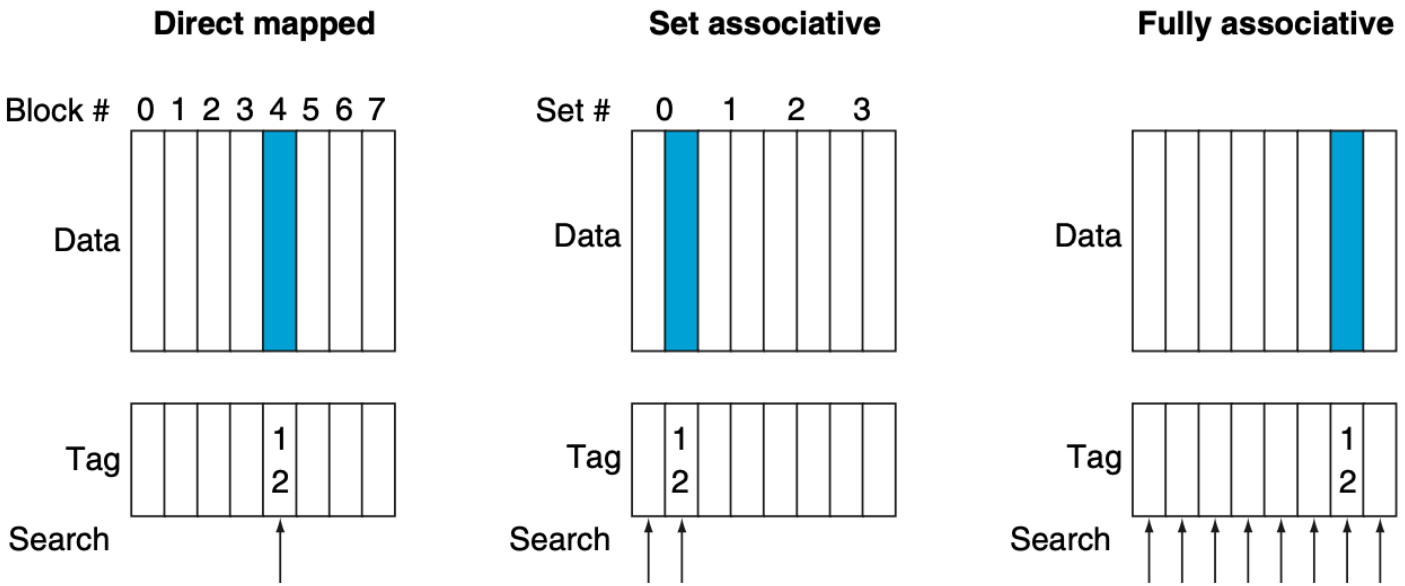

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Example: Assume there is a small cache consisting of eight one-word blocks. Given the following sequence of block addresses: 0, 8, 0, 5, 12, 9, 1, 5, and 8, find the number of misses for 2-way, 4-way, and 8-way set-associative mapping with LRU replacement scheme.

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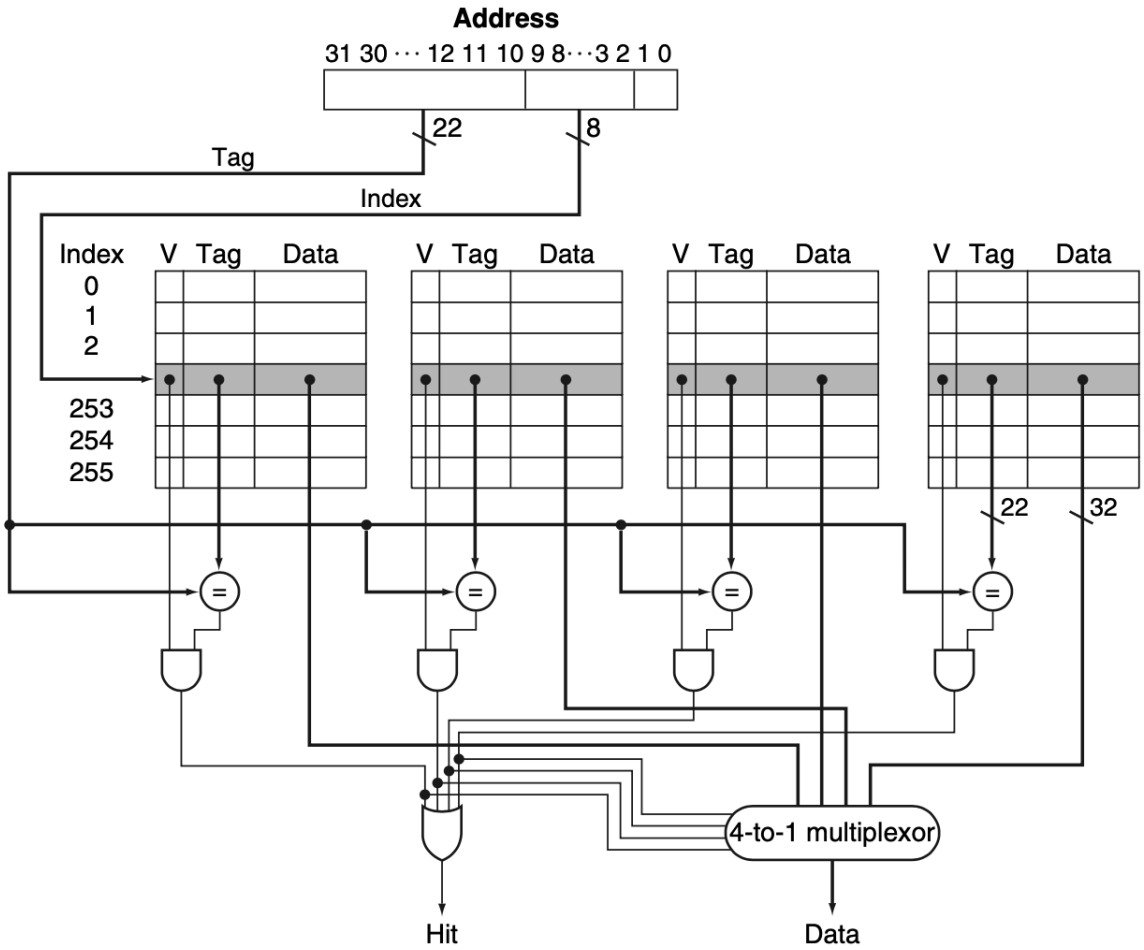
Ans: 8, 6, 6

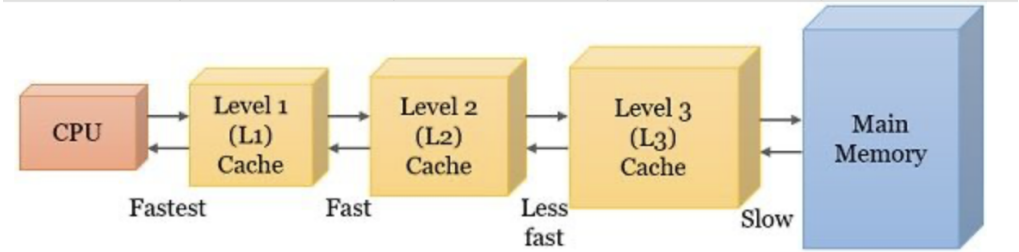
Reducing Cache Misses

The tag of every cache block within the appropriate set is checked to see if it matches the block address from the processor.



Implementation of a 4-way set-associative cache requires four comparators and a 4-to-1 multiplexor.

Reducing Cache Misses - Multilevel Cache



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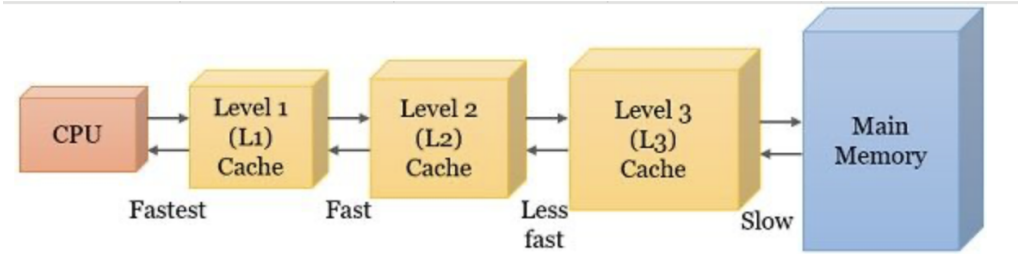

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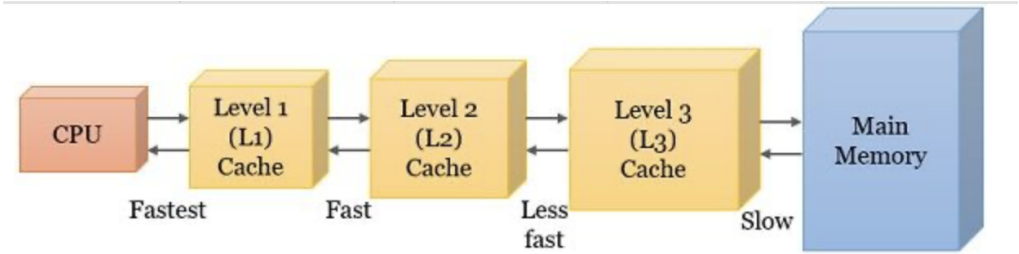

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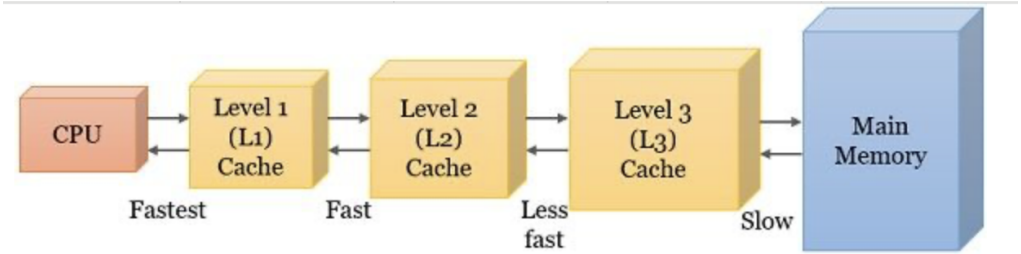

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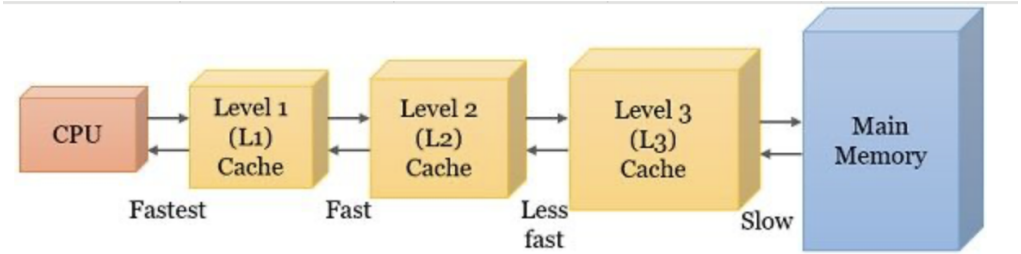

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- If none of the caches contains the data, a main memory access is required, and a larger miss penalty is incurred.

Example: Suppose we have a processor with a base CPI of 1.0 and a clock rate of 4 GHz. Assume a main memory access time of 100 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 2%. How much faster will the processor be if we add a secondary cache that has a 5 ns access time for either a hit or a miss and is large enough to reduce the miss rate to main memory to 0.5%?

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Ans: 2.6

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  - we also need to design memory systems that have less than 4 GB of main memory
- In order to achieve the aforementioned we use virtual memory

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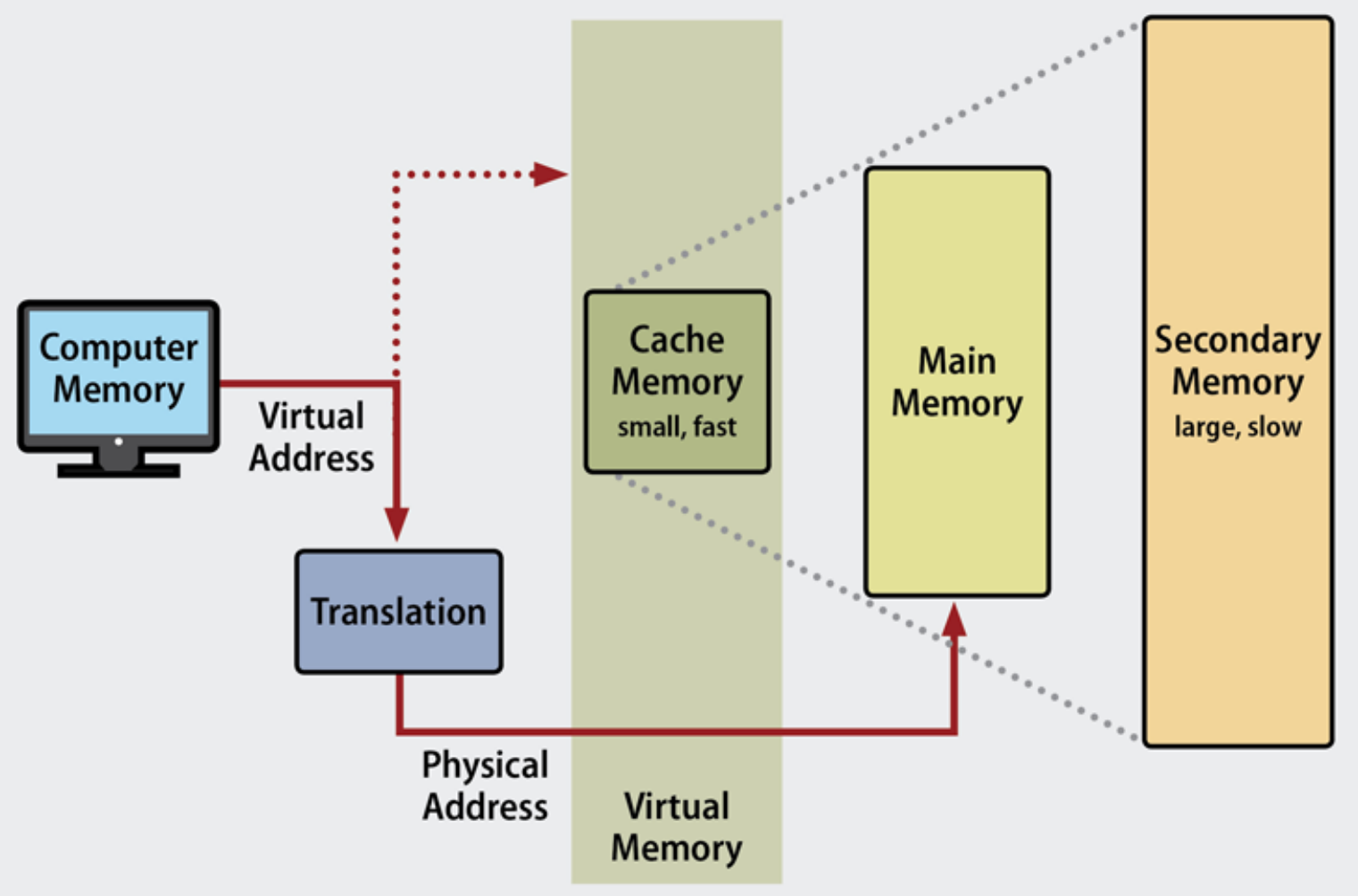
- Address translation system converts a virtual address to a physical address.

Virtual Memory



source: ded9.com

Virtual Memory - Pages

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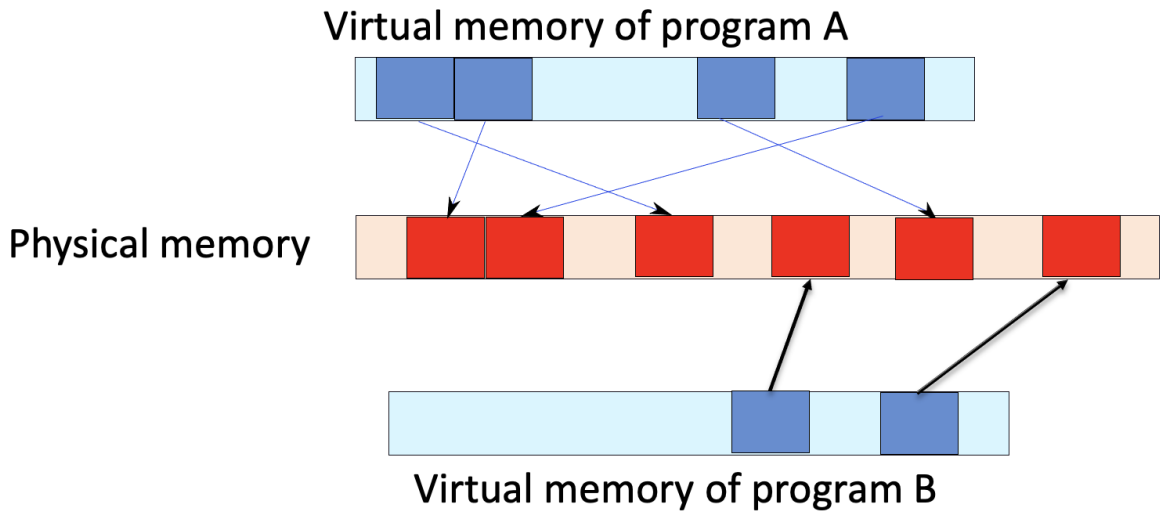
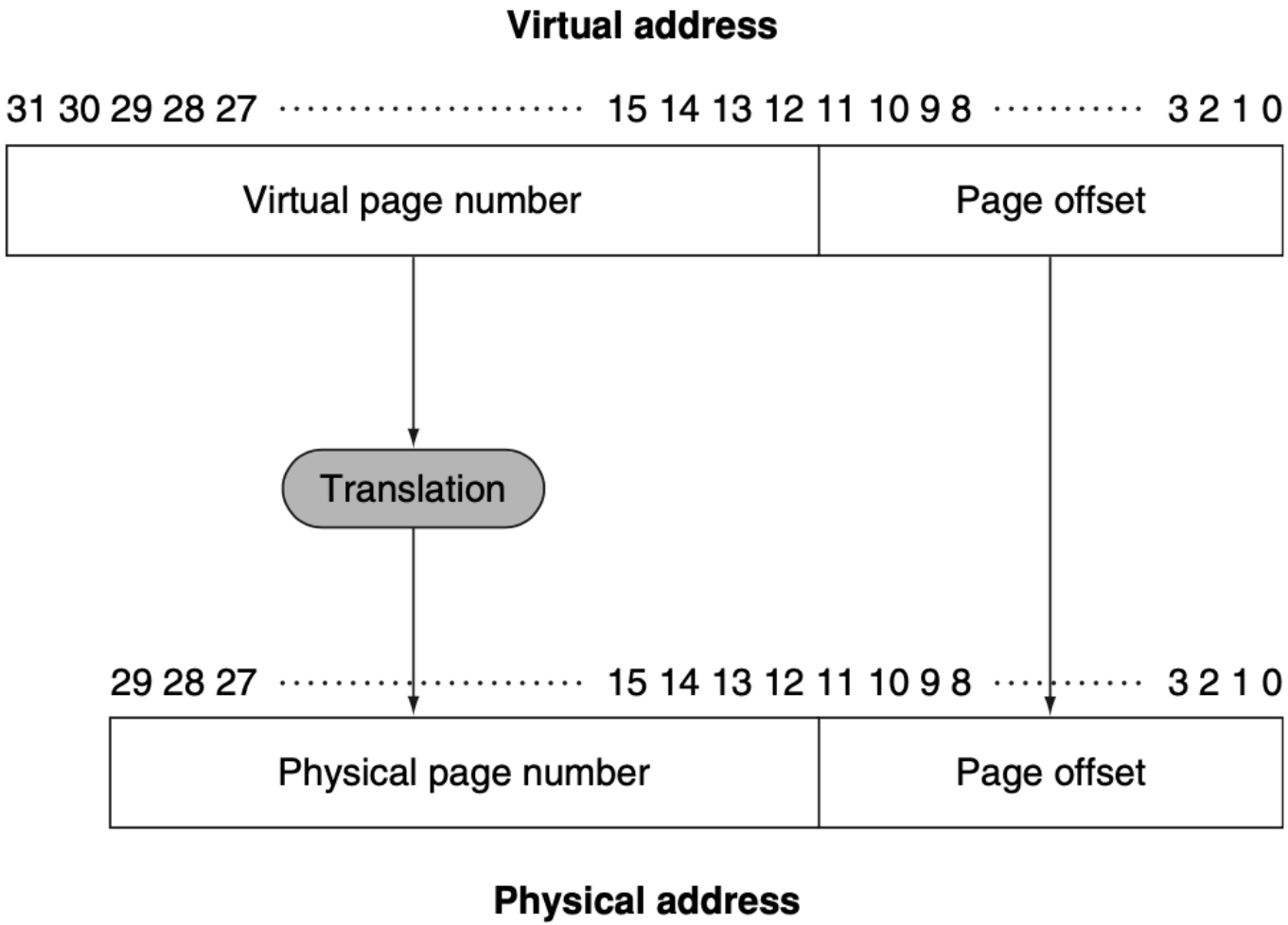


Virtual Memory - Address Translation



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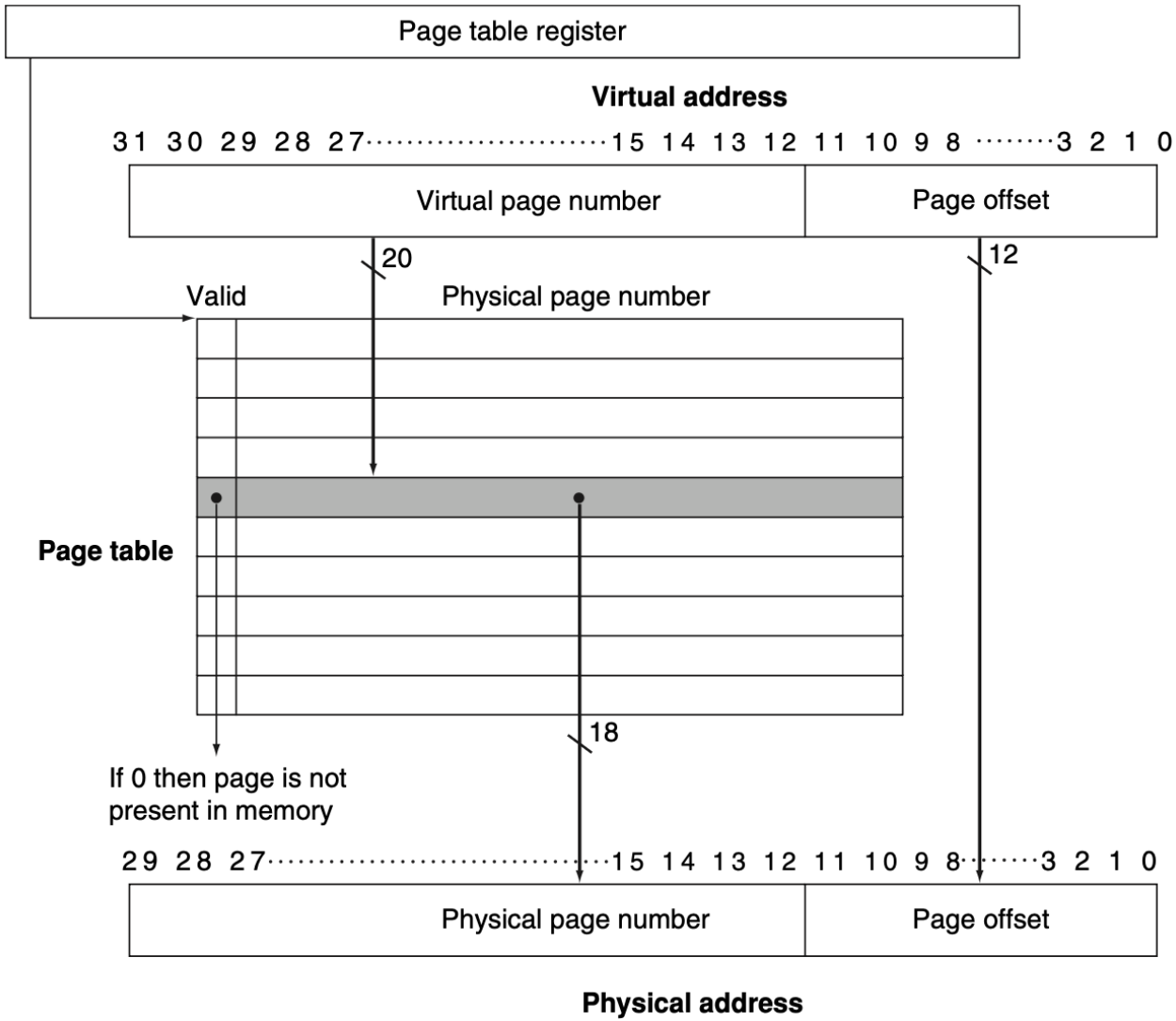
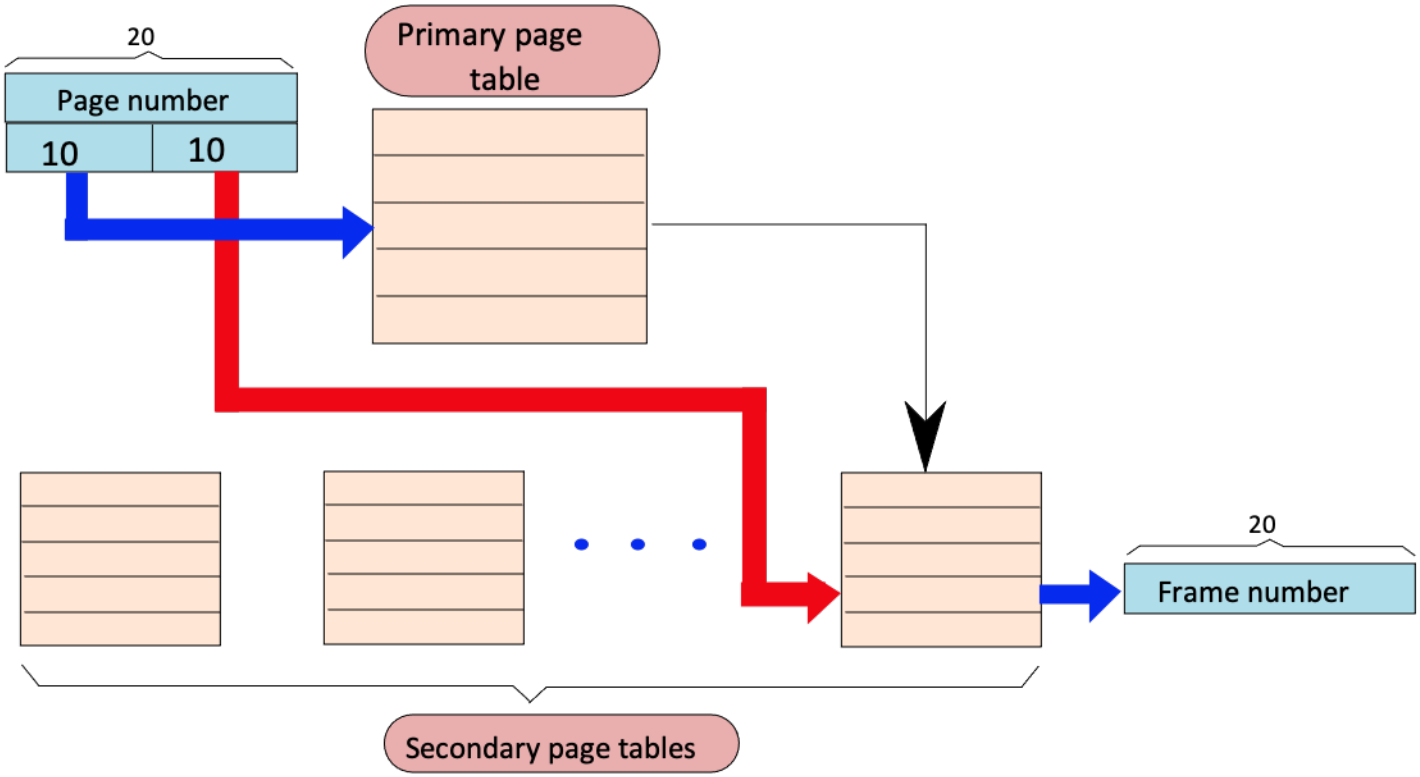
Virtual Memory - Page Table



Valid bit tells whether the page is present in main memory or not.

Virtual Memory - Two Level Page Table

We allocate only those many secondary page tables as required



Source: Basic Computer Architecture by SR Sarangi

Virtual Memory - Page Faults

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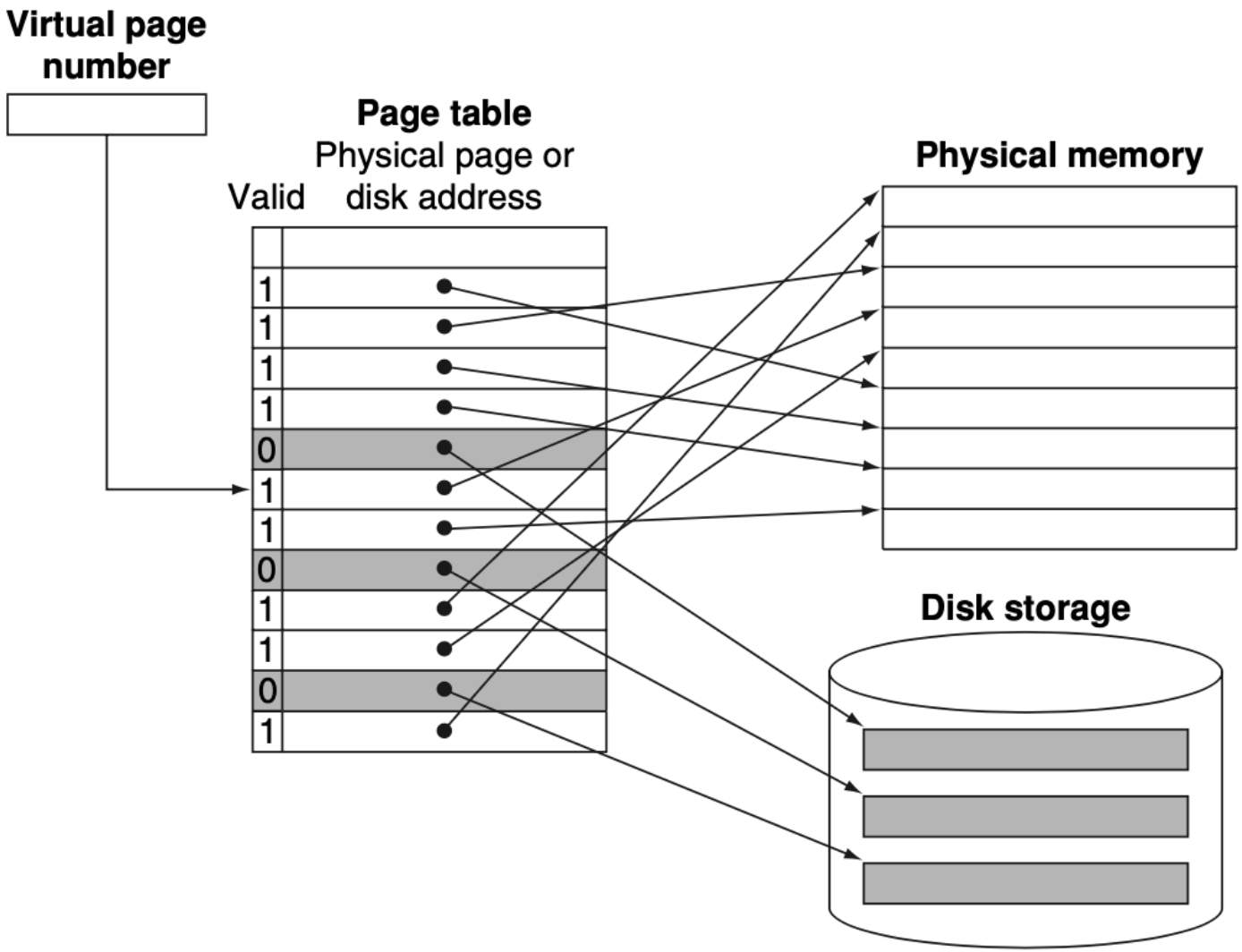
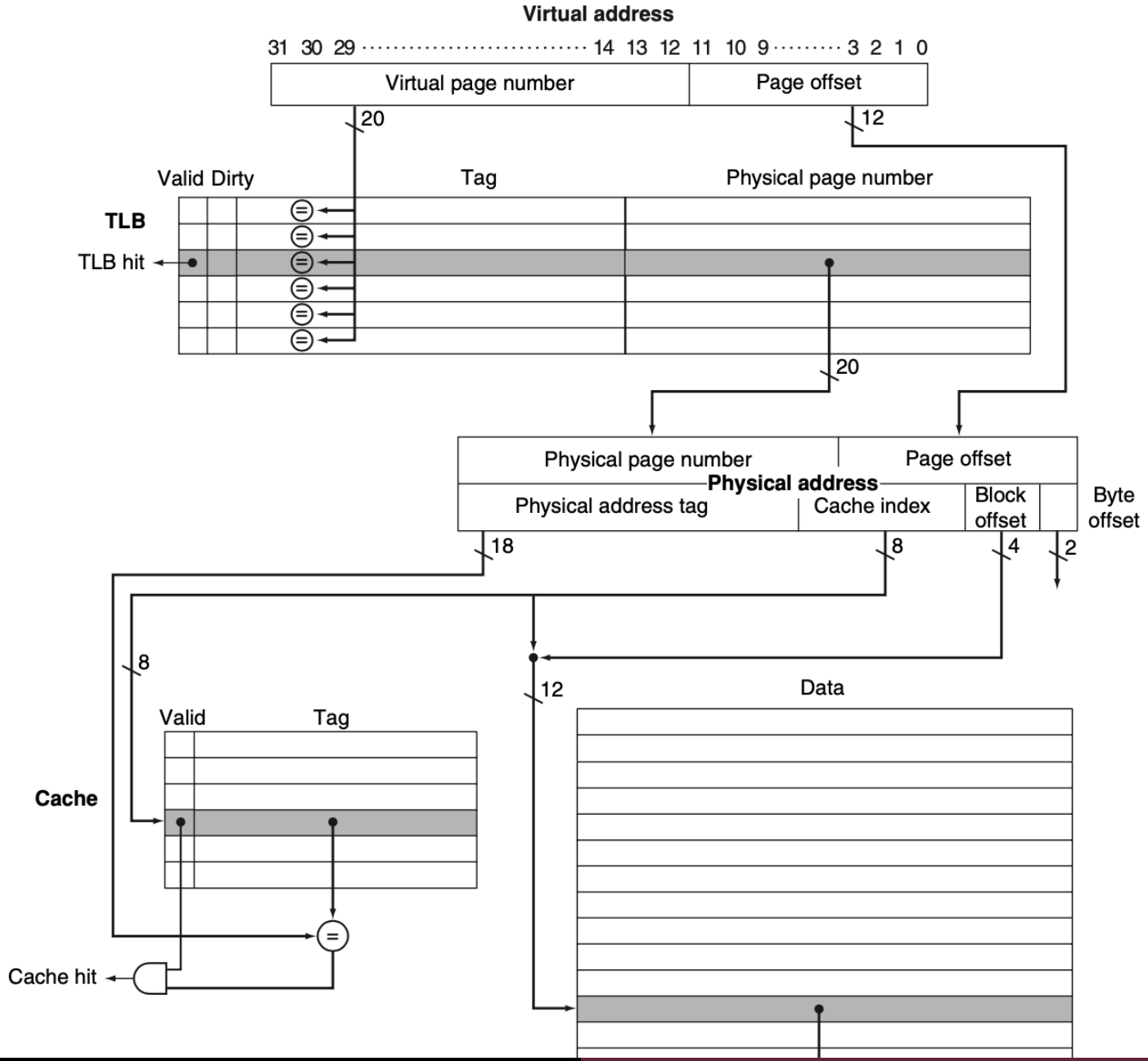
- If main memory is full, OS follows the (approximate) LRU replacement scheme.

Virtual Memory - Swap Space



Virtual Memory - TLB



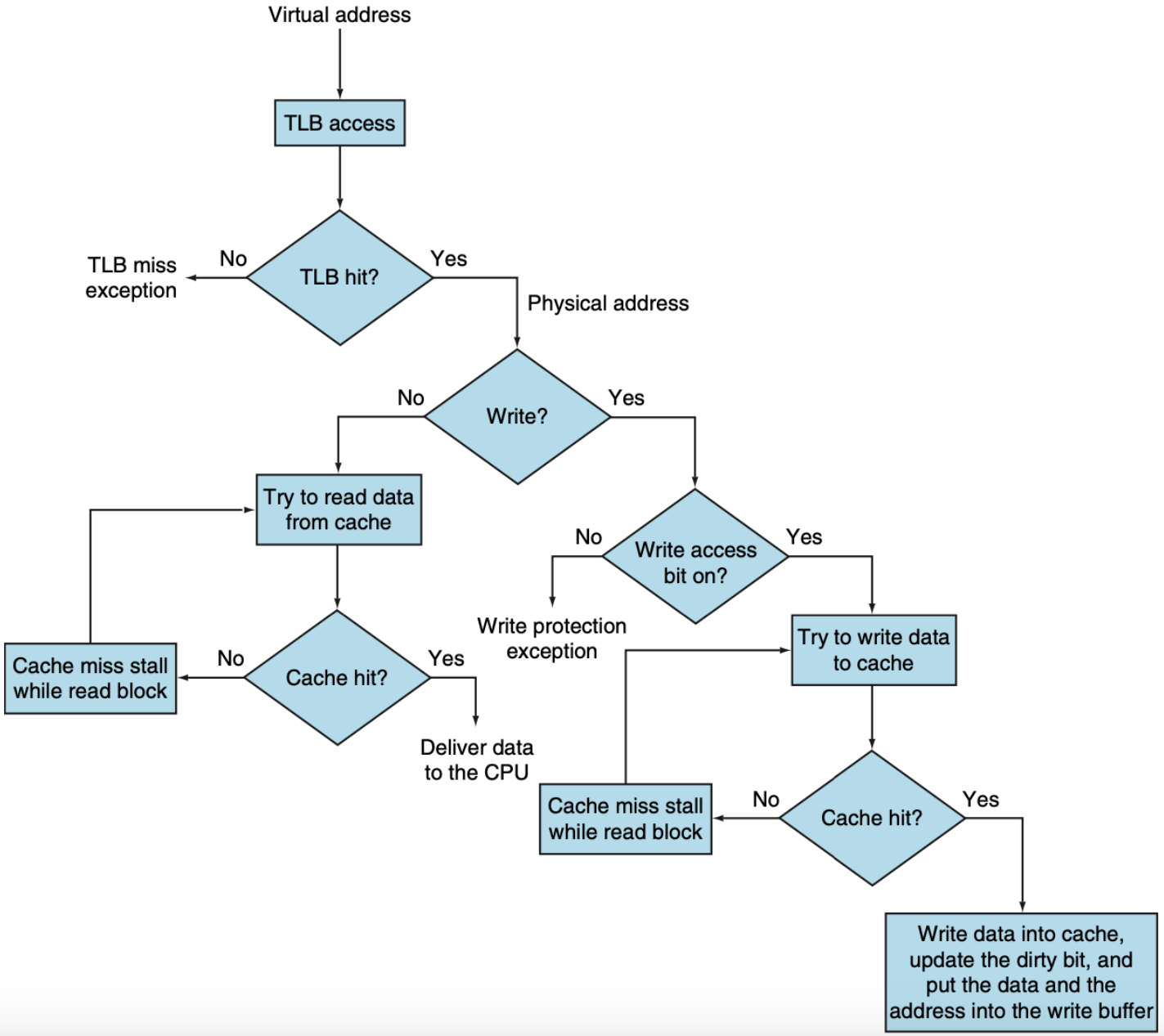
Virtual Memory - TLB

Example: Consider a system with 1 KB of main memory, 8-block cache where each block is of size 1 word, and TLB of size 4 entries. The system supports 1 KB of virtual memory which is divided into pages of size 64 B. If CPU references address 980_{ten}, find the corresponding data from cache. Shown below are the current state of TLB (left) and cache (right).

1	1000	0011
1	1111	1010
1	1010	0111
1	0101	1011

1	00011	010001110....00
1	10001	100000000....11
1	11110	000010001....00
1	10111	1111110001....01
1	10101	0101011111....00
1	10100	101010100....11
1	10000	0000011111....01
1	00101	1100111000....11

Virtual Memory - TLB & ache



Memory - Summary

Caches, TLBs, and virtual memory may initially look very different, but they rely on the same two principles of locality, and they can be understood by their answers to four questions:

Question 1: Where can a block be placed?
Answer: One place (direct mapped), a few places (set associative), or any place (fully associative).

Question 2: How is a block found?
Answer: There are four methods: indexing (as in a direct-mapped cache), limited search (as in a set-associative cache), full search (as in a fully associative cache), and a separate lookup table (as in a page table).

Question 3: What block is replaced on a miss?
Answer: Typically, either the least recently used or a random block.

Question 4: How are writes handled?
Answer: Each level in the hierarchy can use either write-through or write-back.

Memory - Three Cs Model

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Design change	Effect on miss rate	Possible negative performance effect
Increase cache size	Decreases capacity misses	May increase access time
Increase associativity	Decreases miss rate due to conflict misses	May increase access time
Increase block size	Decreases miss rate for a wide range of block sizes due to spatial locality	Increases miss penalty. Very large block could increase miss rate

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Time step	Event	Cache contents for CPU A	Cache contents for CPU B	Memory contents for location X
0				0
1	CPU A reads X	0		0
2	CPU B reads X	0	0	0
3	CPU A stores 1 into X	1	0	1

Memory - Cache Coherence

A memory system is coherent if

- Reads to a location X by multiple processor are consistent.
- Writes to the same location are serialized.

Enforcing Coherence – Snooping

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  - This style of protocol is called a write invalidate protocol.

Memory - Cache Coherence

Processor activity	Bus activity	Contents of CPU A's cache	Contents of CPU B's cache	Contents of memory location X
				0
CPU A reads X	Cache miss for X	0		0
CPU B reads X	Cache miss for X	0	0	0
CPU A writes a 1 to X	Invalidation for X	1		0
CPU B reads X	Cache miss for X	1	1	1

During the write A takes exclusive access, and the copy held by the reading processor (B) is invalidated.