NoCTurnal Networking Solutions

A Daniel Sabogal & Sebastian Sabogal Company

Statement of Work

Task Descriptions

- Software/NoC Simulation (Daniel)
  - Timed stepping capabilities
  - Multithreaded (pthread) application
  - Console or GUI demonstration
- Software/NIC Baremetal Driver (Daniel)
  - Baremetal interface for offloading/accessing packets with the NIC
- HDL/Router (Sebastian)
  - FIFO: Create user-configurable FIFOs leveraging BRAM for Xilinx devices
  - Multi-FIFO Structure: Port map FIFOs to form the skeleton of the router
  - RR & Wormhole:
    - Implement a per-link round-robbin mechanism for packet switching and XY rounting
    - Implement wormhole switching
- HDL/NIC (Daniel)
  - Use FIFOs to buffer packets with send/receive logic
- Testbenching/Router (Sebastian)
  - Test router implementation
- Testbenching/NIC
  - Test NIC implementation
- Testbenching/NoC (Daniel & Sebastian)
  - Test multi-router network
  - Emulate congestion through multiple IoT devices
  - User configurable traffic or packet offloading
- Integration (Sebastian)
  - Package HDL into Vivado IP
  - Create Block Designs
  - Place & Route Constraints to realize NoC on the floorplan
  - Timing Analysis
- Testing/Baseline (Daniel & Sebastian)
  - Testing without P&R Constraints
- Testing/Final (Daniel & Sebastian)
  - Testing with P&R Constraints
  - Fix timing issues

(Note: tasks assigned to Daniel & Sebastian are tightly coupled and involve both engineers)

Deliverables

- Software Demonstration (2/26)
  - A software-based simulation demonstrating the correctness of packet routing in the NoC
- HW/SW Partitioning & Test Plan (3/19)
  - An HDL-based implementation of the router and NIC IP with complete testbenching
  - Representative testbenching for a full NoC system (multiple routers with emulated IoT devices)
- Baseline Demonstration (4/2)
  - Realization of the NoC without P&R constraints (all components are realized, but are not efficiently partitioned)
- Final Demonstration (4/17)
  - Realization of the NoC with P&R constraints (all components are realized and are efficiently partitioned with timing issues fixed)

Acceptance Tests

- Preliminary test plan:
  - A 3x3 2D mesh (9 partitions); each partition has:
    - an IoT device (emulated as a NIC connected to the PS)
  - a local BRAM
  - Write phase:
  - Test 0: the PS creates packet(s) for each NIC the will route the packet(s) to the NIC's neighbor (next logical neighbor). This test is functional, but execution time and bandwidth information are obtained.
  - Test 1: the PS creates packet(s) for each NIC that will route the packet(s) to all NICs present in the network (including self). Execution time and bandwidth information are obtained.
  - Test 2: the PS creates packet(s) to be sent from a NIC on one corner of the NoC to another NIC on the opposite corner of the NoC with no congestion present. Execution time and bandwidth information are obtained.
  - Test B: Behavioral testbench that exercises router operation in simulation.

Requirements vs. Trace-ability Matrix

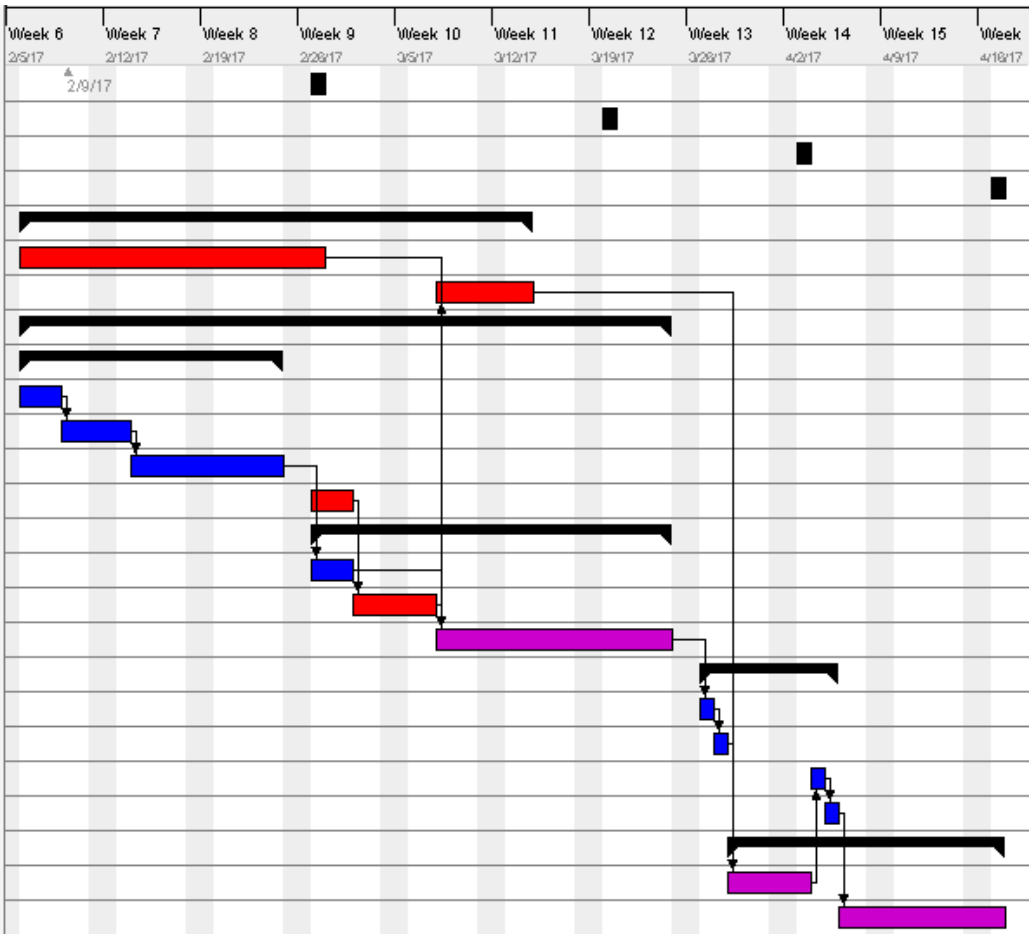
Requirement	Test 0	Test 1	Test 2	Test B
Baseline				
Routing	X	X	X	X
Ordering	X			
Congestion	X	X		
Wormhole	X	X		X
Zero-load Latency			X	
Extra				
Partition	X	X	X	
> 100MHz Fmax	X	X	X	

Invoice

- The successful completion of this work will require 2 payments of **A**

Schedule

Name	Begin ...	End date
SW Demo	2/27/17	2/27/17
HW/SW Part. & Test Plan	3/20/17	3/20/17
Baseline Demo	4/3/17	4/3/17
Final Demo	4/17/17	4/17/17
Software	2/6/17	3/14/17
NoC Simulation	2/6/17	2/27/17
NIC Baremetal Driver	3/8/17	3/14/17
HDL	2/6/17	3/24/17
Router	2/6/17	2/24/17
FIFO	2/6/17	2/8/17
Multi-FIFO Struct	2/9/17	2/13/17
RR & Wormhole	2/14/17	2/24/17
NIC	2/27/17	3/1/17
Testbenching	2/27/17	3/24/17
Router	2/27/17	3/1/17
NIC	3/2/17	3/7/17
NoC	3/8/17	3/24/17
Integration	3/27/17	4/5/17
IP Packaging	3/27/17	3/27/17
Block Design	3/28/17	3/28/17
P&R Constraints	4/4/17	4/4/17
Timing Analysis	4/5/17	4/5/17
Testing	3/29/17	4/17/17
Baseline	3/29/17	4/3/17
Final	4/6/17	4/17/17



(Note: Tasks are assigned by color: Daniel, Sebastian, Both)