ECE 2140 SoC Design

No  Turnal

Network on a Chip

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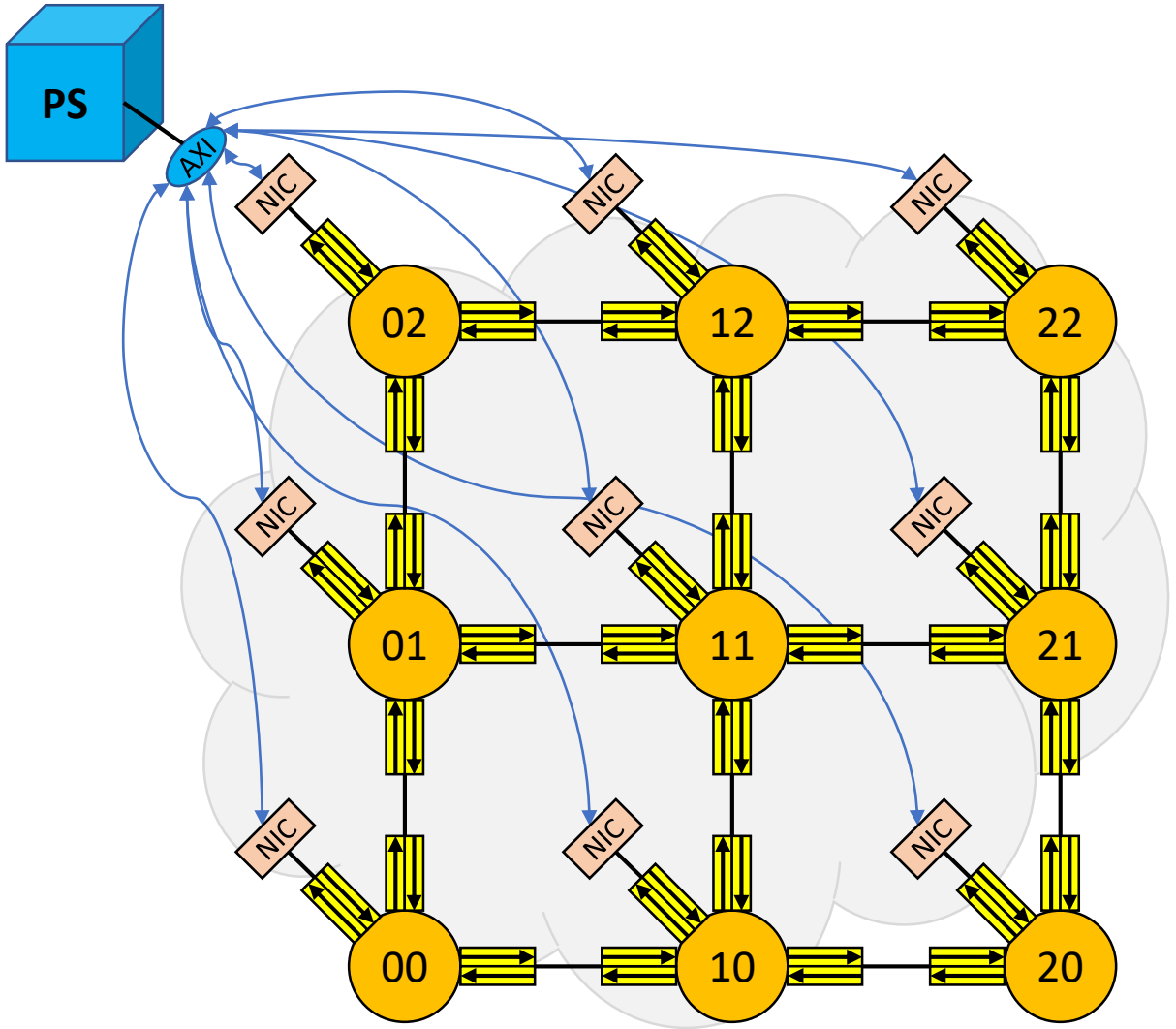
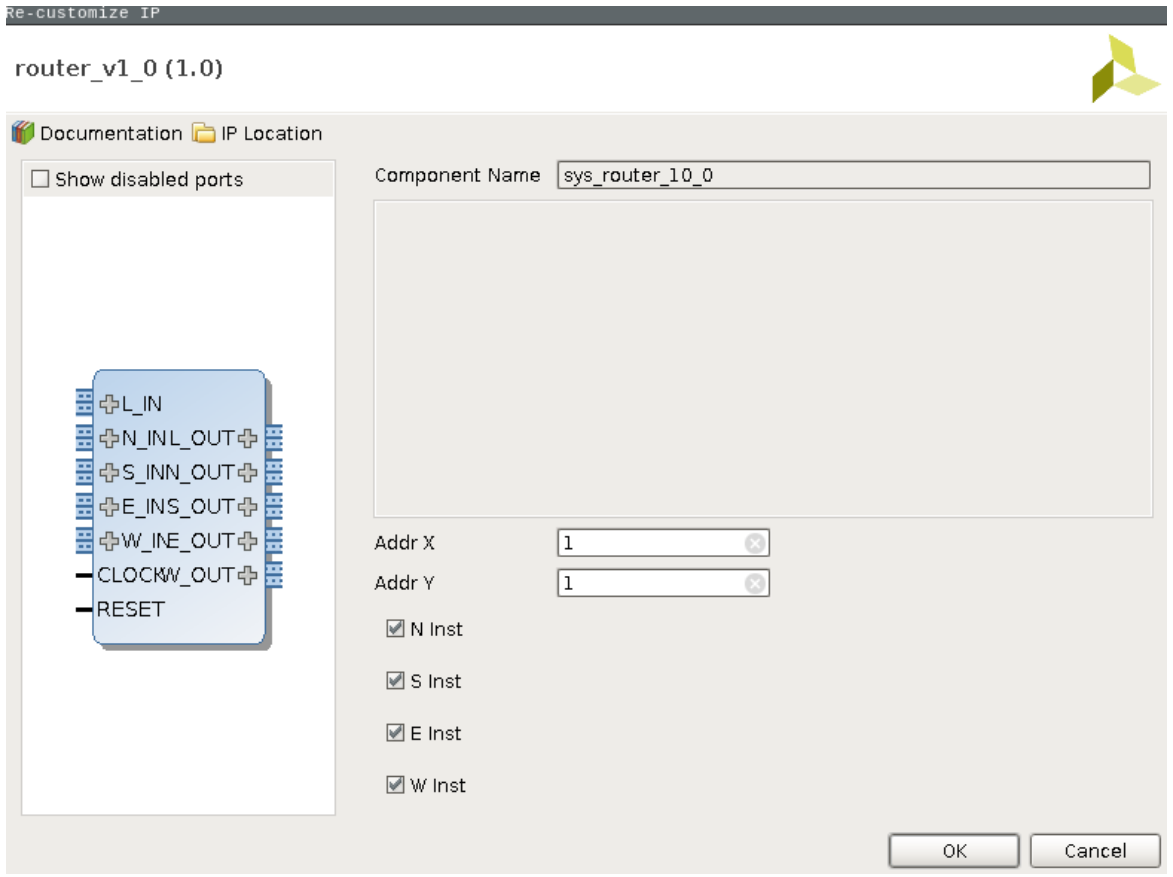
NoCTurnal Description

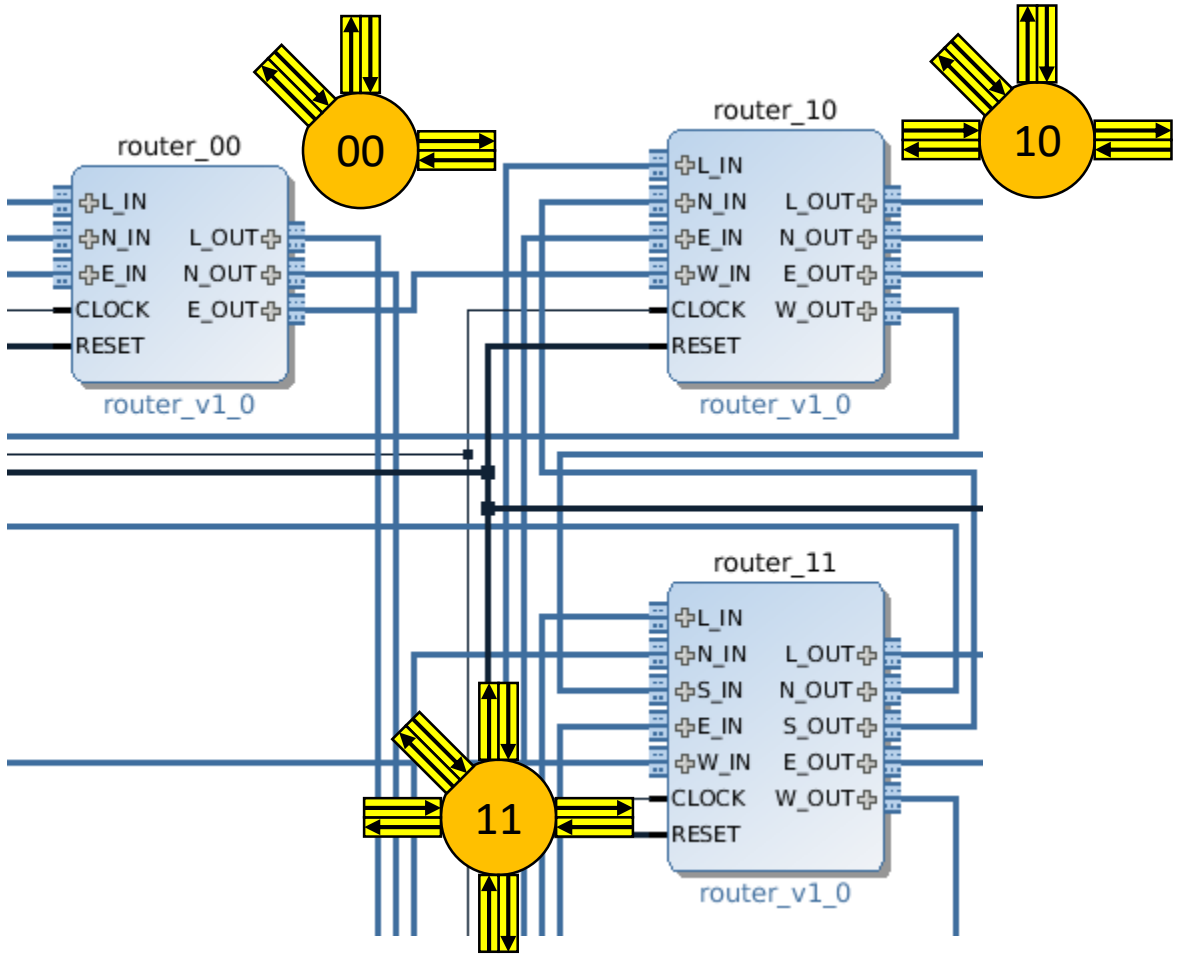


Description of Blocks

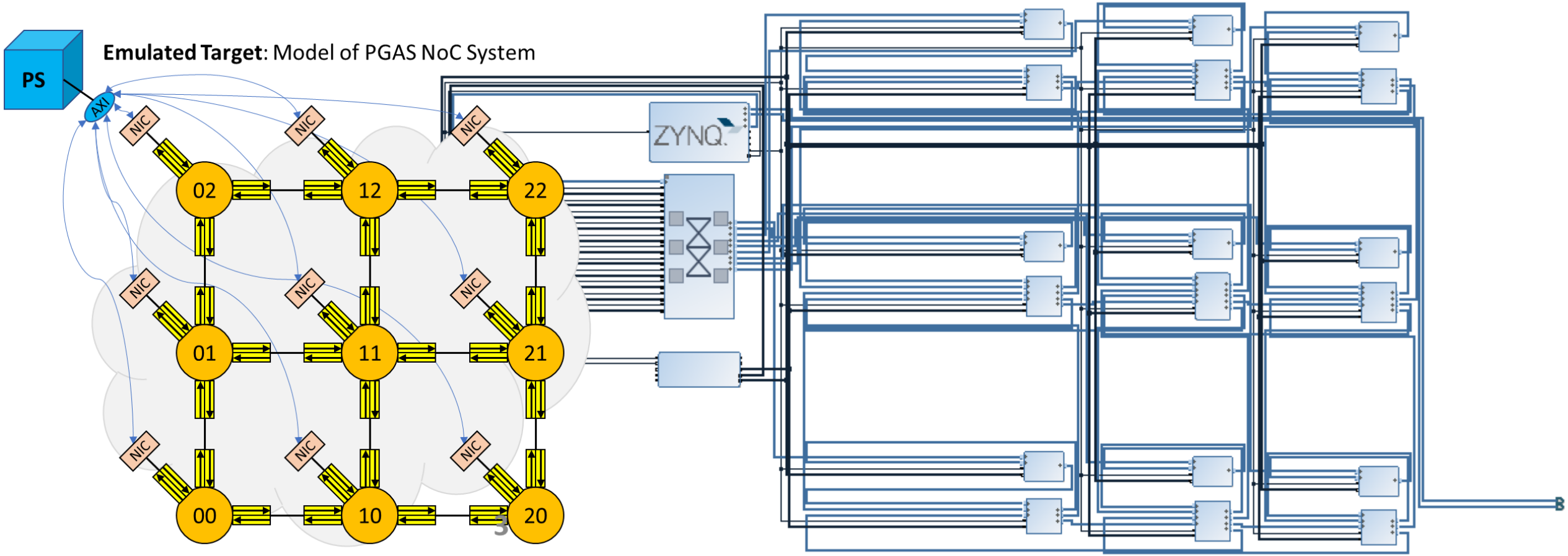
- 1. NoC Simulation
  - Simulation of 3x3 Mesh NoC
- 2. Network Interface Card (NIC)
  - AXI4-interfaced Network Interface
- 3. SW NIC Driver
  - Baremetal Driver for NIC
- 4. FIFO Structure
  - {3,4,5}-of-{N,E,W,S,L} In/Out FIFOs
- 5. Switch Logic
  - Worm-hole XY Packet Switch

NoCTurnal Zynq-7020 Implementation (1/3)

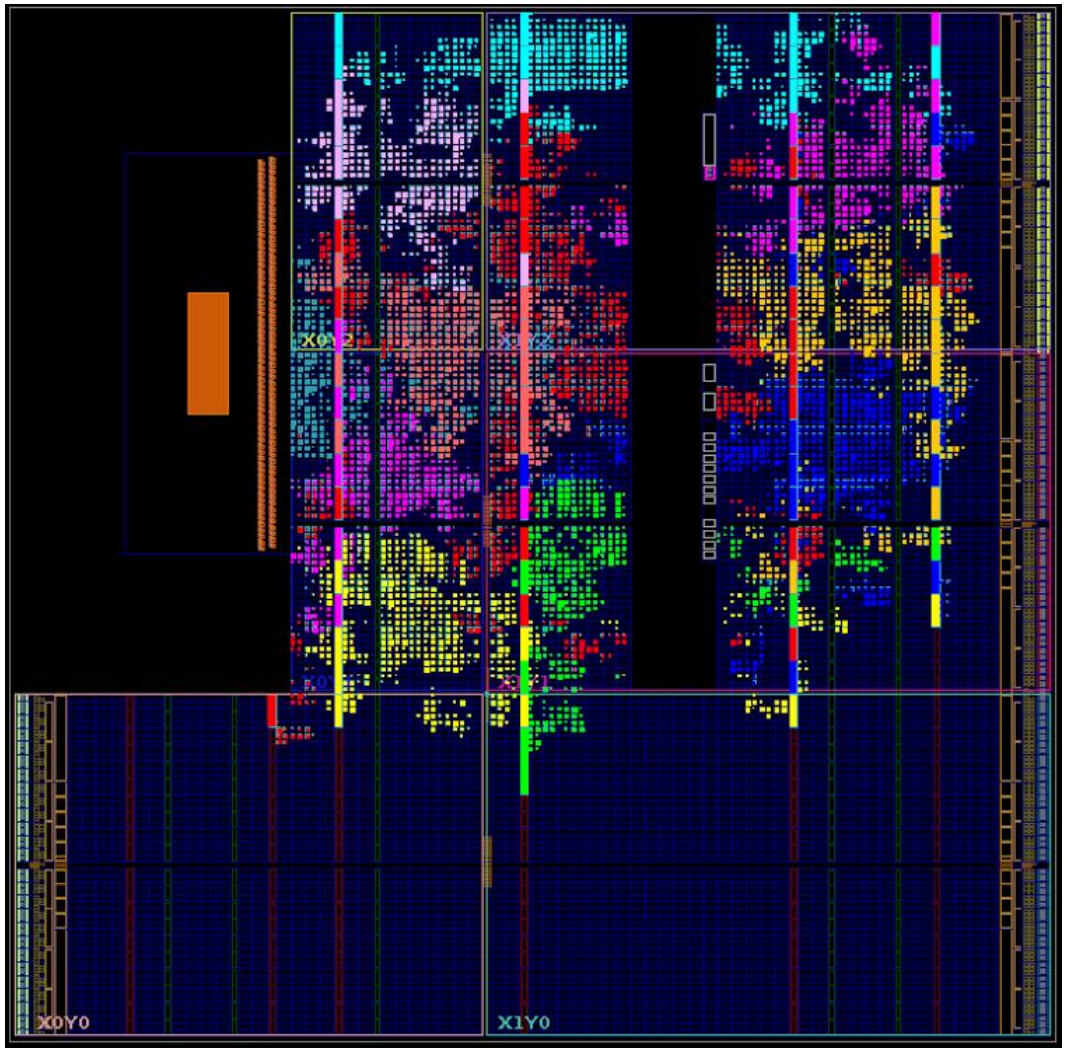


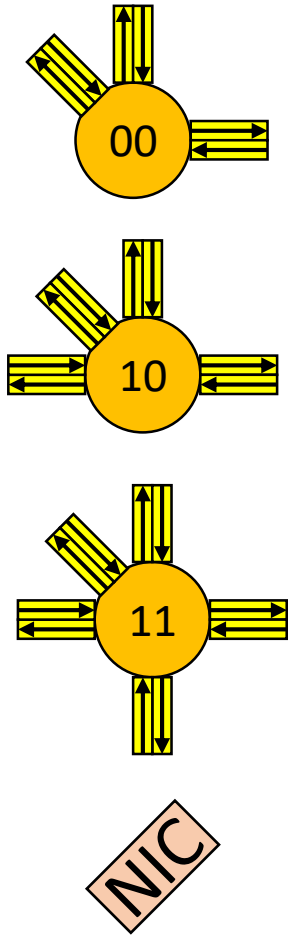


NoCTurnal Zynq-7020 Implementation (2/3)



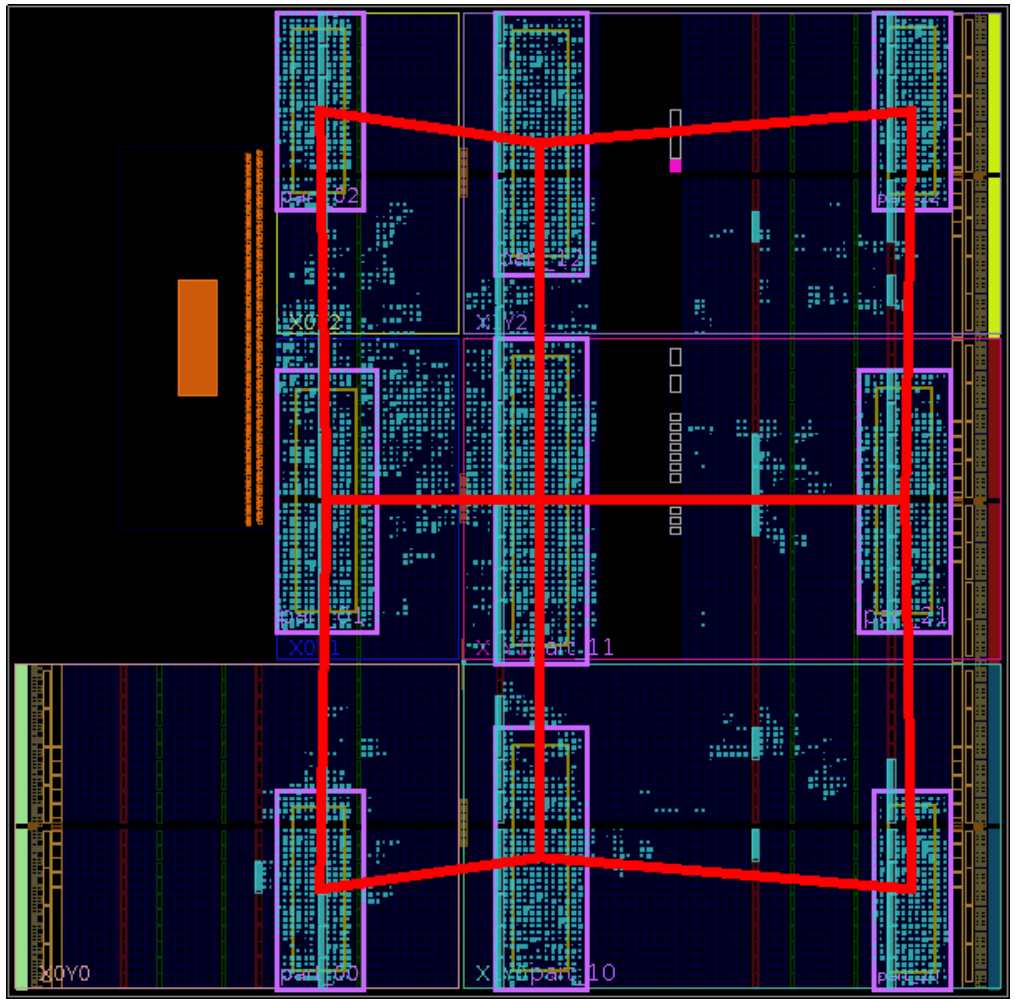
NoCTurnal Zynq-7020 Implementation (3/3)





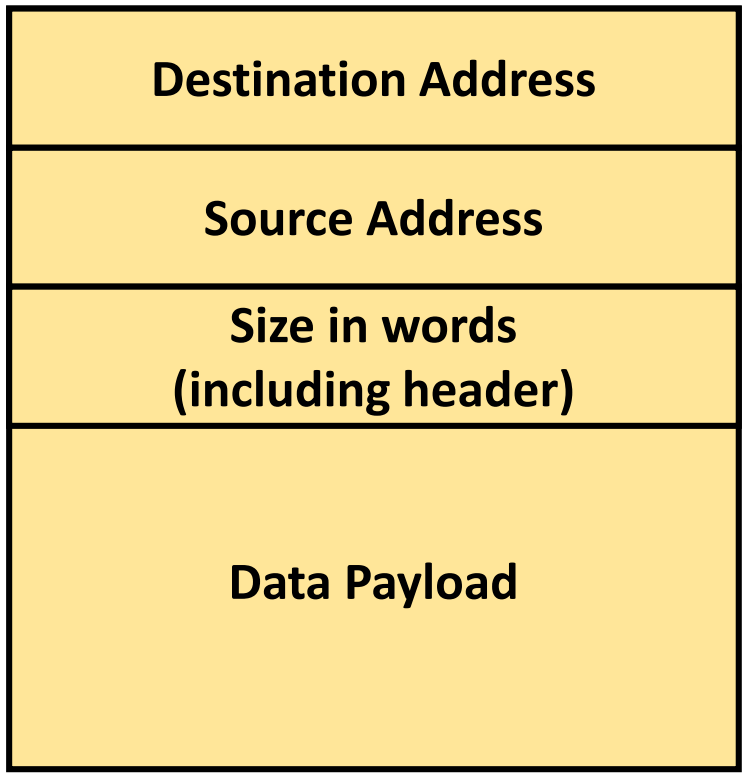
	LUTs	FFs	RAMB36
Router 00	812	987	6
Router 10	1164	1316	8
Router 11	1583	1645	10
NIC	184	323	2

NoTurnal Zynq-7020 and P-Blocks



- Partition fabric into 9 regions using P-blocks
- 2D 3x3 Mesh
- Functionally tested at 100 MHz

NoCTurnal Packet Structure



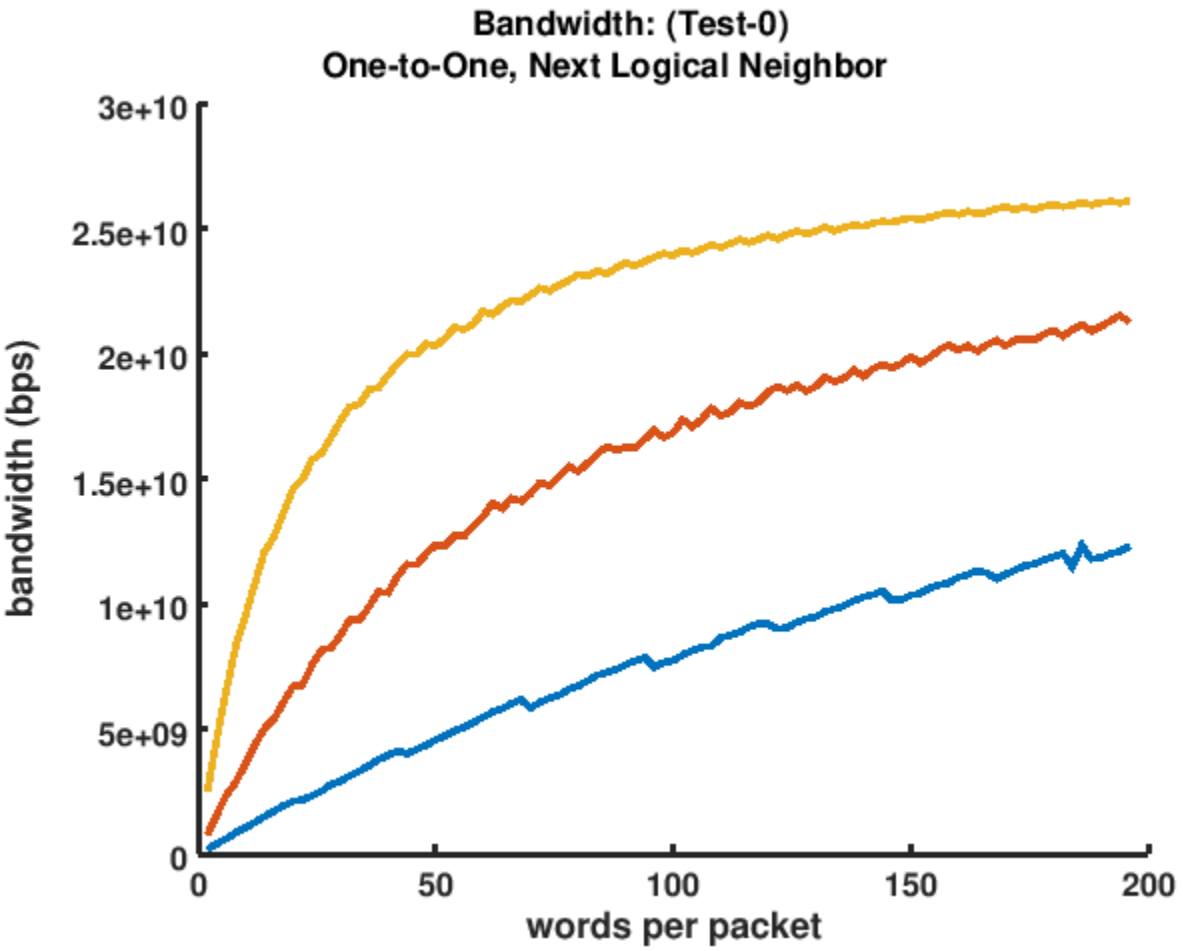
- Packet header consists of 3 32-bit words
  - Destination address
  - Source address
  - Size (including the header)
- PGAS model used to bind nodes to an address range
- Upper 4-bits of addresses are used as the X-Y coordinates used for XY-routing

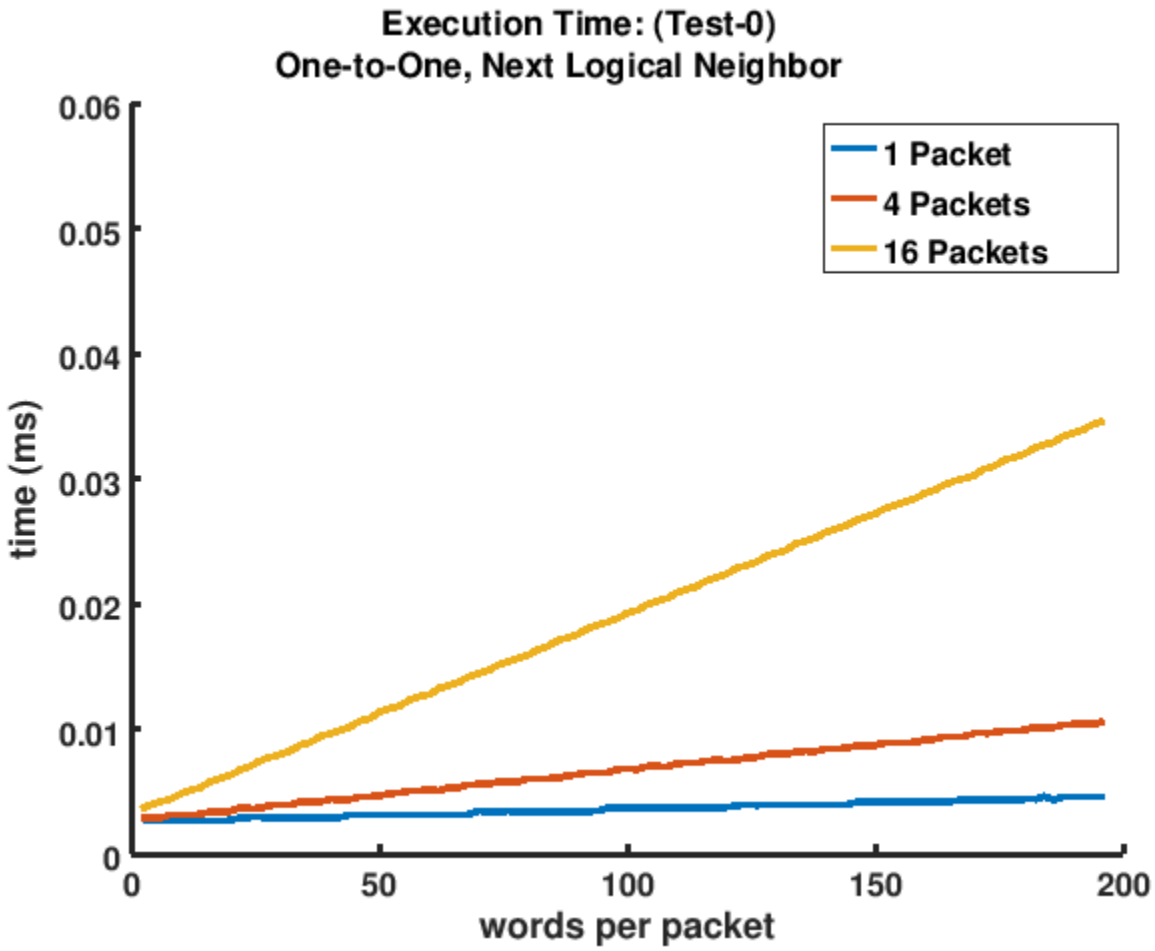
NoCTurnal Requirements vs. Traceability

0. 1-to-1 test with barrier
1. N-to-N test with barrier
2. Worst-case zero-load
B. Router behavioral testbench

Requirement	Test 0	Test 1	Test 2	Test B
Baseline				
Routing	X	X	X	X
Ordering	X			
Congestion	X	X		
Wormhole	X	X		X
Zero-load Latency			X	
Extra				
Partition	X	X	X	
> 100MHz Fmax	X	X	X	

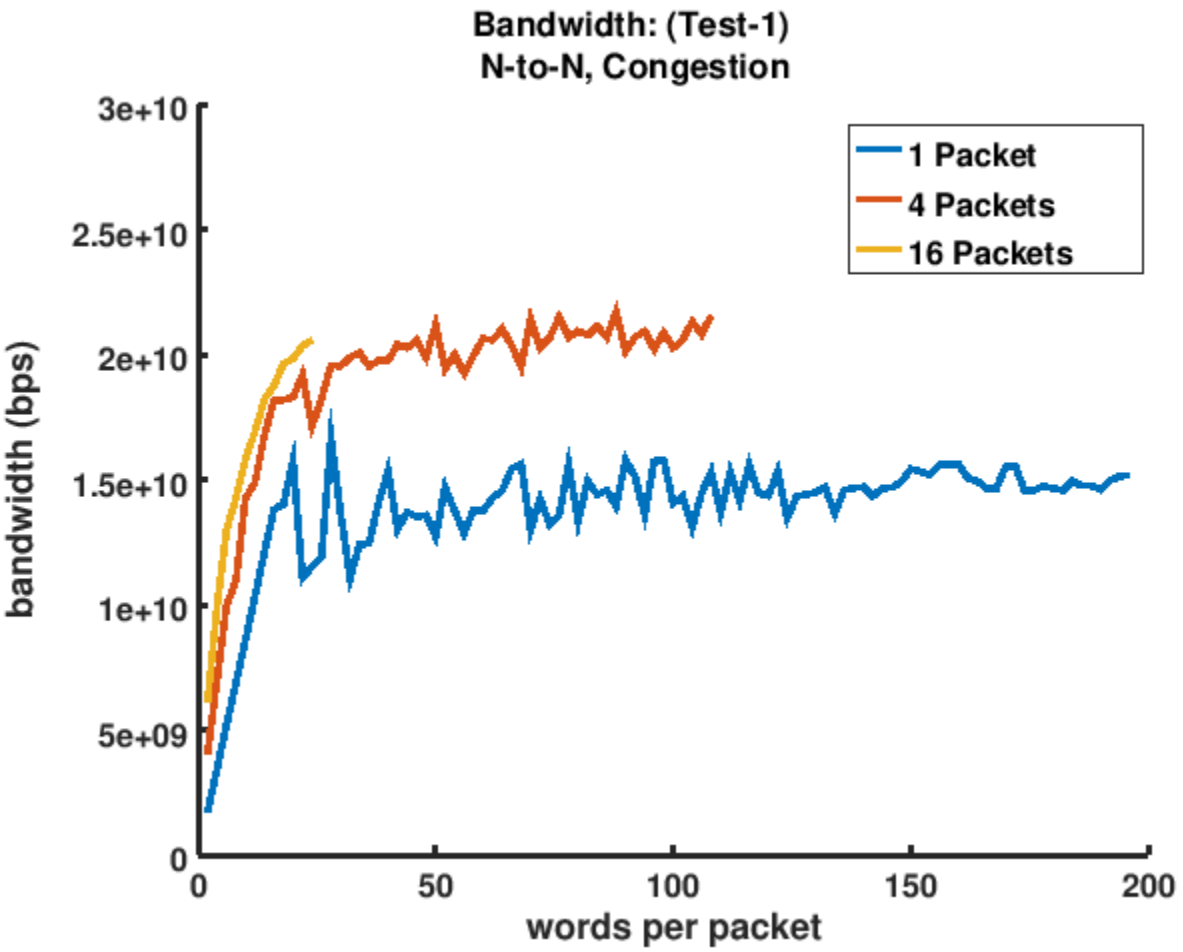
NoCTurnal Test 0 – One-to-One

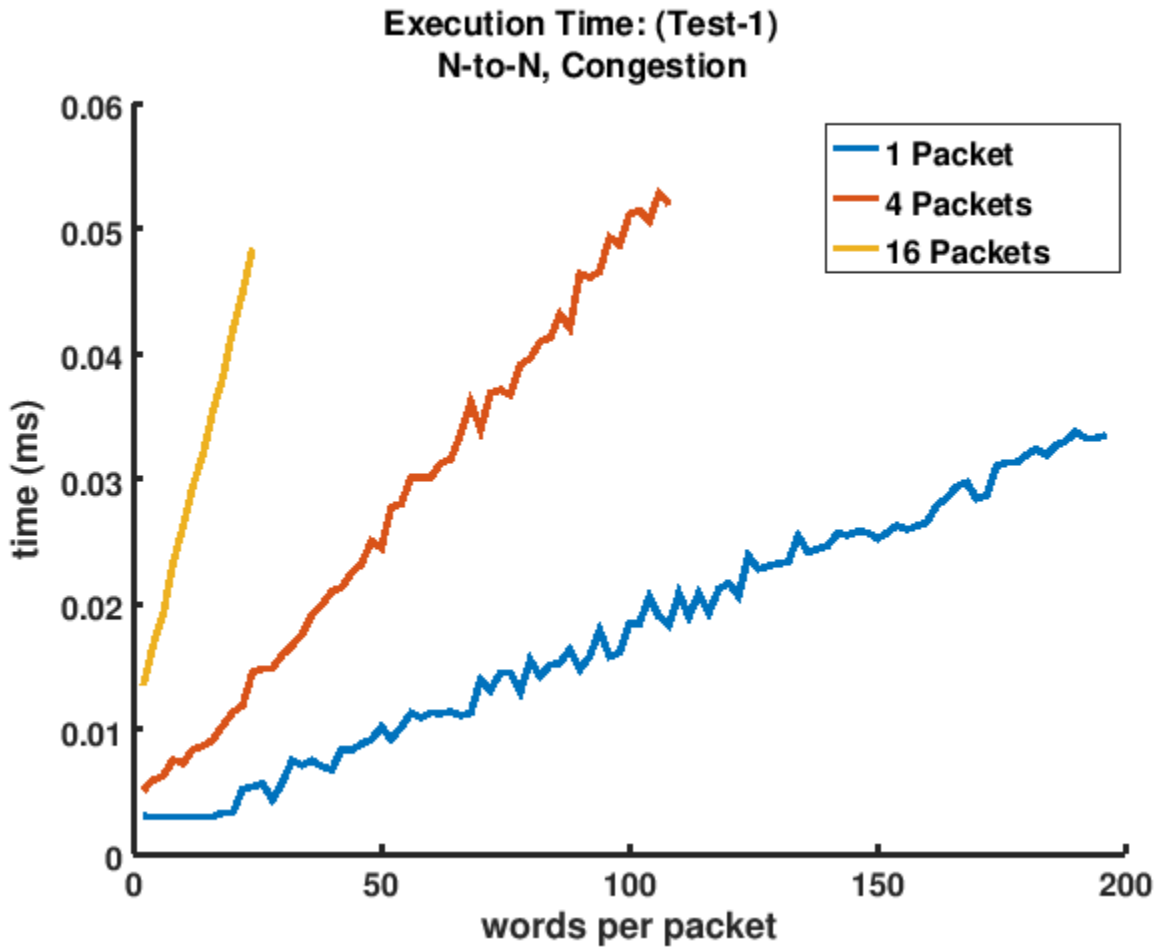




Zynq-7020 FPGA running at 100 MHz

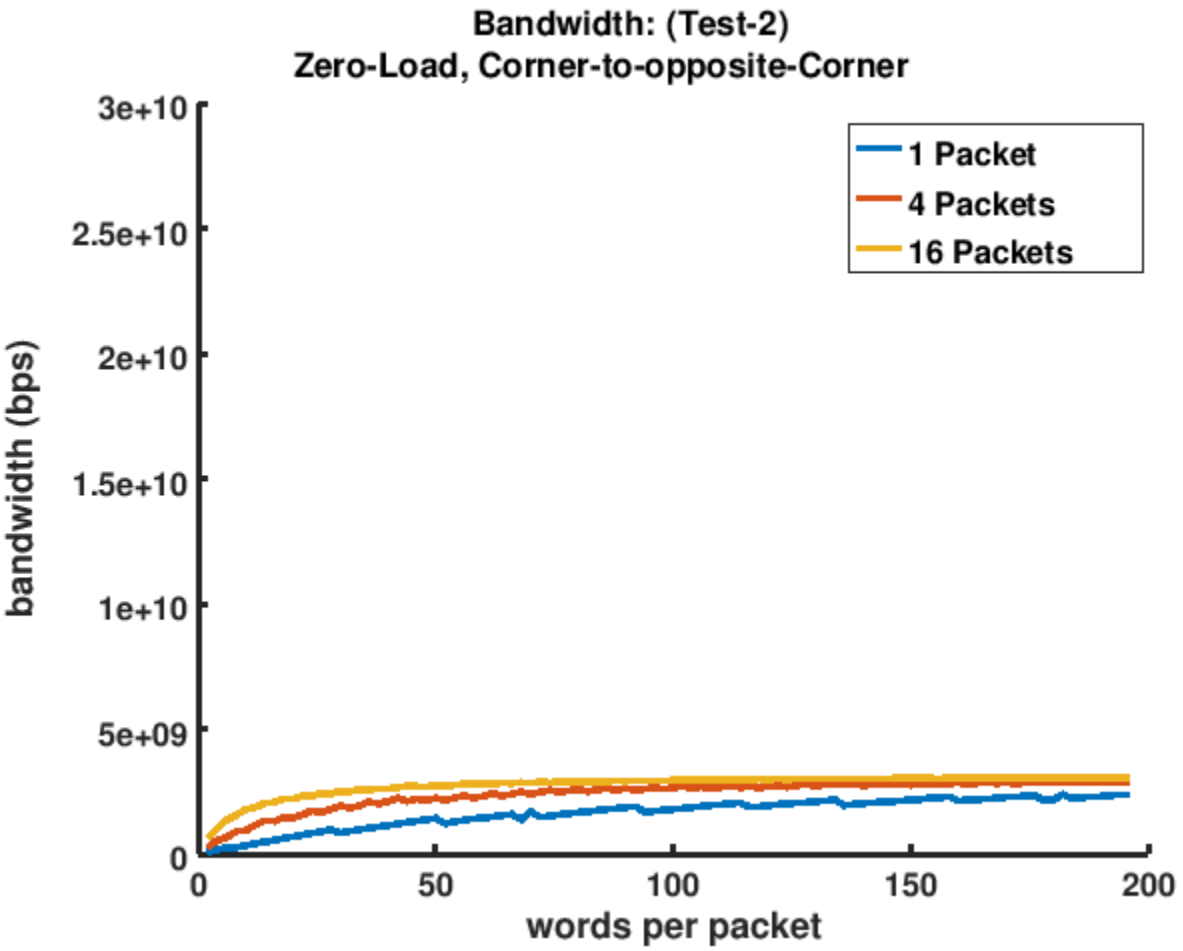
NoTurnal Test 1 – N-to-N

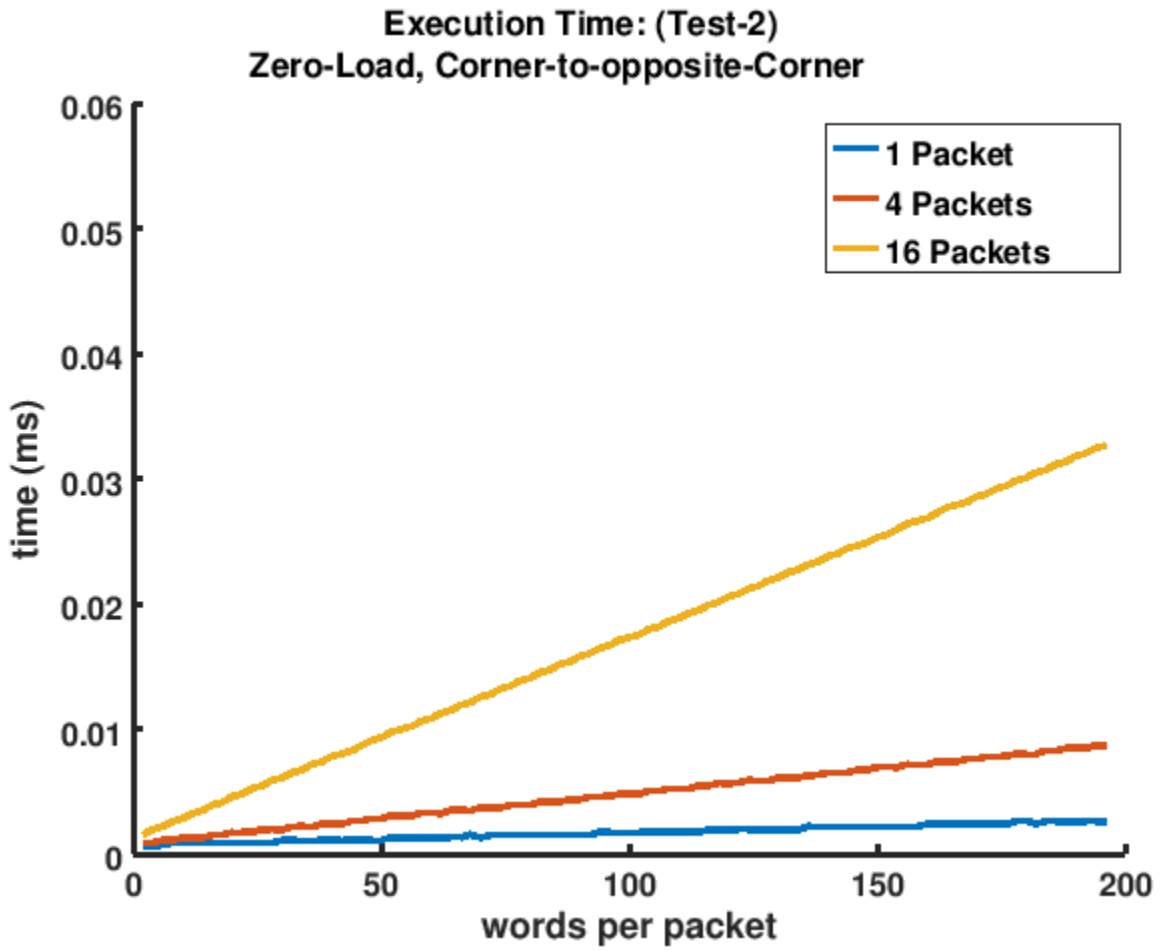




Zynq-7020 FPGA running at 100 MHz

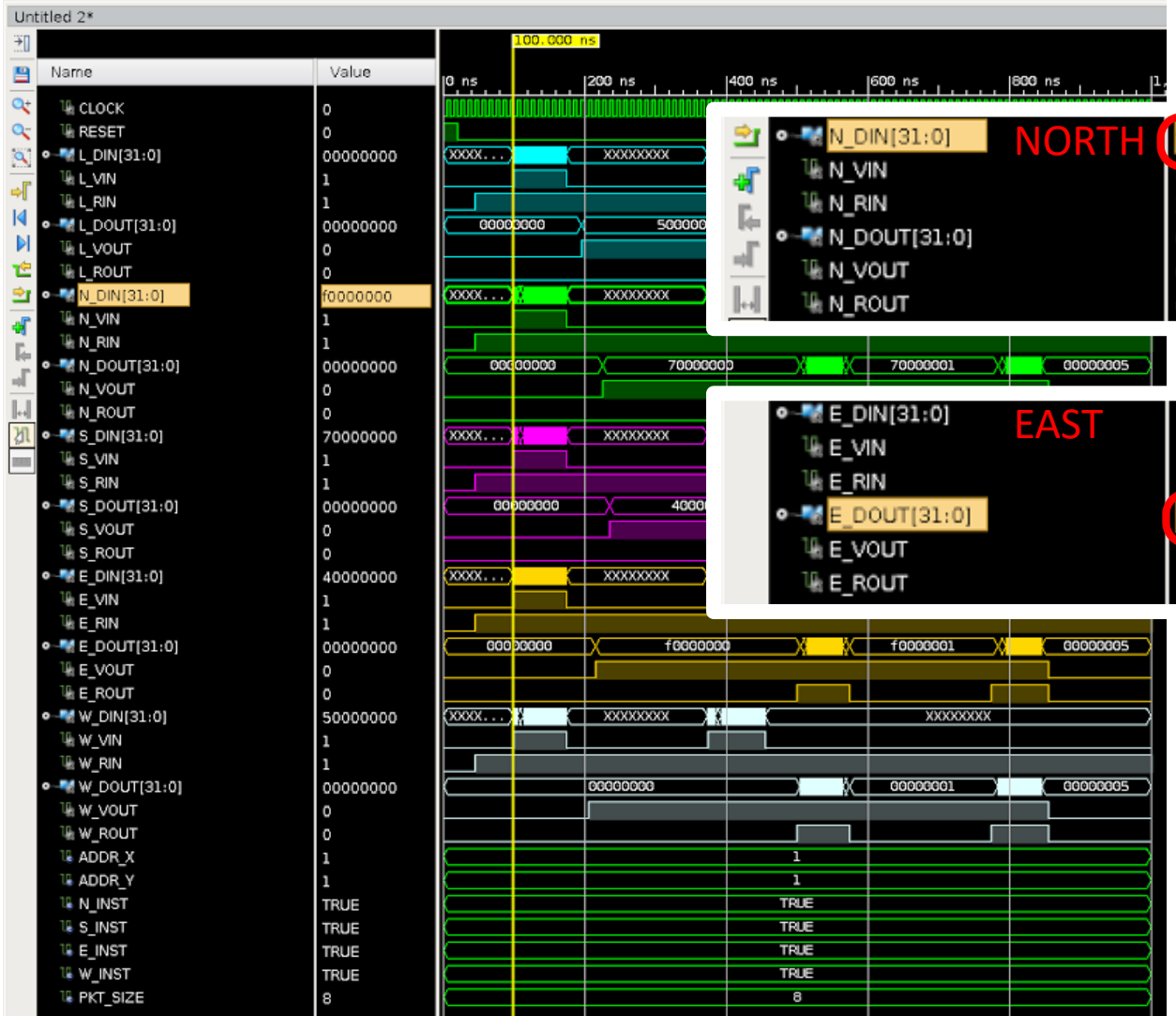
NoCTurnal Test 2 – Zero-load Corners



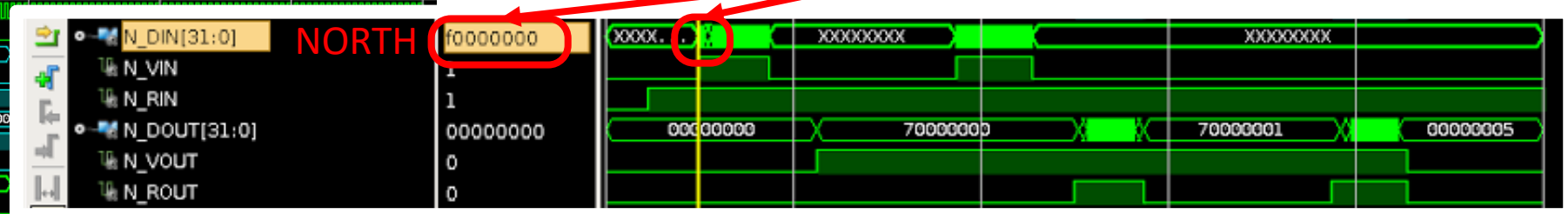


Zynq-7020 FPGA running at 100 MHz

NoTurnal Test B: Router Behavioral



DST Address (first word) is 0xf000_0000



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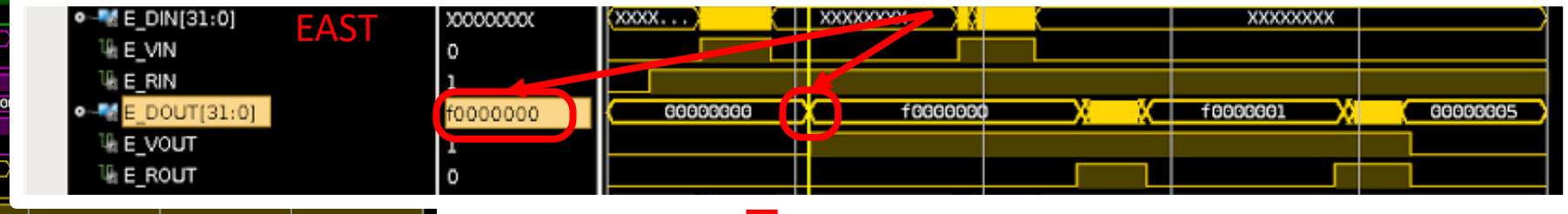
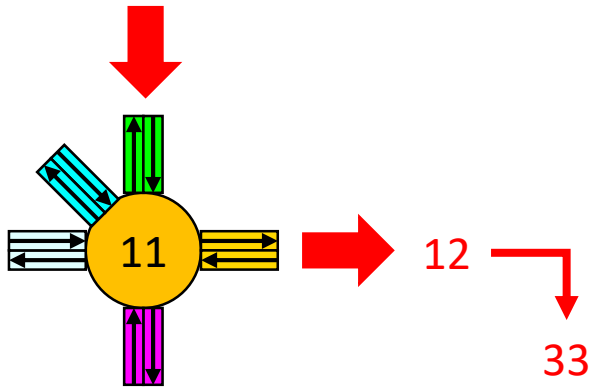
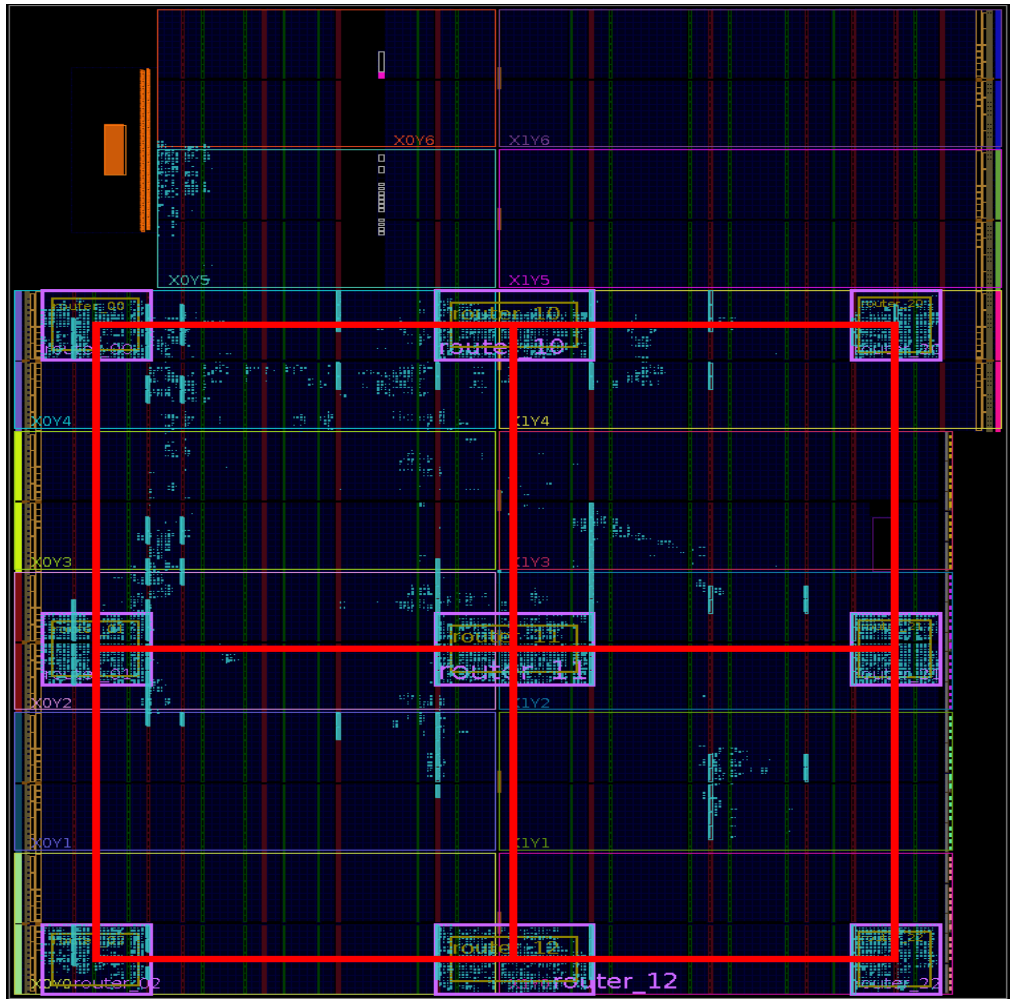




NoCTurnal Zynq-7100 and P-Blocks



- Partition fabric into 9 regions using P-blocks
- 2D 3x3 Mesh
- Implemented 150 MHz

NoCTurnal Summary

				January				February				March				April		
ID	**Task**	**Who**	**Status**	**9**	**16**	**23**	**30**	**6**	**13**	**20**	**27**	**6**	**13**	**20**	**27**	**3**	**10**	**17**
1	SW/NoC Simulation	Daniel	Done															
2	HDL/NIC	Daniel	SoC Tested															
3	SW/NIC Baremetal Driver	Daniel	SoC Tested															
4	HDL/Router/FIFO Struct.	Sebastian	SoC Tested															
5	HDL/Router/Switch Logic	Sebastian	SoC Tested															
6	Vivado Integration	Sebastian	SoC Tested															
7	Testing	Both	Done															