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**The University of Kansas**

**School of Engineering**

**Department of Electrical Engineering and Computer Science**

EECS 645 – Computer Architecture

Fall 2015

Homework 02 (Resource Sharing)

Student Name: Student ID:

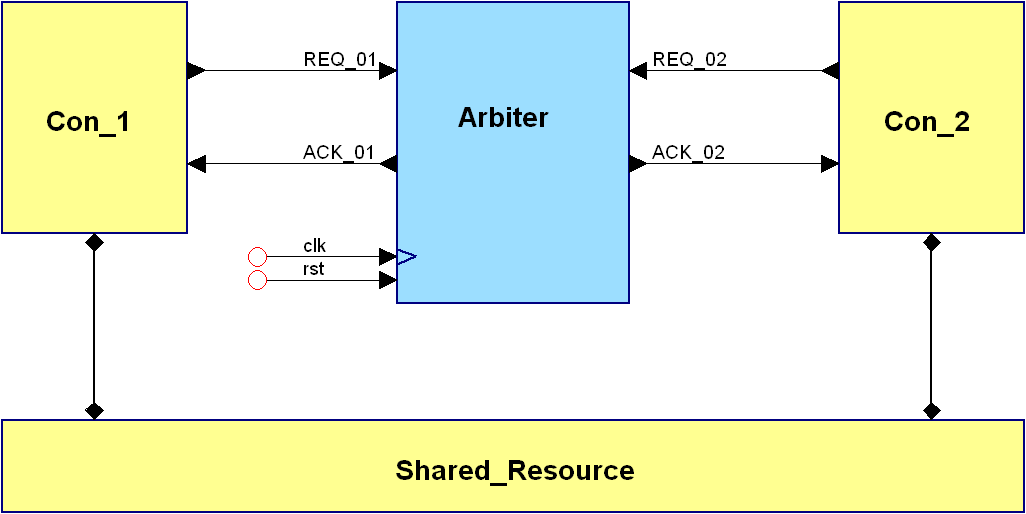
**Lecture Example (Template Answer):**

Given a resource that is to be shared by two consumers such that only one consumer has access to the resource at any given time. The policy of access is non-preemptive with no priority. More specifically the policy is as follows:

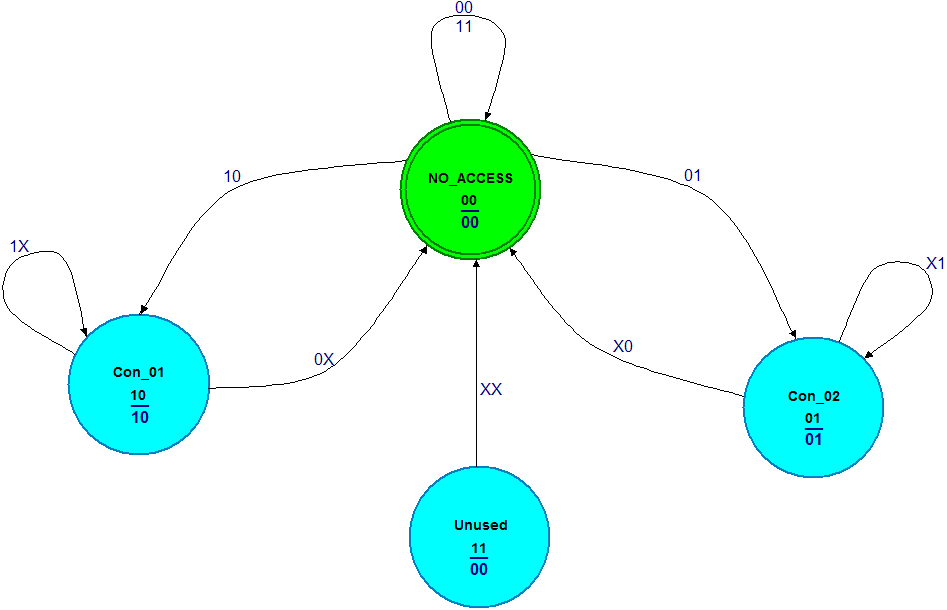
* When the resource is idle and the consumers simultaneously request the resource, their requests are ignored until only one request is submitted
* When the resource is being accessed by any of the consumers, the consumers are scheduled as First-Come-First-Served (FCFS)

Design a two-consumer arbiter/controller that controls the access to the shared resource and implements the above policy. In the design process, provide the following:

1. The system architecture (block diagram) showing the interface ports to the arbiter including the clock and reset signals.
2. Finite State Machine (FSM) diagram showing all possible states, transitions, and output values.
3. K-maps for internal state and output variables.
4. Boolean expressions for internal state and output variables.
5. Detailed logic diagram using synchronous memory elements showing internal connections and external interfaces.
6. Complete description of the arbiter using VHDL code.
7. Complete VHDL testbench along with simulation results.



**Figure 1: System architecture**



**Figure 2: State transition diagram**

**Table 1: State transition table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Next State**  **(S1 , S2)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** | **00** | **01** | **00** | **10** |
| **01** | **00** | **01** | **01** | **00** |
| **11** | **00** | **00** | **00** | **00** |
| **10** | **00** | **00** | **10** | **10** |

**Table 2: K-map for the state variable *S1***

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Next State**  **(S1)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** |  |  |  | **1** |
| **01** |  |  |  |  |
| **11** |  |  |  |  |
| **10** |  |  | **1** | **1** |



**Table 3: K-map for the state variable *S2***

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Next State**  **(S2)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** |  | **1** |  |  |
| **01** |  | **1** | **1** |  |
| **11** |  |  |  |  |
| **10** |  |  |  |  |



**Table 4: Output transition table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Outputs**  **(ACK1 , ACK2)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** | **00** | **00** | **00** | **00** |
| **01** | **01** | **01** | **01** | **01** |
| **11** | **00** | **00** | **00** | **00** |
| **10** | **10** | **10** | **10** | **10** |

**Table 5: K-map for the output variable ACK1**

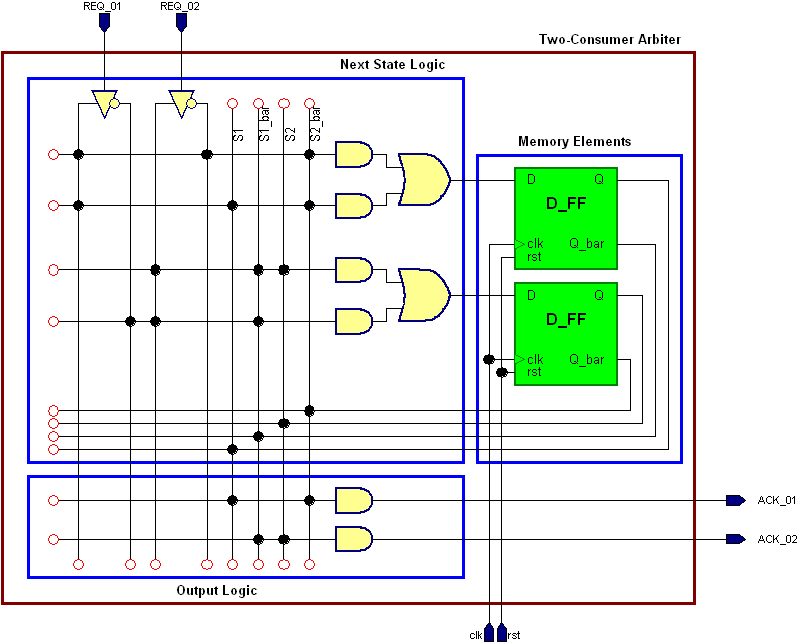
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Outputs**  **(ACK1)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** |  |  |  |  |
| **01** |  |  |  |  |
| **11** |  |  |  |  |
| **10** | **1** | **1** | **1** | **1** |



**Table 6: K-map for the output variable ACK2**

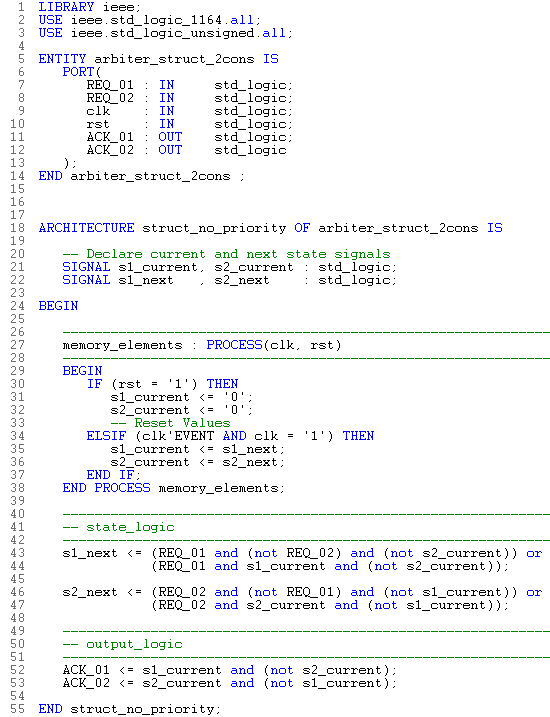
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Outputs**  **(ACK2)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** |  |  |  |  |
| **01** | **1** | **1** | **1** | **1** |
| **11** |  |  |  |  |
| **10** |  |  |  |  |



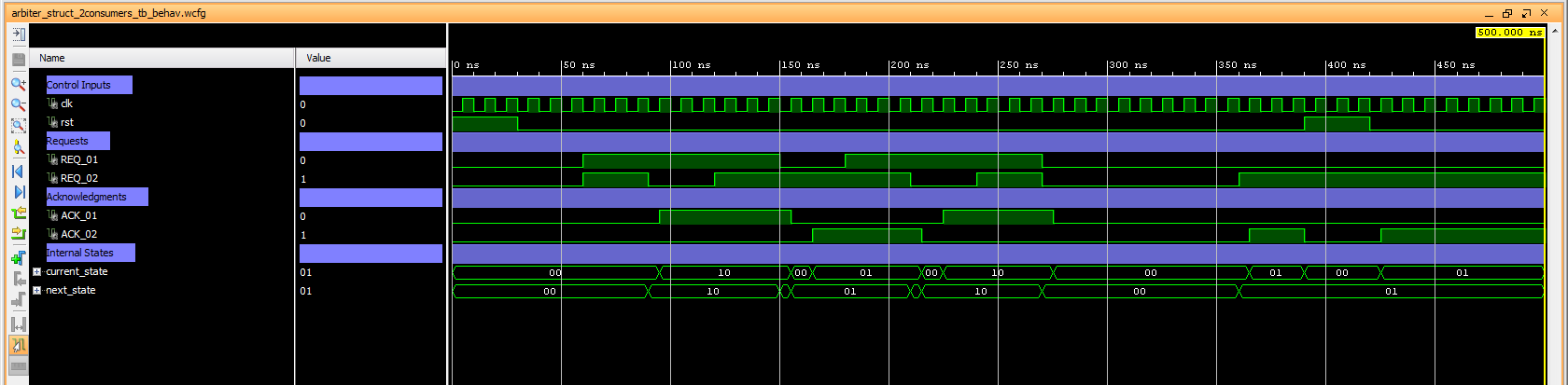


**Figure 3: Synchronous logic diagram**

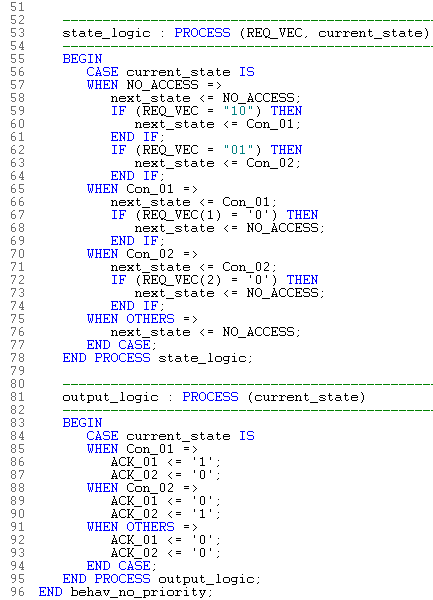
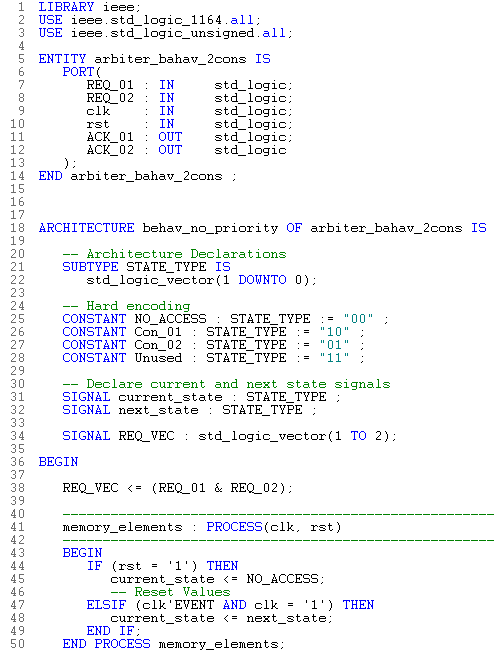
**Structural VHDL code**



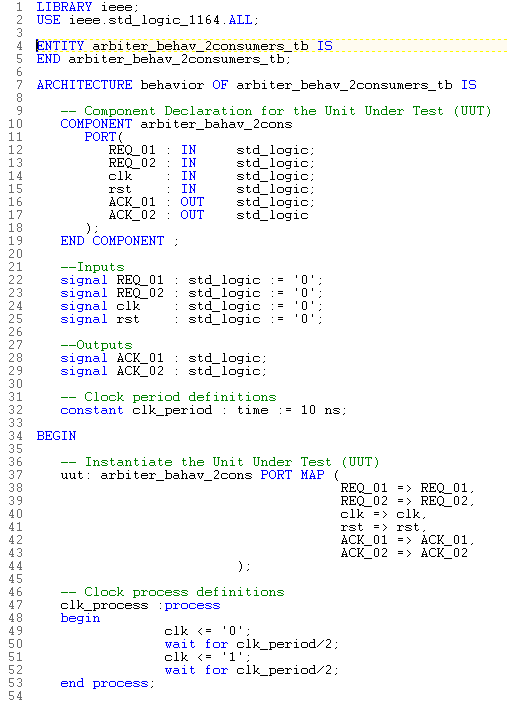
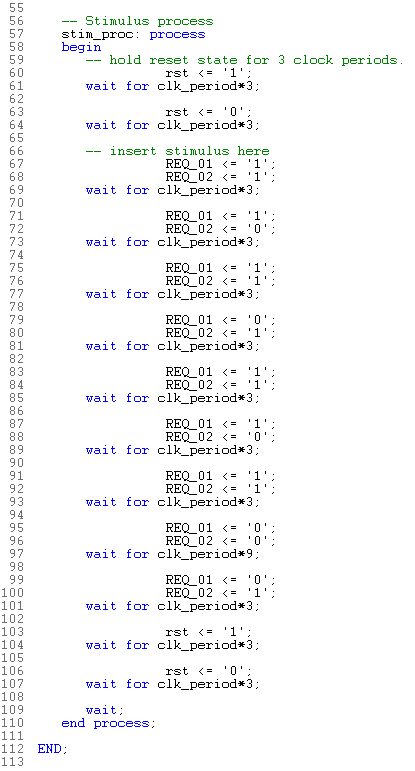
**Testbench and Simulation Results**

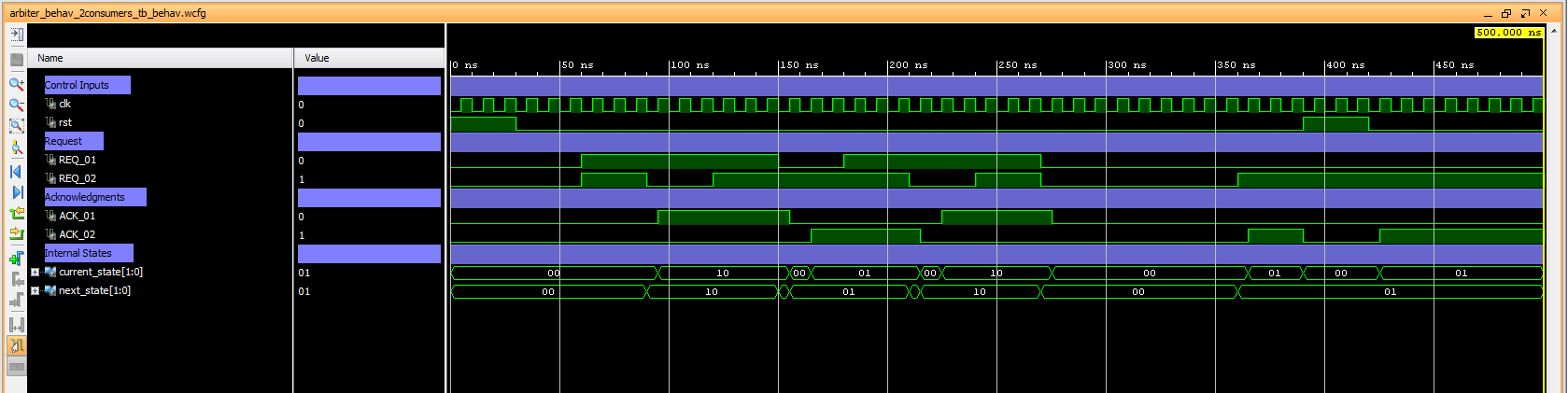


**Behavioral VHDL code**



**Testbench and Simulation Results**



**Homework Problem I:**

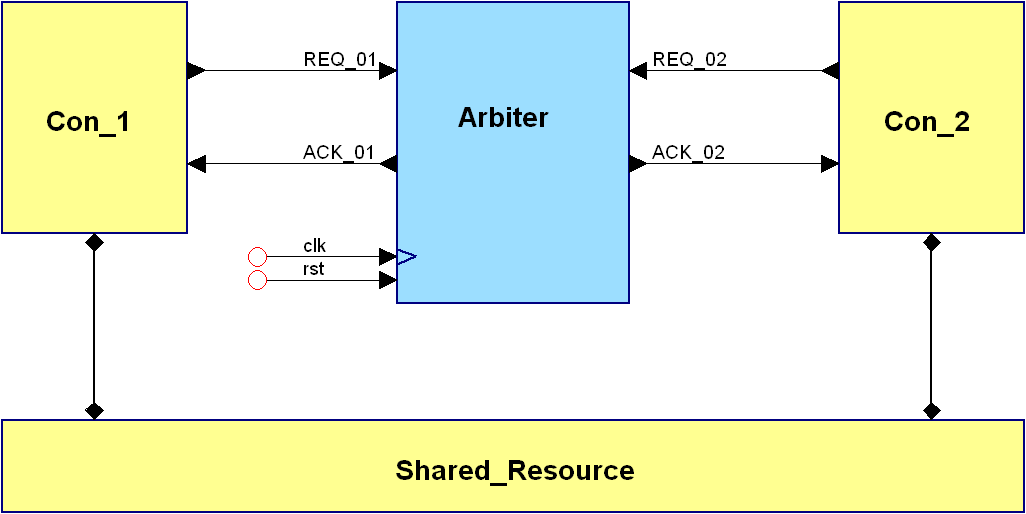
Given a resource that is to be shared by two consumers such that only one consumer has access to the resource at any given time. The policy of access is non-preemptive with priority determined by the consumer index. More specifically the policy is as follows:

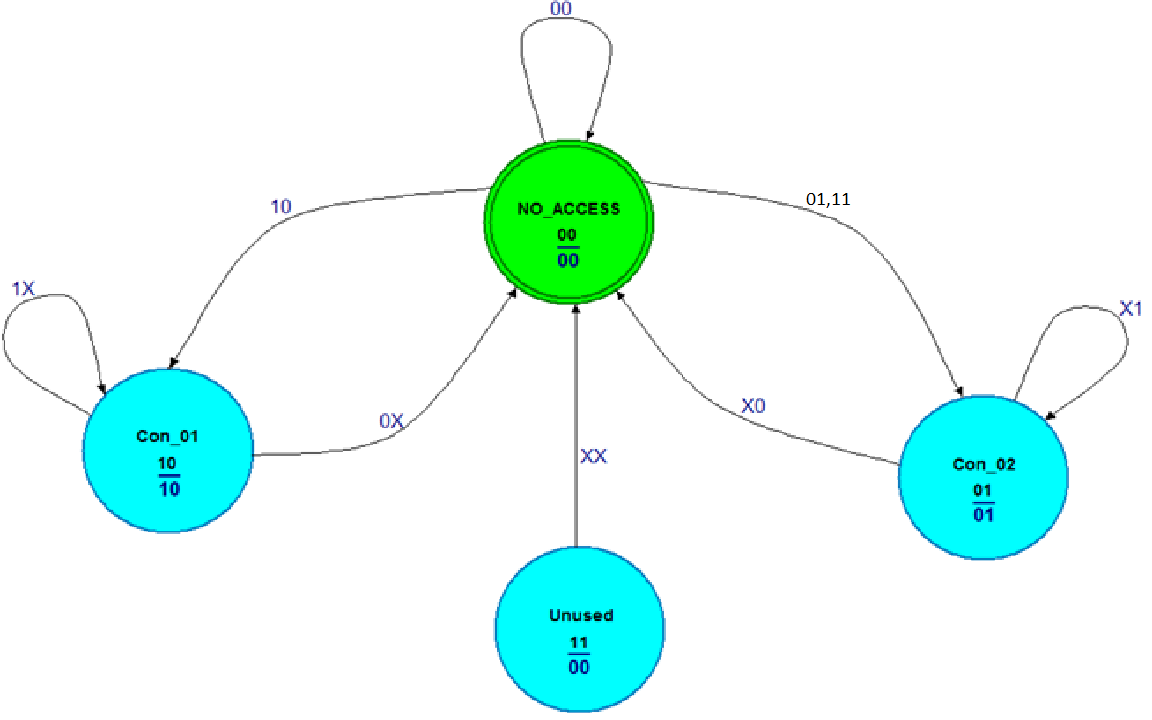
* When the resource is idle and the consumers simultaneously request the resource, the consumers are prioritized according to their consumer number (i.e. consumer 2 has a higher priority than consumer 1)
* When the resource is being accessed by any of the consumers, the consumers are scheduled as First-Come-First-Served (FCFS)

Design a two-consumer arbiter/controller that controls the access to the shared resource and implements the above policy. In the design process, provide the following:

1. The system architecture (block diagram) showing the interface ports to the arbiter including the clock and reset signals.
2. Finite State Machine (FSM) diagram showing all possible states, transitions, and output values.
3. K-maps for internal state and output variables.
4. Boolean expressions for internal state and output variables.
5. Detailed logic diagram using synchronous memory elements showing internal connections and external interfaces.
6. Complete description of the arbiter using VHDL code.
7. Complete VHDL testbench along with simulation results.

**Figure 1: System architecture**

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**Figure 2: State transition diagram**

**Table 1: State transition table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Next State**  **(S1 , S2)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** | **00** | **01** | **01** | **10** |
| **01** | **00** | **01** | **01** | **00** |
| **11** | **00** | **00** | **00** | **00** |
| **10** | **00** | **00** | **10** | **10** |

**Table 2: K-map for the state variable *S1***

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Next State**  **(S1 )** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** |  |  |  | **1** |
| **01** |  |  |  |  |
| **11** |  |  |  |  |
| **10** |  |  | **1** | **1** |



**Table 3: K-map for the state variable *S2***

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Next State**  **(S2)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** |  | **1** | **1** |  |
| **01** |  | **1** | **1** |  |
| **11** |  |  |  |  |
| **10** |  |  |  |  |



**Table 4: Output transition table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Outputs**  **(ACK1 , ACK2)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** | 00 | 00 | 00 | 00 |
| **01** | 01 | 01 | 01 | 01 |
| **11** | 00 | 00 | 00 | 00 |
| **10** | 10 | 10 | 10 | 10 |

**Table 5: K-map for the output variable ACK1**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Outputs**  **(ACK1)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** |  |  |  |  |
| **01** |  |  |  |  |
| **11** |  |  |  |  |
| **10** | 1 | 1 | 1 | 1 |



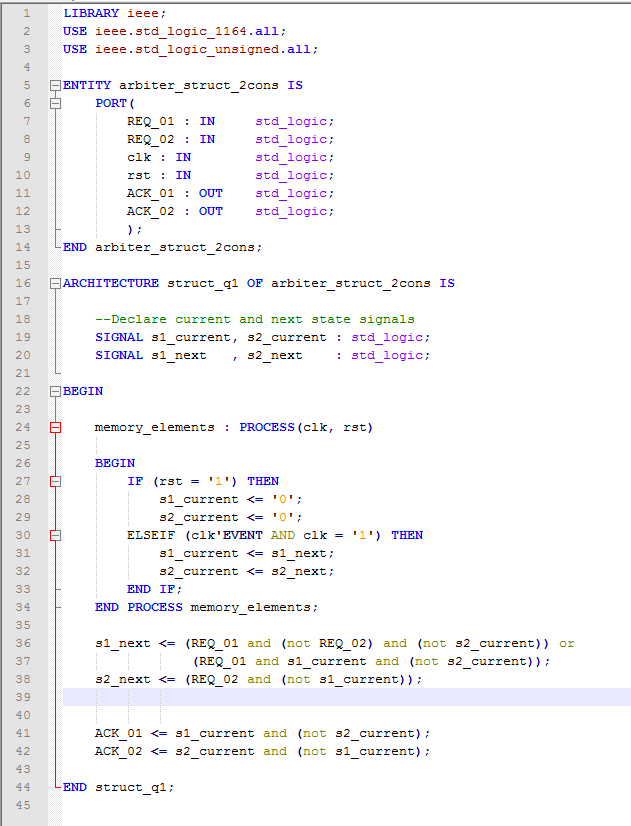
**Table 6: K-map for the output variable ACK2**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Outputs**  **(ACK2)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** |  |  |  |  |
| **01** | 1 | 1 | 1 | 1 |
| **11** |  |  |  |  |
| **10** |  |  |  |  |

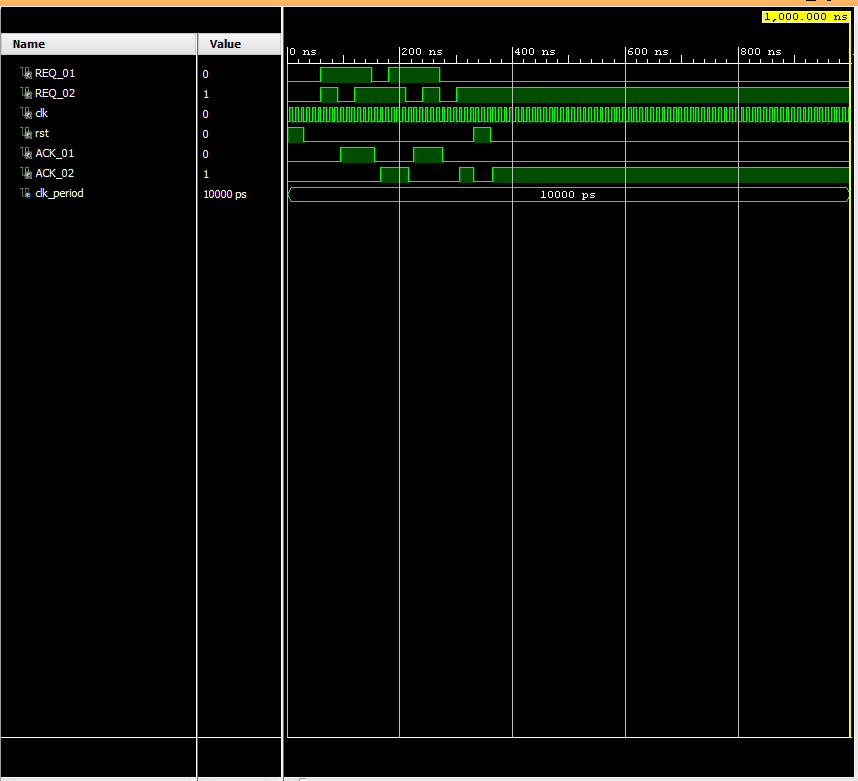


**Figure 3: Synchronous logic diagram**

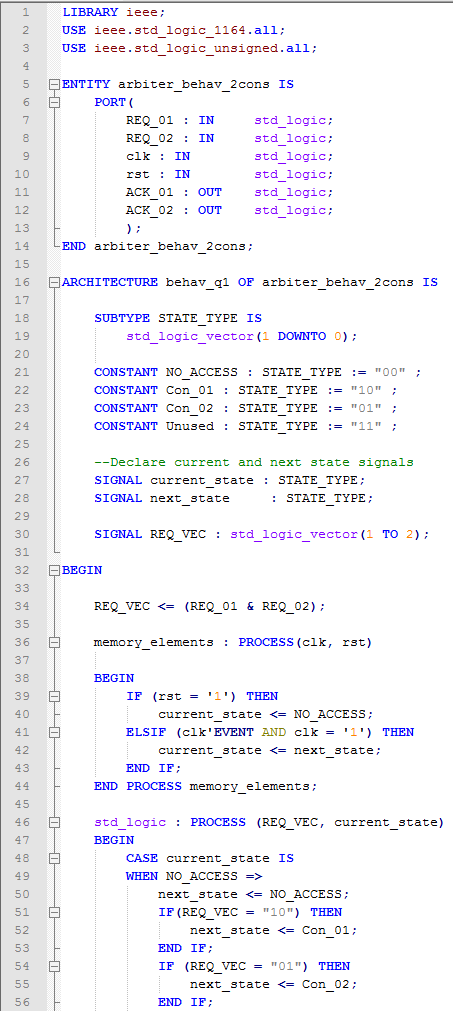
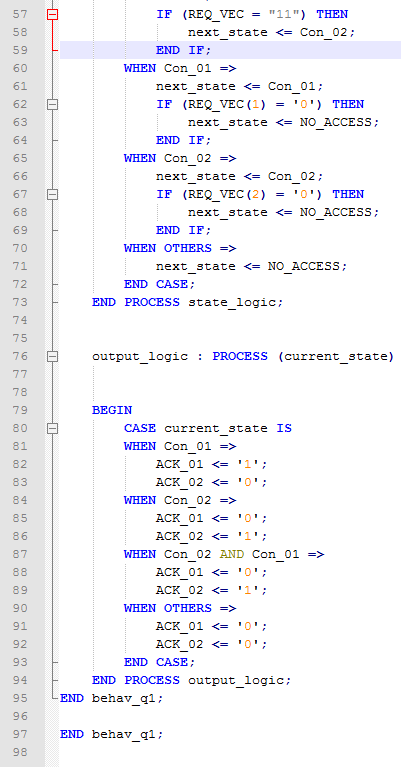
**Structural VHDL code**

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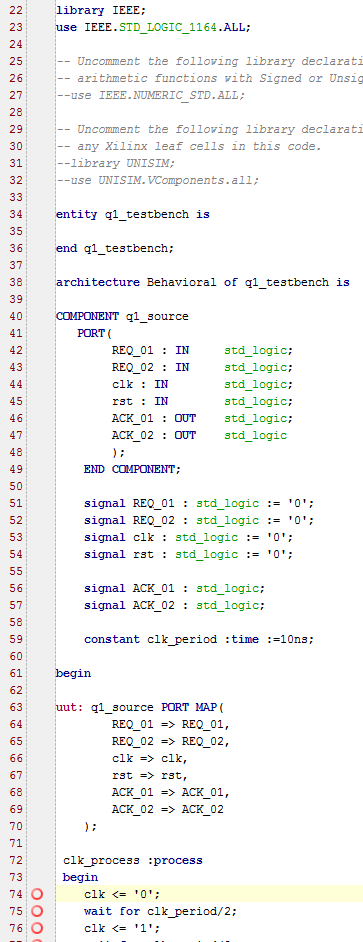
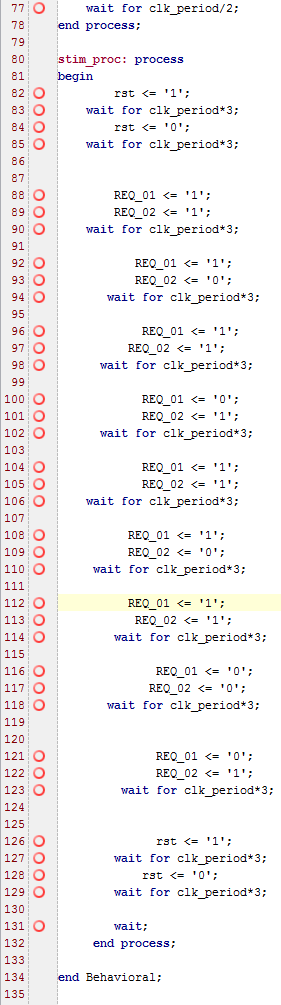
**Testbench and Simulation Results**



**Behavioral VHDL code**

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**Testbench and Simulation Results**

** **

**Homework Problem II:**

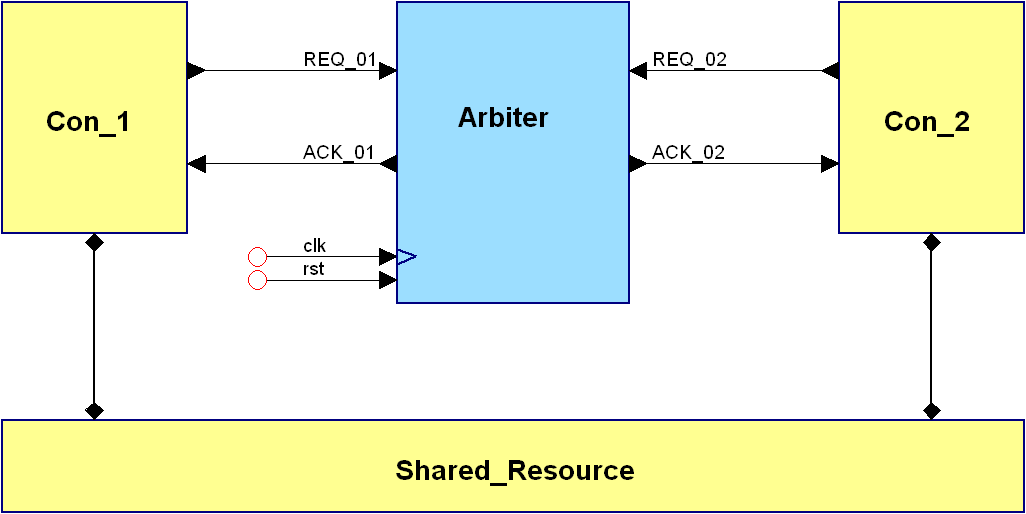
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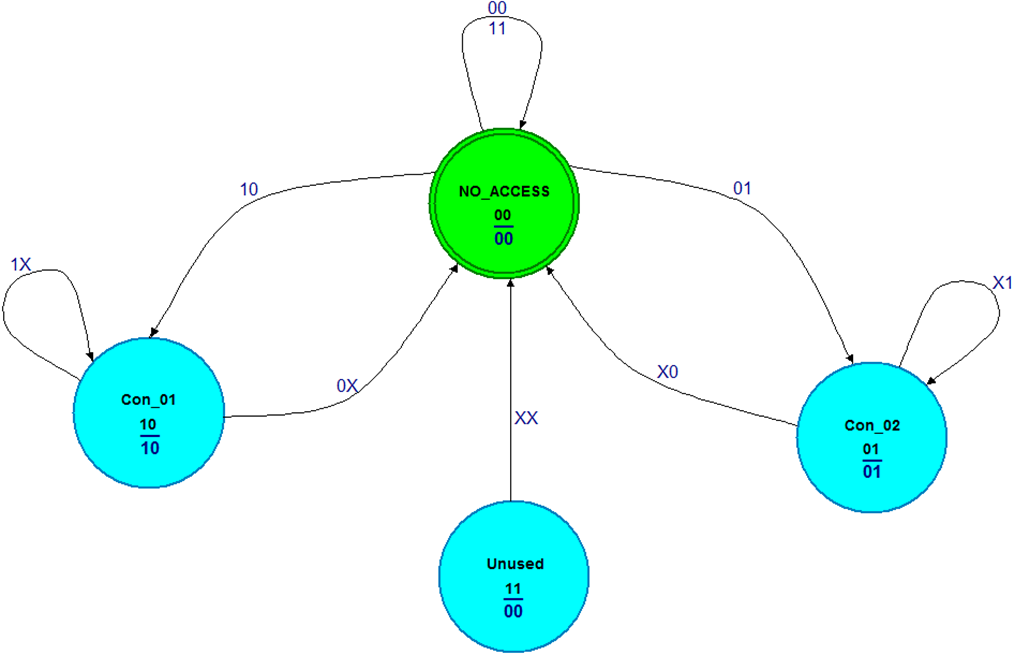
* When the resource is idle and the consumers simultaneously request the resource, the consumers are prioritized according to their consumer number (i.e. consumer 1 has a higher priority than consumer 2)
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Design a two-consumer arbiter/controller that controls the access to the shared resource and implements the above policy. In the design process, provide the following:

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5. Detailed logic diagram using synchronous memory elements showing internal connections and external interfaces.
6. Complete description of the arbiter using VHDL code.
7. Complete VHDL testbench along with simulation results.

**Figure 1: System architecture**

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**Figure 2: State transition diagram**

**Table 1: State transition table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Next State**  **(S1 , S2)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** | **00** | **01** | **10** | **10** |
| **01** | **00** | **01** | **01** | **00** |
| **11** | **00** | **00** | **00** | **00** |
| **10** | **00** | **00** | **10** | **10** |

**Table 2: K-map for the state variable *S1***

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Next State**  **(S1 )** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** |  |  | **1** | **1** |
| **01** |  |  |  |  |
| **11** |  |  |  |  |
| **10** |  |  | **1** | **1** |



**Table 3: K-map for the state variable *S2***

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Next State**  **(S2)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** |  | **1** |  |  |
| **01** |  | **1** | **1** |  |
| **11** |  |  |  |  |
| **10** |  |  |  |  |



**Table 4: Output transition table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Outputs**  **(ACK1 , ACK2)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** | **00** | **00** | **00** | **00** |
| **01** | **01** | **01** | **01** | **01** |
| **11** | 00 | 00 | 00 | 00 |
| **10** | **10** | **10** | **10** | **10** |

**Table 5: K-map for the output variable ACK1**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Outputs**  **(ACK1)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** |  |  |  |  |
| **01** |  |  |  |  |
| **11** |  |  |  |  |
| **10** | **1** | **1** | **1** | **1** |



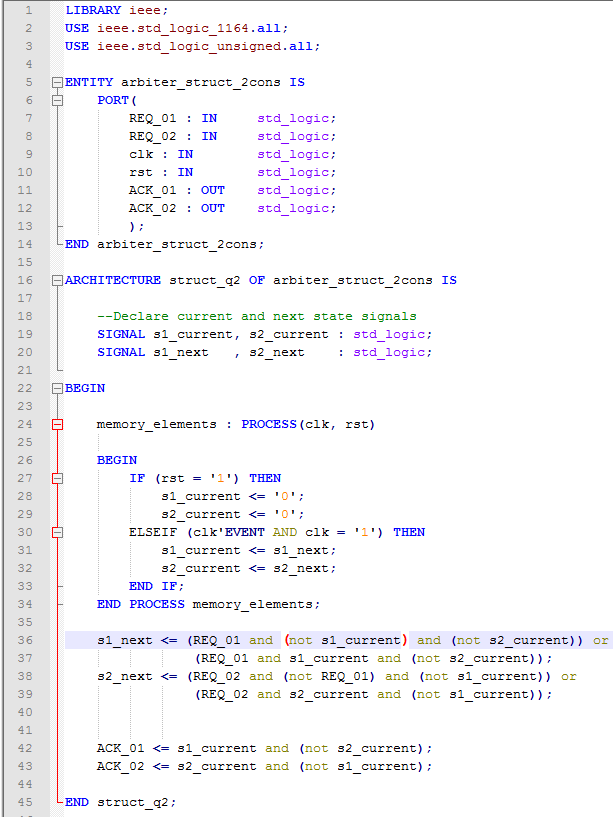
**Table 6: K-map for the output variable ACK2**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Outputs**  **(ACK2)** | | **Inputs**  **(REQ1 , REQ2)** | | | |
| **00** | **01** | **11** | **10** |
| **Current State**  **(S1 , S2)** | **00** |  |  |  |  |
| **01** | **1** | **1** | **1** | **1** |
| **11** |  |  |  |  |
| **10** |  |  |  |  |

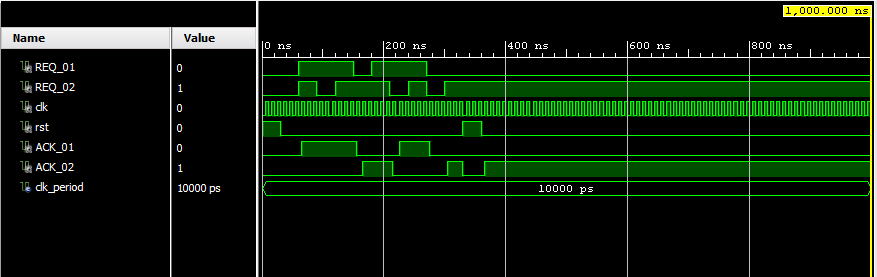


**Figure 3: Synchronous logic diagram**

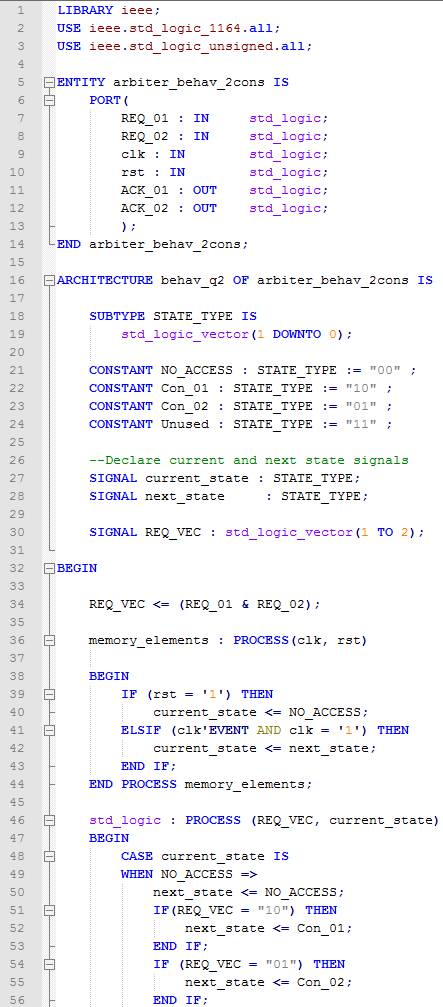
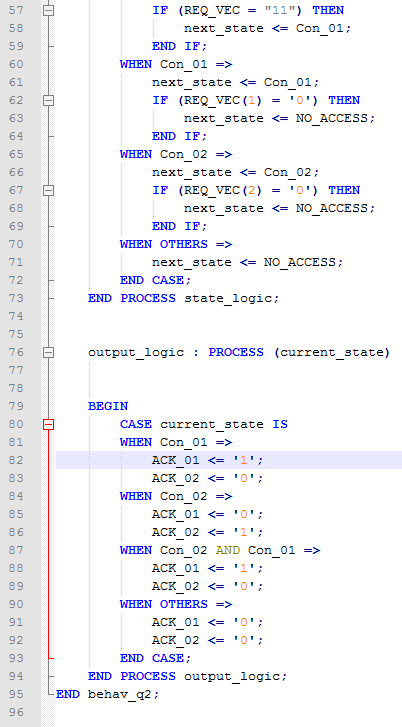
**Structural VHDL code**



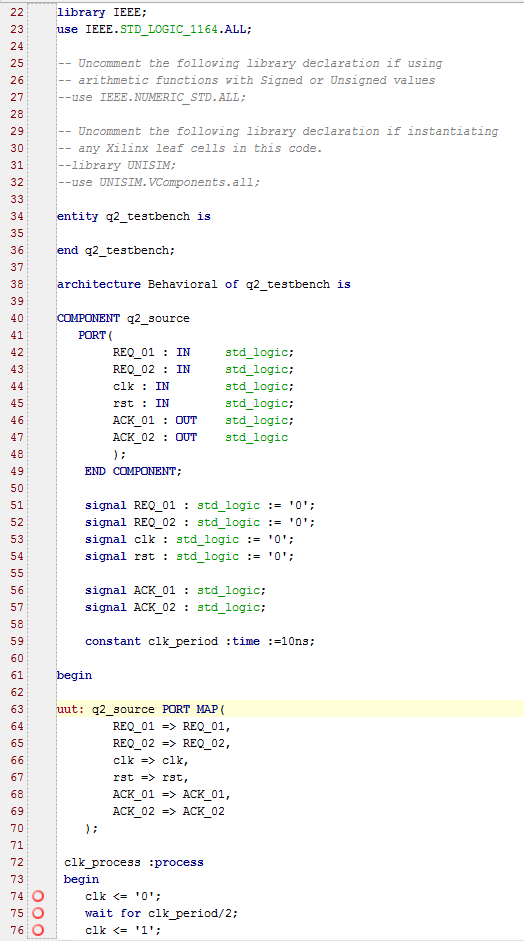
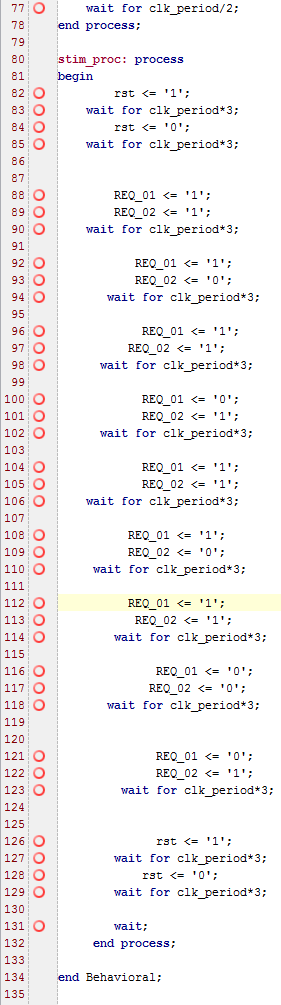
**Testbench and Simulation Results**



**Behavioral VHDL code**

**Testbench and Simulation Results**

**Homework Problem III:**

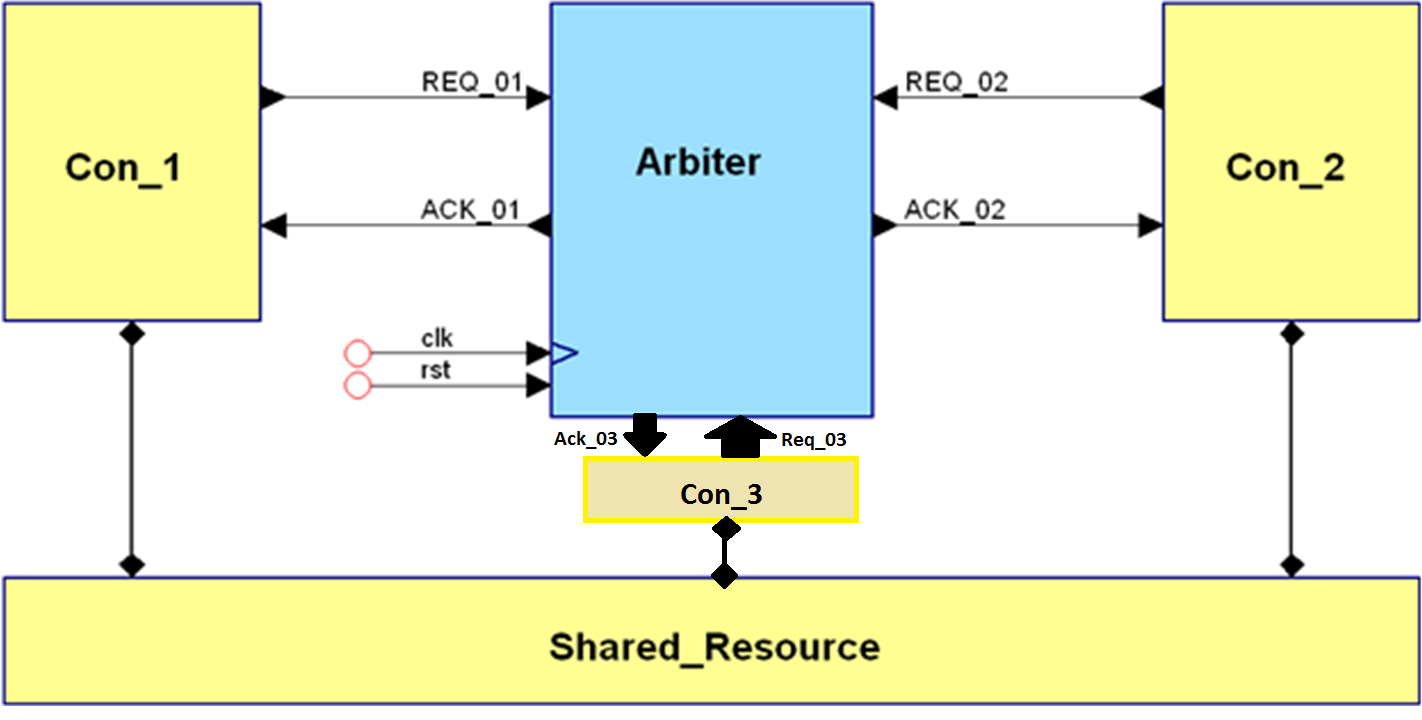
Given a resource that is to be shared by three consumers such that only one consumer has access to the resource at any given time. The policy of access is non-preemptive with no priority. More specifically the policy is as follows:

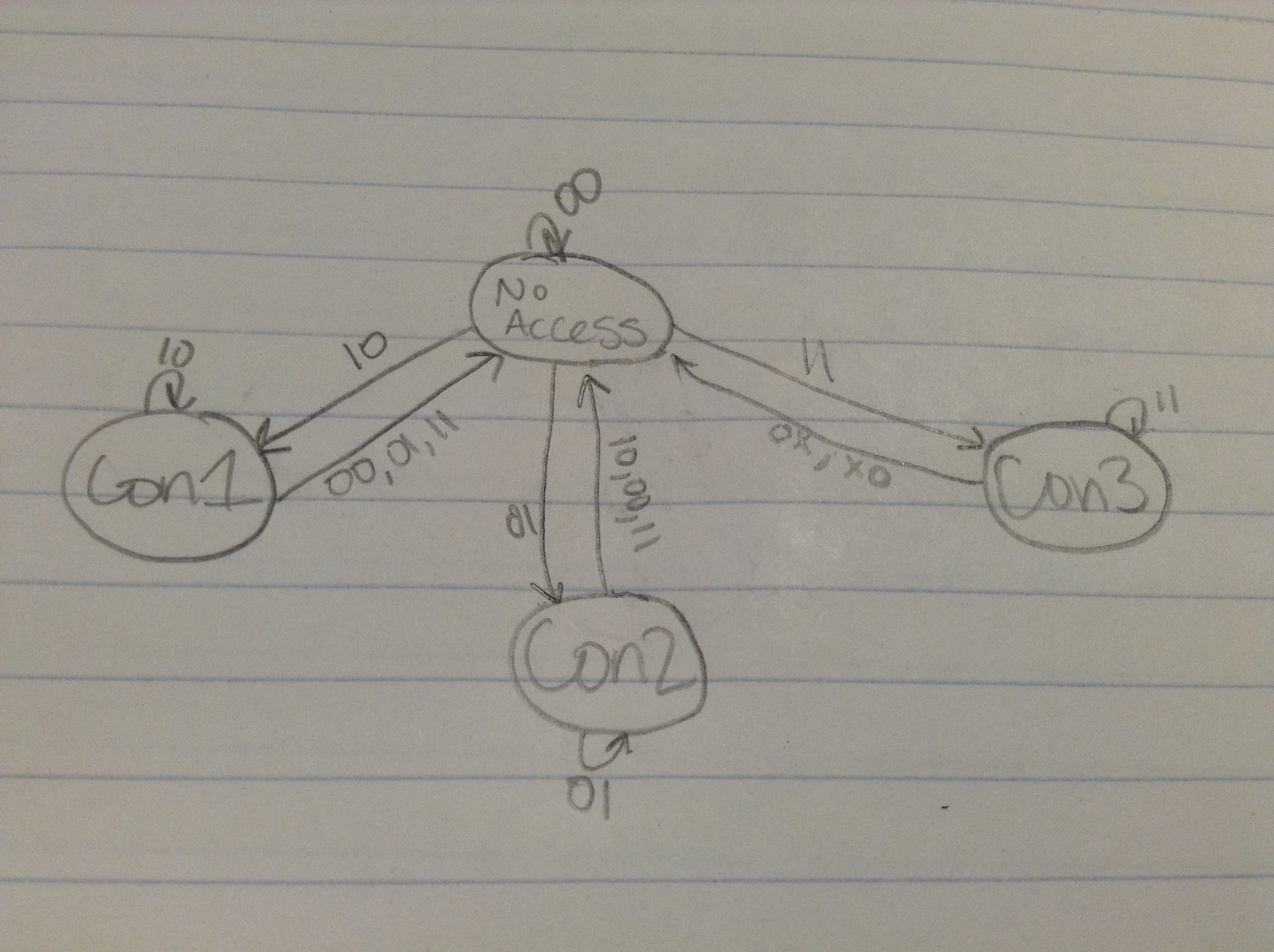
* When the resource is idle and the consumers simultaneously request the resource, their requests are ignored until only one request is submitted
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Design a three-consumer arbiter/controller that controls the access to the shared resource and implements the above policy. In the design process, provide the following:

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7. Complete VHDL testbench along with simulation results.

**Figure 1: System architecture**

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**Figure 2: State transition diagram**

**Table 1: State transition table**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Next State**  **(S1 , S2)** | | **Inputs**  **(REQ1 , REQ2 , REQ3)** | | | | | | | |
| **000** | **001** | **011** | **010** | **110** | **111** | **101** | **100** |
| **Current State**  **(S1 , S2)** | **00** | **00** |  | **00** |  | **00** | **00** | **00** |  |
| **01** |  |  |  |  |  |  |  |  |
| **11** | 00 |  |  |  |  |  |  |  |
| **10** |  |  |  |  |  |  |  |  |

**Table 2: K-map for the state variable *S1***

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Next State**  **(S1)** | | **Inputs**  **(REQ1 , REQ2 , REQ3)** | | | | | | | |
| **000** | **001** | **011** | **010** | **110** | **111** | **101** | **100** |
| **Current State**  **(S1 , S2)** | **00** |  | **1** |  | **1** |  |  |  |  |
| **01** |  |  |  |  |  |  |  |  |
| **11** |  | 1 | 1 |  |  | 1 | 1 |  |
| **10** |  |  | **1** | **1** | **1** | **1** |  |  |



**Table 3: K-map for the state variable *S2***

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Next State**  **(S2)** | | **Inputs**  **(REQ1 , REQ2 , REQ3)** | | | | | | | |
| **000** | **001** | **011** | **010** | **110** | **111** | **101** | **100** |
| **Current State**  **(S1 , S2)** | **00** |  | **1** |  |  |  |  | **1** | **1** |
| **01** |  |  |  |  | **1** | **1** | **1** | **1** |
| **11** |  | 1 | 1 |  |  | 1 | 1 |  |
| **10** |  |  |  |  |  |  |  |  |





**Table 4: Output transition table**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Outputs**  **(ACK1 , ACK2 , ACK3)** | | **Inputs**  **(REQ1 , REQ2 , REQ3)** | | | | | | | |
| **000** | **001** | **011** | **010** | **110** | **111** | **101** | **100** |
| **Current State**  **(S1 , S2)** | **00** |  |  |  |  |  |  |  |  |
| **01** |  |  |  |  |  |  |  |  |
| **11** |  |  |  |  |  |  |  |  |
| **10** |  |  |  |  |  |  |  |  |

**Table 5: K-map for the output variable ACK1**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Outputs**  **(ACK1)** | | **Inputs**  **(REQ1 , REQ2 , REQ3)** | | | | | | | |
| **000** | **001** | **011** | **010** | **110** | **111** | **101** | **100** |
| **Current State**  **(S1 , S2)** | **00** |  |  |  |  |  |  |  |  |
| **01** |  |  |  |  |  |  |  |  |
| **11** |  |  |  |  |  |  |  |  |
| **10** |  |  |  |  |  |  |  |  |



**Table 6: K-map for the output variable ACK2**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Outputs**  **(ACK2)** | | **Inputs**  **(REQ1 , REQ2 , REQ3)** | | | | | | | |
| **000** | **001** | **011** | **010** | **110** | **111** | **101** | **100** |
| **Current State**  **(S1 , S2)** | **00** |  |  |  |  |  |  |  |  |
| **01** |  |  |  |  |  |  |  |  |
| **11** |  |  |  |  |  |  |  |  |
| **10** |  |  |  |  |  |  |  |  |



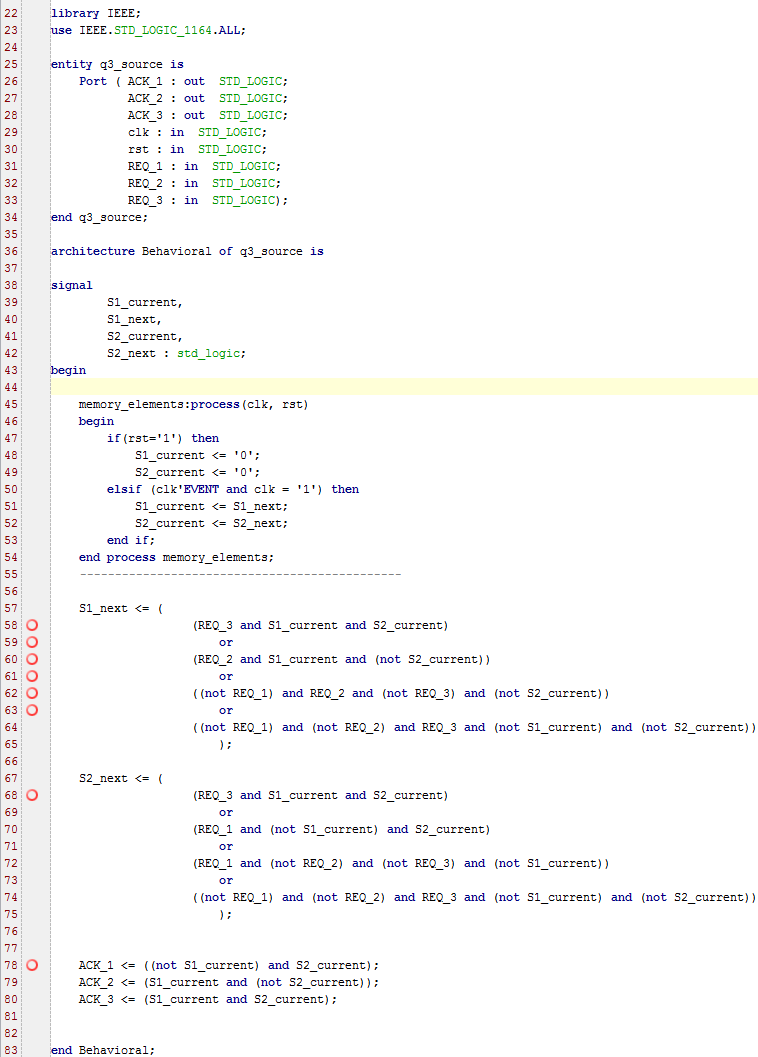
**Table 7: K-map for the output variable ACK3**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Outputs**  **(ACK3)** | | **Inputs**  **(REQ1 , REQ2 , REQ3)** | | | | | | | |
| **000** | **001** | **011** | **010** | **110** | **111** | **101** | **100** |
| **Current State**  **(S1 , S2)** | **00** |  |  |  |  |  |  |  |  |
| **01** |  |  |  |  |  |  |  |  |
| **11** |  |  |  |  |  |  |  |  |
| **10** |  |  |  |  |  |  |  |  |

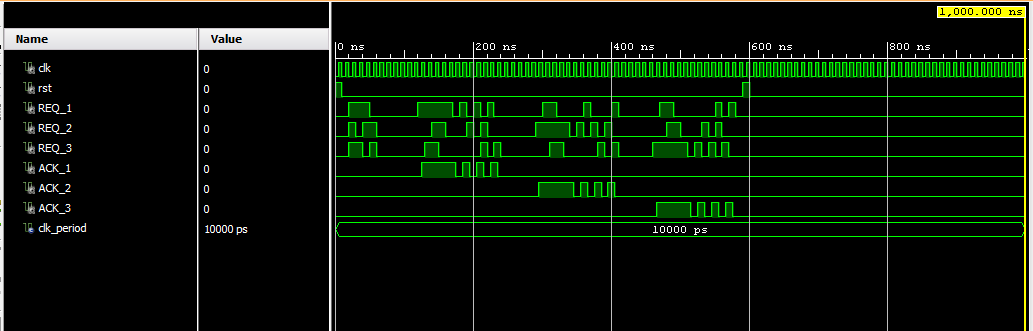


**Figure 3: Synchronous logic diagram**

**Structural VHDL code**



**Testbench and Simulation Results**



**Behavioral VHDL code**

**Testbench and Simulation Results**

