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ECE554 Minilab1a Report

A. Github Repository Info

Link: https://github.com/ssankar25/ECE554_Minilabs/tree/main/1a

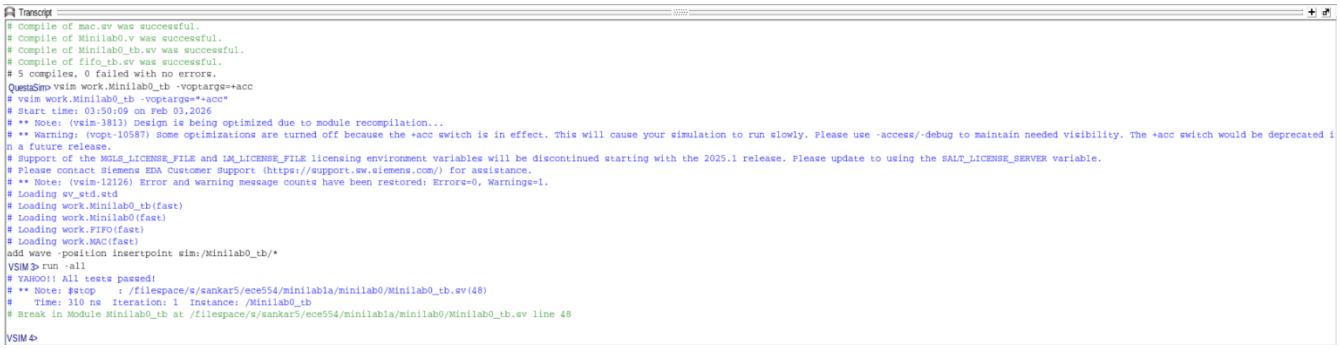
The .sv files for the first part of the project without any IP files are in the root of the repository. The .sv files that contain the implementation with the Quartus-provided IP files are in the "ip" folder of the repository. The waveforms and simulation logs, along with the resource utilization summaries, are located in the "sim" directory.

I created this repository by first creating a new repository from the GitHub homepage. I then used the "add files" and "upload files" features directly from the website to upload these files. This allowed me to easily structure the repository even though the files were in different places on my local machine.

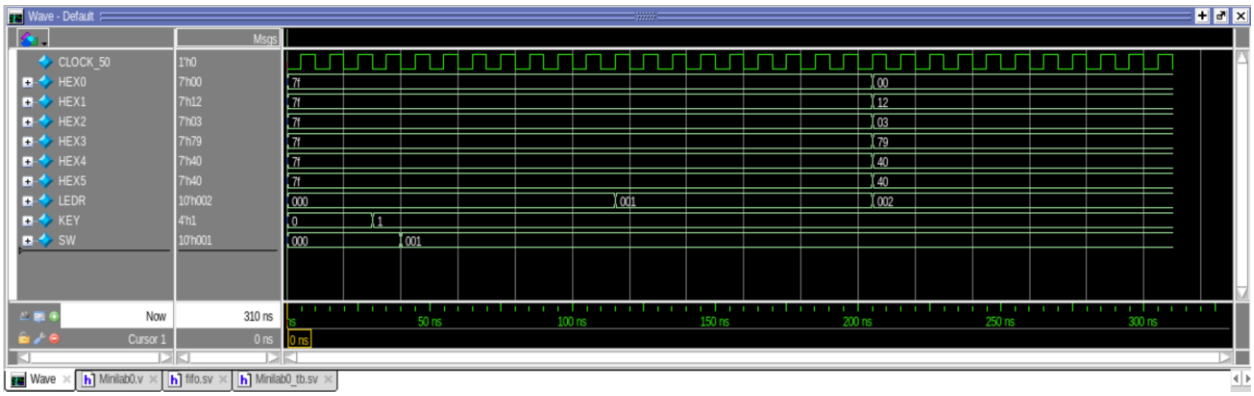
B. Simulation Logs and Waveforms

Screenshots for the Minilab0_tb simulation for both the IP and non-IP implementations are shown below.

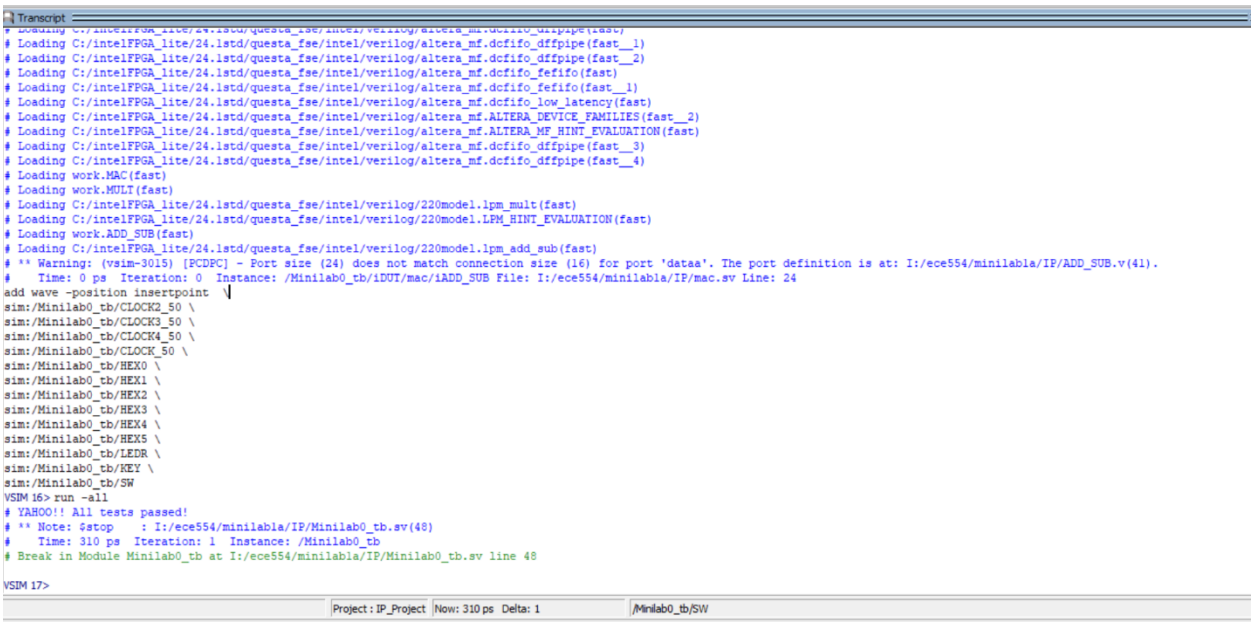
Non-IP simulation log:



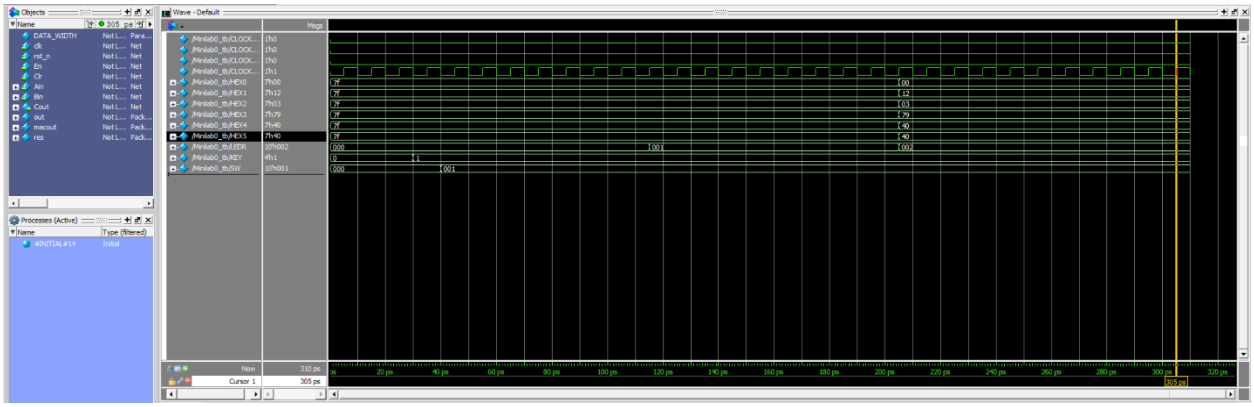
Non-IP waveforms:



IP simulation log:



IP waveforms:



C. Resource Utilization

The resource utilization in the IP implementation in the second summary report file shows that this implementation uses less estimated logic ALMs than our implementation. This is likely because the IP implementations are more optimized for synthesis, which is why it requires less dedicated logic registers and functions. This is also why the IP implementation has less fan-out than our implementation.