

**Sandeep Sankar**

**3 February 2026**

## **ECE554 Minilab1a Report**

### **A. Github Repository Info**

Link: [https://github.com/ssankar25/ECE554\\_Minilabs/tree/main/1a](https://github.com/ssankar25/ECE554_Minilabs/tree/main/1a)

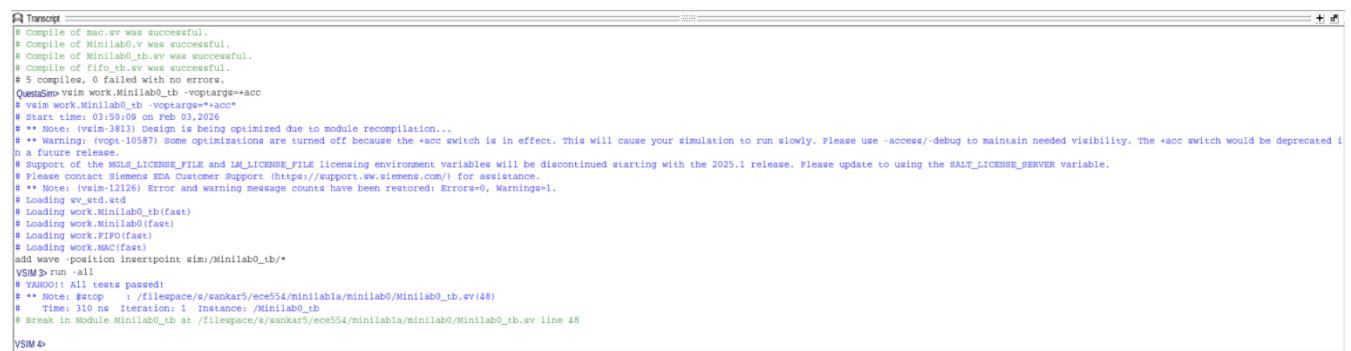
The .sv files for the first part of the project without any IP files are in the root of the repository. The .sv files that contain the implementation with the Quartus-provided IP files are in the “ip” folder of the repository. The waveforms and simulation logs, along with the resource utilization summaries, are located in the “sim” directory.

I created this repository by first creating a new repository from the GitHub homepage. I then used the “add files” and “upload files” features directly from the website to upload these files. This allowed me to easily structure the repository even though the files were in different places on my local machine.

### **B. Simulation Logs and Waveforms**

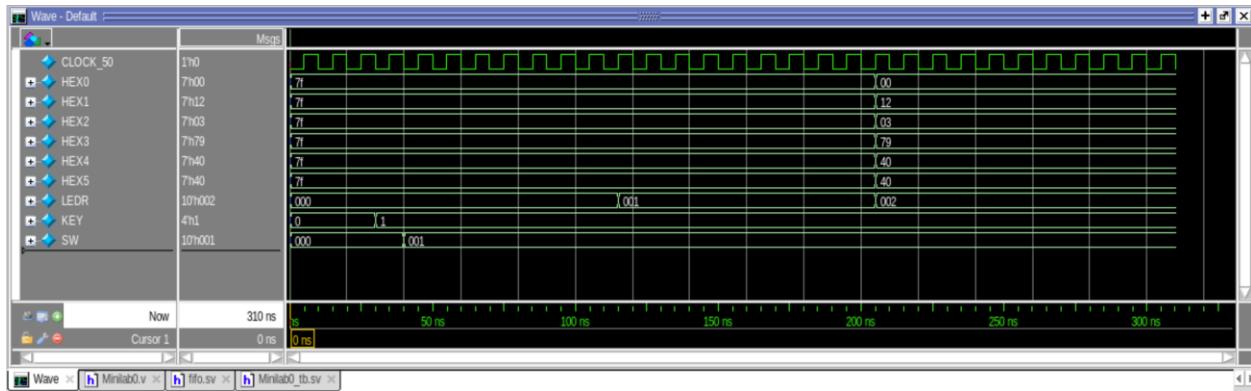
Screenshots for the Minilab0\_tb simulation for both the IP and non-IP implementations are shown below.

Non-IP simulation log:



```
# Transcript
# Compile of mac.sv was successful.
# Compile of Minilab0.v was successful.
# Compile of Minilab0_tb.v was successful.
# Compile of fifo_tb.sv was successful.
# 5 compiles, 0 failures with no errors.
QuartusSim vsim work.Minilab0_tb -voptargs+=acc
# State: 0.000000 ns
# Note: (vopt-1813) Design is being optimized due to module recompilation...
# ** Warning: (vopt-10587) Some optimizations are turned off because the +acc switch is in effect. This will cause your simulation to run slowly. Please use -access/-debug to maintain needed visibility. The +acc switch would be deprecated in a future release.
# Support of the MULS_LICENSE_FILE and LM_LICENSE_FILE licensing environment variables will be discontinued starting with the 2025.1 release. Please update to using the SALT_LICENSE_SERVER variable.
# Please contact Siemens EDA Customer Support (https://support.sv.siemens.com/) for assistance.
# * Note: (vopt-12126) Error and warning message counts have been restored: Errors=0, Warnings=1.
# Loading work.svd
# Loading work.Minilab0_tb(fast)
# Loading work.Minilab0(fast)
# Loading work.FIFO(fast)
# Loading work.MAC(fast)
add wave -position insertpoint sim:/Minilab0_tb/*
VSM> run -all
# VSM> 1000000 tests passed!
# ** Note: $stop - 1 /filespace/s/sankar5/ece554/minilab/minilab0/Minilab0_tb.sv(48)
# * Time: 310 ns Iteration: 1 Instance: /Minilab0_tb
# Break in Module Minilab0_tb at /filespace/s/sankar5/ece554/minilab/minilab0/Minilab0_tb.sv line 48
[VSM 4]
```

Non-IP waveforms:



## IP simulation log:

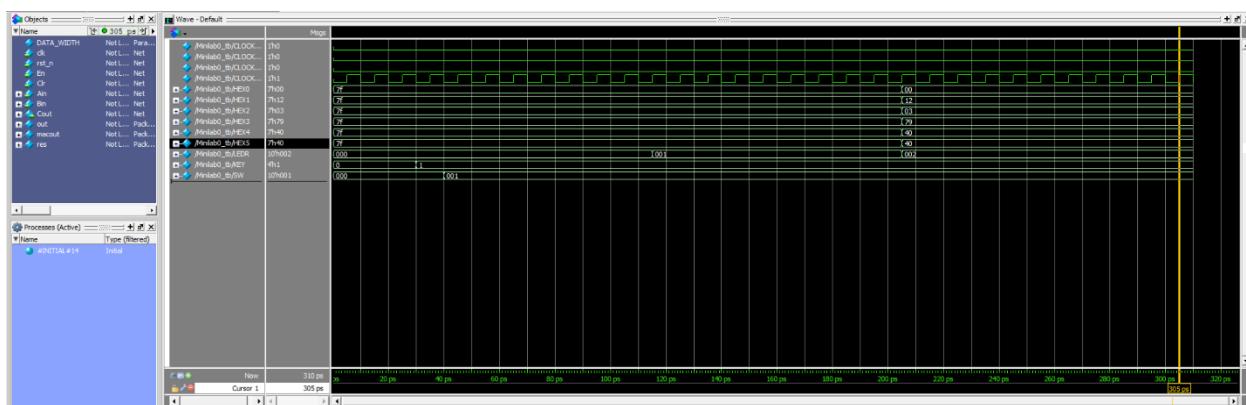
```

Transcript
# Loading C:/intelFPGA_lite/24.lstd/questa_fse/intel/verilog/altera_mf_dffpipe(fast)
# Loading C:/intelFPGA_lite/24.lstd/questa_fse/intel/verilog/altera_mf_dffpipe(fast_1)
# Loading C:/intelFPGA_lite/24.lstd/questa_fse/intel/verilog/altera_mf_dffpipe(fast_2)
# Loading C:/intelFPGA_lite/24.lstd/questa_fse/intel/verilog/altera_mf_dffpipe(fast_3)
# Loading C:/intelFPGA_lite/24.lstd/questa_fse/intel/verilog/altera_mf_dffpipe(fast_4)
# Loading C:/intelFPGA_lite/24.lstd/questa_fse/intel/verilog/altera_mf_ALTERA_DEVICE_FAMILY(fast_2)
# Loading C:/intelFPGA_lite/24.lstd/questa_fse/intel/verilog/altera_mf_ALTERA_M_HINT_EVALUATION(fast)
# Loading C:/intelFPGA_lite/24.lstd/questa_fse/intel/verilog/altera_mf_dffpipe(fast_3)
# Loading C:/intelFPGA_lite/24.lstd/questa_fse/intel/verilog/altera_mf_dffpipe(fast_4)
# Loading work.MAC(fast)
# Loading work.MULT(fast)
# Loading C:/intelFPGA_lite/24.lstd/questa_fse/intel/verilog/220model.lpm_mult(fast)
# Loading C:/intelFPGA_lite/24.lstd/questa_fse/intel/verilog/220model.LPM_HINT_EVALUATION(fast)
# Loading work.ADD_SUB(fast)
# Loading C:/intelFPGA_lite/24.lstd/questa_fse/intel/verilog/220model.lpm_add_sub(fast)
** Warning: (vsim-3015) [FCDCP] - Port size (24) does not match connection size (16) for port 'dataaa'. The port definition is at: I:/ece554/minilabla/IP/ADD_SUB.v(41).
# Time: 0 ps Iteration: 0 Instance: /Minilab0_tb/IDUT/mac/iADD_SUB File: I:/ece554/minilabla/IP/mac.v Line: 24
add wave -position insertpoint \
sim:/Minilab0_tb/CLOCK2_50 \
sim:/Minilab0_tb/CLOCK3_50 \
sim:/Minilab0_tb/CLOCK4_50 \
sim:/Minilab0_tb/CLOCK5_50 \
sim:/Minilab0_tb/HEX0 \
sim:/Minilab0_tb/HEX1 \
sim:/Minilab0_tb/HEX2 \
sim:/Minilab0_tb/HEX3 \
sim:/Minilab0_tb/HEX4 \
sim:/Minilab0_tb/HEX5 \
sim:/Minilab0_tb/LEDR \
sim:/Minilab0_tb/KEY \
sim:/Minilab0_tb/SW
VSIM 1> run -all
! YAYOO!! All tests passed!
# Note: @stop : I:/ece554/minilabla/IP/Minilab0_tb.sv(48)
# Time: 310 ps Iteration: 1 Instance: /Minilab0_tb
# Break in Module Minilab0_tb at I:/ece554/minilabla/IP/Minilab0_tb.sv line 48
VSDM 17>

```

Project: IP\_Project Now: 310 ps Delta: 1 /Minilab0\_tb/SW

## IP waveforms:



## C. Resource Utilization

The resource utilization in the IP implementation in the second summary report file shows that this implementation uses less estimated logic ALMs than our implementation. This is likely because the IP implementations are more optimized for synthesis, which is why it requires less dedicated logic registers and functions. This is also why the IP implementation has less fan-out than our implementation.