

MiniLab 1b Report

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Simulation:

We wrote a testbench that will wait until we have reached the DONE state in our top-level DUT and then we used the waveforms to see if we were reading the correct values from memory and achieving the correct output values from our MACs. These screenshots show the correct signals and output values.

See images of waveform on next page.

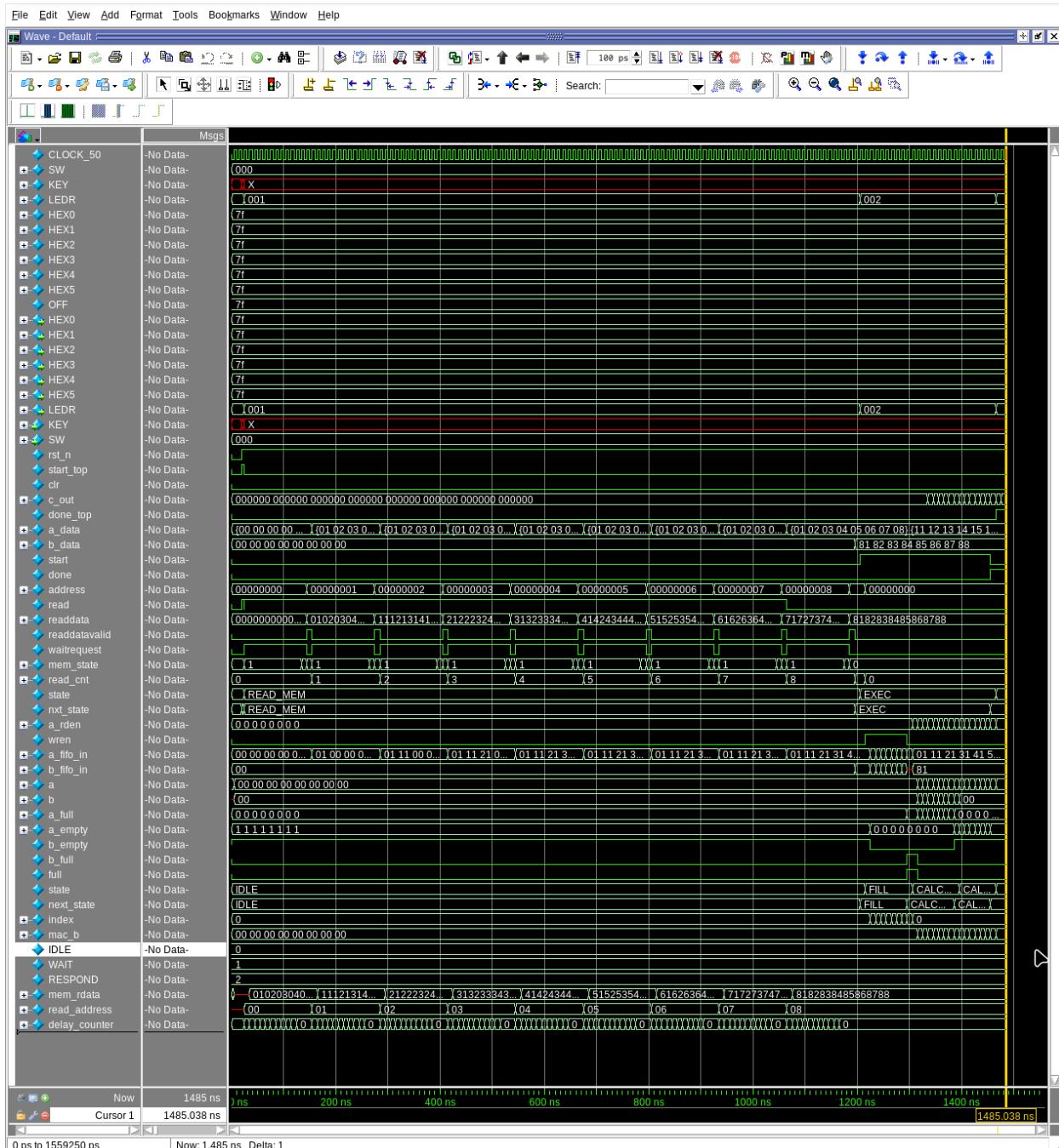


Image 1. Full waveform of whole simulation

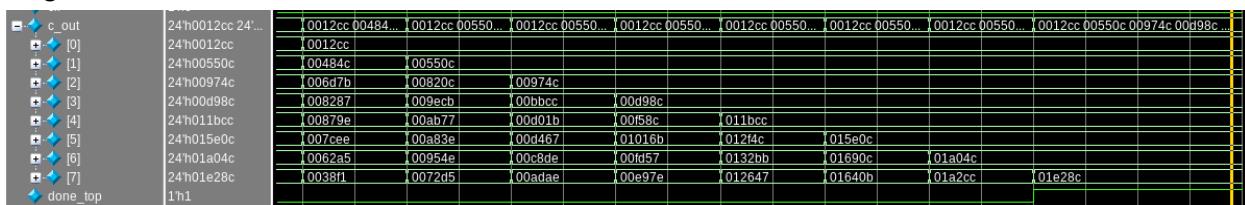


Image 2. Waveform of MAC output signal. Done gets asserted same clock cycle as last output

New Timing Constraints:

To meet a timing requirement of 200MHz, we flopped the multiplication in the MAC so that the multiplication and addition occurred one clock cycle apart. To account for this one clock cycle difference, the done signal also had to wait one clock cycle before assertion so the final MAC could finish. The image below shows that our Fmax is greater than the required 200 MHz.

Slow 1100mV 85C Model Fmax Summary				
	Fmax	Restricted Fmax	Clock Name	Note
1	51.55 MHz	51.55 MHz	altera...ed_tck	
2	217.44 MHz	217.44 MHz	CLOCK_50	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX such that the duty cycle (in terms of a percentage) is maintained.

Image 3. Timing Analysis Summary from Quartus. Row 1 is SignalTap and row 2 is the design

Design On Board:

The red LEDs (one is slightly hidden behind the sticker) represent the state of the state machine in the top level. Our DONE state corresponds to 3 which can be seen on the LEDs in binary. The seven segment display represents one output of the MAC at a time. The switches provide a one-hot signal that selects which MAC output is shown. The image shows our first MAC output (first element of the matrix multiplication result vector) which is the expected result. The first button (KEY0) is used to reset, the second (KEY1) is used to start the matrix multiplication, and the third (KEY2) is used to clear the MACs.

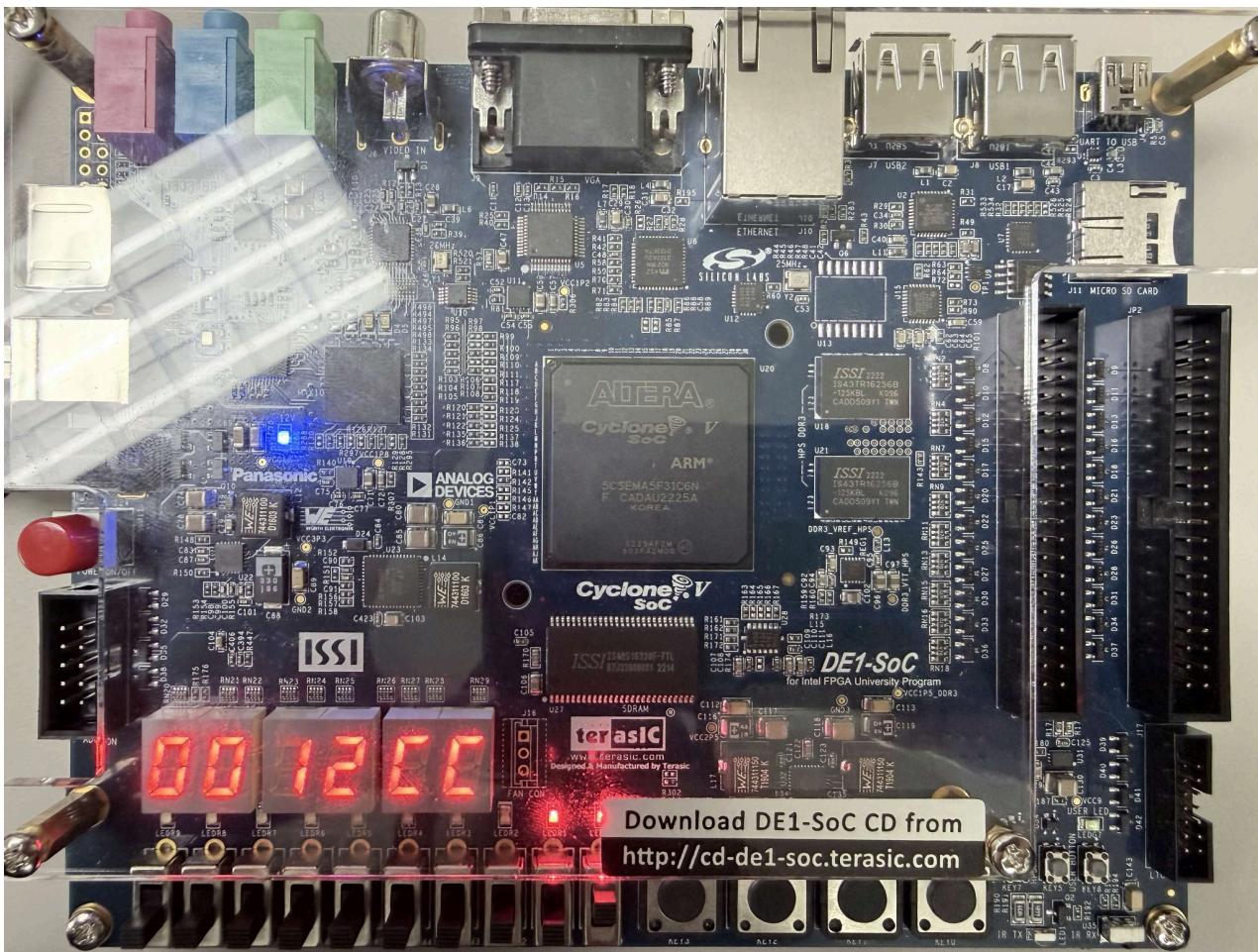


Image 4. Picture of board running the design. Currently selected to first MAC output

SignalTap Analysis:

To confirm functionality of the Avalon MM interface, we used SignalTap to capture the interface signals. We triggered the waveforms on address: 3 and used a centered waveform to show a range of addresses and read data from the memory. The waveform shows correct functionality with the correct read data showing up at the same time `readdatavalid` is asserted and corresponding to the previous address.

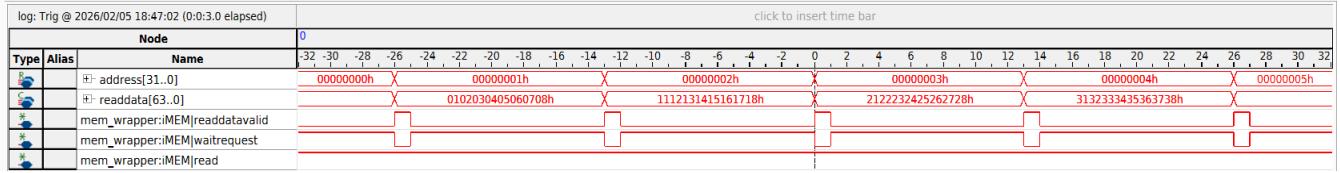


Image 5. SignalTap waveforms of Avalon MM interface

Difficulties:

The only real difficulty we encountered was creating the HDL for the matrix multiplication to meet the specifications. Our first attempt only added 7 of the 8 FIFO inputs. Only after fixing that, we realized that we were adding the columns together instead of the rows. Once we managed to get a functional unit, the rest of the minilab was mostly smooth sailing.