Analog Layout Interview Questions

Basics

1. What is semiconductor & Types ?
2. What is Resistor , Capacitor & Inductor and Parallel & Series?
3. What is diode? Explain characteristics?
4. Energy band?Types of energy band?
5. What is Ohm's law?
6. what is KVL & KCL?
7. What is sheet resistance?
8. What is current & Voltage?
9. Explain ASIC flow?

Fabrication

10. What is the full form of CMOS?
11. What are the steps of CMOS fabrication process?
12. Which semiconductor is used in fabrication?
13. Why silicon is used in IC fabrication?
14. What is the role of SiO2 in IC fabrication?
15. Why is P substrate used?
16. Can NMOS and PMOS be fabricated on same wafer?
17. What is P+,P Sub?
18. What is oxidation ?
19. Why oxidation is used in IC fabrication?
20. How is oxide removed in IC fabrication?
21. What is thin & thick oxide?
22. What is Etching?
23. What is wet and dry oxidation in IC fabrication?
24. What is lithography in VLSI?
25. What is photo resist ?
26. What is ion implantation ?

27. What is the defect in ion implantation and how to overcome it ?
28. What is diffusion?
29. What type of gate material used and why?
30. What is metalization ?
31. What is CMP?
32. Which material is used on metals for fabrication?
33. If poly place metal & metal place poly fabrication what will hapan?
34. Metals fabrication using material ?Contact and Via which material is used in fabrication?

MOSFET

35. What is MOSFET , Explain MOSFET working?
36. MOSFET types?
37. Why we are using MOSFET? Difference between MOSFET and BJT?
38. MOSFET Operation Region? Characteristics
39. What is Threshold Voltage?
40. MOSFET Saturation Region equation & Explain?
41. Explain PMOS ?
42. Explain Body Effect?
43. Explain Channel Length Modulation & Equation?
44. Explain DIBL?
45. Explain Hot Electrons?
46. Explain Punch Through ?
47. Explain Sub threshold effect?

Standard Call

48. What is Standard calls?
49. How do you choose the height of standard call?
50. What is metal track ? what is metal pitch?
51. How many layer in PMOS & NMOS?
52. Draw PMOS layout with all layers?
53. What is device width of PMOS ?

54. How to connect poly to metal?
55. How to connect Diffusion to metal ?
56. Draw inverter 5X ? and explain ?
57. What is PODE layer & explain?
58. PODE layar is draw the active poly what will happen ? LVS is clear or not?
59. Is it necessary to add pode layer in the schematic for clearing LVS ?
60. What is the use of pode layer ?
61. What are the Universal gates?
62. Why NAND & NOR are called universal gates ?
63. Draw the NAND & NOR gate and Truth table?
64. Draw NAND stick diagram?
65. What is Fin bound & pr boundary?
66. Inverter- Gate input =8v , VDD=5v what is output?
67. Differences Between Analog and Digital Layout Design.

Latch-up

68. What is Latch-up & explain?
69. How to clear the latch-up ? are you faced this error in verification tool ? and which verification you saw ?
70. Explain Prevention's?
71. What is Guard-ring & what is use?
72. Without Guard-ring how to clear latch-up?
73. Draw Inverter and explain?
74. Why substrate is p-sub ,why not p+ ?
75. Why VDD is connected PMOS ,why not NMOS?
76. Explain how many Diodes in CMOS?
77. What is the cause of latch-up ?

Antenna Effect

78. Explain Antenna effect?
79. Explain prevention?
80. What is Antenna ratio?

81. What is metal jumper?
82. Why only higher metals are used in metal jumpers ?
83. What is diode connection ,where we connected and why?
84. Diode is RB why not FB?
85. Why antenna effect occurs only for Gate ?

Matching

86. What is Matching & explain matching?
87. Explain types?
88. What is process variations?
89. What is Inter digitization & Common centroid ,explain ?
90. Matching technique, for A=2 and B=4 do a common Centroid matching?
91. Whats is Current mirror ? why we uses current mirror?
92. Why diode connected device should always be under saturation region ?
93. What is diode connected device ? why it is called diode connected device ?
94. How to place matched devices ?
95. What is Dummies? Why we use?
96. Whats is difference between **fingers and multiplier?**
97. If OD brake in layout, what will Happen?

98. What is STI & explain? And how to clear ?
99. What is LOD & explain?And how to clear ?
100. What is WPE & explain?And how to clear ?
101. Are you facing LOD effect in Layout?

EM & IR

102. Explain EM & prevention?
103. Is EM occurs for signals or power ?
104. What type of current used in EM ,AC/DC
105. What is high current density?
106. How to solve the EM?

107. Are you worked on EM error?
108. How to calculate EM?
109. 1mA ---> 1um

   5mA ---> x

110. Explain IR & prevention's?
111. How to solve the IR?
112. Are you worked on IR error?

ESD

113.   Explain ESD? And prevention's?
114. Explain types ?
115. How to solve the ESD?
116. Are you work on ESD blocks?

Shielding

117. Explain shielding?
118. Explain types of shielding?
119. Witch signal you shielding? And why?
120. Without shielding what will happen and how to take care the net?
121. where we connect shielding net ?
122. Are you worked on shielding?
123. What is **cross-talk**?
124. How to avoid cross-talk?

Deep N-WELL

125. What is Deep N_WELL?
126. Draw and explain the Deep N_WELL ?
127. Are you worked on deep n well ?

Finfet

128. Are you worked on finfet?
129. Which technology are you worked?
130. Gate length in 5nm?
131. Your project client name?
132. How many months you worked with client and which tool?
133. Difference between planar and FINFET in layout?
134. Why finfet?
135. Double pattern explain?
136. M1 metal two masks right, red is horizontal & green is vertical like plus , what type of error you face?

TOOL

137. Difference between Virtuoso L & XL in layout?
138. Difference between synchronous copy and cloning?
139. Explain DRC errors?
140. In LVS which one error clear 1st ?
141. What is DRC & LVS ,ERC?
142. What is Density error?
143. Are you worked on density?
144. What is soft check error ?
145. What is stamping error?
146. What are the base layers you have observed while doing layout?
147. What are the things will you take care about before starting layout ?
148. Explain floorplan?