Verification Continuum™

VC Verification IP
PCIe
Release Notes

Version S-2021.06, June 2021

SYNOPSYS®

Copyright Notice and Proprietary Information

Destination Control Statement

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the reader's responsibility to determine the applicable regulations and to comply with them.

Disclaimer

SYNOPSYS, INC., AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Trademarks

Synopsys and certain Synopsys product names are trademarks of Synopsys, as set forth at https://www.synopsys.com/company/legal/trademarks-brands.html.
All other product or company names may be trademarks of their respective owners.

Free and Open-Source Software Licensing Notices

If applicable, Free and Open-Source Software (FOSS) licensing notices are available in the product installation.

Third-Party Links

Any links to third-party websites included in this document are for your convenience only. Synopsys does not endorse and is not responsible for such websites and their practices, including privacy practices, availability, and content.

www.synopsys.com

Contents

1 Product Updates

This chapter discusses the new features and enhancements of the VC VIP for PCIe. The following sections contain STARs fixed for the active components of the PCIe UVM agent. If new features have been added, they are listed with the STAR.

1.1 Active UVM PCIe Agent Updates

1.1.1 Fixed E-STARs

Table 1-1 lists the STARs fixed in this release.

Table 1-1 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
None	

1.1.2 Fixed B-STARs

Table 1-2 lists the STARs fixed in this release.

Table 1-2 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
None	

1.2 Backward Incompatible Changes

Table 1-3 lists the backward incompatible STARs.

Table 1-3 Backward Incompatible STARs

Release	STAR	Backward Compatibility Workaround
Q-2019.12-1	9001562821	The `svt_pcie_pl_service::MBI_CMD` service request now works based on the logical lane numbers instead of physical lane numbers.
	9001577982	The `DataBusWidth` encoding is now fixed in SerDes architecture. Therefore, now the values will be different in SerDes architecture.

Table 1-3 Backward Incompatible STARs

Release	STAR	Backward Compatibility Workaround
O-2018.12-3	9001443220	It is recommended to set `enable_mbi_logging` from `svt_pcie_configuration` handle instead of `svt_pcie_pl_configuration` to generate the MBI logs in the testbench. For example, the hierarchy should be `cfg.<root/endpoint>_cfg.pcie_cfg.enable_mbi_logging = 1`.
O-2018.12-1	9001419796	Currently, two protocol checks will be triggered for a single issue. From P-2019.03 release onwards, `phy_invalid_message_bus_command` and `phy_reserved_mbi_register_address` protocol checks will not be triggering.
O-2018.12-1	9001421501	For more details, contact Synopsys Support**.**
O-2018.06-1	9001344844	NA
N-2018.03-3	9001329630	If the testbench is demoting or disabling Active component's PIPE protocol checks via incorrect VIP model, then compile errors will occur because these SVT Active component's PIPE protocol checks would now be instantiated based on applicable device type as MAC or PHY.
N-2018.03-3	9001329692	If the testbench is demoting or disabling active component's PL protocol checks via incorrect VIP model, then compile errors will occur because these `ACTIVE_PL` protocol checks would now be instantiated based on applicable device type as RC or EP.
N-2018.03-3	9001332753	If error scenario is created for the mentioned checks, then you need to demote them in the test.
N-2018.03-3	9001333125	If the testbench is demoting or disabling active component's PL protocol checks via incorrect VIP model, then compile errors will occur because these `ACTIVE_PL` and `ACTIVE_PL_LANE_OS` protocol checks would now be instantiated based on interface type as PIPE or SERDES or PMA.
N-2018.03-2	9001322903	If the testbench is demoting or disabling active component's PIPE protocol checks via incorrect VIP model, then compile errors will occur because these `ACTIVE_PL_PIPE` protocol checks would now be instantiated based on applicable device type as MAC or PHY.
N-2017.12-3	9001080588	Previously, MPIPE VIP while performing L1 substates PIPE handshake was used to wait for `pclkack_n` de-assertion/assertion from PHY which is required for turning off/on PCLK in PCLK as PHY output mode, whereas now MPIPE VIP will timeout and will issue an error after a timeout value given by PL configuration attribute `pclkackn_timeout_ns` waiting for `pclkack_n` de-assertion/assertion from PHY
N-2017.12-3	9001130110	Changed the default value of PL configuration class attribute `hot_reset_timeout_ns` from 20000 to 2000.
N-2017.12-3	9001293559	The original `ENABLE_ESM` API will continue to work in the N-2017.12-3 release, but should be eliminated in testbenches since it will be fully deprecated in future releases.
N-2017.12-2	9001231391	Users that added a reference to this check will need to remove the call to it.

Table 1-3 Backward Incompatible STARs

Release	STAR	Backward Compatibility Workaround
N-2017.12-1	9001275956	Previously, the name of the PL configuration was `assert_reject_coeff_bit_eq_ph0_8g`, this configuration name has now been changed to `set_reject_coeff_bit_for_reserved_tx_preset_eq_ph0`. Therefore, if you are using the old configuration in your testbench, then replace it with the new configuration.
N-2017.12-1	9001235333	If timescale is set to a value lower than 1ns/1fs (for example, 1ps/1fs) from the testbench and SVT version is lower than N-2017.12, tests might not work. Note: PCIE_SVT N-2017.12-1 is compatible with SVT N-2017.12 or higher.
N-2017.09-2	9000681537	As the error message string has changed, you must update if the error demotion is done using the exact string.
N-2017.09-2	9001228061	An earlier version of PCIe specification (Revision 4.0 Version 0.7) permitted the Reject Coefficient values bit to be clear for this case. This is not recommended, but is permitted. Therefore, the default behavior of the VIP is that it will by default assert the Reject Coefficient bit in `Equalization.Phase0` in response to any reserved transmitter preset. If any DUT does not expect this bit to be asserted, then you can change the value of `svt_pcie_pl_configuration` attribute `assert_reject_coeff_bit_eq_ph0_8g` to "0" so that VIP does not assert this bit in `Equalization.Phase0` in response to any reserved transmitter preset.
N-2017.09-2	9001233195	Now the ASPM/PM L1 and PM L23 API's to move to low power must be called immediately after VIP LTSSM enters L0 and not before VIP LTSSM enters L0, else the transition to low power will be canceled.
N-2017.09-1	9001229100	If the testbench is demoting or disabling PIPE protocol checks `phy_block_align_control_gen1_gen2` and/or `phy_rx_datak_gen3`, then compile errors occur as these protocol checks have been removed from the VIP. Also, PIPE protocol check `phy_local_preset_index_gtr_allowed` will fail if the tests are exercising reserved preset values on `LocalPresetIndex` signal when dynamic preset coefficient updates are enabled.

1.3 Important Notes

- The following quick start examples have been deprecated from Q-2020.06-3 version release onwards:
  - `tb_pcie_svt_ovm_basic_sys`
  - `tb_pcie_svt_uvm_16g_sys`
  - `tb_pcie_svt_uvm_16lane_sys`
  - `tb_pcie_svt_uvm_8lane_sys`
  - `tb_pcie_svt_uvm_basic_program_scope_sys`
  - `tb_pcie_svt_uvm_basic_sys`

- tb_pcie_svt_uvm_intermediate_sys
- tb_pcie_svt_uvm_monitor_16g_basic_sys
- tb_pcie_svt_uvm_monitor_basic_sys
- tb_pcie_svt_uvm_monitor_pipe_4_3_sys
- tb_pcie_svt_uvm_monitor_rc_dut_basic_sys
- tb_pcie_svt_uvm_unified_pipe_sys
- tb_pcie_svt_vmm_16g_sys
- tb_pcie_svt_vmm_8lane_sys
- tb_pcie_svt_vmm_basic_sys
- tb_pcie_svt_vmm_explicit_sys

- The list of examples that have been retained are as follows:
  - tb_pcie_svt_app_agent_uvm
  - tb_pcie_svt_ovm_unified_vip_sys
  - tb_pcie_svt_uvm_ccix_esm_sys
  - tb_pcie_svt_uvm_unified_vip_sys
  - tb_pcie_svt_vmm_intermediate_sys
- The following configurable parameters have been removed from the *hdl_interconnect_macros.sv* file present in the tb_pcie_svt_uvm_unified_vip_sys example:
  - SVT_PCIE_UI_CONNECT_DOWNSTREAM_PORT_MONITOR
  - SVT_PCIE_UI_CONNECT_UPSTREAM_PORT_MONITOR

2 Known Issues and Limitations

This chapter discusses the known issues and limitations of the active components.

2.1 Active UVM Agent Limitations

The PCIe Verification IP has the following verification and methodology limitations:

- STAR 9001516368: VIP changes `PowerDown` before full EIOS is received over PIPE interface.

  EIOS length check fails with the following error:

  ```
  [register_fail:ACTIVE_PL_LANE_OS:TS_OS:ordered_set_checker_early_truncated_eios_2] :
  Detected only 2 symbols of EIOS.  Transmitters are only permitted to terminate EIOS on
  symbols 14 or 15
  ```

- Functional coverage STARs:
  - 9001425640: Some Reasons missing in AC for L1_2_EXIT to L1_IDLE && L1_ENTRY to L1_IDLE
  - 9001425637: L0 to Recovery_lock:: Reason- ELEC_IDLE not available in AC
  - 9001421107: polling complaince reasons mismatch in AC &PM
  - 9001406573: Length 4 is not updating in eios_rx_128b130b_len_cp
  - 9001425638: L0 to Recovery_lock ,Reasons updation
  - 9001335986: Recovery.Speed to Recovery.Rcvrlock via electrical idle inferred bin missing
  - 9001331616: Add 8b/10b symbol coverage to PIPE coverage
- STAR 9001450511: PCIe VIP does not support 12 and 20 symbol size SKIP OS for 64-bit PIPE width at Gen3 and higher data rates.
- STAR 9001420899: Spurious LFSR mismatch violation for SKP seen in a specific situation

  When SKP OS is scheduled at the exact time when LTSSM is transitioning `Recovery.RcvrCfg` to `Recovery.Idle`, VIP issues a protocol check violation stating that LFSR value contained in SKP ordered set does not match the receive scrambler value.
- Test *ts.address_translation_test.sv* of the example area *tb_pcie_svt_uvm_unified_vip_sys* is not supported on NCVerilog simulator.
- This release does not support de-skew at VIP's receiver. Following are the known scenarios (problem is not limited to these) where VIP would fail to de-skew:
  - The VIP is configured with a multi-byte PIPE interface.
  - The skew coming into the VIP exceeds 6 symbols while using 8b10b encoding.

    If you face any issue related to VIP de-skew, contact Synopsys support.

- VIP when run in Verilog mode on VCS version N-2017.12-SP1, VIP has an issue due to which the user may experience performance degradation and it is recommended to use VCS version N-2017.12 instead. If you have a specific requirement to use VCS N-2017.12-SP1, contact Synopsys support.
- Following warnings are expected with VCS version N-2017.12-SP1:
  - `Warning-[IAVCVF-W] Incorrect argument to void cast`
  - `Warning-[TMR] Text macro redefined`
  - `Warning-[GCOIITB] Guard condition on Illegal/Ignore transition bin.`
  - `Warning-[PCWM-W] Port connection width mismatch`
  - `Warning-[RT-MTOCMUCS] More than one condition match in statement`
- The `svt_pcie_phy_transaction_exception` and `svt_pcie_phy_transaction_exception_list` classes are not supported.
- VMM model limitations:

  - Does not support partition compile.

  - No VMM-based test suites.

  - Gen4

  - MPCIe.
- Support for NVME over PCIe is limited to Verilog and UVM. Contact your Synopsys AE or sales office to obtain/download NVME.
- VCS/2012.09-SP1 is no longer qualified.

  If you are using VCS/2012.09-SP1 simulator, you must include the following option in the *vcs_build_options* file—that is, during vcs build.

  ```
  +define+SVT_SVC_MESSAGE_MANAGER_USE_SVT_MESSAGING_EXCLUSIVELY
  ```
- MTI 10.2c/10.1d must use `-permit_unmatched_virtual_intf` switch.
- VIP instantiation in program mode supported only on VCS.
- STAR 9001047447: `svt_pcie_pl_configuration::lane_reversal_mode = SUPPORTED` may result in errors if the VIP targeted link width is not same as the DUT's supported link width. This mode is not useful for controller testing.
- The VIP receive engine may trigger a false message of receiving too many SKPS when it is about to enter recovery.speed and receives a SKP from the link partner.
- VIP serdes model can inject skew unintentionally when configured as loopback slave and VIP ltssm is in Loopback active state and it may result in test failures if design cannot deskew the lanes.
- VIP serdes model can inject skew unintentionally when any error injection is used to misalign the lanes by sending order sets only on few lanes after transmitting EIOS and it may result in test failures if design cannot deskew the lanes.

The *tb_pcie_svt_verilog_basic_sys* example does not support the following command-line options for VCS:

- Precompiled (`USE_SIMULATOR=vcsmxpipvlog`)
- Partition compiled (`USE_SIMULATOR=vcsmxpcvlog`)

- When transmitting modified compliance pattern at 8b/10b encoding, a particular lane's receiver independently signifies a successful lock to the incoming Modified Compliance Pattern by looking for any one occurrence of the Modified Compliance Pattern and then setting the Pattern Lock bit (bit 8 of the 8 bit error status symbol) in the same lane of its own transmitted Modified Compliance Pattern. But VIP never sets the Pattern Lock bit in the transmitted Modified Compliance Patterns. This prevents testing of a PM rule for the same.
- In serdes mode, when polarity inversion is enabled then there is a possibility that VIP issues error messages for the data rate mismatch in polling configuration LTSSM state.
- With up/down configure on serdes interface, the `phy_bad_lane_skew` protocol check fails on VIP Rx path, if Skew and Polarity Inversion are enabled.
- Legacy Gen1/Gen2 instantiation models do not support the following three signals:
  - `TxDeemph`
  - `TxSwing`
  - `TxMargin`
- Rx Margining
  - Some of the current messages for Rx Margining will be changed to protocol messages in the next release. This will impact the message string, therefore any string based demotion of these messages will not have backward compatibility.
- Hot Reset
  - Topology: VIP RC <-> DUT EP
  - Scenario: When root is about to exit `Hot.Reset`, it sends EIOS and transitions to `Det.Quiet` but during this time its SKP schedule time has also reached and it tries to send SKP while in `Det.Quiet`. But it only sends first byte of the SKP and then starts sending EIOS from `Det.Quiet` state. Receiver PCS receives this truncated SKP OS and issues the error message, which it should not have issued as receiver is expected to ignore everything after EIOS reception. Also, when VIP TX has already sent an EIOS in `Hot.Reset` then it should not have attempted sending the scheduled SKIP OS in `Det.Quiet` state.
  - VIP transcript signature: `ReceivePMA: SKP_END` was not detected before byte 20. Forcing `skip_end_detected`.
  - Description: When root is about to exit `Hot.Reset` it sends EIOS and transitions to `Det.Quiet` but during this time its SKP schedule time has also reached and it tries to send SKP while in `Det.Quiet`. But it only sends first byte of the SKP and then starts sending EIOS from `Det.Quiet` state. Receiver PCS receives this truncated SKP OS and issues the error message, which it should not have issued as receiver is expected to ignore everything after EIOS reception. Also, when VIP TX has already sent an EIOS in `Hot.Reset` then it should not have attempted sending the scheduled SKIP OS in `Det.Quiet` state.
  - Workaround: Error Demotion
- The following error occurs with MTI 10.5c. However, this error may not cause any functional issue.

```
** Error (suppressible): (vsim-8385) svt_dynamic_report_object.sv(118):
fork..join_none statements in function 'manage_report_handler' only allowed if
the calling process originates in an initial or always block.
```

- STAR 9001172054: While upgrading the `linkwidth` (within the `supported_linkwidth_vector` range), if Skew is enabled along with the Polarity Inversion, you may get the following error during LTSSM transition from `Config.Complete` to `Config.Idle`:

```
[register_fail:ACTIVE_PL:COMMON_RECEIVER_PARAMETERS:phy_bad_lane_skew] RxDeskewLanes:
Lane skew of 9 has exceeded the maximum allowed lane skew of 7 symbol times
```

- The following test may fail because VIP is not setting the rejection bit in TS1 OS even though it received invalid coefficients.
  - Test: `gen4_pl_recovery_equalization_coefficient_setting_error`
  - Error signature: `VIP has not received rejection bit correctly on lane_11 rejbit = 0 loop`
- STAR 9001182383: RC PHY error injection causes simulation to hang

  Following svt_pcie_phy_transaction_exception class errors are expected to fail:
  - `STP_FRAMING_WRONG_LANE`
  - `SDP_FRAMING_WRONG_LANE`
  - `TWO_STP_FRAMING_PER_SYMBOL_TIME`
  - `TWO_SDP_FRAMING_PER_SYMBOL_TIME`
  - `STP_FRAMING_PACKET_GAP`
  - `SDP_FRAMING_PACKET_GAP`
- PCIe VIP does not support Crosslink feature.
- IEEE Encryption and Incdir flow is supported in VCS and MTI simulators only. For more details, see the sections 2.6 and 2.7 in the *VC VIP Library Installation Guide*.
- PCIe VIP does not support the "`+vcs+initreg+random`" VCS switch.
- PCIe VIP does not support the new NOP TLP type encoding in FLIT mode as mentioned in 0.7v of Gen6 Spec in this release.
- Euclide lint check errors are expected in UVM 1.2 with "`UVM_NO_DEPRECATED`" macro.
- Euclide lint check is currently supported in UVM and OVM methodology.
- STAR 3596632: The following Gen6 test cases in `tb_pcie_svt_uvm_unified_vip_sys` are expected to fail:
  - `base_pipe5_gen6_in_serdes_arch_mode_test`
  - `base_pipe5_gen6_full_eq_in_serdes_arch_mode_test`

2.2 Registering Callbacks During UVM Phasing

These notes only apply to UVM PCIe VIP.

In previous releases, you could register your callbacks during any explicit UVM phase. However, this has changed starting in this release. With the exceptions noted below for PHY and Link layer callbacks, callbacks must now be registered prior to the run phase. Note that callbacks are active from the point where they are registered to the point where they are unregistered.

Callbacks that are registered during run_phase and that are not enabled per the mechanism described below will not be executed.

To support late (run phase) registration of callbacks for the PHY and Link layers, Synopsys has provided two configuration members. See the following code descriptions. Note they are disabled by default.

```
/**
* Enable (1) or disable (0) support for the registration of Link Layer
```

```
* callbacks once the simulation has started. Leaving this feature disabled
* results in improved active component performance.
*/
bit enable_dl_run_phase_cb_reg = 0;
/**
* Enable (1) or disable (0) support for the registration of Physical Layer
* callbacks once the simulation
* has started. Leaving this feature disabled results in improved active
* component performance.
*/
bit enable_pl_run_phase_cb_reg = 0;
```

Note that registering PHY and Link layer callbacks during run_phase incurs a performance penalty. Register these callbacks before run_phase to avoid performance degradation

Synopsys is temporarily providing support for the following define: SVT_PCIE_ENABLE_RUN_PHASE_CB_REG. Setting this define will force ‘enable_dl_run_phase_cb_reg’ and ‘enable_pl_run_phase_cb_reg’ to default to ‘1’, so that callback registration in the run phase will be supported.

Note at a future date, SVT_PCIE_ENABLE_RUN_PHASE_CB_REG will be removed. At that point the only method for enabling run time registration will be with the enable_pl_run_phase_cb_reg and enable_dl_run_phase_cb_reg fields in the configuration class.

3 Supported Platforms, Models, and Software

This chapter discusses the supported platforms, models, and software.

This chapter consists of the following topics:

- Supported Methodology, OS and Simulator Versions
- Software Tools Support

3.1 Supported Methodology, OS and Simulator Versions

3.1.1 Supported Methodologies

Table 3-1 lists the methodologies supported with simulators.

Table 3-1 Supported Methodologies With Simulators (for Active Component)

Methodology	VCS	Xcelium	Questasim
UVM	Supported	Supported	Supported
OVM	Supported	Not supported	Not Supported
VMM	Supported	Not supported	Not Supported
VLOG	Supported	Supported	Supported

Attention

With Questasim 2020.3, you may get the warning as illustrated:

```
** Warning: ** while parsing macro expansion:
'SVC_SOURCE_MAP_SUITE_MODEL_MODULE_SV' starting at
/dw_home/bin/src/sverilog/mti/pciesvc_target_appl.sv(10)

** while parsing file included at
/dw_home/bin/src/sverilog/mti/pciesvc_target_appl.sv(10)

** at /dw_home/bin/src/sverilog/mti/pciesvc_shared_status_pkg.sv(20):
(vlog-2275) Existing package 'pciesvc_shared_status_pkg' will be
overwritten.
```

Table 3-2 lists the methodology versions supported.

Table 3-2 Supported Methodology Versions

Methodology	Supported Version	Unsupported Version
UVM	1.1d, 1.2, 1800.2-2017-1.0	1.1a
OVM	2.1.2	2.1.1_3
VMM	1.2	N/A

3.1.2 Supported OS and Simulator Versions

The simulator matrix table is available at the following location:

VC VIP Library page

https://spdocs.synopsys.com/dow_retrieve/latest/vg/snps_vip_lib/PDFs/simulator_matrix.pdf

For more information on the simulator matrix and library level updates, see *VC VIP Library Release Notes*.

3.2 Software Tools Support

Following are the supported tool sets that work with this version of the VIP:

- Verdi Protocol Analyzer version O-2018.09

4 Documentation

This chapter consists of the following topics:

4.1 Protocol

- PCI Express Base Specification Revision 3.1
- PCI Express Base Specification Revision 4
- PCI Express Base Specification Revision 5
- PCI Express Base Specification Revision 6.0 Version 0.5 draft spec 30 Jan'20

4.2 Methodology

- Universal Verification Methodology (UVM) 1.1d and 1.2
- Open Verification Methodology (OVM) 2.1.2
- IEEE UVM 1800.2.2017

Note IEEE UVM 1800.2.2017 is supported in VCS with a known limitation of `uvm_reg` support.

4.3 Product Guides and Online Help

After the VIP is downloaded and installed, product documentation resides at the following location:

```
$DESIGNWARE_HOME/vip/pcie_svt/latest/doc/
```

The documentation consists of the following:

- *PCIe SVT UVM User Guide*, which is installed at `$DESIGNWARE_HOME/vip/svt/pcie_svt/latest/doc/pcie_svt_uvm_user_guide.pdf`
- *PCIe SVT OVM User Guide,* which is installed at `$DESIGNWARE_HOME/vip/svt/pcie_svt/latest/doc/pcie_svt_ovm_user_guide.pdf`
- *PCIe SVT UVM Class Reference HTML,* which is installed at `$DESIGNWARE_HOME/vip/svt/pcie_svt/latest/doc/pcie_svt_uvm_class_reference/html/index.htm`

- *PCIe SVT OVM Class Reference HTML*, which is installed at `$DESIGNWARE_HOME/vip/svt/pcie_svt/latest/doc/pcie_svt_ovm_class_reference/html/index.htm`
- *PCIe SVT UVM Getting Started*, which is installed at `$DESIGNWARE_HOME/vip/svt/pcie_svt/latest/doc/pcie_svt_uvm_getting_started.pdf`
- *PCIe SVT UVM FAQ*, which is installed at `$DESIGNWARE_HOME/vip/svt/pcie_svt/latest/doc/pcie_svt_faq.pdf`
- *PCIe SVT EP/RC DUT Integration Guide*, which is installed at `$DESIGNWARE_HOME/vip/svt/pcie_svt/latest/doc/pcie_svt_ep_rc_integration_guide.pdf`

4.4 Quickstart Examples

The VIP provides various quickstart examples for each methodology. They are located at

`$DESIGNWARE_HOME/vip/svt/pcie_svt/latest/examples/sverilog`

List of unified examples:

- `tb_pcie_svt_app_agent_uvm`
- `tb_pcie_svt_ovm_unified_vip_sys`
- `tb_pcie_svt_uvm_ccix_esm_sys`
- `tb_pcie_svt_uvm_unified_vip_sys`
- `tb_pcie_svt_vmm_intermediate_sys`

Before executing the examples, you must first install them into a work area which Synopsys names by convention design_dir. Following is the command to install the unified UVM examples:

```
$DESIGNWARE_HOME/bin/dw_vip_setup -path ./design_dir  -e
pcie_svt/tb_pcie_svt_uvm_unified_vip_sys
```

The name of the example is the directory name. Each example has a README which provides testbench architecture and setup information.

5 Customer Support

This chapter discusses the customer support provided for VC VIP for PCIe.

This chapter consists of the following topics:

5.1 SolvNetPlus

Synopsys SolvNetPlus resides at the following location:

https://solvnetplus.synopsys.com

It provides you with the following:

- Download Center for all VIPs
- Support
- Training
- Reference Methodology Retrieval System
- Hundreds of articles on VIP usage
- Register problem reports

5.2 Registering a Problem

To register a problem, perform any of the following tasks:

- Go to https://solvnetplus.synopsys.com and open a case.

  Enter the information according to your environment and your issue.
- Send an e-mail message to support_center@synopsys.com
  - Include the Product name, Sub Product name, and Product version for which you want to register the problem.

5.3 Telephone Support

Telephone your local support center:

- North America:

  Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday

- All other countries:
  https://www.synopsys.com/support/global-support-centers.html

6 Previous Release Notes

This chapter lists the product update for previous releases:

6.1 Release R-2021.03-2

6.1.1 Active UVM PCIe Agent Updates

6.1.1.1 Fixed E-STARs

Table 6-1 lists the STARs fixed in this release.

Table 6-1 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
None	

6.1.1.2 Fixed B-STARs

Table 6-2 lists the STARs fixed in this release.

Table 6-2 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
9001482662	**Problem**: Linkwidth upconfigure fails sometimes when link width change is initiated by MPIPE VIP.
	Resolution: Fixed the VIP to activate the new lanes only on the block count boundary to maintain the block synchronization properly on all the lanes.
3654491	**Problem**: VIP should not transmit EQ TS2 when 8g was skipped.
	Resolution: Fixed the issue wherein the VIP transmitted the EQ TS2 in Rcvr.Cfg even when EQ got completed at Gen4. This issue only occurred when there was a speed change in VIP directly from 2.5G to 16G and 8g was skipped. VIP still kept `'eq_needed_8g'` asserted even though 8G was skipped and EQ was completed at 16G.

6.2 Release R-2021.03-1

6.2.1 Active UVM PCIe Agent Updates

This release contains the following feature set:

- Added the support for Equalization at 64 GT/s, with the exception of Redo and Windowing.

6.2.1.1 Fixed E-STARs

Table 6-3 lists the STARs fixed in this release.

Table 6-3 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
None	

6.2.1.2 Fixed B-STARs

Table 6-4 lists the STARs fixed in this release.

Table 6-4 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
3599075	**Problem**: Compile error in OVM example when Gen6 define is removed from the compile options.
	Resolution: Removed the pipe width configurations that are causing the compile error from the base test as they are no longer needed.
3611976	**Problem**: MAC VIP is not de-asserting RxEqInProgress during mid sim reset.
	Resolution: Fixed the VIP to de-assert the RxEqInProgress in Detect state.

6.3 Release R-2021.03

6.3.1 Active UVM PCIe Agent Updates

This release contains the following feature set:

- Added support for Euclide (Eclipse based IDE) for lint rule checking. The VIP works seamlessly with Euclide IDE when configured with testbench rule setting and would not result in any fatal errors.
  - UVM 1.2 is supported without `"UVM_NO_DEPRECATED"` macro.
  - For resolving SVT related errors, contact Synopsys support for SVT T release.

6.3.1.1 Fixed E-STARs

Table 6-5 lists the STARs fixed in this release.

Table 6-5 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
None	

6.3.1.2 Fixed B-STARs

Table 6-6 lists the STARs fixed in this release.

Table 6-6 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
None	

6.4 Release R-2020.12-3

6.4.1 Active UVM PCIe Agent Updates

This release contains the following feature set:

- PCIe XLVIP is now compatible with 2021.03 XTOR version. Contact Synopsys support for more information.

6.4.1.1 Fixed E-STARs

Table 6-7 lists the STARs fixed in this release.

Table 6-7 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
3536546	**Problem**: Need to reset `symbol_clk` to 0 when there is a change in PCLKRate.
	Resolution: Fixed the VIP to handle the scenario where the input PCLK is X till PclkRate value is driven correctly.

6.4.1.2 Fixed B-STARs

Table 6-8 lists the STARs fixed in this release.

Table 6-8 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
None	

6.5 Release R-2020.12-2

6.5.1 Active UVM PCIe Agent Updates

6.5.1.1 Fixed E-STARs

Table 6-9 lists the STARs fixed in this release.

Table 6-9 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
None	

6.5.1.2 Fixed B-STARs

Table 6-10 lists the STARs fixed in this release.

Table 6-10 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
None	

6.6 Release R-2020.12-1

6.6.1 Active UVM PCIe Agent Updates

This release contains the following feature set:

- EA support for L0p is available with a Gen6 license.

6.6.1.1 Fixed E-STARs

Table 6-11 lists the STARs fixed in this release.

Table 6-11 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
3440591	**Problem**: SVDOC description is insufficient for the PL configuration attributes.
	Resolution: Added detailed SVDOC description for the following PL configuration attributes: • `min_tx_skp_symbols_in_ordered_set_8g` • `max_tx_skp_symbols_in_ordered_set_8g`

6.6.1.2 Fixed B-STARs

Table 6-12 lists the STARs fixed in this release.

Table 6-12 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
None	

6.7 Release R-2020.12

6.7.1 Active UVM PCIe Agent Updates

This release contains the following feature set:

- PCIe VIP is compatible with VCS `+lint=LRM_1800_2009` option.

6.7.1.1 Fixed E-STARs

Table 6-13 lists the STARs fixed in this release.

Table 6-13 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
None	

6.7.1.2 Fixed B-STARs

Table 6-14 lists the STARs fixed in this release.

Table 6-14 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
None	

6.8 Release R-2020.09-3

6.8.1 Active UVM PCIe Agent Updates

6.8.1.1 Fixed E-STARs

Table 6-15 lists the STARs fixed in this release.

Table 6-15 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
3436593	**Problem**: No information in the `update_if_varaiables` method to detect the root cause of the issue during integration.
	Resolution: Added the display statement in `update_if_varaiables` method to print important attributes, say for example, instance name, port_id, link_id, and so on to help debug during integration.
3405087	**Problem**: VIP issues the following error for the read completion received immediately after the write committed over MBI: `[register_fail:ACTIVE_PL_PIPE:MBI:phy_mbi_write_committed_followed_by_nop] : Invalid data(0x40); Write Committed command must be followed by a NOP or a response to a transmitted MBI command on lane 0`
	Resolution: Enhanced the VIP to process the read completion that is received immediately after the write committed over MBI.

6.8.1.2 Fixed B-STARs

Table 6-16 lists the STARs fixed in this release.

Table 6-16 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
3427554	**Problem**: The ctrl skp logging filename generated does not match with the log file name configured in `ctrl_skp_log_filename` configuration.
	Resolution: Fixed the VIP to handle user defined `ctrl_skp_log_filename` configuration attribute such that the generated log file name is in accordance with the log filename configured in the `ctrl_skp_log_filename` configuration.

6.9 Release R-2020.09-2

6.9.1 Active UVM PCIe Agent Updates

6.9.1.1 Fixed E-STARs

Table 6-17 lists the STARs fixed in this release.

Table 6-17 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
None	

6.9.1.2 Fixed B-STARs

Table 6-18 lists the STARs fixed in this release.

Table 6-18 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
3339532	**Problem**: MBI_CMD service request is not working as expected in PIPE 5 for posted-to-posted write addresses when lane reversal is enabled.
	Resolution: Fixed the issue with MBI_CMD service request to perform the transactions based on logical lane numbers instead of physical lane numbers.
3386587	**Problem**: Issue with polarity inversion in PIPE 5 when lane reversal is enabled.
	Resolution: Fixed the issue wherein the RxPolarity transaction over the MBI takes place on incorrect lanes when lane reversal is enabled.

6.10 Release R-2020.09-1

6.10.1 Active UVM PCIe Agent Updates

6.10.1.1 Fixed E-STARs

Table 6-19 lists the STARs fixed in this release.

Table 6-19 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
3332545	**Problem**: Add support for variable `max_pclk` frequency in PIPE5 PCLK as PHY input mode.
	Resolution: Added the support for variable `max_pclk` frequency mode in PIPE5 PCLK as PHY input mode and also added the `svt_pcie_pl_configuration::pipe_max_pclk_mode` to select the desired `max_pclk` mode.
3361297	**Problem**: PCIe XLVIP to support 2020.09/TD ZEBU IP ROOT.
	Resolution: • XLVIP is compliant with 2020.09 version of `ZEBU_IP_ROOT`. • No backward compatibility with previous version of `ZEBU_IP_ROOT`.
3374901	**Problem**: Enhancements of Gen6 coverage.
	Resolution: • Added the new cover points for regular DLLP. • Added the Flit callback for sampling of covergroups. • Updated the Flit cover points to be generic and configurable from defines.
3362688	**Problem**: To Achieve a scenario of ECRC Antithetical TD (like TLP with TD set, and no ECRC, and vice-versa), product not providing any exception.
	Resolution: Enhanced the product to add two different variations of TL Interface Exception: • `CORRUPT_TD_ECRC`: Indicates whether to append the ECRC to the TLP based on the TD bit. - ECRC does not get appended to the TLP, if the TD bit is set. - ECRC gets appended to the TLP, if the TD bit is clear. • `CORRUPT_TD`: Indicates whether to corrupt the TD bit by flipping its value from the original value and keep the original ECRC. Do not inject using TL callback.

6.10.1.2 Fixed B-STARs

Table 6-20 lists the STARs fixed in this release.

Table 6-20 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
3326081	**Problem**: RxEqInProgress does not get de-asserted in abort scenarios with PIPE 5 when `svt_pcie_pl_configuration::simultaneous_deassertion_of_rxeqinprogress` is set to 0.
	Resolution: Fixed the issue to properly de-assert the RxEqInProgress in the abort scenarios.

6.11 Release R-2020.09

6.11.1 Active UVM PCIe Agent Updates

This release contains the following feature set:

- Added the support for IEEE UVM 1800.2.2017 in VCS with a known limitation of `uvm_reg` support.

6.11.1.1 Fixed E-STARs

Table 6-21 lists the STARs fixed in this release.

Table 6-21 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
None	

6.11.1.2 Fixed B-STARs

Table 6-22 lists the STARs fixed in this release.

Table 6-22 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
None	

6.12 Release Q-2020.06-3

6.12.1 Active UVM PCIe Agent Updates

6.12.1.1 Fixed E-STARs

Table 6-23 lists the STARs fixed in this release.

Table 6-23 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
3287731	**Problem**: The MBI transactions gets initiated by MPIPE VIP even before the `phy_status` de-assertion for Reset#.
	Resolution: Fixed the MPIPE VIP to wait for `phy_status` de-assertion for Reset# before initiating the MBI transactions.
3302758	**Problem**: VIP not able to perform receiver detection appropriately because of skewed pclk in PIPE 5 SerDes arch mode.
	Resolution: Fixed the receiver detection issue where the `rx_status` and `phy_status` are not in synchronization with each other for one pclk cycle, when there is a skewed pclk.

STAR Number	Description
3335501	**Problem**: CTRL SKPs at Gen5
	Resolution: Changed the default value of `svt_pcie_pl_configuration::enable_ctrl_skp_support` configuration from "0" to "1". By default, VIP will now generate and expect CTRL SKIP wherever it is expected to generate as per specifications.

6.12.1.2 Fixed B-STARs

Table 6-24 lists the STARs fixed in this release.

Table 6-24 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
None	

6.13 Release Q-2020.06-2

6.13.1 Active UVM PCIe Agent Updates

This release supports the following feature set as per PCI Express® Base Specification Revision 6.0 Version 0.5 draft spec 30 Jan'20:

- Physical Layer:
  - Flit support
    - Flit mode support from Gen 1 onwards
    - Link Retraining at Gen6
  - Flit mode encodings support
    - 8b/10b
    - 128b/130b
    - 1-1 encoding
  - Speed change support
    - Gen1 -> Gen3 -> Gen4 -> Gen5 -> Gen6 with EQ bypassed
    - No EQ needed Gen1 -> Gen6
  - Phy Features available for 64GT/s with SerDes Arch mode
    - Disabled
    - Hot Reset
    - All Link width combination support: X1, X2, X4, X8, X16
    - Link width up/down configure support
    - Lane, UI and Sub UI Skew support
    - Lane reversal

- Low power (L1, L2) modes
- Speed Upgrade/Downgrade support

- Supported Topology
  - PIPE 5.1 80 bit, SerDes Arch
  - mPIPE/sPIPE
- Supported SerDes Arch Interface:

Table 6-25 Supported SerDes Arch Interface

Spec Line Rate	Width	PIPE Clock
Gen6	80 bits (8 Symbols)	1 GHz
Gen5	80 bits (8 Symbols)	500 MHz
Gen4	80 bits (8 Symbols)	250 MHz
Gen3	80 bits (8 Symbols)	125 MHz
Gen2	10 bits (1 Symbol)	500 MHz
Gen1	10 bits (1 Symbol)	250 MHz

- Link Layer:
  - IDLE Flit support
  - TLP packing in Flit mode
    - TLPs in Flit Mode are Non-Flit mode types
  - Flit CRC support
  - Replay support
  - DLLP packing in Flit mode
  - Flit Sequence number checks
  - Support for PL transitions to recovery for power management, speed changes, link width changes
- Additional verification In-progress
  - Exceptions (`AUTO_TX_CORRUPT_CRC`, `AUTO_RX_NAK_GOOD_FLIT`)
  - Loopback states support
  - SSC/SRIS
- Callbacks
  - DL Flit Callbacks support
- Functional Coverage
  - Features Checks support and Coverage support at DL/PL
- Debug Aids
  - Symbol log with Flit markers

- Flit support limitations
  - Flit based TLP frame format not supported
- License Information
  - Perform the Gen 6 VIP License check order and feature names as per the following steps:
    - `VIP-PCIE-G6-SVT`
    - `VIP-LIBRARY2019-SVT VIP-PCIE-G6-EA-SVT`
- Additional Command Line Macros requirement:

  `+define SVT_PCIE_ENABLE_GEN6`
- OVM Install Example: `tb_pcie_svt_ovm_unified_vip_sys`

6.13.1.1 Fixed E-STARs

Table 6-26 lists the STARs fixed in this release.

Table 6-26 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
3230583	**Problem**: VIP changes the power down to P0 on the `internal_pipe_clk` instead of PHY driven `pclk` during L1SS (using SNPS PIPE Sideband signals handshake) exit.
	Resolution: Fixed the VIP to switch to PHY driven `pclk` as soon as PHY asserts the `pclkack_n` signal so that the power down change to P0 occurs with respect to PHY driven `pclk`.

6.13.1.2 Fixed B-STARs

Table 6-27 lists the STARs fixed in this release.

Table 6-27 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
3275594	**Problem:** Lane reversal resets in between an MBI transaction due to which VIP flags the following errors incorrectly: • `mbi_write_ack_occurance_check` • `mbi_read_write_cmd_occurance_check`
	Resolution: Fixed the issue by waiting for the MBI transaction to complete before resetting the lane reversal status.
3214475	**Problem**: The `link_eval_feedback_figure_of_merit` status attribute holds the previous evaluation feedback instead of the latest evaluation feedback.
	Resolution: Fixed the status attribute to indicate the latest evaluation feedback.

6.14 Release Q-2020.06-1

6.14.1 Active UVM PCIe Agent Updates

6.14.1.1 Fixed E-STARs

Table 6-28 lists the STARs fixed in this release.

Table 6-28 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
3267586	**Problem**: Add the support for `XLMOD` licenses for PCIe XLVIP.
	Resolution: PCIe XLVIP needs the following licenses for its usage: • `VIP License` • `Xtor License` • `VIP-XLMODE-OPT License` Hence, the support for `VIP-XLMODE-OPT` license has been added for XLVIP usage in parallel with the other mentioned licenses which were already supported earlier.

6.14.1.2 Fixed B-STARs

Table 6-29 lists the STARs fixed in this release.

Table 6-29 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
3187300	**Problem**: VIP blocks the transmission of TLP in a VC if any malformed TLPs were sent earlier.
	Resolution: Added a new TL configuration attribute, `bypass_tx_flow_control_gate` to control the transmission of good TLPs following Malformed TLPs transmitted by the VIP earlier.
3176802	**Problem**: VIP issues a false error, PHY sent `write_ack` when pclk is not stable during L2 transition.
	Resolution: Fixed the issue where VIP performed the rate change without waiting for the write ack during L2 transition.
3166904	**Problem**: Following MBI checks might get triggered falsely during Link width change: • `mbi_write_ack_occurance_check` • `mbi_read_write_cmd_occurance_check`
	Resolution: Fixed the corner case where the checks are getting triggered on incorrect link width value.

6.15 Release Q-2020.06

6.15.1 Active UVM PCIe Agent Updates

6.15.1.1 Fixed E-STARs

Table 6-30 lists the STARs fixed in this release.

Table 6-30 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
None	

6.15.1.2 Fixed B-STARs

Table 6-31 lists the STARs fixed in this release.

Table 6-31 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
None	

6.16 Release Q-2020.03-3

6.16.1 Active UVM PCIe Agent Updates

6.16.1.1 Fixed E-STARs

Table 6-32 lists the STARs fixed in this release.

Table 6-32 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
3209746	**Problem**: Add the support for Gen1 (8-bits width, 2GHz `pclk_rate`) and Gen2 (8-bits width, 2GHz `pclk_rate`) combinations with PIPE 4.4.
	Resolution: Added the support for Gen1 (8-bits width, 2GHz `pclk_rate`) and Gen2 (8-bits width, 2GHz `pclk_rate`) combinations with PIPE 4.4.

6.16.1.2 Fixed B-STARs

Table 6-33 lists the STARs fixed in this release.

Table 6-33 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
3207546	**Problem**: UVM warning on bad ordered set as illustrated: `UVM_WARNING ... uvm_test_top.env.pcie_env.rc_env.rc_agent.port0.pl0 [register_fail:ACTIVE_PL_LANE_OS:TS_OS:ordered_set_checker_bad_ordered_set_6] : Received bad ordered set: 0x000, 0x0aa 0x0aa 0x0aa 0x0aa 0x0aa 0x0aa 0x0aa 0x0aa 0x0aa 0x0aa 0x0aa 0x0e1 0x068 0x012 0x045`
	Resolution: Fixed the issue where the ordered set checker was not receiving the data properly.
3212651	**Problem**: Issue with the `phy_wrong_eqts_ec_in_equalization_phase_2` check.
	Resolution: Fixed the issue where the ordered set checker was not receiving the data properly.

Table 6-33 Fixed B-STARs for Active PCIe Agent (Continued)

STAR Number	Description
3218724	**Problem**: Issue with the encoder during `HOT_PLUG_UNPLUG`. `UVM_FATAL ... uvm_test_top.env.pcie_env.rc_env.rc_agent.port0.pl0 [report_message] Encoder: Kcode requested 0x166, but no legal encoding found!`
	Resolution: Fixed the issue where VIP Tx FIFO was not getting cleared when mid-sim reset is applied.

6.17 Release Q-2020.03-2

6.17.1 Active UVM PCIe Agent Updates

6.17.1.1 Fixed E-STARs

Table 6-34 lists the STARs fixed in this release.

Table 6-34 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
3135863	**Problem**: Create a configurable parameter for `PIPE_MAX_PCLK_SUPPORTED` for the unified VIP model.
	Resolution: Added `SVT_PCIE_UI_PIPE_MAX_PCLK_SUPPORTED` to the list of configurable parameters of the VIP unified model.
3157341	**Problem**: Issue during Hot Reset as no `CfgWr` is sent prior to `CfgRd` and the device responded with ID 0.
	Resolution: Fixed the issue. When DL_Down occurs, the `expected_bus_num` resets which allows the `TYPE0_CFG_MISMATCHED_COMPLETER_ID` check to correctly expect bus numbers in completions after a reset event.

6.17.1.2 Fixed B-STARs

Table 6-35 lists the STARs fixed in this release.

Table 6-35 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
3166447	**Problem**: Margining test fails waiting for a posted transaction to finish.
	Resolution: Fixed the issue.

6.18 Release Q-2020.03

6.18.1 Active UVM PCIe Agent Updates

None

6.19 Release Q-2019.12-3

6.19.1 Active UVM PCIe Agent Updates

6.19.1.1 Fixed E-STARs

Table 6-36 lists the STARs fixed in this release.

Table 6-36 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
9001578896	**Problem**: Add support for 2 GHz `pclk_rate` and16- bit width for Gen3, 16-bit and 32-bit for Gen4.
	Resolution: Enhanced the model.
3103416	**Problem**: PCIe performance improvement – Compile time improvement for PCIe SVT VIP.
	Resolution: Improved the compile time by using the new parallel partition compile feature. For more information, see "*Appendix D: Partition Compile and Precompiled IP*" in the *VC Verification IP PCIe UVM User Guide* or *"Chapter 17 Partition Compile and Precompiled IP"* in the *VC Verification IP PCIe OVM User Guide.*

6.19.1.2 Fixed B-STARs

Table 6-37 lists the STARs fixed in this release.

Table 6-37 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
9001574047	**Problem**: FIFO underflow when PPM is introduced on the `RxCLK`.
	Resolution: Corrected the behavior.
3116656	**Problem**: [PIPE5] MBI transactions continue happening even when `Pclk` is not stable.
	Resolution: Corrected the behavior.

6.20 Release Q-2019.12-2

6.20.1 Active UVM PCIe Agent Updates

6.20.1.1 Fixed E-STARs

Table 6-38 lists the STARs fixed in this release.

Table 6-38 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
3103019	**Problem:** No debug message when the lanes are turned off by MAC DUT.
	Resolution: A debug tip is added that provides information to the user regarding the turning off of lanes by MAC DUT and that PHY VIP does not provide `Phystatus` on those lanes. SPIPE VIP now prints the following debug tip in the mentioned scenario: `SNPS_PCIE_VIP_DEBUG_TIP: Lane has been turned off by MAC DUT by simultaneously asserting TxCompliance and TxElecIdle. PHY VIP will not assert PhyStatus on this lane in response to Powerdown/Width/Rate/Pclk_Rate change by MAC DUT. If MAC is expecting PhyStatus on this lane then MAC should turn on this lane before changing Powerdown/Width/Rate/Pclk_Rate.`
3106649	**Problem:** Loopback feature is not supported in PIPE 5 SerDes arch mode.
	Resolution: Implemented the Loopback feature. **Added Features**: Loopback support is added in PIPE 5 SerDes arch mode.

6.20.1.2 Fixed B-STARs

Table 6-39 lists the STARs fixed in this release.

Table 6-39 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
9001507806	**Problem:** Pass condition implementation is missing for Retimer protocol checks.
	Resolution: Corrected the behavior.

6.21 Release Q-2019.12-1

6.21.1 Active UVM PCIe Agent Updates

The following lists all the updates for this release.

- Removed the following chapters from the *VC Verification IP PCIe UVM User Guide*:
  - Creating the PLI Object in 32-bit and 64-bit Simulation Modes.
  - Integrated Planning for VC VIP Coverage Analysis
- Moved Appendix “ECN Support” to chapter 1, Introduction.

6.21.1.1 Fixed E-STARs

Table 6-40 lists the STARs fixed in this release.

Table 6-40 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
9001570361	**Problem:** Add a check in instantiation models to flag an error when the incompatible PIPE specification version is set.
	Resolution: Added a check in instantiation models so that VIP flags the following FATAL error if the incompatible PIPE specification version is set: `The attribute svt_pcie_device_configuration::pipe_spec_ver is set to 5.1. This instantiation model only supports pipe_spec_ver < PIPE_SPEC_VER_5_0. Set this attribute to < PIPE_SPEC_VER_5_0 to avoid this error.`
9001572735	**Problem:** Add signals to show scrambled data in the waveform when precoding is on.
	Resolution: Added the following signals in the waveforms to show per-lane scrambled data received off of the PIPE interface after precoding has been removed. • `lane_<n>_tx_scrambed_data` • `lane_<n>_rx_scrambled_data`
9001575765	**Problem:** During loopback equalization, if requests are queued on a lane not under test the VIP will flag a warning and drop all requests for the lanes not under test. Equalization may only be performed on the lane not under test so it is not possible to send requests on the other lanes.
	Resolution: Enhanced the model.
9001576088	**Problem:** Add control to respond with either `FigureMerit` or `DirectionChange` feedback for `RxEqEval` request.
	Resolution: Enhanced the model. **Added Features**: Added `svt_pcie_pl_configuration::evaluation_feedback_response` to choose the response type as shown below. Specifies if SPIPE will respond with FOM (`FigureMerit`) or DIR (`DirectionChange`) or both feedback response to link equalization evaluation (`RxEqEval`) request from the MAC. Significance: • When set to `00`, the VIP will respond with both FOM and DIR feedback response (`WriteUncommitted` followed `WriteCommitted`). • When set to `01`, the VIP will respond with only FOM feedback response (only one `WriteCommitted`). • When set to `10`, the VIP will respond with only DIR feedback response (only one `WriteCommitted`). Note: Only utilized by the SPIPE active component when attribute `pipe_spec_ver` is set to a value greater than or equal to 5.1.
9001576831	**Problem:** Enhancement for SerDes model for making recovered clock adjustments on all edges and not just min bit period edges.
	Resolution: Added a new clock recovery mode `USE_NOMINAL_PERIOD_ONLY`. When enough bits within the lock range are seen, the recovered clock will be based off of the nominal bit period instead of the observed bit min bit periods going by. This avoids overcompensating the recovered clock when there is lots of jitter present.

STAR Number	Description
9001577376	**Problem:** Add a configuration enable VIP to set `use_preset` bit in outgoing TS1s in `Eq.Ph2/Eq.Ph3` while responding with acceptance/rejection to received transmitter settings.
	Resolution: Added a PL configuration `enable_use_preset_bit_in_ts1_with_accepted_rejected_tx_setting` which enables the VIP to set `use_preset` bit in outgoing TS1s in `Eq.Ph2/Eq.Ph3` while responding with acceptance/rejection to received transmitter settings. • When set to 1, VIP will set `use_preset` bit to 1 in outgoing TS1s if it has received a preset request. • When set to 0, VIP will set `use_preset` bit to 0 in outgoing TS1s if it has received a preset request.

6.21.1.2 Fixed B-STARs

Table 6-41 lists the STARs fixed in this release.

Table 6-41 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
9001296185	**Problem:** When multiple Vendor specific capabilities are found in a single function, which is legal per the specification, the model reports an error.
	Resolution: Enhanced the model to designate capabilities as possible multiple instance. **Added Features**: `svt_pcie_uvm_config_space_capability` now includes flag set in constructor, `allow_mulitple_setting`, and method `allow_multiple()` to use when encountering multiple instances.
9001562821	**Problem:** `svt_pcie_pl_service::MBI_CMD` service request is working based on physical lane numbers and not based on logical lane numbers which is creating a problem when lane reversal is enabled.
	Resolution: Corrected the model. **Backwards Compatibility Affected:** Yes. Now, `svt_pcie_pl_service::MBI_CMD` service request will work based on logical lane numbers instead of physical lane numbers.
9001569221	**Problem:** Xcelium issues a warning while randomization with one of the constraints.
	Resolution: Fixed the constraint to make is compatible with Xcelium version 9.09-s001.
9001573016	**Problem:** If unused/reserved bits of TxElecIdle[4:0] are set to 1, then SPIPE VIP does not detect the data properly.
	Resolution: Corrected the behavior.
9001574049	**Problem:** [PIPE 5 SerDes arch] [SPIPE] PCS.TxFifo is cleared even when tx is not idle.
	Resolution: Corrected the model.
9001574050	**Problem:** [PIPE 5 SerDes arch] [SPIPE] `phy_l0s_bad_rx_fts_count` and `phy_l0s_too_few_fts_between_eieos` checks failure.
	Resolution: Fixed the issue.

Table 6-41 Fixed B-STARs for Active PCIe Agent (Continued)

STAR Number	Description
9001574081	**Problem:** RxL0s transition fails when 80-bit PIPE width is used.
	Resolution: Corrected the model.
9001576599	**Problem:** PCS reports decode errors even on lanes which have already been downconfigured.
	Resolution: Fixed the PCS such that it disables the error checking based on `current_link_width` which has correct value of `link_width` irrespective of if downconfiguration happened before or after linkup.
9001576857	**Problem:** When RC aborts APN negotiation in `config.complete`, it does not clear symbol 14 after changing the modified TS usage mode back to PCIe.
	Resolution: Fixed the issue.
9001577369	**Problem:** VIP does not initiate speed change from 8G to 16G automatically because RC VIP was not advertising 16G support before speed change and hence `auto_initiate_speed_change_after_eq` was not getting set to 1.
	Resolution: Fixed the issue.
9001577982	**Problem:** In SerDes architecture, `DataBusWidth` value is driven by SPIPE and processed by MPIPE incorrectly.
	Resolution: Fixed the code. **Backwards Compatibility Affected:** Yes, `DataBusWidth` encoding is now fixed in SerDes architecture. Therefore, now the values will be different in SerDes architecture.
9001577983	**Problem:** In PIPE 5 SerDes architecture (MPIPE), few tasks switched between pclk and rxclk during rx detection.
	Resolution: Corrected the model.
2886527	**Problem:** In PIPE 5 SerDes architecture, unintentional skew occurs due to `rx_data_valid_block_count` variable difference between the lanes.
	Resolution: Fixed the issue.

6.22 Release Q-2019.12

6.22.1 Active UVM PCIe Agent Updates

6.22.1.1 Fixed E-STARs

Table 6-42 lists the STARs fixed in this release.

Table 6-42 Fixed E-STARs for Active PCIe Agent

STAR Number	Description
None	

6.22.1.2 Fixed B-STARs

Table 6-43 lists the STARs fixed in this release.

Table 6-43 Fixed B-STARs for Active PCIe Agent

STAR Number	Description
None	