Verification Continuum™

VC Verification IP
CXL Subsystem
Test Suite Release Notes

Version S-2021.06, June 2021

SYNOPSYS®

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Release Notes

1 Introduction

Compute Express Link (CXL) Subsystem Test Suite provides a test environment to verify CXL Device designs implementing Compute Express Link Specification, June 2019, Revision: 1.1 and Revision: 2.0, Oct 2020.

This version of CXL Test Suite is internally qualified with updated version of 5.95a release of Synopsys DWC CXL controller for Serial topology. You can contact Synopsys support if you need to use the PIPE topology.

Refer the CXL Test Suite user guide for product features and usage.

2 Methodology Support

This release of the CXL Subsystem Test Suite supports the UVM methodology (version 1.1d and version 1.2).

3 Supported Simulators

Simulator support: VCS/VCSMX 2020.12/2020.03

4 Documentation

Refer the 'README' file from installed testbench for more information on example usage.

```
"$DESIGNWARE_HOME/vip/svt/cxl_test_suite_svt/latest/examples/sverilog/tb_dut_cxl/
README"
```

You can contact Synopsys support for CXL Subsystem Test Suite - DW Controller Integration Guide.

4.1 Protocol

- Compute Express Link Specification, June 2019, Revision: 1.1
- Compute Express Link Specification, Oct 2020, Revision 2.0

5 Notes for S-2021.06

These are the enhancements for this release:

- Added the support for PHY DUT integration in CXL TS. Refer the *CXL Subsystem Test Suite UVM User Guide* for features and usage notes.
  - With behavioral model, it has been validated with Pipe5.1 in SerDes architecture with PCLK as phy input and output modes.
  - With actual PHY model, it has been validated with Pipe5.1 in SerDes architecture with PCLK as phy input mode.
- Added the support for Back-Annotation of Test Pass/Fail Results (From VDB). Refer the *CXL Subsystem Test Suite UVM User Guide* for details.
- Enhanced the following PL tests involving enabling of sync header bypass to work with Host as DUT:
  - `cxl_compliance_pl_sync_header_bypass`
  - `cxl_compliance_pl_skp_scheduling`
  - `cxl_compliance_pl_skp_exiting_data_stream`
- Updated the test `cxl_compliance_ras_cpl_timeout` for robustness.

5.1 E-STARs

Table 1 shows the list of Enhancements.

Table 1 Enhancements

STAR ID	Description
3674797	**Problem**: CXL Compliance 2.0: 14.13.13,14,15,16
	Resolution: Enhanced the CXL Test Suite such that it is compliant with • 14.13.13: MMR Device Status registers capabilities header register. • 14.13.14: MMR primary mailbox register capabilities header register. • 14.13.15: MMR secondary mailbox register capabilities header register. • 14.13.16: MMR Memory device register header capabilities register.
3686334	**Problem**: CXL Compliance 2.0: 14.13.10 `CXL_COMPLIANCE_MMR_HDM_DE`
	Resolution: Fixed the MMR test `"cxl_compliance_mmr_hdm_decoder_zero_size_commit"` for swap payload and timeout issue observed.
3699259	**Problem**: CXL Test APP Layer to check for Cache & Mem Enabled or not before initiating the traffic
	Resolution: • Updated the CXL Subsystem Test APP Layer to check for APN negotiation before initiating traffic for Cache/Mem device. • Added the CXL Test APP Layer status attribute to pass DUT side of APN negotiation status `"modified_ts_status"`. You can control the Cache/mem traffic generation based on this attribute. - Full Stack topology automatically pass this information from VIP Modified TS2 Status. Other topologies by default enable both Cache-Mem.

Table 1 Enhancements

STAR ID	Description
3373055	**Problem**: CXL TS V plan information
	Resolution: Updated the CXL Test Suite HVP to support Test Pass/Fail via VDB.
686098	**Problem**: Need to create separate test lists for PCIe TS test cases and CXL applicable test cases
	Resolution: Added the PCIe TS test list by-default in CXL TS. You can disable the default-inclusion with the help of macro `"SVT_CXL_SUBSYSTEM_EXCLUDE_ALL_PCIE_TS_TESTS_INCLUSION"`.

5.2 B-STARs

Table 2 shows the list of fixed Bugs.

Table 2 Fixed Bugs

STAR ID	Description
3689403	**Problem**: False failure in CXL compliance test `cxl_compliance_pl`
	Resolution: Fixed the PL test `"cxl_compliance_pl_link_initialization_resolution"` for an observed issue in `"check_supported_spec_ver"` API and its usage in the test suite.
3687345	**Problem**: CXL Compliance 2.0: 14.13.10 `CXL_COMPLIANCE_MMR_HDM_DE`
	Resolution: Fixed the MMR test `"cxl_compliance_mmr_device_capabilities_array"` for an observed failure wherein the capabilities header base address was not allocated valid values.

5.3 Backward Incompatibility Changes

From this release onwards, the LPIF testlist(cxl_lpif_testlist.svi) and AMUX testlist(cxl_arb_mux_testlist.svi) empty files are removed. The user needs to remove these files from their top.sv, if they have included them.

6 Known Limitations

1. The test enters retrain for the second time and cache/mem DL intermittently reports duplicate packet and fails. This requires VIP update and would be resolved in subsequent release.
   - `cxl_compliance_amux_almp_error_test`
   - `cxl_compliance_amux_entry_into_l0_synchronization`
2. These tests are failing with Designware CXL controller as handling of unexpected ALMP is not supported by the controller:
   - `cxl_compliance_amux_almp_error_test`
   - `cxl_compliance_amux_recovery_re_entry_test`

- `cxl_compliance_amux_unexpected_status_almp_test`

3. Designware CXL controller after being in L0 and when the link goes to Recovery and comes back to L0, has the following issues:
   - Spurious Retry Frame before Recovery entry
   - Protocol flit before RetryAck while exiting Recovery

   You can contact Synopsys support.
4. The tests `cxl_compliance_pl_uncorrectable_framing_error` and `cxl_compliance_pl_uncorrectable_mismatched_pid_error` are failing with Designware CXL Controller with the following error:

   ```
   UVM_ERROR [register_fail:ACTIVE_DL:SEQ_NUM:dl_receive_illegal_seq_num]
   ProcessReceivedTLP: Received TLP with invalid seq num = 1, next_rcv_seq = 0
   ```
5. The test `cxl_compliance_l1_crc_error_injection_retry_abort`Designware CXL Controller version 5.90a GA is reporting the following failure and needs to be demoted:

   ```
   UVM_ERROR [CXL_PROT_TYPE_CACHE].m_cxlChannelInitAgent.m_cxlChannelInitMasterDriver
   [m_cxlChannelInitMasterDriver] Ack is not deasserted by CXL Controller
   in 10000 cycles
   ```
6. The default value of Synopsys controller for CXL Cache and Mem Component registers filed `array_size` is invalid. Therefore, CXL Subsystem VIP `enumerate_cxl_device` API is tweaked such that it cannot access capabilities with value greater than 8.
7. Synopsys DW Controller as DUT: VIP check `phy_flexbus_tlp_ending_on_flit_boundary` fails when both CXL.io and CXL.cache/mem traffic is exchanged. Synopsys DW controller sends a TLP that ends on the flit boundary.
   Contact Synopsys support for assistance. Currently this strict rule is being discussed with CXL Consortium. Until then, this error is demoted in CXL TS.
8. `cxl_compliance_amux_almp_error_test` might fail for few seeds with `expected_retry_req_received` check failure.
9. Currently FLR Compliance Tests for section 14.9.4 (FLR Test), 14.9.5 (Flexbus Range Setup Time), 14.9.6 (FLR Memory Test) are supported for CXL 1.1 version only.
10. For these tests, you can contact Synopsys support:
    - `cxl_compliance_rit_flexbus_range_setup_time`
11. Following tests have been validated only with VIP-VIP b2b set up and should be excluded from simulations with DWIP because of known limitations.
    a. CXL Power Management:
       - `ts.cxl_compliance_amux_l1x_state_resolution.sv`
       - `ts.cxl_compliance_amux_l1x_pm_state_request_rejection_test.sv`
       - `ts.cxl_compliance_amux_active_to_l2_transition_test.sv`
       - `ts.cxl_compliance_amux_active_to_l1x_transition.sv`
       - `ts.cxl_compliance_amux_l1x_to_active_transition.sv`

    b. Drift Buffer and Sync Header Bypass are not supported till 5.90a version of IIP:
       - `ts.cxl_compliance_pl_sync_header_bypass.sv`
       - `ts.cxl_compliance_pl_skp_scheduling.sv`
       - `ts.cxl_compliance_pl_skp_exiting_data_stream.sv`

- ts.cxl_compliance_pl_drift_buffer_enable.sv

c. Device DWIP tries to enter into L1 state when D3 is initialized. For 1.1, this is a limitation and for 2.0 specification ambiguity is observed, which is being discussed with Consortium. Below tests also require PM VDM response from RTL. (DWIP does not support PM VDM. So RTL/ Application has to perform this handshake)

- ts.cxl_compliance_rit_warm_reset.sv
- ts.cxl_compliance_rit_sleep_state.sv
- ts.cxl_compliance_rit_cold_reset.sv

d. Control and Status registers, and Memory Mapped register feature tests (14.8, 14.13):

- IDE, HDM, device Capability, GPF, DOE, Non-CXL Function, Register locator: These capabilities need to be implemented out of DW CXL Controller.
- CXL TS validated these tests with VIP-VIP setup only.

e. Security Feature Tests (14.11):

- IDE feature is not supported by DW CXL Controller.
- CXL TS validated these tests with VIP-VIP setup only.

12. The `cxl_compliance_amux_reset_entry` and `cxl_compliance_pl_protocol_id_check` tests may fail for few seeds with `transaction_inactivity_timeout failure` and the following error:

```
UVM_ERROR
uvm_test_top.env.host_env.cache_mem_env.host[0].tl_driver [sample_response_and_data]
{ADDR('h0) TYPE(CACHE_D2H_DATA_CH_XACT) OPCODE() ID('hd28) TAG('h0)} Received
CACHE_D2H_DATA_CH_XACT response with id('hd28), Tag('h0), LDID(0). But There is no
transaction waiting for CACHE_D2H_DATA_CH_XACT response. Hence, ignoring it.
```

This error is observed as currently CXL VIP doesn't support data before response scenarios for H2D Snoop transactions.

13. Following test may fail with the mentioned UVM_WARNING due to one of the VIP behaviors which is being discussed:

- `cxl_compliance_pl_eds_token`

```
UVM_WARNING
[register_fail:ACTIVE_DL:REPLAY:dl_replay_timer_timeout] UpdateReplayTimer: Replay timer
timed out. replay_timer_limit = 31000
```

Contact Synopsys support for the same.

14. Following PL tests are currently not applicable for Host DUT mode:

- `cxl_compliance_pl_sync_header_bypass`
- `cxl_compliance_pl_skp_scheduling`
- `cxl_compliance_pl_skp_exiting_data_stream`

15. Following MMR tests may fail when run with Synopsys IIP as controller, since Synopsys IIP does not program respective memory mapped registers by default. Contact Synopsys support for any further details.

- `cxl_compliance_mmr_device_capabilities_array`
- `cxl_compliance_mmr_device_status_registers_capabilities_header_register`

- cxl_compliance_mmr_primary_mailbox_registers_capabilities_header_register
- cxl_compliance_mmr_secondary_mailbox_registers_capabilities_header_register
- cxl_compliance_mmr_memory_device_registers_capabilities_header_register

16. Following Arb-Mux compliance tests may fail with the error signature as illustrated when run with 'CXL.IO only' topology in CXL 2.0 mode.
    - cxl_compliance_amux_almp_error_test
    - cxl_compliance_amux_entry_into_l0_synchronization
    - cxl_compliance_amux_recovery_re_entry_test
    - cxl_compliance_amux_unexpected_status_almp_test
    - cxl_compliance_amux_rst_to_active_transition

    Error Signature:

    ```
    UVM_ERROR [body : SNPS_CXL_TS_COMPLIANCE] Sequence is not applicable when only one protocol(IO only) is enabled
    ```
17. The SVT_DEBUG_OPTS is not supported for CXL TestSuite Test Application layer component.

7 Notes for Previous Releases

7.1 Notes for R-2021.03-2

These are the enhancements for this release:

- Fixed the PL Drift Buffer test for an observed constraint failure issue under all topologies.
- DWIP version specific example compile files are delivered as part of TS (under *tb_dut_cxl/dut/iip_<version>* directory). Refer *Appendix A* section in *CXL Subsystem Test Suite UVM User Guide* for details.
- Added back the support for native application interface (Channel protocol interface) for Cache.Mem for 5.80a version of DWIP also. There is no backward incompatibility now.
- Added raise and drop objection for 'svt_cxl_subsystem_ts_base_sequence' class so that it is not required to set in the derived sequences.
- Updated the svt_cxl_subsystem_ts_compliance_crt_doe_capabilities_sequence for lookup for CRT table access DOE in all different DOE capabilities.
- Updated the `include_file macro to resolve compile failure when using the VCS -p1800_macro_expansion option.
- Enhanced the TLP Ends on Flit Boundary and sticky register tests to run with Full stack and IO only topologies. Checks related to Cache-Mem memory mapped registers are bypassed during IO only runs as the Cache-Mem memory mapped registers are not enumerated when Cache-Mem is absent.
- Fixed the CXL 1.1 MDT tests (14.7.1 and 14.7.2). These tests can now run seamlessly with IIP versions that are CXL 2.0 capable but runs in CXL 1.1 mode.
- Added the Compliance Test for section 14.11.3.5.3:
    - ts.cxl_compliance_ide_no_mac_inserted_in_mac_epoch.sv

7.1.1 E-STARs

Table 3 shows the list of Enhancements.

Table 3 Enhancements

STAR ID	Description
3627217	**Problem**: Multiple DOE Capability Enumeration
	Resolution: DOE capabilities base addr is stored in `ep_enumeration_status.ext_cap_base_addr[index]` where index is => `{24'h0,8'h DOE Cap Instance,16'h Cap ID, 16'h Target BDF}`. DOE Types enumeration via all DOE capabilities.
3647193	**Problem**: Compilation issue with the PCIe TS tests included as part of CXL TS execution.

	Resolution: Added the PCIe TS packages import in top module to resolve the issue:
	`import svt_pcie_test_suite_uvm_pkg::*;`
	`import snps_pcie_test_suite_pkg::*;`

3644300	**Problem**: Enhancement: CXL Device Capabilities Array Register
	Resolution: Updated the `cxl_compliance_mmr_device_capabilities_array` test for Steps 5 to 11 in section 14.13.12

7.1.2 B-STARs

Table 4 shows the list of fixed Bugs.

Table 4 Fixed Bugs

STAR ID	Description
3644348	**Problem**: UVM FATAL for `ep_enumeration_status` for Device Full stack VIP
	Resolution: Added check for Host VIP to enable EP enumeration status get via config DB. Refer *CXL Subsystem VIP documents* for more information.

7.2 Notes for R-2021.03-1

These are the enhancements for this release:

- Enabled the parameter, "`enable_gen4_added_imp_note`" by default for PCIe TS tests used in CXL framing.
- Updated the EP Enumeration status for DVSEC/VSEC storage. Refer *CXL Subsystem Release notes* for more information.
- Moved the macros, "`` `SVT_CXL_SUBSYSTEM_TS_GEN_TL_CACHE_MEM_TRAFFIC`" and "`` `SVT_CXL_SUBSYSTEM_TS_GEN_CXL_IO_TRAFFIC`" with "`svt_cxl_subsystem_ts_api_base_sequence.sv`" base sequence API "`generate_random_cxl_io_traffic`" and "`generate_random_cxl_tl_cm_traffic`". Refer the *HTML Class Reference Guide* present at the following location for details on the API:

$DESIGNWARE_HOME/vip/svt/cxl_test_suite_svt/latest/doc/cxl_test_suite_svt_uvm_reference/html/index

- CXL enumeration for PCIe TS Tests:

  While executing the PCIe TS tests, CXL Memory mapped registers enumeration supported is added in CXL TS.

  - Use plusargs "`EN_CXL_ENUMERATION_FOR_PCIE_TS_TEST_IN_CXL`" or base test attribute "`enable_cxl_enumeration_for_pcie_ts_test`" when executing PCIe TS tests in CXL Mode.
  - Added the PCIe TS configurations for this support using the test "`svt_cxl_subsystem_with_pcie_ts_base_test`".
    - Virtual method "`configure_pcie_ts_for_cxl_enumeration`" has been added with following configuration. You can override this method in extended class.

      - "`enable_post_enumeration_user_seq`" is set through config db. This has been added to setup Post enumeration user sequence for PCIe TS.

      - "`enable_user_sequece`" config DB is enabled.
  - Added the "`initiate_enumeration_for_pcie_ts_tests`" in CXL Base test that gets triggered in "`run_phase`".
    - Wait for PCIe Enumeration done and de-assert the status attribute for further processing.
    - Trigger CXL Memory mapped registers enumeration based on spec version negotiated.
    - Again assert "`enumeration_done`" of PCIe TS status class.
  - Added the sequence "`svt_pcie_ts_device_system_virtual_tl_post_enumeration_seq`" in CXL Env sequence collection. The overall responsibility of this sequence is to delay the PCIe TS test execution after enumeration so that CXL memory mapped registers can be enumerated first.
    - This sequence wait for "`enumeration_done`" to be de-asserted first and then wait for assertion.
    - Alternate implementation is available in the sequence to use "`delay`" based approach.

    To enable this feature, you can set the config-db for "`enumeration_status_or_delay_based_framework`" and set the delay using "`hold_pcie_test_exec_delay_in_ns`".
- CXL 1.1 device: Removed the first MWr TLP for RCRB area in "`enumerate_cxl_device`" as "*CXL 1.1 Upstream Port RCRB*" section of CXL 2.0 specification states that TLP should be MRd.
- Enhanced the Sticky Register test (`ts.cxl_compliance_srt_sticky_register.sv`) to work in Full Stack topology.
- Updated the base test API, "`initiate_primitive_io_cm_basic_init_seq`" as illustrated:
  - Added a wait for `cxl_enumeration_completed` before reading the PCIe capability register base address required for FLR testing (reading FLR capability).
- Corrected the register checking for Drift Buffer test (`ts.cxl_compliance_pl_drift_buffer_enable.sv`) to qualify it for VIP-IIP.
- Updated the enumeration API, `enumerate_cxl_device()` to trigger only when APN has been negotiated successfully and the flexbus component is enabled.

- Updated the API call for `enumerate_cxl_cache_mem_memory_mapped_registers()` to enable the calling only when the cache-mem is active. The API initially was getting called even when the cache-mem was not active.
- Updated the TLP end on flit boundary test/sequence (`ts.cxl_compliance_pl_tlp_ends_on_flit_boundary.sv`) to avoid constraint failure in internal regressions.
- **CXL2.0** Version support for FLR Tests (EA):
  - `cxl_compliance_rit_flr_test`
  - `cxl_compliance_rit_flr_memory_test`

    This test fails if the DUT is not mem capable.
  - `cxl_compliance_rit_flr_flexbus_range_setup_time`
    - This test fails if the DUT is not mem capable.
    - Uses Hot Reset (link down) in CXL 1.1 mode.
    - Initiates CXL Device Reset via 8.1.3.4 DVSEC CXL Control2 (Offset 10h) bit[2] in CXL 2.0 mode.
  - Added the new compliance test, `cxl_compliance_rit_cxl_reset_test` (applicable only for CXL 2.0).
  - Verified the `cxl_compliance_rit_cxl_reset_test` and `cxl_compliance_rit_flr_flexbus_range_setup_time` in VIP back to back setup.

    Note: It is not yet validated with Synopsys DWC CXL controller.

  All 4 Reset tests mentioned above are expected to undergo some structural updates in the April monthly release for more effective use model. You can refer the CXL User Guide for more details.
- Updated the RAS Feature Tests:
  - `cxl_compliance_ras_unexpected_cpl`
  - `cxl_compliance_ras_cpl_timeout`
  - `cxl_compliance_ras_io_poison_injection`
  - Updated the API call by passing relevant arguments to subroutine

    `set_cxl_ts_app_algorithm_configuration(app_cfg,enable_host)`
  - Removed the redundant API call for `initiate_primitive_io_cm_basic_init_seq()`. The API was getting triggered twice while executing `cxl_compliance_ras_unexpected_cpl` test.
  - Validated the tests with Synopsys Controller with error injection from VIP end.
- Added the following tests as part of section 14.13.9 CXL HDM Decoder Commit CXL2.0 MMR Compliance Test implementation:
  - `ts.cxl_compliance_mmr_hdm_decoder_commit.sv`
- Updated the AMUX tests to enable the enumeration for VIP-DUT scenario.

7.3 Notes for R-2021.03

These are the enhancements for this release:

- Tests added for the sections:

- 14.9.5, 14.9.9
- 14.8.24
- 14.15.1
- 14.11.3.5.1
- 14.13.8, 14.13.10, 14.13.12.

- License Changes - CXL 2.0 TestSuite is enabled in LIBRARY-19.
- The `mem_bar_mapped_to_internal_reg` attribute is mapped to CSR Status class.
- The global timeout enable issue has been fixed. The default value of `disable_global_timeout` must be disabled.
- CXL 1.1 Specification applicable RCRB next capability offset as '100h' check is fixed .To disable this check a variable `disable_cxl_1_1_upstream_port_rcrb_nxt_cap_off_check` =0 has been added.
- Updated the enumeration API `enumerate_cxl_device()` to use `link_num` in the CFG/MEM traffic generation.
- Fixed the typos in the enumeration API in Device Register interface.
- CXL 2.0 compliance tests for Section 14.9.9, 14.13.8, 14.13.10 and 14.13.12 are validated in VIP-VIP mode only.
- Removed calling of `create_cfg()` multiple times. (Tests are not required to guard code with `create_cfg_called` flag of base test) `create_cfg()` method is now called only once.
- Host DUT Address randomization in macro `SVT_CXL_SUBSYSTEM_TS_GEN_CXL_IO_TRAFFIC` is updated to exclude memory ranges.

7.4 Notes for R-2020.12-2-T-20200129

These are the enhancements for this release:

- CXL 2.0 Compliance Tests added for the sections:
  - 14.8.9, 14.8.15, 14.8.16, 14.8.17, 14.8.18, 14.8.19, 14.8.20
  - 14.13.1, 14.13.2, 14.13.4, 14.13.5, 14.13.7
  - 14.11.3.3
  - 14.14.1, 14.14.2.
- CXL 1.1 Compliance Tests added for the sections:
  - 14.4.5
  - 14.5.15.1

7.5 Notes for R-2020.12-2

These are the enhancements for this release:

- A new attribute `disable_global_timeout` is added in `svt_cxl_subsystem_base_test` to enable or disable the global timeout mechanism with the default setting of global timeout in disabled mode. If it is enabled, then the `global_timeout` attribute is used to configure the global timeout of the test

and you can override this attribute in extended test.
Also, you can re-define the macro in testbench `SVT_CXL_SUBSYSTEM_TEST_TIMEOUT` to override the default value.

- CXL 2.0 Compliance Tests added for the sections:
  - 14.11.3.4
  - 14.11.3.1

7.6 Notes for R-2020.12-1-T-20201221

These are the enhancements for this release:

- CXL 1.1 Compliance Tests for sections 14.4.9.3, 14.9.5, 14.10.1.2, and 14.10.1.9
- CXL 2.0 Compliance Tests added for the sections:
  - 14.4.1, 14.4.2, 14.4.3
  - 14.6.15, 14.6.16
  - 14.8.1, 14.8.2, 14.8.3, 14.8.4, 14.8.5, 14.8.6, 14.8.7, 14.8.8, 14.8.23
  - 14.9.8.2
  - 14.10.1
- Existing CXL 1.1 Tests updated to support Execution with CXL 2.0 Device DUT

7.7 Notes for R-2020.12

These are the enhancements for this release:

- VIP version is updated as R-2020.12.

7.8 Notes for R-2020.09-3-T20201125

These are the enhancements for this release:

- Added Compliance tests for section 14.9 and 14.10.

7.8.1 Backward Incompatibility Changes

From this release onwards for Test Suite, the Cache.Mem stack support with DWC CXL controller version can be 5.90-ea01 or later (The impact is only when channel protocol environment in VTB is used as a BFM to communicate with VIP CacheMem TL, which indicates FULL_STACK mode with DWC CXL controller).

This is because of backward incompatible change introduced in CXL Channel Protocol environment related packages/agents of DWC CXL Controller (For example, `cxlPkg` is now split to `cxlTypesPkg`).

7.9 Notes for R-2020.09-2-T-20201030

These are the enhancements for this release:

- Added a new sequence for back door programming to enable Cache/Mem for Synopsys DWC CXL Controller.
- Added compliance tests for Sections: 14.4, 14,5, 14.9, and 14.10.

7.10 Notes for R-2020.09-1

- For all compliance (cxl_compliance_*) tests, Type(1/2/3) of the CXL Device is updated based on flexbus capability after APN negotiation is successful.
- `svt_cxl_subsystem_ts_virtual_tasks_to_be_overriden_by_user_sequence` class is added which contains virtual methods/tasks that need to be overridden by you based on DUT implementation. Compliance test sequences invoke those methods in their body() methods.
- Compliance Tests for Section: 14.4.3, 14.4.4, 14.4.6, 14.4.8

  Note: Validation criteria for above mentioned tests are limited to VIP-VIP b2b set up.
- Enumeration Updates
  - CXL DVSEC and CXL Test DVSEC finding loop is modified to exit at null extended capability only.
  - Fixed the Capability ID capture from payload from proper bits.
  - Updated Enumeration to resolve conflict with RCRB, MEMBAR0 and BAR Ranges.

7.11 Notes for Q-2020.06-3

- CXL Test Application Layer for Device DUT.
  - Algorithm 1a,1b and 2 for CXL.Cache.

    Note: Full cache-line is processed currently.
- Compliance test for sections: 14.3.6.1.2, 14.3.6.1.3, 14.4.2, 14.5.10, 14.5.11, 14.5.12, 14.7.1, 14.7.2, 14.8.1.

7.12 Notes for Q-2020.06-2

- Env framework for integration of DWC_CXL Controller DUT Protocol If : PIPE 5.1(SerDes Arch), Application IF : CXL.$ Native IF (Product : Compile Only).
- Remove '`+define+SVT_CXL_SUBSYSTEM_EXCLUDE_PCIE_TS_DATA`' from the `sim_build_options` if you are doing the following:

  a. Integrating DUT

  b. Running PCIe TestSuite Tests

  Removing this define will bring in PCIe TestSuite.
- CXL.Cache Integration Test
- CXL Test Application Layer for Device DUT:
  - Algorithm 1b & 2 for CXL.io Device.
  - Algorithm 1a,1b & 2 for CXL.Mem
- Compliance tests for section: 14.3.6.1.4, 14.4.1, 4.5.7.

7.13 Notes for Q-2020.06-1-T-20200619

- CXL Upstream port RCRB and MEMBAR0 enumeration and hooks in enumeration sequence.
- CXL Test Application Layer for Device DUT to support Algorithm 1a for CXL.io Device.
- Env framework for integration of DWC_CXL Controller DUT Protocol If: Serial IF, Application IF: CXL Cache/Memory Native only (Product: Compile Only).

- 10 Compliance Tests added from chapter 14.5 and 14.6.
- `tb_dut_cxl` testbench is enhanced to disable Subsystem Internal debug prints. You can enable through `ENABLE_CXL_SUBSYSTEM_MESSAGES`.

7.14 Notes for Q-2020.03-3-T-20200522

- This is the first release for CXL Subsystem Test Suite.