Verification Continuum™

VC Verification IP
AMBA APB
UVM Getting Started Guide

Version S-2021.06, June 2021

SYNOPSYS®

Copyright Notice and Proprietary Information

Destination Control Statement

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the reader's responsibility to determine the applicable regulations and to comply with them.

Disclaimer

SYNOPSYS, INC., AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Trademarks

Synopsys and certain Synopsys product names are trademarks of Synopsys, as set forth at http://www.synopsys.com/company/legal/trademarks-brands.html.
All other product or company names may be trademarks of their respective owners.

Free and Open-Source Software Licensing Notices

If applicable, Free and Open-Source Software (FOSS) licensing notices are available in the product installation.

Third-Party Links

Any links to third-party websites included in this document are for your convenience only. Synopsys does not endorse and is not responsible for such websites and their practices, including privacy practices, availability, and content.

www.synopsys.com

Contents

Preface

About This Document

This Getting Started Guide presents information about integrating the VC VIP for APB (referred to as VIP) into testbenches that are compliant with the SystemVerilog Universal Verification Methodology (UVM). You are assumed to be familiar with the AMBA APB protocol and UVM.

Web Resources

- Documentation through SolvNet: https://solvnetplus.synopsys.com (Synopsys password required)
- Synopsys Common Licensing (SCL): http://www.synopsys.com/keys

Customer Support

To obtain support for your product, choose one of the following:

1. Go to https://solvnetplus.synopsys.com and open a case.

   Enter the information according to your environment and your issue.
2. Send an e-mail message to support_center@synopsys.com.

   Include the Product name, Sub Product name, and Tool Version in your e-mail so it can be routed correctly.
3. Telephone your local support center.
   - North America:

     Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
   - All other countries:

     https://www.synopsys.com/support/global-support-centers.html

Synopsys Statement on Inclusivity and Diversity

Synopsys is committed to creating an inclusive environment where every employee, customer, and partner feels welcomed. We are reviewing and removing exclusionary language from our products and supporting customer-facing collateral. Our effort also includes internal initiatives to remove biased language from our engineering and working environment, including terms that are embedded in our software and IPs. At the same time, we are working to ensure that our web content and software applications are usable to people of varying abilities. You may still find examples of non-inclusive language in our software or documentation as our IPs implement industry-standard specifications that are currently under review to remove exclusionary language.

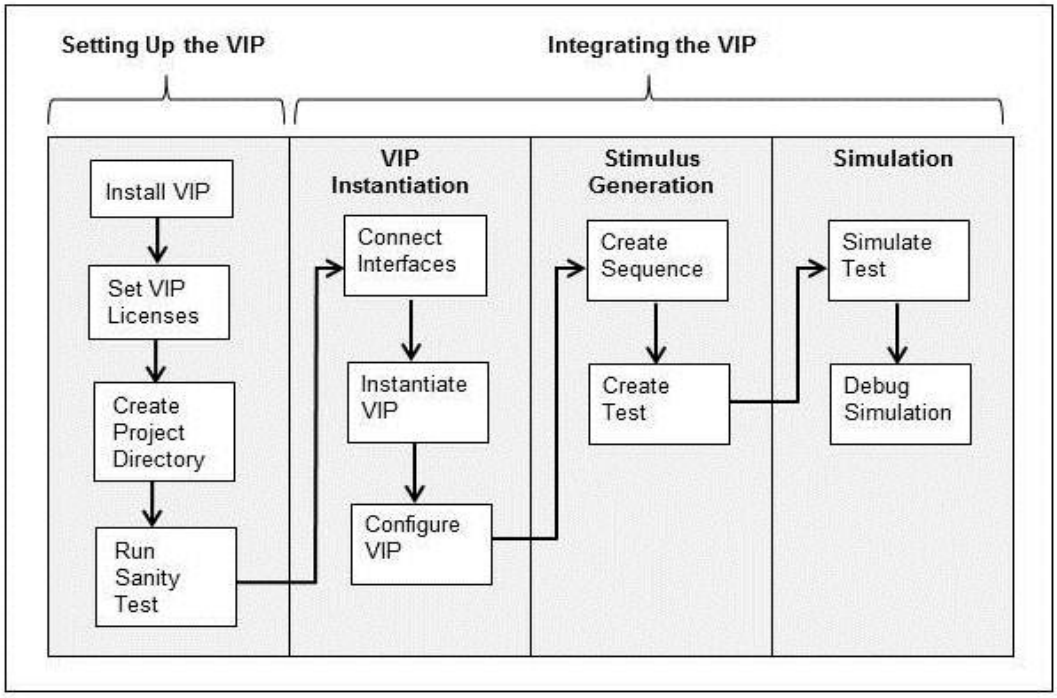
1 Overview of the Getting Started Guide

This Getting Started Guide presents information about integrating the VC VIP for APB (referred to as VIP) into testbenches that are compliant with the SystemVerilog Universal Verification Methodology (UVM). Figure 1-1 is the VIP integration and test work flow presented in this document. The steps for setting up the VIP are documented in the *VC Verification IP UVM Installation and Setup Guide*. This guide is available on the SolvNet Download Center (click here -> VC VIP Library -> R-2019.12-> Installation Guide) and in the VIP installation at the following location:

```
$DESIGNWARE_HOME/vip/svt/common/latest/doc/uvm_install.pdf
```

The VIP setup should be completed before executing the steps in this document.

Figure 1-1 VIP Integration and Test Work Flow



You are assumed to be familiar with the AMBA APB protocol and UVM. For more information on the VIP, refer to the *VC Verification IP AMBA APB UVM User Manual* on SolvNet (click here) or in the VIP installation at the following location:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/apb_svt_uvm_user_guide.pdf
```

2 Integrating the VIP into a User Testbench

The VC VIP for APB provides a suite of advanced SystemVerilog verification components and data objects that are compliant to UVM. Integrating these components and objects into any UVM compliant testbench is straightforward. For a complete list of VIP components and data objects, refer to the main page of the *VC VIP APB Class Reference Manual* (only in HTML format) at the following location:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/apb_svt_uvm_class_reference/html/
index.html
```

2.1 VIP Testbench Integration Flow

The APB system environment (svt_apb_system_env) is the top-level component provided by the VIP. This environment encapsulates all of the VIP components and implicitly constructs the required number of APB master and APB slave agents as specified by its system configuration object. You can instantiate and construct the APB system environment in the top-level environment of your UVM testbench.

Figure 2-1 Top-level Architecture of an APB VIP Testbench

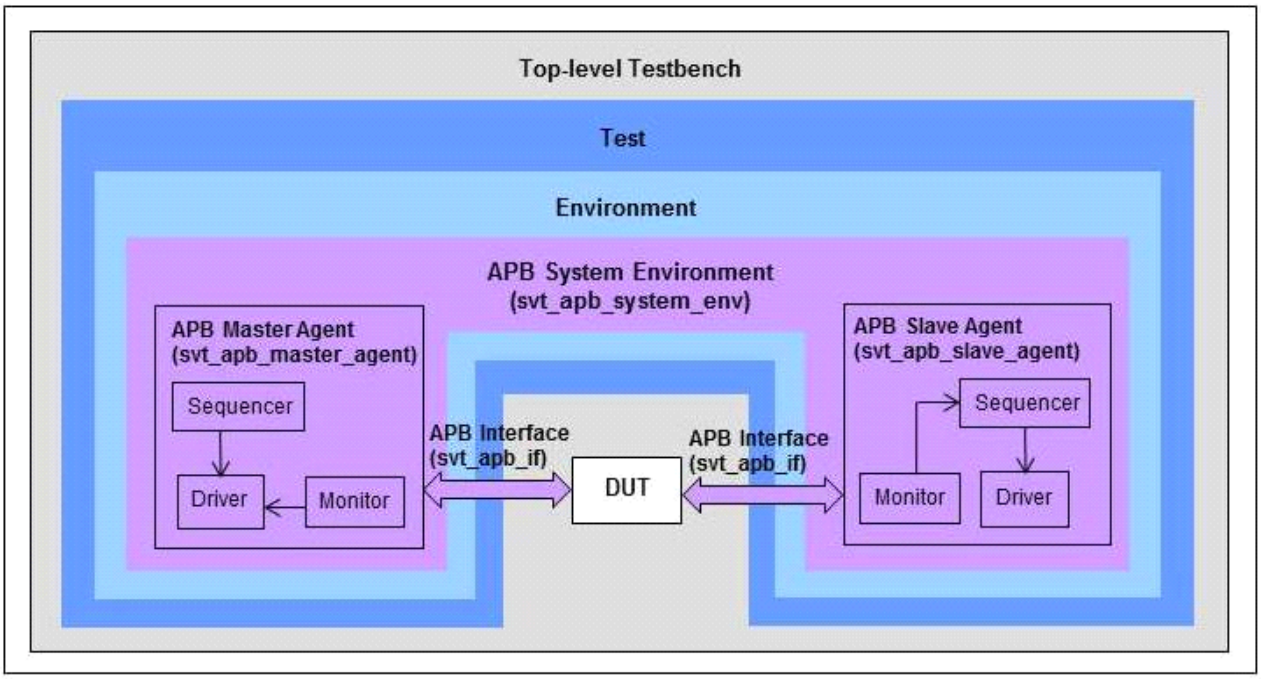


Figure 2-1 is a top-level architecture of a simple VC VIP for APB testbench. The steps for integrating the VIP into a UVM testbench are described in the following sections:

- "Connecting the VIP to the DUT"
- "Instantiating and Configuring the VIP"
- "Creating a Test Sequence"
- "Creating a Test"

The code snippets presented in this chapter are generic and can be applied to any UVM compliant testbench. For more information on the code usage, refer to the following example:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/examples/sverilog/
tb_apb_svt_uvm_basic_sys
```

2.1.1 Connecting the VIP to the DUT

The following are the steps to establish a connection between the VIP to the DUT in your top-level testbench:

- Include the standard UVM and VIP files and packages.

```
`include "uvm_pkg.sv"
`include "svt_apb.uvm.pkg"
`include "svt_apb_if.svi" //top-level APB interface

import uvm_pkg::*;
import svt_uvm_pkg::*;
import svt_apb_uvm_pkg::*;
```

- Instantiate and connect the top-level APB interface to a system clock.

```
svt_apb_if apb_if();
assign apb_if.pclk = <system clock>;
```

- Connect the top-level APB interface to the DUT and the APB system environment.

```
dut dut_inst(apb_if);

uvm_config_db#(svt_apb_vif)::set(uvm_root::get(),
   "uvm_test_top.env.apb_system_env", "vif", apb_if);
```

The `uvm_config_db` command connects the top-level APB interface to the virtual interface of the APB system environment. The "`uvm_test_top`" represents the top-level module in the UVM environment. The "`env`" is an instance of your testbench environment. The "`apb_system_env`" is an instance of the APB system environment (svt_apb_system_env).

- Connect the common reset pin of the APB interface. The reset connection propagates to each master and slave interface instance in the environment.

```
assign apb_if.preset = <User-select Reset Signal>;
```

2.1.2 Instantiating and Configuring the VIP

The following are steps to instantiate and configure the APB system environment in your testbench environment.

- Instantiate the APB system environment (svt_apb_system_env) in the build phase of your testbench environment.

```
svt_apb_system_env apb_system_env;

apb_system_env =
svt_apb_system_env::type_id::create("apb_system_env", this);
```

- Create a customized APB system configuration class by extending the APB system configuration class (`svt_apb_system_configuration`) and specifying the required configuration parameters.

  For example:

```
class cust_svt_apb_system_configuration extends
svt_apb_system_configuration;
  function new (string name =
"cust_svt_apb_system_configuration");
    super.new(name);

   // Create a single APB master agent and a single slave agent
    this.num_masters = 1;
    this.num_slaves  = 1;

    // Create port configurations
    this.create_sub_cfgs(1,1);

    this.paddr_width =
svt_apb_system_configuration::PADDR_WIDTH_16;
    this.pdata_width =
svt_apb_system_configuration::PDATA_WIDTH_32;
    this.apb4_enable = 0;
  endfunction
endclass
```

For more information on the configuration class, refer to the `svt_apb_system_configuration` and `svt_apb_slave_configuration` *Class References* at the following locations:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/apb_svt_uvm_class_reference/ht
ml/class_svt_apb_system_configuration.html
```

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/apb_svt_uvm_class_reference/ht
ml/class_svt_apb_slave_configuration.html
```

- Construct the customized APB system configuration and pass the configuration to the APB system environment (instance of svt_apb_system_env) in the build phase of your testbench environment.

```
cfg =
cust_svt_apb_system_configuration::type_id::create("cfg");

uvm_config_db#(svt_apb_system_configuration)::set(this,
"apb_system_env", "cfg", cfg);
```

The "`cust_svt_apb_system_configuration`" is the customized APB system configuration as defined in the previous step. The "`cfg`" is an instance of this configuration.

2.1.3 Creating a Test Sequence

The VIP provides a base sequence class for the APB master agent (`svt_apb_master_base_sequence`) and the APB slave agent (svt_apb_slave_base_sequence). You can extend these base sequences to create test sequences for the APB master and slave agents.

For more information on the APB master and slave base sequences, and the VIP sequence collection, refer to the Sequence Page of the *VC VIP APB Class Reference Manual* at the following location:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/
apb_svt_uvm_class_reference/html/sequencepages.html
```

In addition, a list of random and directed sequences are available in the VIP examples. For more information on the example sequences, refer to the example directories at the following location:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/examples/sverilog
```

Note
You must set a slave response sequence for active slaves in the run phase.

2.1.4 Creating a Test

You can create a VIP test by extending the uvm_test class. In the build phase of the extended class, you construct the testbench environment and set the respective APB master and slave sequences.

```
class random_wr_rd_test extends uvm_test;

  // build_phase
  env = apb_basic_env::type_id::create("env", this);

  uvm_config_db#(uvm_object_wrapper)::set(this,
     "env.apb_system_env.master*.sequencer.main_phase",
     "default_sequence",
apb_master_wr_rd_sequence::type_id::get());

  uvm_config_db#(uvm_object_wrapper)::set(this,
     "env.apb_system_env.slave*.sequencer.run_phase",
     "default_sequence",
     svt_apb_slave_memory_sequence::type_id::get());
```

2.2 Compiling and Simulating a Test with the VIP

The steps for compiling and simulating a test with the VIP are described in the following sections:

- “Directory Paths for VIP Compilation”
- “VIP Compile-time Options”
- “VIP Runtime Option”

2.2.1 Directory Paths for VIP Compilation

You need to specify the following directory paths in the compilation commands for the compiler to load the VIP files.

```
+incdir+project_directory_path/include/sverilog
+incdir+project_directory_path/src/sverilog/vendor
```

where *project_directory_path* is your project directory and *vendor* is your simulator vendor.

For example:

```
+incdir+/home/project1/testbench/vip/include/sverilog
+incdir+/home/project1/testbench/vip/src/sverilog/vcs
```

2.2.2 VIP Compile-time Options

The following are the required compile-time options for compiling a testbench with the VC VIP for AMBA APB:

```
+define+SVT_UVM_TECHNOLOGY
+define+UVM_PACKER_MAX_BYTES=1500000
+define+UVM_DISABLE_AUTO_ITEM_RECORDING
+define+SYNOPSYS_SV
```

Note

`UVM_PACKER_MAX_BYTES define` needs to be set to maximum value as required by each VIP title in your testbench. For example, if VIP title 1 needs `UVM_PACKER_MAX_BYTES` to be set to 8192, and VIP title 2 needs `UVM_PACKER_MAX_BYTES` to be set to 500000, you need to set `UVM_PACKER_MAX_BYTES` to 500000.

Macro	Description
SVT_UVM_TECHNOLOGY	Specifies SystemVerilog based VIPs that are compliant with UVM
UVM_PACKER_MAX_BYTES	Sets to 1500000 or greater
UVM_DISABLE_AUTO_ITEM_RECORDING	Disables the UVM automatic transaction begin and end event triggering and recording
SYNOPSYS_SV	Specifies SystemVerilog based VIPs that are compliant with UVM

The following compile-time option is required if and only if you have created a user-defined file to override the VIP default maximum values of the system constants such as maximum delay values and maximum address width.

```
+define+SVT_APB_INCLUDE_USER_DEFINES
```

For more information, refer to Section 3.3.7, "Overriding System Constants" of the *VC Verification IP AMBA APB UVM User Manual*.

2.2.3 VIP Runtime Option

No VIP specific runtime option is required to run simulations with the VIP. Only relevant UVM runtime options are required.

For example:

```
+UVM_TESTNAME=random_wr_rd_test
```

A Summary of Commands, Documents, and Examples

A.1 Commands in This Document

Display VIP models and examples under the VIP installation directory specified by $DESIGNWARE_HOME:

```
% $DESIGNWARE_HOME/bin/dw_vip_setup -info home
```

Add VIP models to the project directory:

```
% $DESIGNWARE_HOME/bin/dw_vip_setup  -path project_directory -add
VIP_model -svlog
```

Add VIP examples to the directory where the command is executed:

```
% $DESIGNWARE_HOME/bin/dw_vip_setup -e VIP_example -svlog
```

A.2 Primary Documentation for VC VIP APB

VC Verification IP UVM Installation and Setup Guide:

```
$DESIGNWARE_HOME/vip/svt/common/latest/doc/uvm_install.pdf
```

VC VIP APB UVM User Manual:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/apb_svt_uvm_user_guide.pdf
```

VC VIP APB Getting Started Guide:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/apb_svt_uvm_getting_started.pdf
```

VC VIP APB Quickstart:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/examples/sverilog/
tb_apb_svt_uvm_basic_sys/doc/tb_apb_svt_uvm_basic_sys/index_basic.html
```

VC VIP APB Class Reference Manual:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/apb_svt_uvm_class_reference/html/
index.html
```

VC VIP APB Verification Plans:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/VerificationPlans
```

A.3 Example Home Directory

Directory that contains a list of VIP example directories:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/examples/sverilog
```

View simulation options for each example:

```
gmake help
```