Verification Continuum™

VC Verification IP
AMBA AHB
UVM Getting Started Guide

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SYNOPSYS®

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Preface

About This Document

This Getting Started Guide presents information about integrating the VC VIP for AHB (referred to as VIP) into testbenches that are compliant with the SystemVerilog Universal Verification Methodology (UVM). You are assumed to be familiar with the AMBA AHB protocol and UVM.

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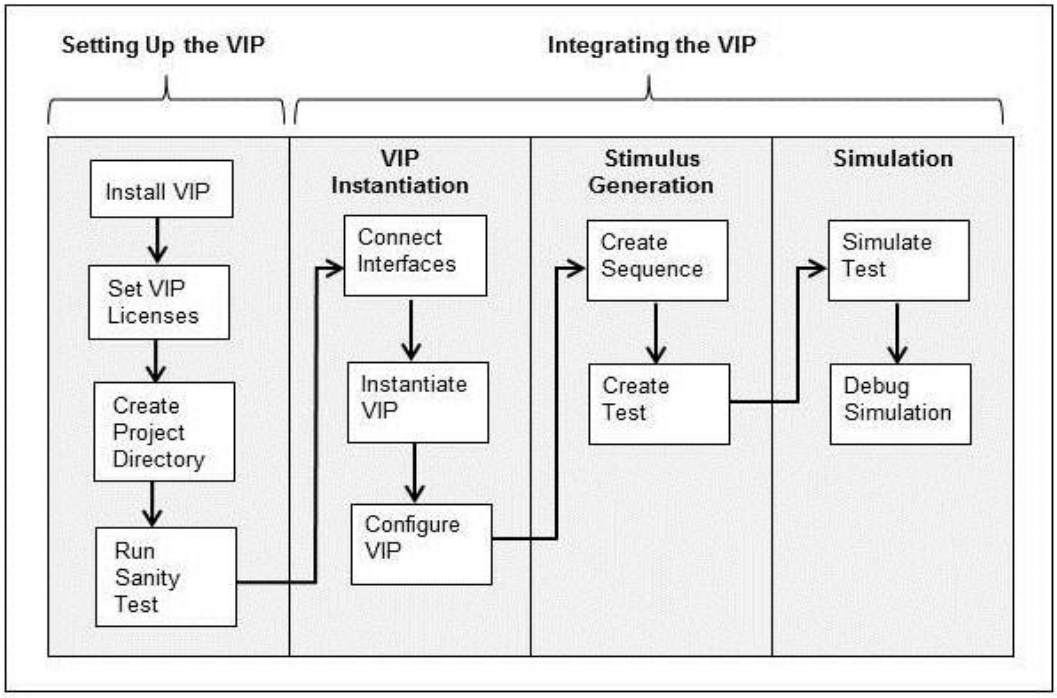
1 Overview of the Getting Started Guide

This Getting Started Guide presents information about integrating the VC VIP for AHB (referred to as VIP) into testbenches that are compliant with the SystemVerilog Universal Verification Methodology (UVM). Figure 1-1 is the VIP integration and test work flow presented in this document. The steps for setting up the VIP are documented in the *VC Verification IP UVM Installation and Setup Guide*. This guide is available on the SolvNet Download Center (click here -> VC VIP Library -> R-2020.12-> Installation Guide) and in the VIP installation at the following location:

```
$DESIGNWARE_HOME/vip/svt/common/latest/doc/uvm_install.pdf
```

The VIP setup should be completed before executing the steps in this document.

Figure 1-1 VIP Integration and Test Work Flow



You are assumed to be familiar with the AMBA AHB protocol and UVM. For more information on the VIP, refer to the *VC Verification IP AMBA AHB UVM User Manual* on SolvNet (click here) or in the VIP installation at the following location:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/ahb_svt_uvm_user_guide.pdf
```

2 Integrating the VIP into a User Testbench

The VC VIP for AHB provides a suite of advanced SystemVerilog verification components and data objects that are compliant to UVM. Integrating these components and objects into any UVM compliant testbench is straightforward. For a complete list of VIP components and data objects, see the main page of the *VC VIP AHB Class Reference Manual* (only in HTML format) at the following location:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/ahb_svt_uvm_class_reference/html/
index.html
```

2.1 VIP Testbench Integration Flow

The AHB system environment (`svt_ahb_system_env`) is the top-level component provided by the VIP. This environment encapsulates all of the VIP components and implicitly constructs the required number of AHB master and AHB slave agents as specified by its system configuration object. You can instantiate and construct the AHB system environment in the top-level environment of your UVM testbench.

Figure 2-1 Top-level Architecture of an AHB VIP Testbench

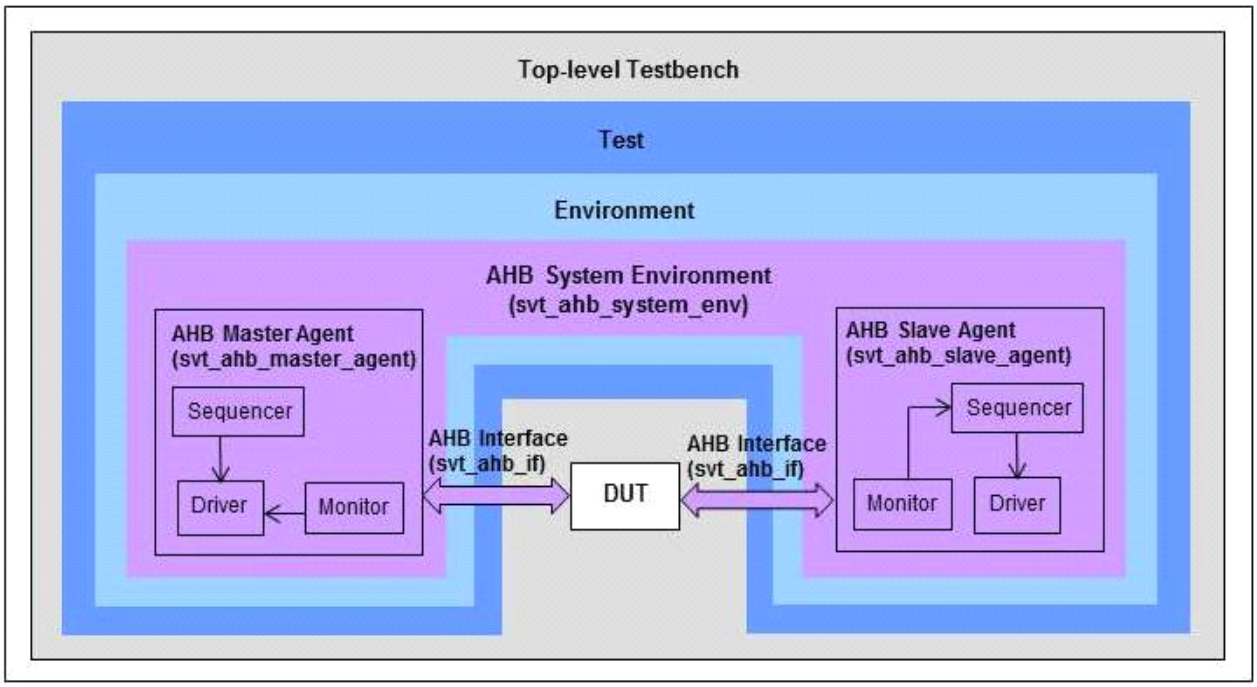


Figure 2-1 is a top-level architecture of a simple VC VIP for AHB testbench. The steps for integrating the VIP into a UVM testbench are described in the following sections:

- "Connecting the VIP to the DUT"
- "Instantiating and Configuring the VIP"
- "Creating a Test Sequence"
- "Creating a Test"

The code snippets presented in this chapter are generic and can be applied to any UVM compliant testbench. For more information on the code usage, see the following example:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/examples/sverilog/
tb_ahb_svt_uvm_basic_sys
```

2.1.1 Connecting the VIP to the DUT

The following are the steps to establish a connection between the VIP to the DUT in your top-level testbench:

- Include the standard UVM and VIP files and packages.

```
`include "uvm_pkg.sv"
`include "svt_ahb.uvm.pkg"
`include "svt_ahb_if.svi" //top-level AHB interface

import uvm_pkg::*;
import svt_uvm_pkg::*;
import svt_ahb_uvm_pkg::*;
```

- Instantiate and connect the top-level AHB interface to a system clock.

```
svt_ahb_if ahb_if();

assign ahb_if.hclk = <system clock>;"
assign ahb_if.hresetn = <System reset>;
```

- Connect the top-level AHB interface to the DUT and the AHB system environment.

```
dut dut_inst(ahb_if);

uvm_config_db#(svt_ahb_vif)::set(uvm_root::get(),
"uvm_test_top.env.ahb_system_env", "vif", ahb_if);
```

  The `uvm_config_db` command connects the top-level AHB interface to the virtual interface of the AHB system environment. The `uvm_test_top` represents the top-level module in the UVM environment. The `env` is an instance of your testbench environment. The `ahb_system_env` is an instance of the AHB system environment (`svt_ahb_system_env`).

- Connect the common reset pin of the AHB interface. The reset connection propagates to each master and slave interface instance in the environment.

```
assign ahb_if.hresetn = <User-select Reset Signal>;
```

2.1.2 Instantiating and Configuring the VIP

The following are steps to instantiate and configure the AHB system environment in your testbench environment.

- Instantiate the AHB system environment (`svt_ahb_system_env`) in the build phase of your testbench environment.

```
svt_ahb_system_env ahb_system_env;

ahb_system_env =
svt_ahb_system_env::type_id::create("ahb_system_env", this);
```

- Create a customized AHB system configuration class by extending the AHB system configuration class (`svt_ahb_system_configuration`) and specifying the required configuration parameters.

  For example:

```
class cust_svt_ahb_system_configuration extends
svt_ahb_system_configuration;
  function new (string name =
"cust_svt_ahb_system_configuration");
    super.new(name);

    // Create a single AHB master agent and a single slave agent
    this.num_masters = 1;
    this.num_slaves  = 1;

    // Create port configurations
    this.create_sub_cfgs(1,1);

    this.master_cfg[0].data_width = 256;
    this.slave_cfg[0].data_width = 256;

    // Set interface as AHB_LITE
    this.ahb_lite = 1;

  endfunction
endclass
```

For more information on the configuration class, see the *svt_ahb_configuration*, *svt_ahb_master_configuration* and *svt_ahb_slave_configuration Class References* at the following locations:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/
ahb_svt_uvm_class_reference/html/class_svt_ahb_configuration.html

$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/
ahb_svt_uvm_class_reference/html/
class_svt_ahb_master_configuration.html

$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/
ahb_svt_uvm_class_reference/html/
class_svt_ahb_slave_configuration.html
```

- Construct the customized AHB system configuration and pass the configuration to the AHB system environment (instance of `svt_ahb_system_env`) in the build phase of your testbench environment.

```
cfg =
cust_svt_ahb_system_configuration::type_id::create("cfg");

uvm_config_db#(svt_ahb_system_configuration)::set(this,
"ahb_system_env", "cfg", cfg);
```

The `cust_svt_ahb_system_configuration` is the customized AHB system configuration as defined in the previous step. The "`cfg`" is an instance of this configuration.

2.1.3 Creating a Test Sequence

The VIP provides a base sequence class for the AHB master agent (`svt_ahb_master_transaction_base_sequence`) and the AHB slave agent (`svt_ahb_slave_transaction_base_sequence`). You can extend these base sequences to create test sequences for the AHB master and slave agents.

For more information on the AHB master and slave base sequences, and the VIP sequence collection, see the Sequence Page of the *VC VIP AHB Class Reference Manual* at the following location:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/
ahb_svt_uvm_class_reference/html/sequencepages.html
```

In addition, a list of random and directed sequences are available in the VIP examples. For more information on the example sequences, refer to the example directories at the following location:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/examples/sverilog
```

2.1.4 Creating a Test

You can create a VIP test by extending the `uvm_test` class. In the build phase of the extended class, you construct the testbench environment and set the respective AHB master and slave sequences.

```
class random_wr_rd_test extends uvm_test;

  // build_phase
  env = ahb_basic_env::type_id::create("env", this);

  uvm_config_db#(uvm_object_wrapper)::set(this,
     "env.ahb_system_env.master*.sequencer.main_phase",
     "default_sequence",
ahb_master_wr_rd_sequence::type_id::get());

  uvm_config_db#(uvm_object_wrapper)::set(this,
     "env.ahb_system_env.slave*.sequencer.run_phase",
     "default_sequence",
     ahb_slave_mem_response_sequence::type_id::get());
```

Note
You must set a slave response sequence for active slaves in the run phase.

2.2 Compiling and Simulating a Test with the VIP

The steps for compiling and simulating a test with the VIP are described in the following sections:

- "Directory Paths for VIP Compilation"
- "VIP Compile-time Options"
- "VIP Runtime Option"

2.2.1 Directory Paths for VIP Compilation

Specify the following directory paths in the compilation commands for the compiler to load the VIP files.

```
+incdir+project_directory_path/include/sverilog
+incdir+project_directory_path/src/sverilog/vendor
```

where *project_directory_path* is your project directory and vendor is your simulator vendor.

For example:

```
+incdir+/home/project1/testbench/vip/include/sverilog
+incdir+/home/project1/testbench/vip/src/sverilog/vcs
```

2.2.2 VIP Compile-time Options

The following are the required compile-time options for compiling a testbench with the VC VIP for AMBA AHB:

```
+define+SVT_UVM_TECHNOLOGY
+define+UVM_PACKER_MAX_BYTES=1500000
+define+UVM_DISABLE_AUTO_ITEM_RECORDING
+define+SYNOPSYS_SV
```

Note
`UVM_PACKER_MAX_BYTES define` needs to be set to maximum value as required by each VIP title in your testbench. For example, if VIP title 1 needs `UVM_PACKER_MAX_BYTES` to be set to 8192, and VIP title 2 needs `UVM_PACKER_MAX_BYTES` to be set to 500000, you need to set `UVM_PACKER_MAX_BYTES` to 500000.

Macro	Description
SVT_UVM_TECHNOLOGY	Specifies SystemVerilog based VIPs that are compliant with UVM
UVM_PACKER_MAX_BYTES	Sets to 1500000 or greater
UVM_DISABLE_AUTO_ITEM_RECORDING	Disables the UVM automatic transaction begin and end event triggering and recording
SYNOPSYS_SV	Specifies SystemVerilog based VIPs that are compliant with UVM

The following compile-time option is required if and only if you have created a user-defined file to override the VIP default maximum values of the system constants such as maximum delay values and maximum address width.

```
+define+SVT_AHB_INCLUDE_USER_DEFINES
```

For more information, seeSection 3.3.7, *Overriding System Constants* of the *VC Verification IP AMBA AHB UVM User Manual*.

2.2.3 VIP Runtime Option

No VIP specific runtime option is required to run simulations with the VIP. Only relevant UVM runtime options are required.

For example,

```
+UVM_TESTNAME=random_wr_rd_test
```

A Summary of Commands, Documents, and Examples

A.1 Useful Commands

Display VIP models and examples under the VIP installation directory specified by $DESIGNWARE_HOME:

```
% $DESIGNWARE_HOME/bin/dw_vip_setup -info home
```

Add VIP models to the project directory:

```
% $DESIGNWARE_HOME/bin/dw_vip_setup  -path project_directory -add
VIP_model -svlog
```

Add VIP examples to the directory where the command is executed:

```
% $DESIGNWARE_HOME/bin/dw_vip_setup -e VIP_example -svlog
```

A.2 Primary Documentation for VC VIP AHB

VC Verification IP UVM Installation and Setup Guide:

`$DESIGNWARE_HOME/vip/svt/common/latest/doc/uvm_install.pdf`

VC VIP AHB UVM User Manual:

`$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/ahb_svt_uvm_user_guide.pdf`

VC VIP AHB Getting Started Guide:

`$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/ahb_svt_uvm_getting_started.pdf`

VC VIP AHB Class Reference Manual:

`$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/ahb_svt_uvm_class_reference/html/index.html`

VC VIP AHB Verification Plans:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/VerificationPlans
```

A.3 Example Home Directory

Directory that contains a list of VIP example directories:

```
$DESIGNWARE_HOME/vip/svt/amba_svt/latest/examples/sverilog
```

View simulation options for each example:

```
gmake help
```