Verification Continuum™

VC Verification IP PCIe Test Suite Release Notes

Version S-2021.06, June 2021

SYNOPSYS®

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Contents

1 Product Updates

This chapter discusses the new features and enhancements of the VC VIP PCIe Test Suite S-2021.06 release.

Attention

- From N-2018.03-3 release, the following legacy testbenches are removed and the equivalent functionality is part of the unified testbench (`tb_dut_pcie`):
  - `tb_dut_ep_gen2_pipe`
  - `tb_dut_ep_gen2_serdes`
  - `tb_dut_ep_gen3_pipe`
  - `tb_dut_ep_gen3_serdes`
  - `tb_dut_ep_gen4_pipe`
  - `tb_dut_ep_gen4_serdes`
  - `tb_dut_phy`
  - `tb_dut_rc_gen2_pipe`
  - `tb_dut_rc_gen2_serdes`
  - `tb_dut_rc_gen3_pipe`
  - `tb_dut_rc_gen3_serdes`
- Additionally, the following user guides have been removed from the installation doc directory:
  - *VC Verification IP PCIe Test Suite EP DUT User Guide*
  - *VC Verification IP PCIe Test Suite RC DUT User Guide*
  - *VC Verification IP PCIe Test Suite PHY DUT User Guide*

  For more information, contact Synopsys Support.
- Starting with O-2018.06-3 release, DUT integration and Application BFM sections have been moved to the following new guides:
  - *VC Verification IP PCIe Test Suite EP/RC DUT Integration Guide*
  - *VC Verification IP PCIe Test Suite PHY DUT Integration Guide*
  - *VC Verification IP PCIe Test Suite Reference External Application BFM*

1.1 New and Changed Features

1.1.1 Fixes/E-STARs

Table 1-1 lists the E-STARS fixed in this release.

Table 1-1 E-STARs

E-STAR	Description
3654084	**Problem**: The `pl_config_lanenum_accept_to_config_lanenum_wait_link_width_down_case1_error-phy` testcase fails when run with X12 Link width.
	Resolution: Enhanced the sequence to work with X12 link width.
3634651	**Problem**: The `pl_fifo_underflow_in_all_speeds_error-phy` testcase uses the hardcoded ppm value to generate the underflow scenario
	Resolution: Added the following new variables in the `pl_fifo_overflow/underflow_in_all_speeds_error-phy` tests to control the ppm values being used to generate overflow or underflow scenarios: • `seq_cfg.ppm_fifo_overflow` • `seq_cfg.ppm_fifo_underflow`

1.1.2 Fixes/B-STARs

Table 1-2 lists the B-STARs fixed in this release.

Table 1-2 Fixed B-STARs

B-STAR	Description
None	

1.2 Early Adopter Features in This Release

None

1.3 Important Notes

The following configurable parameters have been removed from the *hdl_interconnect_macros.sv* file present in the `tb_dut_pcie` example:

- `SVT_PCIE_TEST_SUITE_MON_PHY_INTERFACE_TYPE`
- `SVT_PCIE_TEST_SUITE_CONNECT_DOWNSTREAM_PORT_MONITOR`
- `SVT_PCIE_TEST_SUITE_CONNECT_UPSTREAM_PORT_MONITOR`

2
Known Issues and Limitations

This chapter discusses the known issues and limitations of PCIe Test Suite.

- If you are using Gen3 test suite, change the link speed from `GEN4` to `GEN3` in the installed example:

  File: *tb_dut_pcie/tests/svt_pcie_test_suite_default_plusargs.scr*

  Current Setting (line number 3): `+svt_pcie_link_speed=GEN4`

  Required Setting: `+svt_pcie_link_speed=GEN3`

  Without the above change the common tests will fail with the following error:

  ```
  UVM_FATAL  @ 201000.00 ps: uvm_test_top.env.ep_env.ep_agent.port0.pl0
  [report_message] : Detected attempt to enable 16G as a supported speed, but the
  attribute svt_pcie_pl_configuration::pcie_spec_ver is set to 3.000000. The
  attribute pcie_spec_ver must be set to >= 4.0 to enable 16G operation
  ```

- Following tests are not stable with Gen5:
  - `pl_config_lanenum_wait_to_detect_ts1_error-phy`
  - `pl_random_speed_change-phy`
  - `pl_polling_active_to_polling_config_ts2_error-phy`
  - `pl_config_lanenum_accept_to_config_complete_error-phy`
  - `dl_dlcmsm-rc`
  - `dl_enable_vc_supported_with_different_credit_range-rc`
  - `pl_recovery_idle_to_config_linkwidth_start_to_disabled_error-phy/ep/rc`
  - `pl_recovery_idle_to_config_linkwidth_start_error-ep/rc/phy`
  - `pl_pmg_stress_test-phy`
  - `pl_pmg_pci_pm_l1_clkreq_asserted-phy`
  - `pl_config_linkwidth_accept_to_config_lanenum_wait_error-ep/rc`
  - `pl_random_data_on_turned_off_lanes-phy`
  - `pl_lane_reenable_with_reset_assertion-phy`
  - `pl_lane_turn_off_and_reenable-phy`
  - `pl_pmg_aspm_rx_l0s_to_recovery_rcvrlock_error-phy`
  - `pl_config_idle_to_l0_error-phy`
  - `pl_config_lanenum_accept_to_config_lanenum_wait_link_width_down_case1_error-phy`

  - pl_config_complete_to_config_idle_rx_8_ts2_error-phy
  - pl_l1_pm_substates_aspm_l1_2_entry_to_l1_0-phy
  - pl_l1_pm_substates_aspm_l1_1_to_l1_0-phy
  - pl_random_width_change-phy
- Following tests are applicable with DWC PCIe 5.50a and later:
  - gen5_pl_verify_physical_layer_32g_cap_registers-ep
  - gen5_pl_verify_physical_layer_32g_cap_registers-rc
- Following tests are applicable with DWC PCIe GPHY model 5.50a and later:
  - pl_pmg_supported_pci_pm_states-phy
  - pl_pmg_pci_pm_l2_to_detect_quiet-phy
  - pl_pmg_pci_pm_l2_to_detect_exit_with_beacon-phy
- STAR 9001532834 (IIP): Following tests are expected to fail with DWC PCIe IIP:
  - *ts.gen5_pl_precoding_req_stored_for_32gts-rc.sv*
  - *ts.gen5_pl_loopback_w_precoding_requested_previously-rc.sv*
- STAR 9001516368: VIP changes `PowerDown` before full EIOS is received over PIPE interface.
- ATS tests are validated only in VIP-VIP environment on VCS simulator.
- Following tests are not supported in the PCIe test suite as PCIe VIP does not support 12 and 20 symbol size SKIP OS for 64-bit PIPE width at Gen3 and higher data rates:
  - gen3_pl_skp_length_variation
  - gen4_pl_skp_length_variation
  - gen5_pl_skp_length_variation
- MTI simulator is not supported. This will be fixed in future releases. For more details on using MTI simulator, contact Synopsys Support.
- STAR 9001447411: Constraints within some of the test suite sequences where the lane is selected to be masked does not consider when the link width is 12 causing the constraints failure.
- STAR 9001388115: Currently, all PTM test cases are valid only for VIP-IIP mode. The PTM test cases does not support VIP-VIP mode as PTM functionality in not implemented in the VIP.
- STAR 9001346195: VCS does not find the Verilog source file passed via `-f` option.

This limitation is applicable only for VCSMX flows and works fine with VCS.

- The test suite PHY DUT test cases are not qualified with SVC PHY VIP as PIPE 4.0 and above versions are not supported. Therefore, the test cases may fail when you try to validate in demo mode. However, internally all the test cases are qualified with PHY Generic IIP.
- This release does not support de-skew at VIP's receiver. Following are the known scenarios (problem is not limited to these) where VIP would fail to de-skew:
  - The VIP is configured with a multi-byte PIPE interface.
  - The skew coming into the VIP exceeds 6 symbols while using 8b10b encoding.

If you face any issue related to VIP de-skew, contact Synopsys support.

- For SSC MODE, the value of `min_ppm` cannot be less than 0. Therefore, do not pass negative value to plusarg `SVT_PCIE_MIN_PPM`.
- Following warnings are expected with VCS version N-2017.12-SP1:
  - `Warning-[IAVCVF-W] Incorrect argument to void cast`
  - `Warning-[TMR] Text macro redefined`
  - `Warning-[GCOIITB] Guard condition on Illegal/Ignore transition bin.`
  - `Warning-[PCWM-W] Port connection width mismatch`
  - `Warning-[RT-MTOCMUCS] More than one condition match in statement`
- STAR 9001306245: Some TL test cases that use both types of transaction item—that is, `svt_pcie_tlp` (sent on `tlp_seqr`) and `svt_pcie_driver_app_transaction` (sent on `driver_transaction_seqr`) may fail with the following error:

  ```
  SendPacket: TLP appl_id = 0xffffffff, requester_id = 0x0001, already mapped to appl_id = 0x00000001
  ```

  This is a random failure. And it occurs only when random `requester_id` generated by transaction of type `svt_pcie_tlp = 0x0001`.
- Following tests do not support the multi-link environment:

  EP DUT

  - *pl_detect_active_to_detect_quiet_error-ep*
  - *tl_ats_separate_itags_per_function-ep*

  RC DUT

  - *gen4_pl_sds_eds_skp_eds_eieos_skp_ts1-rc*
  - *demo_gen3_pl_all_supported_speed_change_test-rc*
  - *pl_config_linkwidth_accept_to_config_lanenum_wait_error-rc*

  10-bit tag feature is not supported on multi-link environment.
- Some of the new (Equalization, RxMargining, and so on) cases run on PIPE 4.0/4.2/4.3 and cannot run with VIP PHY (demo mode). But these cases are validated internally with PHY IIP.
- The following case may fail with different symbol-related errors/warnings from MAC VIP side. All known errors are already demoted. But, all possible scenarios cannot be predicted.
  - `pl_fifo_overflow_in_all_speeds_error`: This case creates a scenario of buffer overflow in PHY. Once buffer has overflowed, PHY can transmit any garbage data on the PIPE interface on the respective lane. MAC VIP can throw different errors/warnings if it is not handled previously.
  - The following cases are associated with Mid-Sim Reset behavior. Therefore, both VIPs (MAC side VIP and Serial side VIP) go out of sync and flag the error/warning.

    `pl_mid_sim_reset_both_side_without_delay-phy`
    `pl_mid_sim_reset_during_traffic-phy`
    `pl_mid_sim_reset_randomly_any_time-phy`

- PCLK Turn on / off utility for PHY specific substates will not work in PHY DUT TB area with VIP PHY model when PCLK is PHY output. Therefore, the following PL configuration will not work (as expected) with VIP PHY model.
  - `generate_pclk_in_phy_specific_power_state`
- The following test fails in PHY TB with VIP PHY model (with pipe width x16 and x32) due to VIP PHY limitation. The test is expected to pass when the PHY VIP model is replaced with actual PHY DUT.
  - `gen2_pl_8b_10b_err_with_skp_removed`
- Scoreboard does not compare the TLP when TLP prefix is enabled. In all PASID tests cases, the Scoreboard is disabled.
- STAR 9001228026 – Transaction ordering cases failing due to LN bit miscomparison in demo mode.

  Workaround: When any outbound TLP is initiated from EP VIP side (specially in demo mode or RC DUT mode), then user has to constrain "LN bit = 0" of transaction `svt_pcie_tlp/svt_pcie_driver_app_transaction` type. If this is not constrained, then EP VIP will further propagate this with 0 value and this might create an issue in end-to-end checking. Constraints in test suite test will be enhanced in the upcoming release.
- Following are the known limitations in Test Cases:

Table 2-1 shows the Test Cases with known limitations.

Table 2-1 Test Cases

Test Case	STAR/Case #	Description
tl_rn_no_frs_if_pending_np_requests-ep	3113098	The test may fail with following error: `UVM_ERROR: PF /0d transmitted FRS message after clearing VF Enable bit even though there were pending non-posted requests either with the PF or one of its associated VFs.`
pl_lanenum_wait_to_lanenum_accept_ts1_error-ep	3102672	The test may fail with following error: `UVM_ERROR: EP DUT LTSSM is not in CONFIGURATION_LANENUM_WAIT after transmitting few Error TS1s.` Workaround: You can avoid this error by increasing the value of the configuration variable, `pl_cfg.ltssm_configuration_linkwidth_start_rx_count` by 5 for this test.

Table 2-1 Test Cases

Test Case	STAR/Case #	Description
tl_split_cpld_last_cpl_addr_error tl_poisoned_tlp_detected_parity_error-ep tl_split_cpld_first_cpl_addr_error-ep tl_split_cpld_rcb_error-ep gen4_dl_scaled_fc_with_corrupted_updatefc_dllps-ep gen4_dl_scaled_fc_transmitting_unused_credit_for_hdr_and_data-ep gen4_dl_scaled_fc_zero_fc_scale_value_on_scaled_flow_control_activated_for_initfc_dllps-ep gen3_pl_recovery_equalization_phase2_to_recovery_speed_timeout_case1_error-ep tl_tx_vendor_defined_msg-ep	9001016246 (IIP)	For split completions with length and byte-count mismatch, IIP core does not treat completion as Malformed.
`pl_hot_reset_to_detect_phy_reset_error`	9001089628 (VIP)	PHY should de-assert PhyStatus after Reset# de-assertion when PCLK is stable. Test may fail with PCLK frequency checker error when you run with VIP PHY model.

`tl_tx_infinite_cr_in_initfc`	9001173739 (IIP)	The test may fail with following error:
		`For EP(DUT) : Explicit timeout of 1200000000.00 ps hit`
		`For RC(DUT) : Flow Control Protocol Error (FCPE) is not logged in AER Register at BDF 0000`

`gen3_pl_register_check_invalid_sync_header_l0_error-ep` `gen3_pl_register_check_invalid_sync_header_l0_error-rc`	8001015082 (IIP)	This test may fail with following error (only with SNPS IIP core): `Lane error is not flagged in corresponding bits of Lane Error Register`
`gen4_pl_sds_eds_skp_eds_eieos_skp_ts1`	9001303758 (Applicable to VIP-VIP only)	VIP does not enter Recovery after receiving EIEOS.
`gen3_pl_skip_in_tlp_payload_after_scrambling-ep`	8001067574 (IIP)	The test may fail with following error: `CheckAttachedTimers: ACK rcvd late.`

Table 2-1 Test Cases

Test Case	STAR/Case #	Description

pl_link_width_change_disable_lane-phy	9001303990	The test may fail with the following error when you run with lane reversal switch:
		`UVM_WARNING : [register_fail:ACTIVE_PL:LTSSM_POLLING_ACTIVE_RULES:phy_bad_link_number_polling_active] LTSSM: Incoming training sets have link number set to 0x000 instead of 0x1f7 (PAD) on lane 0 in state POLLING_ACTIVE`
		`UVM_FATAL : Explicit timeout of 1200000000.00 ps hit, indicating a probable testbench issue`

gen3_pl_recovery_idle_loopback_entry_to_loopback_active-ep gen3_pl_recovery_idle_to_loopback_entry_to_active_to_exit_detect-ep	9001285281	The test may fail with following error: [register_fail:ACTIVE_PL:128B130B_FRAMING:phy_data_block_after_eds] : Detected data block after EDS token on lane 0. As per the PCIe specification VIP will consider this as a framing error
pl_l0_to_recovery_linkwidth_change_error-ep pl_l0_to_recovery_linkwidth_change_error-rc pl_config_linkwidth_start_to_config_linkwidth_accept_upconfigure_link_width_up_error-ep	9001337818 (IIP)	Tests may fail with following error: [register_fail:ACTIVE_PL_PIPE:CONTROL_SIGNALS:phy_tx_start_block_asserted_tx_elec_idle_asserted] : DUT[MAC] has asserted tx_start_block signal on lane 1 while tx_elec_idle signal is asserted. The PIPE specification prohibits assertion of tx_start_block when tx_elec_idle is asserted. Ignoring tx_start_block assertion. Note: This error occurs for link width change tests when the DUT wrongly asserts `tx_start_block` and `tx_elec_idle` together even after link width has changed successfully.
pl_pmg_loop_test-phy		The test may fail with following error: `[register_fail:ACTIVE_PL_PIPE:SIDEBAND_SIGNALS:phy_rx_valid_reasserted_while_block_align_control_is_deasserted_error] : RxValid is re-asserted on lane 0 when BlockAlignControl is de-asserted`
pl_pmg_pci_pm_l2_to_detect_quiet-ep pl_pmg_supported_pci_pm_states-ep	9001364523	The test may fail with following error: `[register_fail:ACTIVE_PL_PIPE:SIDEBAND_SIGNALS:phy_phystatus_asserted_too_long] : PIPE signal PhyStatus on lane 10 asserted for more than 1 clk cycle in response to PowerDown assertion`
pl_pmg_aspm_l0s_variations-phy		The test may fail with following error: `UVM_ERROR : Received data block without preceding SDS on lane \d`

Table 2-1 Test Cases

Test Case	STAR/Case #	Description
pl_cfg_lw_start_directed_to_disabled_upstream_crosslink-phy pl_cfg_lw_start_downstream_to_upstream_crosslink-phy pl_cfg_lw_start_to_disabled_upstream_crosslink-phy pl_cfg_lw_start_upstream_to_downstream_crosslink-phy pl_recov_idle_directed_to_disabled_upstream_crosslink-phy pl_recov_idle_directed_to_hotreset_upstream_crosslink-phy	9001192426	The test may fail with following error: `UVM_ERROR Received number of TS\d is outside the range of \d to \d`
gen3_pl_config_loopback_entry_active_exit_detect-phy	9001349893	The test may fail with following error: `UVM_ERROR : Detected change of supported_speeds field from \dx\de to \dx\de. This field must not change in state RECOVERY_RCVRCFG`
gen3_pl_config_complete_to_config_idle_error-phy	9001359072	The test may fail with following error: `[register_fail:ACTIVE_PL:CONFIGURATION_COMPLETE:phy_configuration_complete_supported_speeds_change] : Detected change of supported_speeds field from \dx\de to \dx\de. This field must not change in state CONFIGURATION_COMPLETE`
pl_config_lanenum_accept_to_config_lanenum_wait_link_width_down_case2_error-phy	9001358911	EP VIP fails to make LTSSM transition from `Configuration.Lanenum.wait` to `Configuration.Lane.Accept.` EP VIP when receives two consecutive TS1s OSs with different lane number than which were received when EP first entered `Configuration.Lanenum.Wait` state and all lanes link number is not PAD, it is expected to move to Configuration.Lanenum.Accept. This transition does not happen because the condition for different lane number is not met correctly by the VIP.

Table 2-1 Test Cases

Test Case	STAR/Case #	Description
`tl_tlp_prefix_not_supported_or_prefix_count_error`	9001315601	The test may fail in VIP-VIP mode with the following errors: • `[appl_driver_missing_good_status] Received completion for TLP with unexpected status of 1 (Unsupported Req), expecting status Completion Timeout` • `[appl_driver_spurious_cpl] ProcessReceivedPacket: Spurious completion received with transaction ID \hx\d` • `[tl_receive_tlp_route_cpl_to_function_failed] .ReceiveTLP: TLP XID =\hx\d GetApplidFromRid could not map Rid =\hx\d to Appl ID check BDF field. Discarding Completion.` These errors occur because VIP treats TLPs with `end_to_end_prefix >4` as unsupported instead of Malformed.
tl_root_en_sec_bus_reset_to_trigger_hot_reset-rc gen4_pl_recovery_equalization_phase1_to_recovery_speed_detect_timeout_error-ep gen4_pl_recovery_equalization_phase3_to_recovery_speed_detect_timeout_error-ep	9001340498 (VIP)	This test fails with FIFO underflow `UVM_FATAL`.
pl_pmg_pci_pm_l2_to_detect_quiet-ep pl_pmg_supported_pci_pm_states-ep	9001364523 (VIP)	These tests fail in EP DUT demo mode (VIP-VIP) when PIPE signal `PhyStatus` on lane 10 is asserted for more than 1 clk cycle in response to `PowerDown` assertion.
tl_tx_vendor_defined_msg-rc tl_tx_vendor_defined_msg-ep	9001177435 (VIP)	These tests fail in EP/RC demo mode. Target Application BFM requires modification for Vendor Defined Message.
gen4_pl_recovery_equalization_phase3_to_recovery_speed_timeout_error-rc gen3_pl_recovery_equalization_phase3_to_recovery_speed_timeout_error-rc	9001367715 (TS)	This test fails with Synopsys IIP regression.
pl_l0_to_recovery_linkwidth_change_error-ep pl_config_linkwidth_start_to_config_linkwidth_accept_upconfigure_link_width_up_error-ep	9001337818 (IIP)	These cases will fail with SNPS IIP core, when TX ELEC IDLE and TX START BLOCK are asserted together.

Table 2-1 Test Cases

Test Case	STAR/Case #	Description
tl_cfg_valid_range_test-ep	9001202753 (VIP)	This will fail with SNPS IIP core, when rx_valid signal of the ReceivePCS block gets de-asserted in the middle of the TLP receiv . Error signature: • [register_fail:ACTIVE_PL:128B130B_FRAMING :phy_rx_invalid_data_in_data_stream] : Terminating data stream processing due to invalid data on lane 0, last_pclk_not_valid_count[receive_lanen um] 1, receive_lanenum 0 • [register_fail:ACTIVE_DL:FRAMING:dl_idle_ received_in_middle_of_packet] ReceivePhy: Received IDLE in middle of a packet on lane = 0.
gen3_pl_config_complete_to_detect_error-phy pl_srns_ppm_to_sris_ppm_to_no_ppm-phy	9001369878	These tests may fail with the following error when SRIS or SSC is enabled: [register_fail:ACTIVE_PL:SKP_OS:phy_max_rx_skp_interval] ReceivePhy: Exceeded maximum interval of \d blocks on lane \d before receiving a skp ordered set
pl_pmg_pci_pm_l2_to_detect_quiet pl_pmg_supported_pci_pm_states	9001364523	These tests may fail in EP DUT and PHY DUT area with the following UVM warning: phy_phystatus_asserted_too_long: PIPE signal PhyStatus on lane %d asserted for more than 1 clk cycle in response to PowerDown assertion
gen3_pl_loopback_speed_change_5g_to_8g-phy	9001382741	The test may fail with following error: [register_fail:ACTIVE_PL:LTSSM_OS_COUNT_RULES:phy_config_linkwidth_start_no_eieos_before_ts1] LTSSM: EIEOS was not received before TS1 on lane 0 in state CONFIGURATION_LINKWIDTH_START
pl_config_lanenum_accept_to_config_complete_error-rc	9001383392	Test fails in RC DUT (VIP-VIP) with the following error: ACTIVE_PL:CONFIGURATION_LANENUM_WAIT:phy_configuration_lanenum_wait_timeout] LTSSMStateMachine: Timeout in state CONFIGURATION_LANENUM_WAIT as conditions to transition to next state Configuration.Lanenum.Accept are not met. VIP will now transition back to Detect.Quiet.
gen3_pl_recovery_equalization_phase2_to_recovery_speed_timeout_case1_error-ep	9001383056	The test may fail with the following error: DUT not in Recovery.Equalization Phase \d Current state = RECOVERY_SPEED

Table 2-1 Test Cases

Test Case	STAR/Case #	Description
gen4_dl_scaled_fc_with_corrupted_updatefc_dllps-rc	9001217475	This test fails with earlier versions of IIP 5.20a: UVM_ERROR /vip/pcie_test_suite_svt/src/svt_pcie_ts_device_system_virtual_sequence_collection.sv(\d) @ \d.\d ps: uvm_test_top.env.test_env_seqr@@svt_pcie_ts_device_system_virtual_gen\d_dl_scaled_fc_with_corrupted_updatefc_dllps_sequence [check_aer_status_bits] Value found in Correctable Error Status Register at bdf =\hx\d different from expected. Observed =\hx\d Expected =\hx\d.
tl_locked_transactions-rc	6100033915 (IIP)	This test may fail only with SNPS IIP Core with the following errors: • register_fail:ACTIVE_TL:DW_BYTE_ENABLE:tl_malformed_tlp_first_dw_be_0 • register_fail:ACTIVE_TL:DW_BYTE_ENABLE:tl_malformed_tlp_last_dw_be_0
gen3_pl_eds_corruption_error-ep	9001150060 (IIP)	This test fails with timeout error due to EP IIP controller issue in the earlier versions of 5.30a.
gen4_dl_feature_dlcmsm gen4_dl_feature_exit_on_detection_remote_not_supporting_dl_feature gen4_dl_feature_exit_to_dl_Init gen4_dl_scaled_fc_dl_tlp_gated_on_credit_consumed gen4_dl_scaled_fc_with_corrupted_updatefc_dllps gen4_dl_scaled_fc_receiver_credit_overflow gen4_dl_scaled_fc_transmitting_unused_credit_for_hdr_and_data gen4_dl_scaled_fc_zero_fc_scale_value_on_scaled_flow_control_activated_for_initfc_dllps	9001406141	• DL and Scaled Flow Control cases must be renamed as these are applicable for all speeds. • Remove "gen4_" suffix from all cases.

Table 2-1 Test Cases

Test Case	STAR/Case #	Description
pl_srns_ppm_to_sris_ppm_to_no_ppm-phy	9001434817 (VIP)	The test may fail with following warning. When PhyStatus is delayed and RxStatus is asserted (due to SKP) at the same edge where Rate is changed (this happens in a corner situation). [register_fail:ACTIVE_PL_PIPE:SIDEBAND_SIGNALS:phy_skp_inserted_not_on_comma] : SKP inserted status received data other than K28.5 on lane 0
pl_polling_active_to_polling_config_compliance_bit_0_error-phy	9001461405 (TS)	The test case may fail with the following error: register_fail:ACTIVE_PL_LANE_OS:PROTOCOL:phy_rx_skp_symbol_outside_ordered_set_\d] : Detected SKP symbol outside of ordered set.
tl_application_error_reporting-rc	9001463281 (TS)	The test case may fail with multiple error types for different PF and VF. • [check_aer_status_bits] Value found in Uncorrectable Error Status Register at bdf =\hx\d different from expected. Observed =\hx\d Expected =\hx\d. • [check_error_messages] Value found in Root Error Status Register at bdf =\hx\d different from expected. Observed at bit [\d] =\hx\d & bit [\d] =\hx\d Expected Bit Location [\d] =\h & [\d] =\h'b\d
pl_config_lanenum_accept_to_detect_error	9001463273 (TS)	The test case may fail with the following error: register_fail:ACTIVE_PL:CONFIGURATION_LTSSM:phy_config_linkwidth_accept_unexpected_eios] LTSSM: Received unexpected EIOS on lane \d in state CONFIGURATION_LINKWIDTH_ACCEPT
gen3_pl_invalid_sync_header_config_idle_error-rc	9001463966 (TS)	The test may fail in VIP-VIP setup with following error: register_fail:ACTIVE_PL:CONFIGURATION_COMPLETE:phy_configuration_complete_bad_lane_skew] LTSSM: Timeout in state CONFIGURATION_COMPLETE as VIP is unable to deskew lanes. VIP will now transition back to Detect.Quiet.
pl_config_linkwidth_start_to_config_linkwidth_accept_error-rc	9001487544	The test case may fail with the following error: [svt_pcie_ts_device_system_virtual_cfg_linkwidth_start_to_cfg_linkwidth_accept_sequence] State Transition does not happen from CONFIGURATION_LINKWIDTH_START to CONFIGURATION_LINKWIDTH_ACCEPT

Table 2-1 Test Cases

Test Case	STAR/Case #	Description
pl_pmg_aspm_l0s_to_l0_tlp-rc	9001490054	The test case may fail with the following error: [phy_l\ds_bad_rx_fts_count] : Lane \d FTS transmit count of \d did not equal expected count of \d before exiting L\dS.
pl_config_lanenum_accept_to_detect_error-phy	9001490932	The test case may fail with the following error: 'LTSSM: Incoming TS\d sets have lane number set to \dx\d instead of \d or \d (lane reversal) on lane \d in state CONFIGURATION_LINKWIDTH_ACCEPT.' & 'Test got hanged and timedout'
pl_polling_config_to_detect_error-ep	9001502775	The test may fail with timeout failure setup on Link Speed Gen3.
pl_pmg_aspm_rx_l0s_to_recovery_rcvrlock_error-phy	9001503967	The test case may fail with the Synopsys behavioral generic PHY model error: RxValid assertion aligns with the first RxStartBlock assertion, Reference: PIPE v4.3: 7.26 128b/130b Encoding and Block Synchronization - Active VIP detected that RxValid assertion by PHY is not aligned with first RxStartBlock assertion on lane <>
pl_srns_ppm_to_sris_ppm_to_no_ppm-ep	9001505804	The test case may fail with the following error: Exceeded maximum interval of \d symbol times on lane \d before receiving a skp ordered set” in EP DUT set up
pl_pmg_aspm_l0s_variations-phy	9001522936 (VIP)	The test case may fail with the following error due to VIP issue: [register_fail:ACTIVE_PL:SKP_OS:phy_too_many_skp_sets] : Received \d skip ordered sets on lane \d expected to receive at most \d skip ordered sets after \d symbols times The test case may fail with the Synopsys behavioral generic PHY model error: [register_fail:ACTIVE_PL_PIPE:SIDEBAND_SIGNALS:pipe_rxstartblock_rxvalid_check] Description: RxValid assertion aligns with the first RxStartBlock assertion Reference: PIPE v\d.\d: \d.\d \db/\db Encoding and Block Synchronization - Active VIP detected that RxValid assertion by PHY is not aligned with first RxStartBlock assertion on lane \d.

Table 2-1 Test Cases

Test Case	STAR/Case #	Description
pl_recovery_rcvrlock_to_config_linkwidth_start_to_l0_error-phy pl_recovery_rcvrlock_to_config_linkwidth_start_timeout_error-phy	9001539834	The test cases may fail with the following errors: • [register_fail:ACTIVE_PL:CONFIGURATION_LTSSM:phy_upconfigure_past_initial_negotiated_linkwidth] : Received more than \d consecutive TS\d on \d lanes but the initial configured linkwidth is \d. An upconfigure should not exceed the initial configured linkwidth. • [register_fail:ACTIVE_PL_LANE_OS:CONFIGURATION_LTSSM:ordered_set_checker_bad_ts1_link_pad_lane_non_pad_0] : Received TS1 with PAD link number and non-PAD lane number = 0x000
pl_polling_active_to_polling_config_compliance_bit_0_timeout_error-phy/rc pl_link_width_accept_to_detect_error-ep pl_configuration_linkwidth_start_to_loopback_error-ep/phy pl_polling_config_to_config_tx_16_rx_8_ts2_error-phy pl_polling_active_to_detect_quiet_error-phy/ep pl_polling_config_to_detect_error-phy pl_cfg_lw_start_upstream_to_downstream_crosslink-phy/ep pl_cfg_lw_start_downstream_to_upstream_crosslink-phy	9001550009	These tests may fail with the following error when both sides advertise different speeds: [register_fail:ACTIVE_PL:FRAMING:phy_data_rate_identifier_changed] LTSSMStateMachine: Data rate identifier field on lane \d of \dx\de does not match previously recorded value of \dx\de
pl_polling_compliance_to_polling_active_eios_receive	9001552227	The test may fail with the following error: [register_fail:ACTIVE_PL:TS_OS:phy_eq_bypass_without_32g_support] LTSSM: Attached device has advertised support for equalization bypass to highest data rate without also advertising support for 32G. EQ bypass can only be done when 32G support is advertised.
gen5_pl_recovery_idle_to_loopback_entry_to_active_to_exit_detect-phy gen5_pl_recovery_idle_to_cfg_lwstart_to_loopback_entry_active_exit-phy	9001558917	These tests may fail with DWC PCIe GPHY error: register_fail:ACTIVE_PL:LTSSM_LOOPBACK_RULES:phy_no_loopback_pattern_detected] : VIP did not detect transmitted loopback pattern on lane \d before exiting loopback.

Table 2-1 Test Cases

Test Case	STAR/Case #	Description
gen5_pl_invalid_sync_header_on_partial_lane_config_idle_error-ep/rc	9001550353	The test may fail with the following error: `Timeout in state CONFIGURATION_COMPLETE as VIP is unable to deskew lanes. VIP will now transition back to Detect.Quiet.`
gen3_pl_recovery_equalization_phase3_to_recovery_speed_timeout_error-rc	9001576387	The test may fail with the following error: `DUT state transition not happend in Recovery.Equalization Phase 3 after tol time`
pl_config_lanenum_accept_to_config_lanenum_wait_link_width_down_case1_error-ep pl_config_lanenum_accept_to_config_lanenum_wait_link_width_down_case2_error-ep	9001577471	These tests may fail due to timeout or with the following error: `uvm_test_top.env.test_env_seqr@@svt_pcie_ts_device_system_virtual_lanenum_accpet_to_lanenum_wait_link_width_down_case1_sequence [svt_pcie_ts_device_system_virtual_lanenum_accpet_to_lanenum_wait_link_width_down_case1_sequence] DUT or VIP is not in state CONFIGURATION_LANENUM_ACCEPT`
gen5_pl_precoding_req_stored_for_32gts-rc, gen5_pl_polling_compliance_via_enter_compl_precoding_req_previously-rc, gen5_pl_loopback_w_precoding_requested_previously-rc, gen5_pl_no_eq_sanity_test-rc, gen5_pl_recovery_equalization_phase3_to_recovery_speed_detect_timeout_error-ep	9001575208	These tests may fail with the following error if VIP's PL configuration `transmitter_precode_request_32g` is set to 1 and both VIP and DUT are configured to advertise No-Equalization required: `[register_fail:ACTIVE_PL_LANE_OS:TS_OS:ordered_set_checker_bad_ordered_set_2] : Received bad ordered set: 0x01e`
gen5_pl_eq_via_loopback_mac_master-phy	3093026	This test may fail with the following error: `Timeout in state CONFIGURATION_COMPLETE as VIP is unable to deskew lanes. VIP will now transition back to Detect.Quiet`
pl_lanenum_wait_to_lanenum_accept_ts2_error-phy	3132101	This test may fail with the following error: `Timeout in state CONFIGURATION_LANENUM_ACCEPT as conditions to transition to next state Configuration.Complete or Configuration.Lanenum.Wait are not met. VIP will now transition back to Detect.Quiet`

Table 2-1 Test Cases

Test Case	STAR/Case #	Description
Framing Error test cases (VIP-VIP mode)	3143108	These test cases may fail in VIP-VIP mode with the following error: `[register_fail:ACTIVE_PL:FRAMING:phy_data_stream_without_eds] : Detected ordered set on lane \d in data stream without preceding EDS token. As per the PCIe specification VIP will consider this as a framing error.`
`gen5_pl_no_eq_sanity_test-phy`	3142686	This test may fail with the following error: `Received data block without preceding SDS on lane 0" with Generic Phy(v5.60a) due to large skew issue`
`gen5_pl_eds_followed_by_ts2_error-ep`, `gen5_pl_skp_followed_by_sds-rc`	3143108	These test cases may fail with the following error: `Detected ordered set on lane \d in data stream without preceding EDS token. As per the PCIe specification VIP will consider this as a framing error`
`pl_lanenum_wait_to_lanenum_accept_ts2_error-phy`	3202125	This test may fail with the following error: `UVM_ERROR ../../../../pcie_svc/PCIE/Verilog/PhyLayer/pciesvc_ltssm.sv(7604) @ 54668427.60 ps: uvm_test_top.env.rc_env.rc_agent.port0.pl0 [register_fail:ACTIVE_PL:CONFIGURATION_LANENUM_ACCEPT:phy_configuration_lanenum_accept_timeout] LTSSMStateMachine: Timeout in state CONFIGURATION_LANENUM_ACCEPT as conditions to transition to next state Configuration.Complete or Configuration.Lanenum.Wait are not met. VIP will now transition back to Detect.Quiet.`
`gen3_pl_recovery_rcvrcfg_to_recovery_speed_128ts2tx_error-ep`	3221998	This test may fail with the following error: `UVM_ERROR ../../../../pcie_svc/PCIE/Verilog/PhyLayer/pciesvc_ltssm.sv(18355) @ 47526454.00 ps: uvm_test_top.env.rc_env.rc_agent.port0.pl0 [register_fail:ACTIVE_PL:EQUALIZATION:phy_rx_upstream_dllp_before_downstream_tx_dllp] : Received DLLP before downstream has transmitted a packet. Upstream ports must not transmit any DLLP until it received a DLLP from the downstream port.`

Table 2-1 Test Cases

Test Case	STAR/Case #	Description

gen2_dl_invalid_tlp_with_disparity_error-phy	3242646	This test may fail with the following error:
		`UVM_ERROR : ProcessReceivedDLLP: Received ACK when NAK expected. Exp EI seq num = 20, acknak_seq_num = 21,`
		`UVM_FATAL : Explicit timeout of 120000000.00 ps hit, indicating a probable testbench issue`

dl_dllp_rate_of_reception-ep	3315676	This test may fail with the following error: `UVM_WARNING: [register_fail:ACTIVE_DL:ACK_NAK:dl_acknak_latency_late_timeout] CheckAttachedTimers: ACK rcvd late, expected attached acknak_latency value = 352. (attached_max_acknak_latency(237), attached_internal_delay(19), internal_delay(19), internal_phy_delay(27), attached_internal_phy_delay(50))`

Gen5 Speed test cases with LIBRARY19 keys	3359384	For running the Gen5 Speed test cases with LIBRARY19 keys, it is required to update the symlink manually in the *DW_HOME* path (*pcie_test_suite_svt/R-2020.09/examples/sverilog*) before the extraction of any example.
		symlink before modification:
		`“tb_dut_pcie -> ./tb_dut_pcie_gen4_file”`
		symlink after modification:
		`“tb_dut_pcie -> ./tb_dut_pcie_gen5_file”`

gen5_pl_no_eq_sanity_test-phy	3348436	This test may fail with the following error signature: `"ACTIVE_PL_LANE_OS:TS_OS:ordered_set_checker_bad_ordered_set_8] : Received bad ordered set: 0x01e"`
gen4_pl_different_os_on_different_lane_error-phy	3572084	This test may fail with the following error signature: `UVM_WARNING: [register_fail:ACTIVE_DL:FLOW_CTRL_INIT:dl_initfc_credit_timeout] TransmitPhy: All 3 VC0 InitFC credit types were not received within 34000 ns`

Table 2-1 Test Cases

Test Case	STAR/Case #	Description
gen5_pl_config_complete_to_detect_no_modified_ts_when_expected-phy	3617930	This test may fail with the following error signature: [register_fail:ACTIVE_PL:CONFIGURATION_LANENUM_ACCEPT:phy_configuration_lanenum_accept_timeout] LTSSMStateMachine: Timeout in state CONFIGURATION_LANENUM_ACCEPT as conditions to transition to next state Configuration.Complete or Configuration.Lanenum.Wait are not met. VIP will now transition back to Detect.Quiet.
pl_pmg_pci_pm_l2_to_detect_quiet-ep, pl_pmg_pci_pm_d3_corrupt_pm_request_ack_of_enter23_error-ep	3622191	These test cases may fail with the following error signature: [register_fail:ACTIVE_PL_PIPE:MBI_TRANSACTION:mbi_write_ack_occurance_check] Description: Write Ack MBI command should be issued in response to Write Committed command only.

- Following are the limitations for the Synopsys provided scoreboard:
  - For a multi-function DUT there is a temporary limitation with some Atomic Op tests which expect all functions to support AtomicOp Completer capability if even one supports it.
  - For a multi-function DUT, the non-virtual functions are expected to have continuous function numbers.
  - There are certain fields, which cannot be populated because of AXI limitation. Hence, by default, comparisons of all these fields are disabled in a scoreboard. To enable comparisons for all these fields, users can enable the corresponding configuration variable (part of svt_pcie_test_suite_configuration class) from the customer Base Test.

    Inbound TLP: IDO (attr_id_order), TD, EP, BYTE_ENABLE (FBE and FBE), byte_count, Reserved Bit

    Outbound TLP: TAG, EP, BYTE_ENABLE (FBE and FBE)
  - Configuration Transaction and its completion are disable, because these transaction are absorbed by DUT and not transmitted to the APP_BFM side.
  - Scoreboard: The scoreboard cannot determine the original request type from completions outbound from the DUT; and hence, comparisons of all completions with length 1 and tc == 0 are by default disabled.
- MTI warnings:

```
======================
# ** Warning:
../examples/sverilog/pcie_test_suite_svt/tb_dut_ep_gen3_pipe/env/snps_pcie_ep_
env.sv(163): (vopt-2250) Function "get_agent" has no return value assignment.
# ** Warning:
../examples/sverilog/pcie_test_suite_svt/tb_dut_ep_gen3_pipe/env/snps_pcie_rc_
env.sv(160): (vopt-2250) Function "get_agent" has no return value assignment.
```

```
# ** Warning:
../examples/sverilog/pcie_test_suite_svt/tb_dut_ep_gen3_pipe/env/snps_pcie_ep_
dut_env.sv(721): (vopt-2250) Function "get_sequencer" has no return value
assignment.
# ** Warning: ../pcie_test_suite_svt/J-2014.12-
SP3/sverilog/src/mti/svt_pcie_ts_device_system_virtual_config_space_sequence_c
ollection.svp(117): (vopt-2239) Treating stand-alone use of presumed external
function as an implicit VOID cast.
==========================
```

- VCS PC and PIP flow is not supported in this release. Contact Synopsys Support if you want to use this flow.
- Removed the test case `gen4_pl_skp_length_corruption_error` from EP, RC and PHY TB DUT area as the SKP length variation does not qualify with the framing error category.
- IEEE Encryption and Incdir flow is supported in VCS and MTI simulators only. For more details, see the sections 2.6 and 2.7 in the *VC VIP Library Installation Guide*.

3 Supported Platforms, Models, and Software

This chapter discusses the supported platforms, models, and software of PCIe Test Suite.

This chapter consists of the following topics:

- Supported Methodology, OS and Simulator Versions
- Software Tools Support
- Dependent Products

3.1 Supported Methodology, OS and Simulator Versions

3.1.1 Supported Methodologies

Table 3-1 lists the methodologies supported with simulators.

Table 3-1 Supported Methodologies With Simulators

Methodology	VCS	Xcelium	Questasim
UVM	Supported	Not supported	Not Supported
OVM	Not Supported	Not supported	Not Supported
VMM	Not Supported	Not supported	Not Supported
VLOG	Not Supported	Not supported	Not Supported

Attention

With Questasim 2020.3, you may get the warning as illustrated:

```
** Warning: ** while parsing macro expansion:
'SVC_SOURCE_MAP_SUITE_MODEL_MODULE_SV' starting at
/dw_home/bin/src/sverilog/mti/pciesvc_target_appl.sv(10)

** while parsing file included at
/dw_home/bin/src/sverilog/mti/pciesvc_target_appl.sv(10)

** at /dw_home/bin/src/sverilog/mti/pciesvc_shared_status_pkg.sv(20):
(vlog-2275) Existing package 'pciesvc_shared_status_pkg' will be
overwritten.
```

Table 3-2 lists the methodology versions supported.

Table 3-2 Supported Methodology Versions

Methodology	Supported Version	Unsupported Version
UVM	1.1d, 1.2, 1800.2-2017-1.0	1.1a
OVM	N/A	N/A
VMM	N/A	N/A

3.1.2 Supported OS and Simulator Versions

The simulator matrix table is available at the following location:

VC VIP Library page

https://spdocs.synopsys.com/dow_retrieve/latest/vg/snps_vip_lib/PDFs/simulator_matrix.pdf

For more information on the simulator matrix and library level updates, see *VC VIP Library Release Notes*.

3.2 Software Tools Support

Following are the supported tool sets that work with this version of the VIP:

- Verdi Protocol Analyzer version P-2019.06

3.3 Dependent Products

This release of the PCIe VIP Test Suite is dependent on the following VIP products:

- SVT library version S-2021.06
- PCIe SVT VIP version S-2021.06
- AMBA SVT VIP version S-2021.06

4 Documentation

This chapter discusses the documentation of PCIe VIP.

This chapter consists of the following topics:

4.1 Protocols

The PCIe Test Suite supports the following protocol-related features:

- DUT type: PCIe End Point / Root Complex / PHY
- Signaling Interface: PIPE, SERIAL
- Signaling width: x4, x16, x32
- Speed: Gen1 / Gen2 / Gen3 / Gen4
- Enumeration sequence for basic and extended capabilities
- Transaction layer, DataLink layer, Physical layer normal and error test scenarios
- Modes of operation configurable by define
- VIP as EP | RC | PHY
- RTL as EP | RC | PHY
- Verification Plans

The PCIe test suite is delivered with test plans mapping to the specification attribute with tests. The test plans are compatible with the Synopsys Verification Planner tool available as part of VCS distribution, and can be used to back annotate test pass / fail metrics from the text file generated with regression run results.

The verification plans are available in the test suite install tree doc / Verification Plans directory.

4.2 Methodology

PCIe Test Suite currently supports the following methodology functions:

- UVM as per version 1.2

4.3 Product Guides and Online Help

VC VIP for PCIe Test Suite document set includes the following:

- *AMBA System Env UVM User Guide*, which is installed at:

  $DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/amba_svt_uvm_user_guide.pdf

- *AXI UVM User Guide*, which is installed at:

  $DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/axi_svt_uvm_user_guide.pdf

- *VC VIP for PCIe UVM User Guide*, which is installed at:

  $DESIGNWARE_HOME/vip/svt/pcie_svt/latest/doc/pcie_svt_uvm_user_guide.pdf

- *VC VIP PCIe Verification IP Test Suite UVM User Guide*, which is installed at

  $DESIGNWARE_HOME/vip/svt/pcie_test_suite_svt/latest/doc/pcie_test_suite_svt_uvm_user_guide.pdf

  HTML reference documentation consists of the following:

- *AMBA System Env UVM class reference HTML*, which is accessed by:

  $DESIGNWARE_HOME/vip/svt/amba_svt/latest/doc/amba_svt_uvm_class_reference/html/index.html

- *PCIe SVT Test Suite UVM Class Reference*, which is accessed by:

  $DESIGNWARE_HOME/vip/svt/pcie_test_suite_svt/latest/doc/pcie_test_suite_svt_uvm_class_reference/html/index.html

- *PCIe SVT UVM Class Reference*, which is accessed by:

  $DESIGNWARE_HOME/vip/svt/pcie_svt/latest/doc/pcie_svt_uvm_class_reference/html/index.html

4.4 Quickstart Examples

The VIP provides various levels of quickstart tutorials for each methodology. For a complete list of the available tutorials and their associated examples, see the following documents:

- The *Example Testbench Setup* and *Running Testcases* section in Chapter 3, “Installation and Setup” in the *VC Verification IP PCIe Test Suite UVM User Guide*.

5 Customer Support

This chapter discusses the customer support provided for PCIe VIP.

This chapter consists of the following topics:

5.1 SolvNetPlus

Synopsys SolvNetPlus resides at the following location:

https://solvnetplus.synopsys.com

It provides you with the following:

- Download Center for all VIPs
- Support
- Training
- Reference Methodology Retrieval System
- Hundreds of articles on VIP usage
- Register problem reports

5.2 Registering a Problem

To register a problem, perform any of the following tasks:

- Go to https://solvnetplus.synopsys.com and open a case.

  Enter the information according to your environment and your issue.
- Send an e-mail message to support_center@synopsys.com
  - Include the Product name, Sub Product name, and Product version for which you want to register the problem.

5.3 Reporting a Problem

To report a problem, keep the following information ready before you contact technical support:

- Provide a description of the following:
  - The issue under investigation
  - Your verification environment
- Create a Value Change Dump (VCD) file.
- Generate a log file for the simulation.
- Provide other files such as translation logs.

For information on reporting a problem for each methodology, see the following sections in the respective user guide:

- Sending Debug Information to Synopsys section in Chapter A, “Reporting Problems” in the *VC Verification IP PCIe Test Suite UVM User Guide*.

5.4 Telephone Support

Telephone your local support center:

- North America:

  Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday
- All other countries:

  https://www.synopsys.com/support/global-support-centers.html

6 Previous Release Notes

This chapter lists the product update for previous releases:

6.1 R-2021.03-2 Release - April 2021

6.1.1 New and Changed Features

6.1.1.1 Fixes/E-STARs

Table 6-1 lists the E-STARS fixed in this release.

Table 6-1 E-STARs

E-STAR	Description
None	

6.1.1.2 Fixes/B-STARs

Table 6-2 lists the B-STARs fixed in this release.

Table 6-2 Fixed B-STARs

B-STAR	Description
None	

6.2 R-2021.03-1 Release - March 2021

6.2.1 New and Changed Features

6.2.1.1 Fixes/E-STARs

Table 6-3 lists the E-STARS fixed in this release.

Table 6-3 E-STARs

E-STAR	Description
None	

6.2.1.2 Fixes/B-STARs

Table 6-4 lists the B-STARs fixed in this release.

Table 6-4 Fixed B-STARs

B-STAR	Description
None	

6.3 R-2021.03 Release - March 2021

6.3.1 New and Changed Features

6.3.1.1 Fixes/E-STARs

Table 6-5 lists the E-STARS fixed in this release.

Table 6-5 E-STARs

E-STAR	Description
None	

6.3.1.2 Fixes/B-STARs

Table 6-6 lists the B-STARs fixed in this release.

Table 6-6 Fixed B-STARs

B-STAR	Description
None	

6.4 R-2020.12-3 Release - February 2021

6.4.1 New and Changed Features

6.4.1.1 Fixes/E-STARs

Table 6-7 lists the E-STARS fixed in this release.

Table 6-7 E-STARs

E-STAR	Description
None	

6.4.1.2 Fixes/B-STARs

Table 6-8 lists the B-STARs fixed in this release.

Table 6-8 Fixed B-STARs

B-STAR	Description
None	

6.5 R-2020.12-2 Release - January 2021

6.5.1 New and Changed Features

6.5.1.1 Fixes/E-STARs

Table 6-9 lists the E-STARS fixed in this release.

Table 6-9 E-STARs

E-STAR	Description
3476776	**Problem**: Add a test case for PCI_PM for L1_2 sub-state.
	Resolution: Added an EP DUT test, `pl_l1_pm_substates_pci_pm_l1_0_to_l1_2_entry-ep` for PCI_PM L1_2 sub-state.

6.5.1.2 Fixes/B-STARs

Table 6-10 lists the B-STARs fixed in this release.

Table 6-10Fixed B-STARs

B-STAR	Description
None	

6.6 R-2020.12-1 Release - December 2020

6.6.1 New and Changed Features

6.6.1.1 Fixes/E-STARs

Table 6-11 lists the E-STARS fixed in this release.

Table 6-11E-STARs

E-STAR	Description
3423955	**Problem**: Add the PCI-PM L1.1 and L1.2 sub-state test cases in the PCIe Test suite.
	Resolution: Following test cases are added for EP DUT setup for L1 SS PCI_PM feature: • `L1_0 to L1_1 L -pl_l1_pm_substates_pci_pm_l1_0_to_l1_1-ep` • `L1_1 to L1_0 -pl_l1_pm_substates_pci_pm_l1_1_to_l1_0-ep` These test cases are applicable for all the link speeds.

6.6.1.2 Fixes/B-STARs

Table 6-12 lists the B-STARs fixed in this release.

Table 6-12Fixed B-STARs

B-STAR	Description
None	

6.7 R-2020.12 Release - December 2020

6.7.1 New and Changed Features

6.7.1.1 Fixes/E-STARs

Table 6-13 lists the E-STARS fixed in this release.

Table 6-13E-STARs

E-STAR	Description
None	

6.7.1.2 Fixes/B-STARs

Table 6-14 lists the B-STARs fixed in this release.

Table 6-14Fixed B-STARs

B-STAR	Description
None	

6.8 R-2020.09-3 Release - November 2020

6.8.1 New and Changed Features

6.8.1.1 Fixes/E-STARs

Table 6-15 lists the E-STARS fixed in this release.

Table 6-15E-STARs

E-STAR	Description
3391619	**Problem**: Rx Margining new test requirement where Rx margining is done first and after that speed changes between GenX and Gen4 for at least 3 pairs (GenX<->Gen4) with Gen4 margining.
	Resolution: Added a new testcase, `"gen4_pl_rx_margin_local_phy_data_rate_change_after_margining-phy"`.

6.8.1.2 Fixes/B-STARs

Table 6-16 lists the B-STARs fixed in this release.

Table 6-16Fixed B-STARs

B-STAR	Description
9001303990	**Problem**: The testcase, `"pl_link_width_change_disable_lane-phy"` fails when run with lane reversal enabled with the following error signature: `register_fail:ACTIVE_PL:LTSSM_POLLING_ACTIVE_RULES:phy_bad_link_number_polling_active] LTSSM: Incoming training sets have link number set to \dx\d instead of \dx\df\d (PAD) on lane \d in state POLLING_ACTIVE.`
	Resolution: Test is not applicable if lane reversal is enabled. Added a warning in the sequence for the same.

6.9 R-2020.09-2 Release - October 2020

6.9.1 New and Changed Features

6.9.1.1 Fixes/E-STARs

Table 6-17 lists the E-STARS fixed in this release.

Table 6-17E-STARs

E-STAR	Description
3326586	**Problem**: The test, `gen4_pl_recovery_equalization_phase0_to_recovery_speed_timeout_case1_error-ep` fails with the following error signature: `"ACTIVE_PL:CONFIGURATION_LTSSM:phy_expected_speed_not_equal_to_negotiated_speed] : Expected data rate 16Gb/s does not match current rate of 8Gb/" when user sequence added during the time of activate link sequence.`
	Resolution: Fixed the sequence and the test.
3405919	**Problem**: A number of test cases reconfigure the `requester_id` for RC DUT with forced value of `device_number` as 0 even when the user initialized device number of RC DUT is non-zero.
	Resolution: Enhanced the TS test cases to work correctly with RC DUT when the user initialized device number of RC DUT is non-zero.

6.9.1.2 Fixes/B-STARs

Table 6-18 lists the B-STARs fixed in this release.

Table 6-18Fixed B-STARs

B-STAR	Description
None	

6.10 R-2020.09-1 Release - September 2020

6.10.1 New and Changed Features

This release contains the following feature set:

- Added a new field, `ptm_cap_registers_reset_on_flr` under the `svt_pcie_test_suite_sequence_configuration` class as illustrated in Table 6-19.

Table 6-19Newly Added Field Description

Class Name	New Field Name	Description
svt_pcie_test_suite_sequence_configuration	ptm_cap_registers_reset_on_flr	Specifies if the EP DUT resets the PTM registers on FLR of function that contains the PTM Extended Capability. If DUT resets the PTM registers, then this attribute should be set to 1. This attribute is used by the tl_ptm_pf_flr_between_dialogs_case1-ep test case. Default value is 0. **Note**: As per spec version 5 revision 1.0, it is strongly recommended that all the registers in PTM Capability Structure should not reset to their initialization values upon FLR.

6.10.1.1 Fixes/E-STARs

Table 6-20 lists the E-STARS fixed in this release.

Table 6-20E-STARs

E-STAR	Description
3293229	**Problem**: Upgrade the Test Suite to throw an error or warning when the SVT_PCIE_ENABLE_BACKWARDS_COMPATIBILITY macro is used.
	Resolution: Enhanced the PCIe Test Suite Base Environment and added a message.
9001518139	**Problem**: Reset during PTM dialogs.
	Resolution: • Added one new PTM test case, tl_ptm_pf_flr_between_dialogs_case1-ep that initiates FLR at different times during PTM dialogs. The targeted function for FLR is the one which has the PTM Extended Capability in its configuration space. • As per spec version 5 revision 1.0, it is strongly recommended that all the registers in PTM Capability Structure should not reset to their initialization values upon FLR (since PTM Capability and PTM dialogs are device wide). By default, the TS PTM test cases expects spec compliant behavior. In case, you reset the PTM registers on FLR of function that contains the PTM Extended Capability, then you must set the svt_pcie_test_suite_sequence_configuration attribute, "ptm_cap_registers_reset_on_flr" to 1.
3358283	**Problem**: Enumerate selective (non-continuous) functions for ARI device.
	Resolution: Enhanced the Test Suite enumeration sequence for enumerating the selective functions only for an ARI device by reading 'Next Function Number' field from ARI Capability Register. • You must set svt_pcie_test_suite_configuration attribute, "enable_selective_function_enumeration" to enable this feature. • You must set the macro value for SVT_PCIE_TEST_SUITE_MAX_FUNC_SUPPORTED_BY_DUT as (highest_numbered_function_in_device + 1). For example, consider if the ARI device have functions 0, 1, 5, 7, and 9, then you must set the SVT_PCIE_TEST_SUITE_MAX_FUNC_SUPPORTED_BY_DUT macro value to 10. This is required to keep the compatibility with the existing Test Suite architecture which was originally for sequential function numbers. • Once this feature is enabled, all Test Suite test cases will run with only the selective functions in the ARI device.

Table 6-20E-STARs

E-STAR	Description
3358285	**Problem**: Test to validate non-zero reserved PH field value is ignored by the receiver.
	Resolution: Enhanced the existing Test Suite test cases, `tl_tlp_rsvd_bit_ignore-ep/rc` to send non-zero value in reserved fields for Memory, Atomic-Op, IO, and Cfg TLPs. The test cases checks that the receiver ignores the reserved fields and does not treat the TLP as malformed.
3347126	**Problem**: The non-function specific error Multi-Function device should generate at most one error reporting message of same severity. However, when the DUT is sending multiple message of same severity then the VIP is not throwing error for that scenario.
	Resolution: Currently, the `main_aer` sequence checking is focused on the reporting of Function Severity Error Message and does not take into consideration the error count. The sequence has been enhanced to consider the error count. The Multi-Function device should generate at most one error reporting message of a given severity.
3374094	**Problem**: Test missing for verification of `"ARI Extended Capability Structure"` from PCI Express Architecture Configuration Space.
	Resolution: Added a new test case, `cfg_sig_compliance_test_td_1_43` in the product for the testing of this feature.
3357846	**Problem**: Deliver GPHY supporting PIPE 5.1.1 in release.
	Resolution: Added GPHY supporting Pipe 5.1.1 LPC mode.

6.10.1.2 Fixes/B-STARs

Table 6-21 lists the B-STARs fixed in this release.

Table 6-21Fixed B-STARs

B-STAR	Description
3350316	**Problem**: Unable to iterate all the possible L1 scenarios in the following test cases: • ts.pl_pmg_loop_test-phy.sv • ts.pl_pmg_stress_test-phy.sv
	Resolution: Fixed the `enable_l1` API usage in the sequences to iterate all the possible combinations.
3366429	**Problem**: Test `pl_recovery_rcvrlock_to_detect_error-phy` in Pipe 5.1 LPC mode fails with the following error signature: `[svt_pcie_ts_device_system_virtual_recovery_rcvrlock_to_detect_sequence] DUT LTSSM transision to DETECT_QUIET did not happen or last state was not RECOVERY_RCVRLOCK`
	Resolution: Fixed the sequence.
3361084	**Problem**: The following test cases in Gen4 Pipe 5.1 LPC mode fails with the error signature as illustrated: • `ts.gen2_pl_recovery_speed_to_detect_1_from_l0_error-phy.sv` • `ts.gen2_pl_recovery_speed_to_detect_1_from_l1_error-phy.sv` • `ts.gen2_pl_recovery_speed_to_detect_1_from_pm_l1_error-phy.sv` UVM_WARNING: `[register_fail:ACTIVE_PL:INFERRING_ELECTRICAL_IDLE:phy_recovery_rcvrcfg_inferred_electrical_idle] LTSSM: Inferred electrical idle on lane 0 in absence of TS2 from DUT in state RECOVERY_RCVRCFG at Gen1/Gen2 speed.`
	Resolution: Fixed the test case.
3352289	**Problem**: Test `gen3_pl_recovery_rcvrlock_to_recovery_rcvrcfg_timeout_corruption_error-phy` in Pipe 5.1 LPC mode fails with the following error signature: `[register_fail:ACTIVE_PL_LANE_OS:TS_OS:ordered_set_checker_bad_ordered_set_0] : Received bad ordered set: 0x0bc 0x0bd 0x094 0x06d 0x0dd 0x0c6 0x058 0x084 0x01a 0x020 0x03f 0x08b 0x04e 0x005 0x089 0x0ff`
	Resolution: Fixed the sequence.
3349514	**Problem**: Test `pl_pmg_pci_pm_l1_clkreq_asserted-phy` fails with the following error signature: `[PH_TIMEOUT] Explicit timeout of 1200000000.00 ps hit`
	Resolution: Fixed the sequence.

6.11 R-2020.09 Release - September 2020

6.11.1 New and Changed Features

6.11.1.1 Fixes/E-STARs

Table 6-22 lists the E-STARS fixed in this release.

Table 6-22E-STARs

E-STAR	Description
None	

6.11.1.2 Fixes/B-STARs

Table 6-23 lists the B-STARs fixed in this release.

Table 6-23Fixed B-STARs

B-STAR	Description
None	

6.12 Q-2020.06-3 Release - August 2020

6.12.1 New and Changed Features

6.12.1.1 Fixes/E-STARs

Table 6-24 lists the E-STARS fixed in this release.

Table 6-24E-STARs

E-STAR	Description
3318214	**Problem**: The Phy DUT `gen4_pl_recovery_equalization_coefficient_setting_error-phy` fails with the following error signature: `"VIP not Received Correct FS and LF values in Phase1"`
	Resolution: Fixed the sequence.
3324455	**Problem**: The `gen3_pl_recovery_equalization_phase3_illegal_preset_setting_error-ep` test fails with the following error signature: `"ACTIVE_PL:LTSSM_OS_RULES:phy_recovery_rcvrlock_timeout] LTSSMStateMachine: Timeout in state RECOVERY_RCVRLOCK as conditions to transition to next state Recovery.Cfg or Recovery.Equalization are not met."`
	Resolution: Fixed the sequence.

6.12.1.2 Fixes/B-STARs

Table 6-25 lists the B-STARs fixed in this release.

Table 6-25Fixed B-STARs

B-STAR	Description
3287166	**Problem**: MPIPE VIP is performing GetLocalPresetCoefficient request on all 16 lanes. However, only 2 lanes are active.
	Resolution: Fixed the issue where the sequence is holding an outdated linkwidth value due to which the GetLocalPresetCoefficient request is getting initiated even on the inactive lanes.
3323519	**Problem**: Low Power EP DUT `pl_l1_pm_substates_aspm_l1_0_to_l1_2_entry-ep` test case fails with the following error signature: `"ACTIVE_DRIVER_APP:COMPLETION:appl_driver_command_timeout] CheckForCommandTimeout: Request number 28 [CfgRd0] with tag 1 (0x001), requester id 0x0000, addr 0x0000000001000110 and length 1 (0x001) has timed out"`
	Resolution: Fixed the sequence.
3326085	**Problem**: The `pl_random_speed_change-phy` test when ran out of box fails with the following error signature: `“Supported speeds = 2 , should be greater than 2 (GEN1) for successful execution of the test.”`
	Resolution: Updated the default combination selected for the `pl_random_speed_change-phy` test so that Gen1 speed does not get selected when the test is run at installation area without passing any switches.
3314428	**Problem**: Spurious error from PIPE as illustrated: `UVM_ERROR [register_fail:ACTIVE_PL_PIPE:DATAVALID:pipe_rxdatavalid_deassertion_after_every_n_blocks_check] Description: RxDataValid must be de-asserted for one clock exactly every N blocks when the PIPE interface is operating at 8 GT/s or 16 GT/s or 32 GT/s`
	Resolution: Demoted the expected error in FIFO overflow and underflow test scenarios.
3343873	**Problem**: Following tests fails with “`expected speed set to unsupported rate issue when with redo equalization enabled at 8G or 16G`”: • `pl_pmg_aspm_l0s_variations-phy` • `pl_pmg_stress_test-phy` • `pl_random_speed_change-phy` • `tl_tx_max_payload_size-phy`
	Resolution: Fixed the sequence.

Table 6-25Fixed B-STARs (Continued)

B-STAR	Description
3341789	**Problem**: Linkwidth dependent tests should have checks for link width.
	Resolution: Added warning in the following test cases when run with X1 link width: • `pl_polling_active_to_polling_compliance_partial_lanes_timeout_error-ep/rc/phy` test case • `gen3_pl_idle_followed_by_no_idle_next_lane_error-ep/rc` test case - The test had a debug message when run with X1 link width; updated the error level to warning so that there is no false pass when run with X1 link width.
3288154	**Problem**: The `gen3_pl_recovery_equalization_phase3_illegal_coefficient_setting_error` test fails with the following error signature: `"DUT sent either different pre-Cursor coefficient on lane = 0 or rejection bit low"`
	Resolution: Enhanced the sequence.

6.13 Q-2020.06-2 Release - July 2020

6.13.1 New and Changed Features

6.13.1.1 Fixes/E-STARs

Table 6-26 lists the E-STARS fixed in this release.

Table 6-26E-STARs

E-STAR	Description
3289883	**Problem**: The `pl_config_lanenum_accept_to_config_lanenum_wait_link_width_down_case2_error-ep` test case fails with the following error signature: `"CTRL-SKP OS detected outside of data stream must be followed by a SDS"`
	Resolution: Enhanced the sequence.
3261953	**Problem**: Errors do not get injected as expected in the following test cases because of which VIP does not wait in `CONFIGURATION_LANENUM_ACCEPT` • `ts.pl_config_lanenum_accept_to_config_lanenum_wait_link_width_down_case1_error-phy.sv` • `ts.pl_config_lanenum_accept_to_config_lanenum_wait_link_width_down_case2_error-phy.sv` • `ts.pl_config_lanenum_accept_to_config_lanenum_wait_link_width_down_case1_error-ep.sv` • `ts.pl_config_lanenum_accept_to_config_lanenum_wait_link_width_down_case2_error-ep.sv`
	Resolution: Fixed the corner case where the error injection did not happen as expected.

Table 6-26E-STARs (Continued)

E-STAR	Description
3294539	**Problem**: The `gen3_pl_pmg_aspm_rx_l0s_to_recovery_rcvrlock_error-phy` test case fails with the following error signature: `"UVM_WARNING: SKIP ordered set parity 0 does not match expected value 1" when PHY is correcting 1 bit error"`
	Resolution: Removed the `force_scramble` option from the callback so that the receiver can visualize more than 1 bit error.

6.13.1.2 Fixes/B-STARs

Table 6-27 lists the B-STARs fixed in this release.

Table 6-27Fixed B-STARs

B-STAR	Description
3294819	**Problem**: The `pl_config_linkwidth_accept_to_config_lanenum_wait_error-rc` test case fails with the error signature, `phy_wrong_link_width` in multi-link RC DUT setup.
	Resolution: Fixed the sequence.
3289711	**Problem**: The `ltssm_state_timer` expiry in the sequence results in the abrupt time-out for following test cases: • `ts.pl_polling_active_to_polling_compliance_partial_lanes_timeout_error-phy.sv` • `ts.gen1_pl_polling_to_cfg_lwstart_to_loopback_entry_exit_error-phy.sv` • `ts.gen3_pl_recovery_speed_to_detect_1_from_l1_error-phy.sv` • `ts.gen4_pl_recovery_equalization_phase1_to_rcvrlock_case2_error-phy.sv`
	Resolution: Corrected the usage of `wait_for_ltssm_state` API in the sequences to handle the time-out scenarios.
3285138	**Problem**: The `pl_recovery_idle_to_detect_error-phy` test case fails with the following error signature: `"Received STP token of length 1788"`
	Resolution: Demoted the expected error for corner case scenario when garbage data resembles the STP token in the `pl_recovery_idle_to_detect_error-phy/ep/rc` test cases.
3281561	**Problem**: The `gen4_pl_rx_margin_local_phy_step_margin_to_timing_incrementing_offset-phy` test case fails with the following error signature: `"timer timer_phy_dut_max_time_to_update_margin_status expired. No change in Margin Status 0 register on lane 00000000001d."`
	Resolution: The pipe specification is not clear when only write committed is to be used for stopping margining and resetting margining parameters to default values. Enhanced the sequence based on the customer's interpretation. The control is provided to the user using the newly added Test Suite sequence configuration attribute, `reset_margin_offset_before_stop` and the backward compatibility has also been maintained.
3287737	**Problem**: The `gen4_pl_recovery_equalization_phase3_to_recovery_speed_timeout_case1_error-phy` test case fails with the following error signature: `"UVM_WARNING: Requested equalization preset 2 on lane 0 returned precursor/cursor/postcuror coefficients 0x00/0x13/0x06. Expected 0x00/0x13/0x05 in Phase3"`
	Resolution: Updated the sequence to send the user TS based on the requested preset 2. Initially, the sequence issued the preset request randomly for preset value 2. However, the user TS sent by VIP in recovery Eq PH3 sets the symbol 7, 8, and 9 based on preset 0. This resulted in the issue as specified when `preset_to_coefficient_mapping` differs for preset 0 and 2.

6.14 Q-2020.06-1 Release - June 2020

6.14.1 New and Changed Features

6.14.1.1 Fixes/E-STARs

Table 6-28 lists the E-STARS fixed in this release.

Table 6-28E-STARs

E-STAR	Description
9001535251	**Problem**: Test description is same for the test cases related to recovery speed.
	Resolution: Corrected the description of the following test cases: • `gen2_pl_recovery_speed_to_detect_0_from_pm_l1_error-ep` • `gen2_pl_recovery_speed_to_detect_1_from_pm_l1_error-ep`
2885222	**Problem**: Test case execution fails with the following UVM_ERROR when the PIPE 5.1 interface is used: `[register_fail:ACTIVE_PL_PIPE:EQUALIZATION:phy_get_local_preset_coefficients_timeout] GetLocalPresetStateMachine: Timeout waiting for WriteCommitted(Tx Status0, Tx Status1, Tx Status2 registers) to get 'LocalTxPresetCoefficients' values on lane 0 - return to 'Idle'`
	Resolution: For test case execution with PIPE 5.1 interface, • Configured the value of `get_local_preset_coefficients_timeout_ns` configuration variable to 240ns in the following test cases: – `gen3_pl_recovery_equalization_dynamic_eq_remote_eq_direction_change-phy` – `gen5_pl_recovery_equalization_dynamic_eq_remote_eq_direction_change-phy` • Updated the test description for the above mentioned test cases and added the following debug tip in the sequence: `[SNPS_PCIE_TS_DEBUG_TIP] For GetLocalPresetCoefficients request max response time by PHY is defined 128ns as per PIPE SPEC Version 5.1 but at GEN1 speed & PIPE 5.1 interface, the MBI command response may take at least 10 PCLK cycles to complete which is greater than 128ns. In this testcase we are sending this request at GEN1 and have configured get_local_preset_coefficients_timeout_ns = 240 using Test Suite Seq Cfg variable get_local_preset_coeff_timeout_ns. Please configure this attribute as per PHY response behavior`
9001546438	**Problem**: Currently in TS PTM test cases, sequences sends PTM_RSP immediately after PTM_REQ is received from EP DUT. There is no delay between t3 and t2.
	Resolution: Added the following `svt_pcie_test_suite_sequence_configuration` attributes to control the delay for the PTM Master to respond to PTM_REQ: • `min_propagation_delay_for_ptm_master_ns` • `max_propagation_delay_for_ptm_master_ns`

6.14.1.2 Fixes/B-STARs

Table 6-29 lists the B-STARs fixed in this release.

Table 6-29Fixed B-STARs

B-STAR	Description
3269750	**Problem**: Issue with the `pl_recovery_rcvrlock_to_config_linkwidth_start_timeout_error-ep` test behavior.
	Resolution: Enhanced the sequence check to check for the current and last DUT LTSSM state.
3203604	**Problem**: Test description is missing in PHY tests.
	Resolution: Added the descriptions for the following test cases: • `ts.pl_pmg_aspm_l1_variations-phy.sv` • `ts.pl_pmg_pci_pm_l1_variations-phy.sv`
3248726	**Problem**: Following UVM_ERROR is observed while waiting for the EP VIP to transmit LF and FS values: `[svt_pcie_ts_device_system_virtual_gen4_pl_recovery_equalization_coefficient_rule_error_sequence]VIP not received FS and LF values in Phase1 on ane 0`
	Resolution: Fixed the following sequence to capture the LF and FS values properly: • `svt_pcie_ts_device_system_virtual_gen4_pl_recovery_equalization_coefficient_rule_error_sequence`
3248758	**Problem**: Following tests are not able to capture LS/FS values properly: • `ts.gen3_pl_recovery_equalization_full_swing_mode_error-rc.sv` • `ts.gen3_pl_recovery_equalization_phase2_legal_coefficient_setting_error-rc.sv` • `ts.gen3_pl_recovery_equalization_coefficient_rule_2_error-rc.sv`
	Resolution: Fixed the following sequences to capture the LF and FS values properly: • `svt_pcie_ts_device_system_virtual_gen3_pl_recovery_equalization_full_swing_mode_error_sequence` • `svt_pcie_ts_device_system_virtual_gen3_pl_recovery_equalization_phase3_legal_coefficient_setting_error_sequence` • `svt_pcie_ts_device_system_virtual_gen3_pl_recovery_equalization_coefficient_rule_error_sequence`

6.15 Q-2020.06 Release - June 2020

6.15.1 New and Changed Features

6.15.1.1 Fixes/E-STARs

Table 6-30 lists the E-STARS fixed in this release.

Table 6-30E-STARs

E-STAR	Description
None	

6.15.1.2 Fixes/B-STARs

Table 6-31 lists the B-STARs fixed in this release.

Table 6-31Fixed B-STARs

B-STAR	Description
None	

6.16 Q-2020.03-3 Release - May 2020

6.16.1 New and Changed Features

6.16.1.1 Fixes/E-STARs

Table 6-32 lists the E-STARS fixed in this release.

Table 6-32E-STARs

E-STAR	Description
3175855	**Problem**: Test `gen3_pl_recovery_rcvrcfg_to_detect_ts2_non_matching_rate_error-ep.sv` fails with `UVM_FATAL` as `test_max_timeout` value is set incorrectly.
	Resolution: Fixed the test case.
3150842	**Problem**: Test `pl_srns_ppm_to_sris_ppm_to_no_ppm-ep` fails with the error signature "`phy_max_rx_skp_interval`".
	Resolution: Fixed the sequence.

6.16.1.2 Fixes/B-STARs

Table 6-33 lists the B-STARs fixed in this release.

Table 6-33Fixed B-STARs

B-STAR	Description
3222607	**Problem:** The `gen5_pl_verify_32g_lane_eq_ctrl_reg_rc` test reads the incorrect value for comparing it with the value read from the PL32 G register for Upstream port 32G and downstream port 32G.
	Resolution: Fixed the sequence to read the correct value from the Equalization Control Register for comparing it with the received preset values from the TS1 OS.

6.17 Q-2020.03-2 Release Notes - April 2020

6.17.1 New and Changed Features

- Starting Q-2020.03-2 release, the PCIe test suite does not support the defining of `SVT_PCIE_ENABLE_BACKWARDS_COMPATIBILITY` macro for accessing the VIP status information through variables directly in `svt_pcie_pl_status` instance.

  It is recommended to access the PCIe VIP status information using the `lane_status` instances.

6.17.1.1 Fixes/E-STARs

Table 6-34 lists the E-STARS fixed in this release.

Table 6-34 E-STARs

E-STAR	Description
3106230	**Problem:** Add a new warning or error message for the test cases which are not applicable when run with PIPE 5.1 and above.
	Resolution: Added a warning in the following test cases stating that the test cases are not applicable when run with PIPE 5.1 and above: • `gen4_pl_rx_margin_local_phy_margining_on_disabled_lanes-phy` • `pl_lane_turn_off_and_reenable-phy` • `pl_random_data_on_turned_off_lanes-phy` • `pl_lane_reenable_with_reset_assertion-phy`
3166421	**Problem:** The `gen3_pl_skip_err_check_rxstatus_error-phy` test case fails with VIP check "`phy_rx_stp_token_bad_fcrc_gen3`".
	Resolution: Fixed the test.

Table 6-34 E-STARs (Continued)

E-STAR	Description
3154516	**Problem:** The `gen3_pl_recovery_equalization_phase2_to_recovery_speed_timeout_case1_error` test case fails with the following error signature: `"DUT not in Recovery.Equalization Phase 2, Current state = RECOVERY_EQUALIZATION_3,"`
	Resolution: The following test cases are enhanced such that the test cases are applicable for Serial mode only. • `gen3_pl_recovery_equalization_phase2_to_recovery_speed_timeout_case1_error-ep` • `gen3_pl_recovery_equalization_phase3_to_recovery_speed_timeout_error-rc` • `gen4_pl_recovery_equalization_phase3_to_recovery_speed_timeout_error-rc` • `gen5_pl_recovery_equalization_phase3_to_recovery_speed_timeout_error-rc`
3142893	**Problem:** The `tl_split_cpld_last_cpl_addr_error` test case fails due to SB Miscompare of Requester-ID as the test cases used • TL Interface to generate the traffic, and • random Requester-ID
	Resolution: Primitive sequence enhanced to constraint the Requester-ID for outbound transactions so that the Requester gets inclined with the Driver app interface configured value.
3149447	**Problem**: Issue with `pl_passive_compliance_test_elec_idle_timeout_error-ep` test case.
	Resolution: Fixed the passive compliance sequence to handle the `x1` scenarios.
3161408	**Problem:** Sequence configuration for number of RX modified compliance patterns.
	Resolution: Added `wait_for_num_rx_modified_compliance_pattern` Test Suite sequence configuration.
3119175	**Problem:** Few Test Suite common cases (that followed the conventional credit update mechanism) were not compatible with Scale Flow Control mode.
	Resolution: Enhanced the Test Suite to add the following configuration variables: • `enable_dl_feature_scaled_flow_control` • `configure_fc_scale_factor` The users can configure these variables so that the base test cases act accordingly and configure the scale value. Few failing cases has also been enhanced to work with scale flow control mode. The users can see some of the cases failing with optional Feature warning as the cases are not applicable with `X4` and `X16` mode.

6.17.1.2 Fixes/B-STARs

Table 6-35 lists the B-STARs fixed in this release.

Table 6-35 Fixed B-STARs

B-STAR	Description
3133678	**Problem:** The `tl_split_cpld_first_cpl_addr_error` test fails with DUT that does not support RCB rule check as when the VIP sends the corrupted completion with length more than the received request length, then along with Malformed TLP status, the DUT also gets logged for completion time-out.
	Resolution: Test enhanced to send good completion at the end followed by corrupted completion so that the DUT does not get logged with completion time-out error.

6.18 Q-2020.03 Release Notes - March 2020

6.18.1 New and Changed Features

None

6.19 Q-2019.12-3 Release Notes - February 2020

6.19.1 New and Changed Features

6.19.1.1 Fixes/E-STARs

Table 6-36 lists the E-STARS fixed in this release.

Table 6-36 E-STARs

E-STAR	Description
3103465	**Problem**: PCIe performance improvement – Compile time improvement for PCIe Test Suite.
	Resolution: Improved the compile time by using the new parallel partition compile feature. For more information, see "*Appendix D: Implementing Partition Compile in Testbench*" in the *VC Verification IP PCIe Test Suite UVM User Guide.*

6.19.1.2 Fixes/B-STARs

Table 6-37 lists the B-STARs fixed in this release.

Table 6-37 Fixed B-STARs

B-STAR	Description
9001578380	**Problem**: The `ts.gen5_pl_invalid_sync_header_error-ep.sv` test case fails with NOA error.
	Resolution: Fixed the test case.

6.20 Q-2019.12-2 Release Notes - January 2020

6.20.1 New and Changed Features

6.20.1.1 Fixes/E-STARs

Table 6-38 lists the E-STARS fixed in this release.

Table 6-38 E-STARs

E-STAR	Description
N/A	

6.20.1.2 Fixes/B-STARs

Table 6-39 lists the B-STARs fixed in this release.

Table 6-39 Fixed B-STARs

B-STAR	Description
2888538	**Problem:** Constraint solver error while using `svt_pcie_ts_driver_app_random_tlp_transaction_primitive_sequence`.
	Resolution: Added soft constraint in base sequence(`svt_pcie_ts_driver_app_transaction_enumeration_constraints_sequence`) so that CPLs are not generated upon randomization of `transaction_type` field.

6.21 Q-2019.12-1 Release Notes - December 2019

6.21.1 New and Changed Features

- Backward incompatible change to file *tb_dut_pcie/env/hdl_interconnect_macros.sv*.
  - The macros in the *hdl_interconnect_macros.sv* file are shown for illustration only. If you are using these as-is and not using the Synopsys top module (*top.sv*), then you must ensure to add the following lines in your top module before including *hdl_interconnect_macros.sv*.

```
parameter string PARENT_COMPONENT_FOR_PRIMARY_PCIE_UNIFIED_BASE_TEST =
"uvm_test_top";
```

6.21.1.1 Fixes/E-STARs

Table 6-40 lists the E-STARS fixed in this release.

Table 6-40 E-STARs

E-STAR	Description
9001573874	**Problem:** Test `gen4_pl_stp_token_framing_error-ep/rc/phy` fails with `Replay timer timed out` VIP warning in multilink environment.
	Resolution: Demoted the VIP warning as this warning is expected.

Table 6-40 E-STARs (Continued)

E-STAR	Description
9001577238	**Problem:** Test `gen1_pl_recovery_rcvrlock_to_recovery_rcvrcfg_error-phy` fails with the following error: `DUT LTSSM is not in RECOVERY_RCVRLOCK after transmitting few Error TS1s`
	Resolution: Enhanced the sequence to consider the large latency.

6.21.1.2 Fixes/B-STARs

Table 6-41 lists the B-STARs fixed in this release.

Table 6-41 Fixed B-STARs

B-STAR	Description
9001570445	**Problem:** Test `pl_fifo_underflow_in_all_speeds_error` fails with the following error: `[register_fail:ACTIVE_PL:128B130B_FRAMING:phy_data_stream_wrong_os_after_eds] : Detected ordered set other than SKP, SDS, EIOS or EIEOS on lane 0 in data stream after EDS token. As per the PCIe specification VIP will consider this as a framing error.`
	Resolution: Fixed the test.
9001576544	**Problem:** Test `dl_dlcmsm-rc` fails with fast simulation scaling factor of 64 (1ms -> 16us) with following error: `[svt_pcie_ts_device_system_virtual_dl_dlcmsm_sequence] VIP did not receive Initfc1 DLLP packets from DUT, VIP DLCMSM states are in DL_INIT , whare as expected is DL_Init. Also Nnumber of Received Initfc1 packet from DUT is 9 where as Expected is > 10`
	Resolution: Fixed the test.

6.22 Q-2019.12 Release Notes - December 2019

6.22.1 New and Changed Features

6.22.1.1 Fixes/E-STARs

Table 6-42 lists the E-STARS fixed in this release.

Table 6-42 E-STARs

E-STAR	Description
None	

6.22.1.2 Fixes/B-STARs

Table 6-43 lists the B-STARs fixed in this release.

Table 6-43 Fixed B-STARs

B-STAR	Description
None	