Siva Satyendra Sahoo,

Research Scholar (Ph.D.)

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About Me

Objective

- Postdoctoral Researcher with a demonstrated history of working in the field of Electronic System Design. My doctoral research has been focused on optimizing the distribution of reliability methods across multiple layers of the system stack with appropriate scheduling of tasks on heterogeneous embedded systems. My prior research experience includes machine learning, reconfigurable systems and embedded systems design.

Research Interests

- Embedded Systems, Fault-tolerant System Design, Reconfigurable Computing, Machine Learning, Digital VLSI, Electronic Design Automation (EDA).

Research Experience

Sep 2019 – present
- **Postdoctoral Researcher.** Chair for Processor Design, Computer Science Department, Technische Universität Dresden, Germany. *Supervised by* Dr. Akash Kumar.

Feb 2019 – Sep 2019
- **Guest Researcher.** Chair for Processor Design, Computer Science Department, Technische Universität Dresden, Germany. *Supervised by* Dr. Akash Kumar.

Jan 2015 – Feb 2019
- **Research Scholar (Ph.D.).** Signal Processing and VLSI Lab, Department of Electrical and Computer Engineering, National University of Singapore, Singapore. *Supervised by* Dr. Bharadwaj Veeravalli and Dr. Akash Kumar.

Feb 2017 – Dec 2017
- **Guest Researcher.** Chair for Processor Design, Computer Science Department, Technische Universität Dresden, Germany. *Supervised by* Dr. Akash Kumar.

Industry Experience

Aug 2012 – Dec 2014
- **Digital Design Engineer.** Intel India, Bangalore, India. Physical design of dense VLSI System-on-Chip.

Jul 2008 – Mar 2010
- **Assistant Systems Engineer.** Tata Consultancy Services, Hyderabad, India. Business Intelligence and Web design.

Education

2015 – 2019
- **Ph.D., National University of Singapore, Singapore** in Electrical and Computer Engineering.
  Thesis title: *Cross-layer Reliability-based Embedded System Design.*
  Advisors: Bharadwaj Veeravalli, *Ph.D.* and Akash Kumar, *Ph.D*

Education (continued)

2010 – 2012 **M.Tech., Indian Institute of Science, Bangalore (India)** in Electronic Design and Technology.
Project title: *Hardware Accelerator for Support Vector Machines.*
Advisor: Kuruvilla Varghese, *Principal Research Scientist*

2004 – 2008 **B.Tech., College of Engineering and Technology, Bhubaneswar (India)** in Instrumentation and Electronics Engineering.
Project title: *Short Message Service (SMS)-based Home Automation.*
Advisor: Kanhu Charan Bhuyan, *Ph.D*

Teaching Experience

Graduate Assistant **Department of Electrical and Computer Engineering, NUS**
Modules:
EE 4218 - *Embedded Hardware Systems Design*
Instructors: Akash Kumar, Ph.D., Yajun Ha, Ph.D. and Rajesh Panicker, Ph.D
EE 4214 - *Real-time Embedded Systems*
Instructor: Rajesh Panicker, Ph.D
EE 5903 - *Real-time Systems*
Instructor: Bharadwaj Veeravalli, Ph.D
EE 2020 - *Digital Fundamentals*
Instructor: Xu Yong Ping, Ph.D

Teaching Assistant **School of Continuing and Lifelong Education, NUS**
Modules:
TE 3801 - *Robust Design of Electronic Circuits*
Instructors: Bharadwaj Veeravalli, Ph.D. and Rajesh Panicker, Ph.D
TE 2101 - *Programming Methodology*
Instructor: Bharadwaj Veeravalli, Ph.D

Research Publications

Journal Articles

1. Ullah, S., Schmidl, H., **S. S. Sahoo**, Rehman, S., & Kumar, A. (2020). Area-optimized accurate and approximate softcore signed multiplier architectures. *IEEE Transactions on Computers*, 1–1.

2. **S.S. Sahoo**, Nguyen, T., Veeravalli, B., & Kumar, A. (2019). Multi-objective design space exploration for system partitioning of FPGA-based Dynamic Partially Reconfigurable Systems. *Integration*, *67*, 95–107. doi:https://doi.org/10.1016/j.vlsi.2018.10.006

Conference Proceedings

1. **Sahoo, Siva Satyendra**, Veeravalli, B., & Kumar, A. (2020, July). CL(R)Early: An Early-stage DSE Methodology for Cross-Layer Reliability-aware Heterogeneous Embedded Systems. In *Proceedings of the 57th annual design automation conference 2020*. DAC '20. (Accepted for publishing). San Francisco, CA, USA: Association for Computing Machinery.

2. Rai, S., Raitza, M., **Siva Satyendra Sahoo**, & Kumar, A. (2020, March). DISCERN: Distilling Standard Cells for Emerging Reconfigurable Nanotechnologies. In *2020 Design, Automation Test in Europe Conference Exhibition (DATE)*. (Accepted for publishing).

3. **Sahoo, Siva Satyendra**, Veeravalli, B., & Kumar, A. (2019). A hybrid agent-based design methodology for dynamic cross-layer reliability in heterogeneous embedded systems. In *Proceedings of the 56th annual design automation conference 2019*. DAC '19. Las Vegas, NV, USA: Association for Computing Machinery. doi:10.1145/3316781.3317746

4. **Siva Satyendra Sahoo**, Nguyen, T. D. A., Veeravalli, B., & Kumar, A. (2018a). Lifetime-aware design methodology for dynamic partially reconfigurable systems. In *23rd Asia and South Pacific Design Automation Conference, ASP-DAC 2018, Jeju, Korea (South), January 22-25, 2018* (pp. 393–398). doi:10.1109/ASPDAC.2018.8297355

5. **Siva Satyendra Sahoo**, Nguyen, T. D. A., Veeravalli, B., & Kumar, A. (2018b). QoS-aware Cross-layer Reliability-integrated FPGA-based Dynamic Partially Reconfigurable System Partitioning. In *International Conference on Field-Programmable Technology, ICFPT 2018, Naha, Okinawa, Japan, December 10-14, 2018*.

6. **Siva Satyendra Sahoo**, Veeravalli, B., & Kumar, A. (2018). CLRFrame: An analysis framework for designing cross-layer reliability in embedded systems. In *31st International Conference on VLSI Design and 17th International Conference on Embedded Systems, VLSID 2018, Pune, India, January 6-10, 2018* (pp. 307–312). doi:10.1109/VLSID.2018.81

7. **Siva Satyendra Sahoo**, Kumar, A., & Veeravalli, B. (2016). Design and evaluation of reliability-oriented task re-mapping in MPSoCs using time-series analysis of intermittent faults. In *2016 Design, Automation & Test in Europe Conference & Exhibition, DATE 2016, Dresden, Germany, March 14-18, 2016* (pp. 798–803). http://ieeexplore.ieee.org/document/7459415/

8. **Siva Satyendra Sahoo**, Veeravalli, B., & Kumar, A. (2016). Cross-layer fault-tolerant design of real-time systems. In *2016 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, DFT 2016, Storrs, CT, USA, September 19-20, 2016* (pp. 63–68). doi:10.1109/DFT.2016.7684071

Skills

Language Proficiency	English, Odia, Hindi
Programming Languages	C, C++, Python, MATLAB
Design Languages	VHDL, Verilog, SystemC
EDA Tools	Xilinx Vivado, Gem5, ARM Development Studio

Awards and Achievements

Scholarships

2015 – 2018 **NUS Graduate Scholarship**, National University of Singapore, Singapore.

2010 – 2012 **MHRD (GATE) Scholarship**, Ministry of Human Resource Development, Government of India, India.

2004 – 2008 **CET Merit Scholarship**, College of Engineering and Technology, Bhubaneswar, India.

References

Akash Kumar
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