# Curriculum vitae: Siva Satyendra Sahoo

## Professional Objective

**About Me**

I am a post-doctoral researcher with a demonstrated history of working in the field of Electronic System Design. I am currently working as a Senior Staff Engineer, AI Computing with Samsung Advanced Institute of Technology (SAIT). Prior to joining SAIT, I was working with the Chair of Processor Design, TU Dresden, on the design of low-cost accelerators for AI/ML applications, primarily targeted for embedded and cyber-physical systems. The design involves leveraging approximation and quantization techniques and innovations in system-, architecture- and IP-level for FPGA-based systems. My current responsibilities in the research group also involve supervision of research interns and master's students.My doctoral research was focused on optimizing the distribution of reliability methods across multiple layers of the system stack with appropriate scheduling of tasks on heterogeneous embedded systems. My prior research experience includes machine learning, reconfigurable systems and embedded system design.

**Research Interests**

Electronic Design Automation, Embedded System Design, RTL Design, Digital Synthesis, Electronic System-level Design, Reconfigurable Computing, Machine Learning, Digital VLSI, Approximate Computing.

## Industry Experience

since 08/2021 | **Senior Staff Engineer**, AI Computing, SAIT,
Samsung Semiconductor India Research, Bangalore, India
Individual contributor for modelling and design space exploration (DSE) of AI computing architectures. Collaborator in the analysis and optimization of mapping AI workloads on modern inference engines.

08/2012–12/2014 | **Digital Design Engineer**, Intel India, Bangalore, India
Worked in the domain of *Physical Design* of dense VLSI System-on-chip. Was primarily responsible for design quality assessment of full-chip as well as design blocks.

07/2008–03/2010 | **Assistant Systems Engineer**, Tata Consultancy Services, India.
Worked in the domain of *Business Intelligence and Performance Management*. Primarily involved in using state-of-the-art tools for integrating data from heterogeneous sources for data analysis.

## Academic Research Experience

02/2019–07/2021 | **Post-doctoral Researcher**, Chair for Processor Design,
Computer Science Department,
Technische Universität Dresden, Germany.
Prof. Akash Kumar

01/2015–02/2019 | **Research Scholar (Ph.D.)** at Signal Processing and VLSI Lab,
Department of Electrical and Computer Engineering,
National University of Singapore, Singapore.
Prof. Bharadwaj Veeravalli and Prof. Akash Kumar

## Skills

| | |
|---|---|
| Design Skills | AI/ML, IP design (HLS and RTL), Physical design, EDA Tool design |
| Design Languages | VHDL, SystemC, Verilog |
| Programming Languages | C, C++, Python, MATLAB |
| EDA Tools | Xilinx Vitis & Vivado, Gem5 |
| Language Proficiency | English, Oriya, Hindi |

## Recent Publications

**[ACM TECS]** S. Ullah, S. S. Sahoo, N. Ahmed, D. Chaudhury, & A. Kumar. *AppAxO: Designing Application-specific Approximate Operators for FPGA-based Embedded Systems*, in **ACM Trans. Embed. Comput. Syst.** Just Accepted (January 2022). DOI:https://doi.org/10.1145/3513262

**[IEEE TCAD]** B. Ranjbar, A. Hosseinghorban, S. S. Sahoo, A. Ejlali & A. Kumar. *BOT-MICS: Bounding Time Using Analytics in Mixed-Criticality Systems*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, doi: 10.1109/TCAD.2021.3127867.

**[IEEE ACCESS]** Nambi, S., Ullah, S., Lohana, A., S. S. Sahoo, Merchant, F., & Kumar, A, *ExPAN(N)D: Exploring Posits for Efficient Artificial Neural Network Design in FPGA-based Edge Processing*. in **IEEE Access**, vol. 9, pp. 103691-103708, 2021, doi: 10.1109/ACCESS.2021.3098730.

**[IEEE TCAD]** A. R. Baranwal, S. Ullah, S. S. Sahoo & A. Kumar, ReLAccS: *A Multi-level Approach to Accelerator Design for Reinforcement Learning on FPGA-based Systems*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, doi: 10.1109/TCAD.2020.3028350.

**[IEEE TC]** S. Ullah, H. Schmidl, S. S. Sahoo, S. Rehman & A. Kumar, *Area-optimized Accurate and Approximate Softcore Signed Multiplier Architectures*, in **IEEE Transactions on Computers**, doi: 10.1109/TC.2020.2988404.

**[VLSI-SoC 2021]** S. S. Sahoo & A. Kumar, *Using Monte Carlo Tree Search for EDA – A Case-study with Designing Cross-layer Reliability for Heterogeneous Embedded Systems*, in 2021 IFIP/IEEE 29th International Conference on Very Large Scale Integration (**VLSI-SoC 2021**), 2021, pp. 1-6, doi: 10.1109/VLSI-SoC53125.2021.9606987.

**[GLSVLSI 2021]** S. S. Sahoo, A. R. Baranwal, S. Ullah & A. Kumar, *MemOReL: A Memory-oriented Optimization Approach to Reinforcement Learning on FPGA-based Embedded Systems*, in Proceedings of the 2021 on Great Lakes Symposium on VLSI (**GLSVLSI 2021**), 339-346.

**[DAC 2021]** Ullah, S. Sahoo, S. S., & Kumar, A. (2020). *CLAppED: A Design Framework for Implementing Cross-Layer Approximation in FPGA-based Embedded Systems*. In Proceedings of the 58th Annual Design Automation Conference. **DAC '21**.

**[DFTS 2020]** S. S. Sahoo, B. Veeravalli and A. Kumar, *Markov Chain-based Modeling and Analysis of Checkpointing with Rollback Recovery for Efficient DSE in Soft Real-time Systems*. (2020) IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (**DFT 2020**), Frascati, Italy, 2020, pp. 1-6, doi: 10.1109/DFT50435.2020.9250892.

## Technical Education

06/2019 — Doctorate degree, Doctor of Philosophy (Ph.D.)
National University of Singapore, Singapore
Grade: 4.0/5.0

01/2015–02/2019 — PhD Scholar at Department of Electrical and Computer Engineering

Thesis: *A Cross-layer Reliability-integrated System-level Design Methodology for Heterogeneous Multiprocessor SoC-based Embedded Systems.* The thesis involved research into optimizing the distribution of reliability methods across multiple layers of the system stack during both design-time and run-time.

09/2012 — Master's Degree, Master of Technology (M.Tech)
Indian Institute of Science, Bangalore, India
Grade: First Class (6.6/8.0)

07/2010–06/2012 — Electronics Design and Technology

Project: *Hardware Accelerator for Support Vector Machines.* The project aimed at accelerating the training phase of Support Vector Machine using FPGAs for hardware/software co-design.

12/2008 — Bachelor's Degree, Bachelor of Technology (B.Tech)
Biju Patnaik University of Technology, Rourkela, India
(College of Engineering and Technology, Bhubaneswar, India)
Grade: 8.65/10.0

07/2004–06/2008 — Instrumentation and Electronics Engineering

Project: *Short Message Service (SMS)-based Home Automation.* The project work involved the implementation of a wireless embedded system, using a mobile phone or a GSM modem, for the purpose of automation and control.

## Awards and Achievements

Jan. 2017 — **HiPEAC Collaboration Grants**, HiPEAC4 Network of Excellence
2015 – 2018 — **NUS Graduate Scholarship**, National University of Singapore, Singapore.
2010 – 2012 — **MHRD (GATE) Scholarship**, Government of India, India
2004 – 2008 — **CET Merit Scholarship**, CET, Bhubaneswar, India.

## Personal Data


Name: Siva Satyendra Sahoo
Gender: Male
Place and Date of Birth: Dhuturdah SHC, India | 15 November 1985
Address: 1818/4123 Nigamvihar, Sriram Nagar lane 4, Bhubaneswar, India
Phone: +91 9945676167
email: s.satyendra.sahoo@gmail.com
Family status: Single

## References


| | |
|---|---|
| Akash Kumar | Head of Chair, Chair for Processor Design,<br>Computer Science Department,<br>Technische Universitåt Dresden, Dresden, Germany.<br>akash.kumar@tu-dresden.de |
| Bharadwaj Veeravalli | Associate Professor, Communication and Networks,<br>Department of Electrical and Computer Engineering,<br>National University of Singapore, Singapore.<br>elebv@nus.edu.sg |
| Kuruvilla Varghese | Principal Research Scientist,<br>Department of Electronic Systems Engineering,<br>Indian Institute of Science, Bangalore, India.<br>kuru@iisc.ac.in |
| Kanhu Charan Bhuyan | Assistant Professor,<br>Department of Instrumentation & Electronics Engineering,<br>College of Engineering and Technology, Bhubaneswar, India.<br>kcbhuyan@cet.edu.in |

# All Publications

## Published Journals

**[J7]** S. Ullah, S. S. Sahoo, N. Ahmed, D. Chaudhury, & A. Kumar. *AppAxO: Designing Application-specific Approximate Operators for FPGA-based Embedded Systems*, in **ACM Trans. Embed. Comput. Syst.** Just Accepted (January 2022). DOI:https://doi.org/10.1145/3513262

**[J6]** B. Ranjbar, A. Hosseinghorban, S. S. Sahoo, A. Ejlali & A. Kumar. *BOT-MICS: Bounding Time Using Analytics in Mixed-Criticality Systems*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, doi: 10.1109/TCAD.2021.3127867.

**[J5]** S. S. Sahoo, Ranjbar, B., & Kumar, A, *Reliability-aware Resource Management in Multi-/Many-core Systems: A Perspective Paper*, in **MDPI Journal of Low Power Electronics and Applications**, 2021.

**[J4]** Nambi, S., Ullah, S., Lohana, A., S. S. Sahoo, Merchant, F., & Kumar, A, *ExPAN(N)D: Exploring Posits for Efficient Artificial Neural Network Design in FPGA-based Edge Processing.* in **IEEE Access**, vol. 9, pp. 103691-103708, 2021, doi: 10.1109/ACCESS.2021.3098730.

**[J3]** A. R. Baranwal, S. Ullah, S. S. Sahoo & A. Kumar, ReLAccS: *A Multi-level Approach to Accelerator Design for Reinforcement Learning on FPGA-based Systems*, in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, doi: 10.1109/TCAD.2020.3028350.

**[J2]** S. Ullah, H. Schmidl, S. S. Sahoo, S. Rehman & A. Kumar, *Area-optimized Accurate and Approximate Softcore Signed Multiplier Architectures*, in **IEEE Transactions on Computers**, doi: 10.1109/TC.2020.2988404.

**[J1]** Sahoo, S. S., Nguyen, T. D. A., Veeravalli, B., & Kumar, A, *Multi-objective design space exploration for system partitioning of FPGA-based Dynamic Partially Reconfigurable Systems*, In **Integration, the VLSI Journal, Elsevier**, November 2018.

## Published Conference Proceedings

**[C15]** S. S. Sahoo, A. Kumar, M. Decky, S. C. B. Wong, G. V. Merrett, Y. Zhao, Jiachen Wang, X. Wang & A. K. Singh, *Emergent design challenges for embedded systems and paths forward: mixed-criticality, energy, reliability and security perspectives*, in Proceedings of the 2021 International Conference on Hardware/Software Codesign and System Synthesis (**CODESS, ESWeek 2021**). Association for Computing Machinery, New York, NY, USA, 1–10. DOI:https://doi.org/10.1145/3478684.3479246

**[C14]** S. S. Sahoo & A. Kumar, *Using Monte Carlo Tree Search for EDA – A Case-study with Designing Cross-layer Reliability for Heterogeneous Embedded Systems*, in 2021 IFIP/IEEE 29th International Conference on Very Large Scale Integration (**VLSI-SoC 2021**), 2021, pp. 1-6, doi: 10.1109/VLSI-SoC53125.2021.9606987.

**[C13]** S. S. Sahoo & A. Kumar, *CLEO-CoDe: Exploiting Constrained Decoding for Cross-Layer Energy Optimization in Heterogeneous Embedded Systems*, in 2021 IFIP/IEEE 29th International Conference on Very Large Scale Integration (**VLSI-SoC 2021**), 2021, pp. 1-6, doi: 10.1109/VLSI-SoC53125.2021.9606983.

**[C12]** S. S. Sahoo, A. R. Baranwal, S. Ullah & A. Kumar, *MemOReL: A Memory-oriented Optimization Approach to Reinforcement Learning on FPGA-based Embedded Systems*, in Proceedings of the 2021 on Great Lakes Symposium on VLSI (**GLSVLSI 2021**), 339-346.

**[C11]** Ullah, S. Sahoo, S. S., & Kumar, A. (2020). *CLAppED: A Design Framework for Implementing Cross-Layer Approximation in FPGA-based Embedded Systems.* In Proceedings of the 58th Annual Design Automation Conference. **DAC '21**(Accepted for publication).

**[C10]** Ranjbar, B., Hoseinghorban, A., Sahoo, S. S., Ejlali, A. & Kumar, A. (2020). *Improving the Timing Behaviour of Mixed-Criticality Systems Using Chebyshev's Theorem.* In Design, Automation & Test in Europe Conference & Exhibition, **DATE 2021**, Virtual Conference and Exhibition, February 01-05, 2021.

**[C9]** S. S. Sahoo, B. Veeravalli and A. Kumar, *Markov Chain-based Modeling and Analysis of Checkpointing with Rollback Recovery for Efficient DSE in Soft Real-time Systems*. (2020) IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (**DFT 2020**), Frascati, Italy, 2020, pp. 1-6, doi: 10.1109/DFT50435.2020.9250892.

**[C8]** Sahoo, S. S., Veeravalli, B., & Kumar, A. (2020). *CL(R)Early: An Early-stage DSE Methodology for Cross-Layer Reliability-aware Heterogeneous Embedded Systems*. In Proceedings of the 57th Annual Design Automation Conference. **DAC '20**. A Virtual Experience.

**[C7]** Rai, S., Raitza, M., Sahoo, S. S., & Kumar, A. (2020). *DISCERN: Distilling Standard Cells for Emerging Reconfigurable Nanotechnologies*. In 2020 Design, Automation & Test in Europe Conference & Exhibition, **DATE 2020**, Virtual Conference and Exhibition, April 21- May 31, 2020.

**[C6]** Sahoo, S. S., Veeravalli, B., & Kumar, A. (2019). *A Hybrid Agent-based Design Methodology for Dynamic Cross-layer Reliability in Heterogeneous Embedded Systems*. In Proceedings of the 56th Annual Design Automation Conference. **DAC '19**. Las Vegas, NV, USA.

**[C5]** Sahoo, S. S., Nguyen, T. D. A., Veeravalli, B., & Kumar, A. (2018). *QoS-aware Cross-layer Reliability-integrated FPGA-based Dynamic Partially Reconfigurable System Partitioning*. In International Conference on Field-Programmable Technology, **ICFPT 2018**, Naha, Okinawa, Japan, December 10-14, 2018.

**[C4]** Sahoo, S. S., Nguyen, T. D. A., Veeravalli, B., & Kumar, A. (2018). *Lifetime-aware design methodology for dynamic partially reconfigurable systems*. In 23rd Asia and South Pacific Design Automation Conference, **ASP-DAC 2018**, Jeju, Korea (South), January 22-25, 2018(pp. 393–398).

**[C3]** Sahoo, S. S., Veeravalli, B., & Kumar, A. (2018). *CLRFrame: An analysis framework for designing cross-layer reliability in embedded systems*. In 31st International Conference on VLSI Design and 17th International Conference on Embedded Systems, **VLSID 2018**, Pune, India, January 6-10, 2018 (pp. 307–312).

**[C2]** Sahoo, S. S., Kumar, A., & Veeravalli, B. (2016). *Design and evaluation of reliability-oriented task re-mapping in MPSoCs using time-series analysis of intermittent faults*. In 2016 Design, Automation & Test in Europe Conference & Exhibition, **DATE 2016**, Dresden, Germany, March 14-18, 2016 (pp. 798–803).

**[C1]** Sahoo, S. S., Veeravalli, B., & Kumar, A. (2016). *Cross-layer fault-tolerant design of real-time systems*. In 2016 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, **DFT 2016**, Storrs, CT, USA, September 19-20, 2016 (pp. 63–68).

## Book Chapters

**[BC3]** S. Ullah, S. S. Sahoo, & A. Kumar, *Efficient Hardware Arithmetic for Embedded Machine Learning*, in **Embedded Machine Learning for Cyber-Physical, IoT, and Edge Computing, Springer 2022**. *To appear*.

**[BC2]** Ranjbar, B., Sahoo, S. S., Singh, A., Dziurzanski, P., & Kumar, A., *Power management of Multicore systems*, in **Handbook of Computer Architecture, Springer 2022**. *To appear*.

**[BC1]** Sahoo, S. S., & Kumar, A., *Fault-tolerant Computer Architectures*, in **Handbook of Computer Architecture, Springer 2022**. *To appear*.