Final Exam Problem 1

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# 2 Analytical Design

Diagram

Description automatically generatedBased on the project parameters, a state transition diagram was generated for the Quadrature Phase Encoder as shown in Figure 1, this design is detailed in the file “01Exam-FSMDiagram.fsm.”

**Figure 1: FSM Diagram**

Graphical user interface, application, table

Description automatically generatedEach distinct state represents a quadrant with the FSM state numbers 0, 1, 3, and 2 corresponding to quadrants 1, 2, 3, and 4, respectively. Further, the transitions are designed as specified with a Direction value of 0 corresponding to a clockwise traversal and a Direction value of 1 corresponding to a counterclockwise direction. From this diagram, the state transition table and equations were generated, seen in Figure 2.

**Figure 2: Equations and State Transition Table**

The FSM states proceed in the 0, 1, 3, 2 order to improve the efficiency of the system. Through this ordering, each state’s binary encoding can be outputted with no further processing, to be seen in the circuit.

Diagram, schematic

Description automatically generatedThrough analysis of the equations and state transition table displayed in Figure 2, a circuit was generated as shown in Figure 3.

**Figure 3: Generated Circuit**

As one can see, the X and Y output are very simple, connected directly to the Z­1 and Z0 values, respectively. This is an artifact of the strange FSM state ordering.

Diagram, schematic

Description automatically generatedThis circuit was modified slightly to incorporate the asynchronous reset by replacing the current synchronous D flip-flops with asynchronous D flip-flops as well as a reset input (resets to initial state) as shown in Figure 4.

**Figure 4: Reset Incorporated Circuit**

# 3 Numerical Verification

Graphical user interface, application, table

Description automatically generatedTo test the circuit, a series of test vectors were generated from the provided timing graph in Figures 5 and 6, respectively.

**Figure 5: Input Test Vectors**

Chart

Description automatically generated with medium confidence

**Figure 6: Timing Graph from Project Brief**

The designed test vectors test all primary functions of the FSM including the asynchronous reset and the directional input. This is through the program’s provided Reset input at line 14 as well as its change in the Direction input to a constant 1 at line 14. The test results in both graphical and tabular format are detailed in Figures 7 and 8, respectively.

Table

Description automatically generatedChart

Description automatically generatedThe problem requirement for this assignment was to design a quadrature phase encoding, a technique used in motors. Further, this design was required to incorporate an asynchronous reset. As seen through the extensive test vectors in Figure 5 that were based on the provided timing graph in Figure 6 and the circuit passing said tests as seen in Figures 7 and 8, we can conclude that the design does indeed satisfy the problem requirements.

**Figure 8: Test Results (Table)**

**Figure 7: Test Results (Graph)**