Final Exam Problem 2

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CS/ECE 2330 Digital Logic Design

May 10, 2021

# 2 Analytical Design

Diagram

Description automatically generatedBased on the project parameters, a state transition diagram was generated for the Pushbutton incorporated FSM as shown in Figure 1, this design is detailed in the file “02ExamDiagram.fsm.”

**Figure 1: FSM Diagram**

Text

Description automatically generatedTraditionally, this circuit would be built with two FSMs one 3-state FSM for debouncing and another 4-state FSM for encoding each state. By debouncing the input, the state FSM would be able to receive a “pure” input. By designing it as shown in Figure 1 instead, each pair of states represents a single output. This is due to the coupling of the debouncing circuit with the state-based output. By creating the circuit as detailed in Figure 1, only a single circuit that incorporates a debouncing aspect can be employed without the utilization of multiple distinct circuits. From this diagram, the equations and state transition table were generated, seen in Figures 2 and 3, respectively.

**Figure 2: Generated Equations**

Diagram, schematic

Description automatically generatedTable

Description automatically generatedThrough analysis of the equations and state transition table displayed in Figure 2, a circuit was generated as shown in Figure 4.

**Figure 4: Generated Circuit**

**Figure 3: State Transition Table**

# 3 Numerical Verification

Graphical user interface, application, table

Description automatically generatedTo test the circuit, a series of test vectors were generated from the provided timing graph in Figures 5 and 6, respectively.

**Figure 5: Input Test Vectors**

Calendar

Description automatically generated with medium confidence

**Figure 6: Timing Graph from Project Brief**

The designed test vectors test the primary functions of the FSM including the debouncer integration as well as the four-state transition. This is through the program’s pseudo-bounce input at lines 5-8 as well as its confirmation of the state progression throughout the program. The test results in both graphical and tabular format are detailed in Figures 7 and 8, respectively.

Table

Description automatically generated Chart

Description automatically generated

**Figure 8: Test Results (Table)**

**Figure 7: Test Results (Graph)**

The problem requirement for this assignment was to design essentially a 4-state encoding with an input debouncer. As seen through the extensive test vectors in Figure 5 that were based on the provided timing graph in Figure 6 and the circuit passing said tests as seen in Figures 7 and 8, we can conclude that the design does indeed satisfy the problem requirements.

A key decision to combine the debouncer and state circuits was due to the lower resources required in combination. In either case, the same number of flip-flops are used but when combined some resources can be saved in terms of wires.