Opcode Decoder

By Sidhardh Burre

CS/ECE 2330 Digital Logic Design

February 13, 2021

Table of Contents

Contents

[1 Problem Statement 1](#_Toc64119703)

[2 Analytical Design 2](#_Toc64119704)

[3 Numerical Verification 3](#_Toc64119705)

[4 Summary 4](#_Toc64119706)

Table of Figures

[Figure 1: Simple CPU Instruction Format 1](#_Toc64120195)

[Figure 2: Truth Table and Logical Expressions for Opcode Decoder 2](#_Toc64120196)

[Figure 3: Circuit for Opcode Decoder 2](#_Toc64120197)

[Figure 4: Input Test Vectors 3](#_Toc64120198)

[Figure 5: Test Results (Table) 3](#_Toc64120199)

[Figure 6: Test Results (Graph) 4](#_Toc64120200)

# 1 Problem Statement

Design a digital decoding circuit to decode the 3-bit opcode for the instruction format shown in Figure 1. The 8 instructions and corresponding outputs are featured in Table 1. The corresponding command should be outputted only when execute is activated.

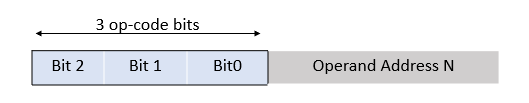


Figure : Simple CPU Instruction Format

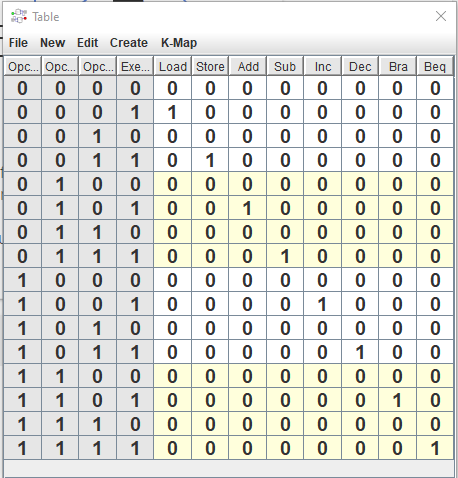
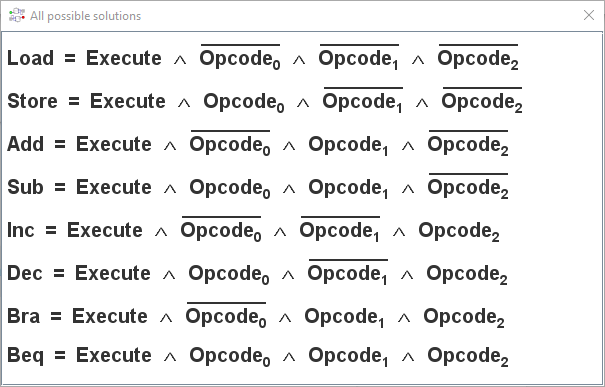
|  |  |  |
| --- | --- | --- |
| Opcode | Mnemonic | Operation |
| 000 | Load N | Load D0 with the contents at memory address = N |
| 001 | Store N | Store contents of D0 at memory address = N |
| 010 | Add N | The contents at memory address = N are added to the contents of D0 and then stored in D0 |
| 011 | Sub N | The contents at memory address = N are subtracted from the contents of D0 and then stored in D0 |
| 100 | Inc N | The contents at memory address = N are incremented by 1 |
| 101 | Dec N | The contents are memory address = N are incremented by 1 |
| 110 | Bra N | The Program Counter (PC) is loaded with the memory address = N |
| 111 | Beq N | The Program Counter (PC) Is loaded with the memory address = N if the last arithmetic operation produced a result of zero (indicated by the zero bit of the ALU, Z = 1). |

Table : Simple CPU Instructions

# 2 Analytical Design

The truth table for the opcode decoder is shown in Figure 2 along with the logical equations that allow the opcode input to be converted into the corresponding signal.

Figure : Truth Table and Logical Expressions for Opcode Decoder



The logical expressions were analyzed to form the circuit schematic shown in Figure 3.

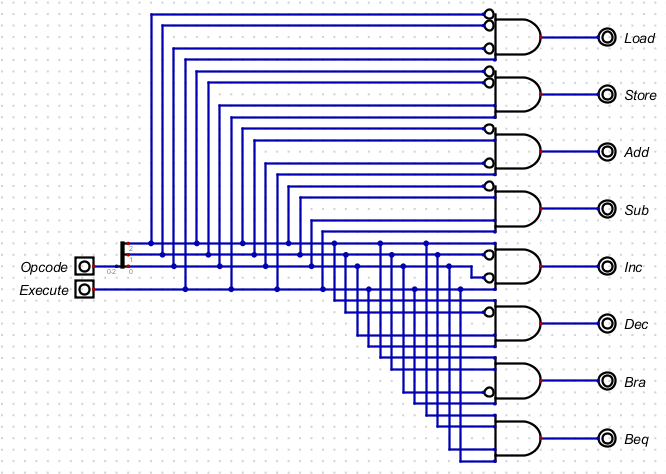


Figure : Circuit for Opcode Decoder

# 3 Numerical Verification

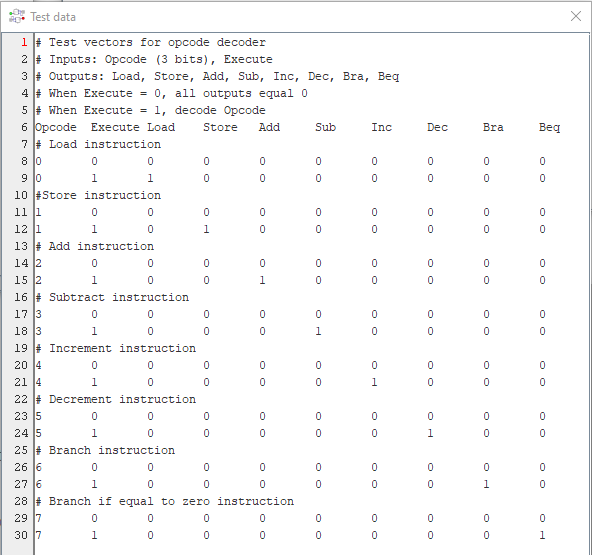
Shown in Figure 4, Figure 5, and Figure 6 are the numerical verification results, where an extensive set of input test vectors (Figure 4) were applied to the circuit.

Figure : Input Test Vectors

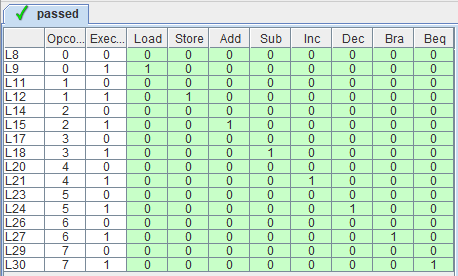


Figure : Test Results (Table)

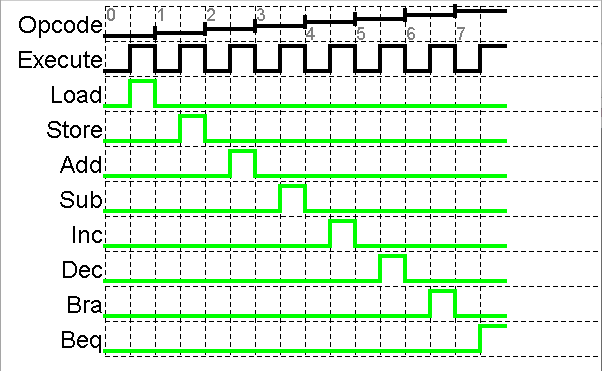


Figure : Test Results (Graph)

# 4 Summary

The problem requirement for this assignment was to design an opcode decoder circuit gated by an execute input that triggers a unique output for each unique value of the opcode input. When the execute produces a 0, nothing is output but when the execute is a 1, the corresponding opcode output is outputted.

The truth table and corresponding logical equations were essential to defining functionality and developing a logic expression, that was then used to specify a digital circuit solution. The digital circuit was tested with an extensive set of input vectors (16 test vectors for 9 inputs) and produced the expected output for each test vector. Therefore, the specified digital circuit design solution satisfies the problem requirements.