Control Signals Logic

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# 1 Problem Statement

Design circuits to generate the control signals for the Central Processing Unit (CPU) architecture shown in Figure 1. The signals are listed in Table 1, and the arithmetic operations defined by F0 and F1 are listed in Table 2.

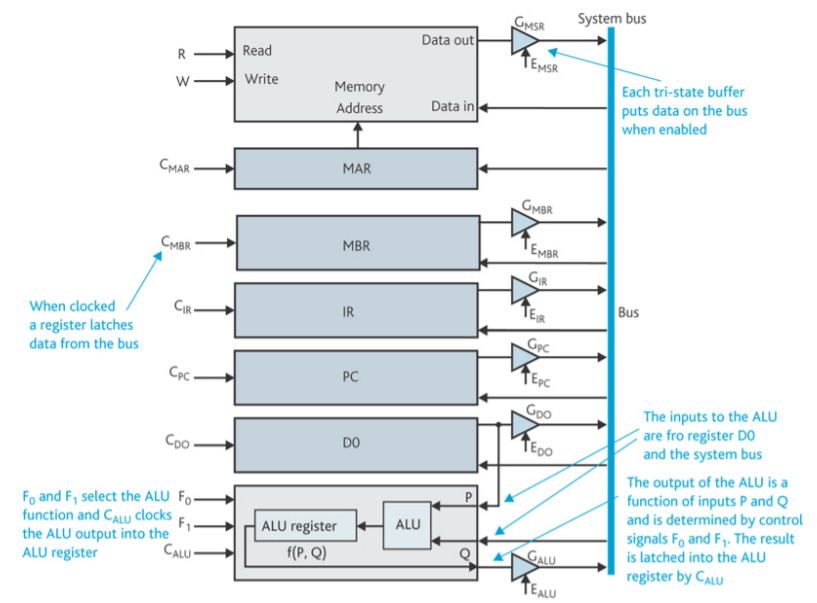


Figure 1: Simple CPU Architecture

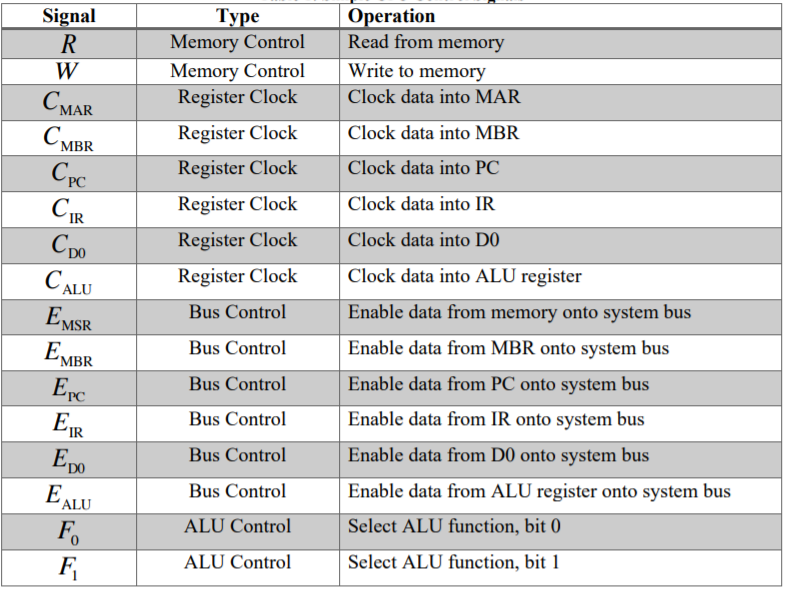


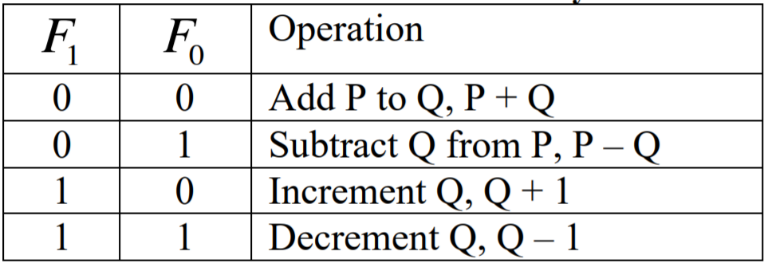
Table : Simple CPU Control Signals

Table 2: Arithmetic Functions Defined by F0 and F1

The table in Figure 2 provides the Register Transfer Level (RTL) operations, or microinstructions, which indicate the sequence of operations that must occur for a given instruction is not executed. The sequencing of these microinstructions occurs within the timing signals, T0-T7. For example, the 4 microinstructions associated with the fetch operation are:

* MAR 🡨 [PC]: The content of the PC is loaded into the MAR
* IR 🡨 [MAR]: The memory content at the address contained in MAR is loaded into the IR
* ALU (Q) 🡨[PC]: The content of the PC is provided as the Q input to the ALU
* PC 🡨 [ALU]: The output of the ALU is then loaded into the PC

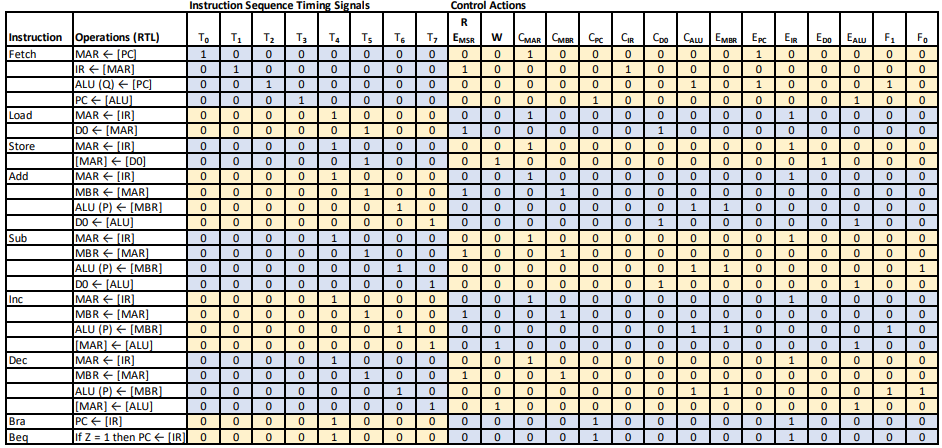


Figure 2: Instruction Sequencing and Control Signals

The Z signal is an output from the ALU and indicates whether the ALU operation produced a result equal to zero. Z=1 indicates that the ALU operation result equals zero; Z = 0 indicates otherwise. This signal is used by the **Beq** instruction to determine if the contents of the IR are loaded into the PC, thus executing what is known as a conditional branch. Because Z is used by a subsequent instruction, your control signals logic design should include a simple sequential logic circuit to store the value of Z after any ALU operation during the T6 instruction sequence period (that is, when T6 = 1).

# 2 Analytical Design

The logical equations for the Control Signals are shown in Figure 2 that allows for the Control Signal input to be converted into the corresponding command output.

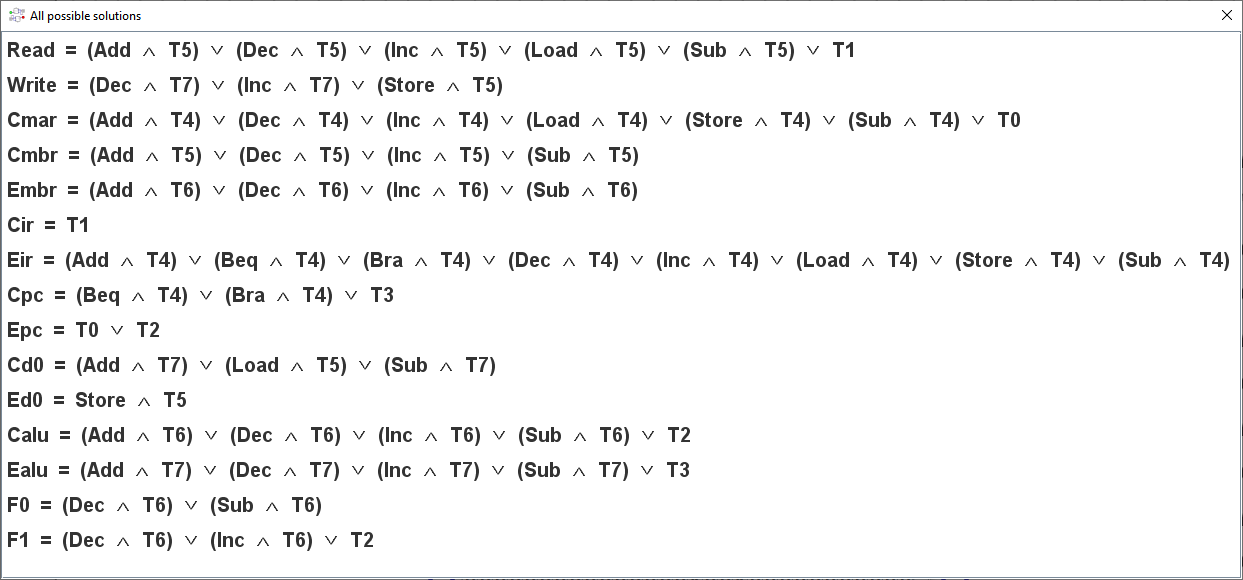


Figure : Logical Expressions for Control Signals Logic

The logical expressions were analyzed to form the circuit schematic shown in Figure 3 and the Z value storage Figure 4.

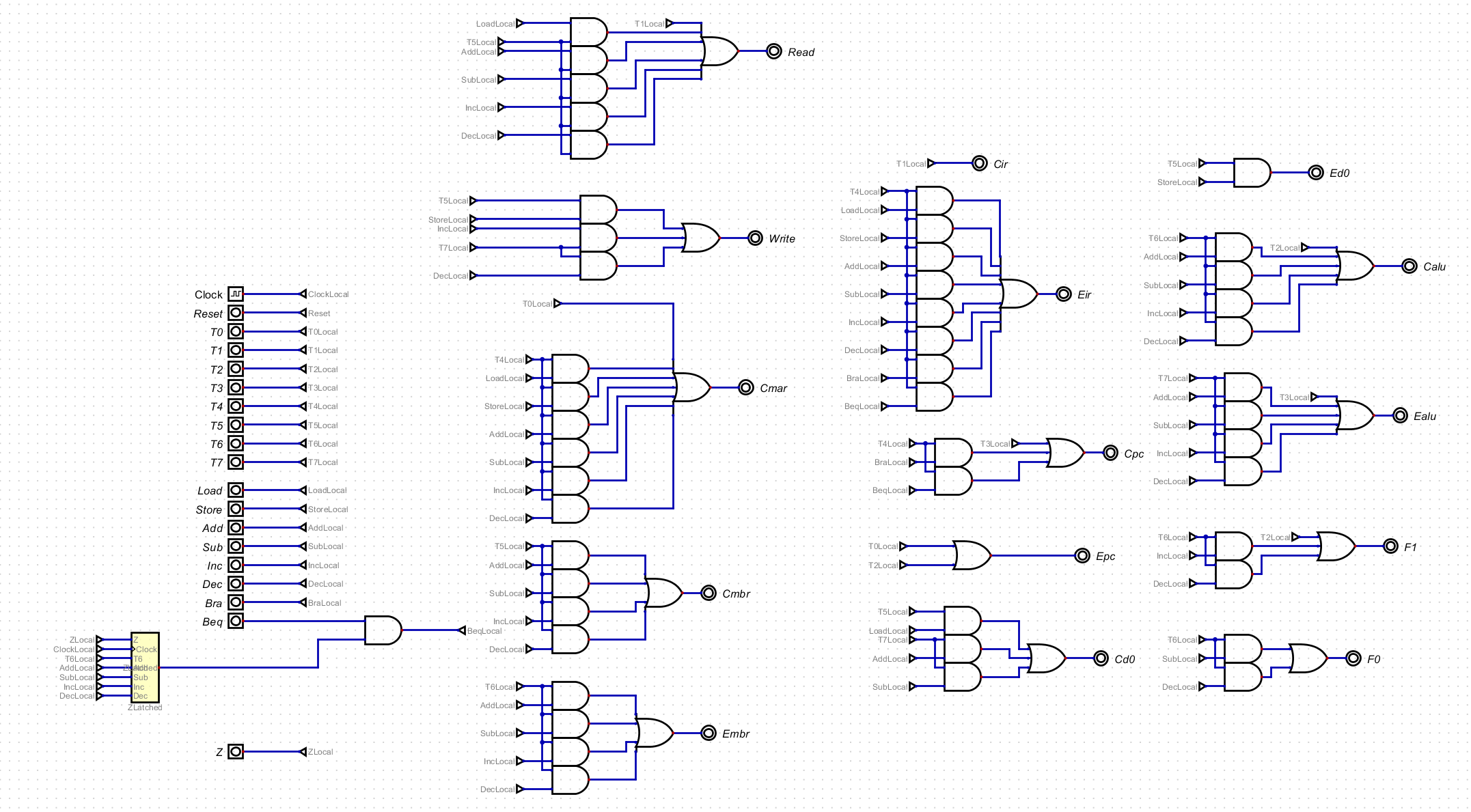


Figure 4: Circuits for Control Signals Logic

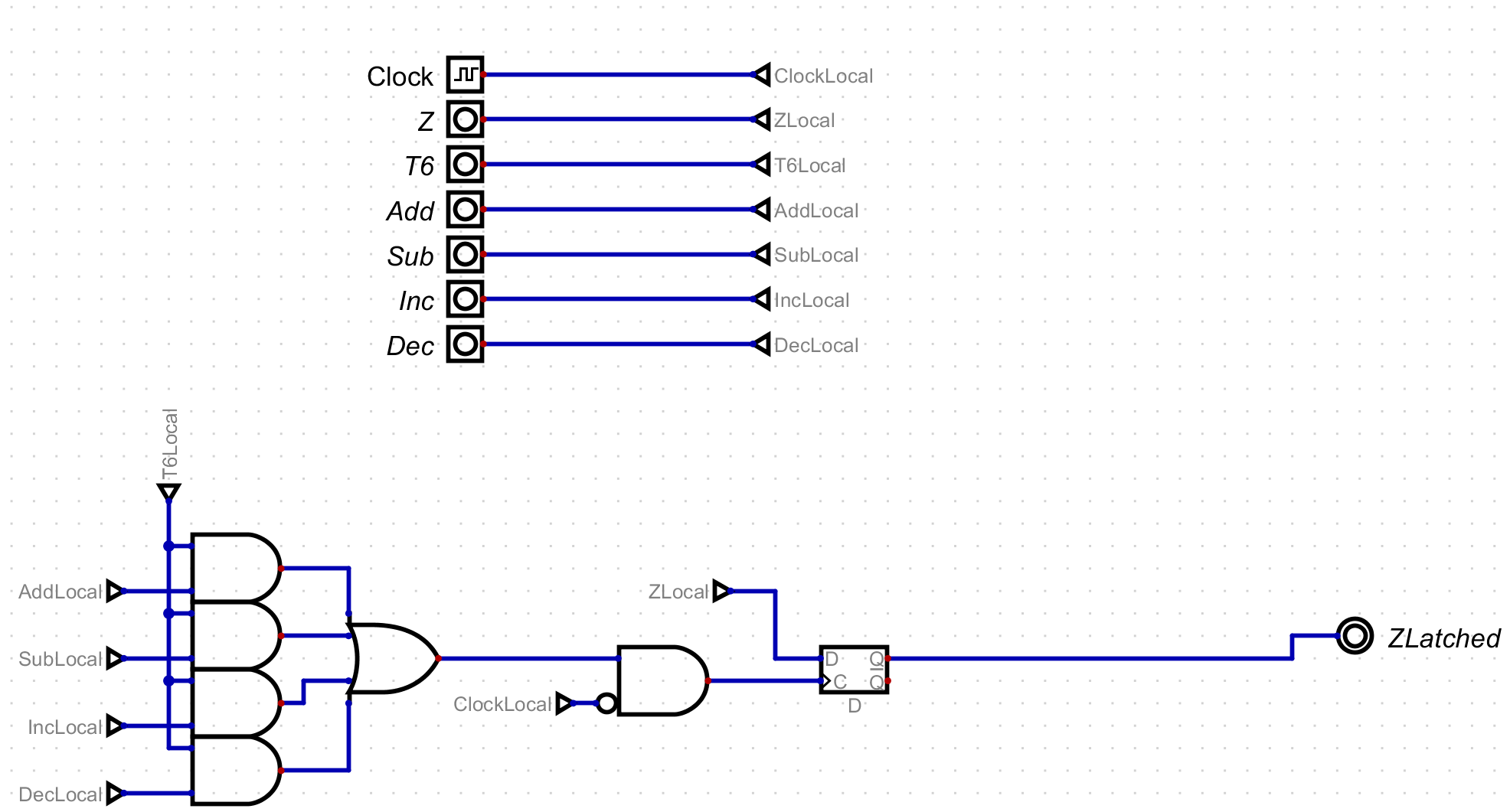


Figure 5: Circuit for Z storage

# 3 Numerical Verification

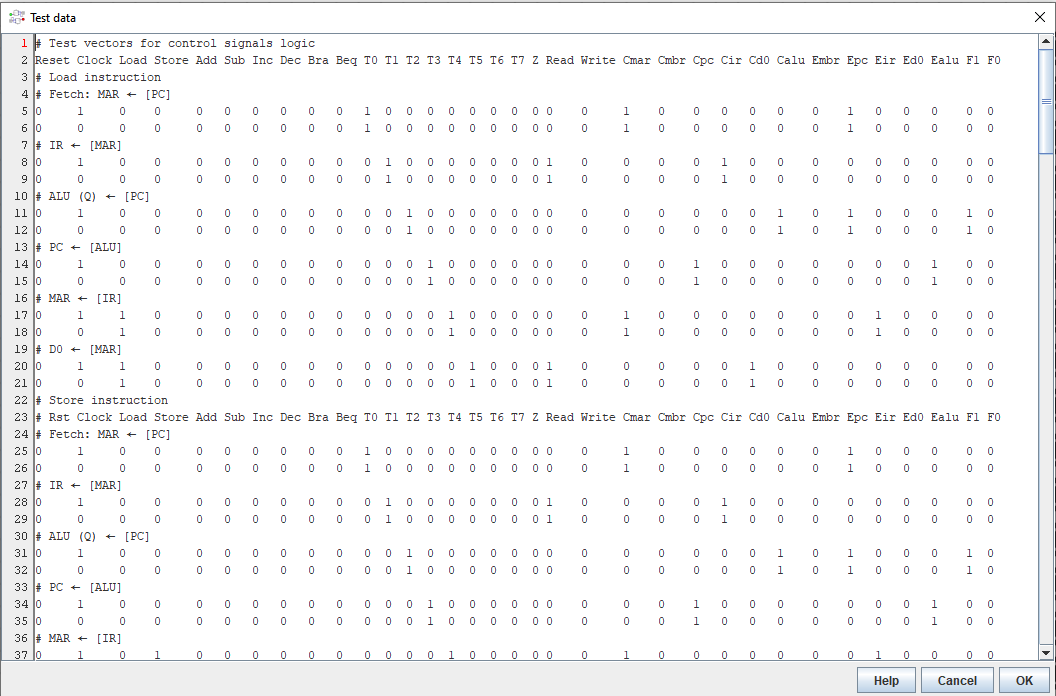
 Shown in Figure 4, Figure 5, and Figure 6 are the numerical verification results, where an extensive set of input test vectors (Figure 4) were applied to the circuit.

Figure 6: Input Test Vectors

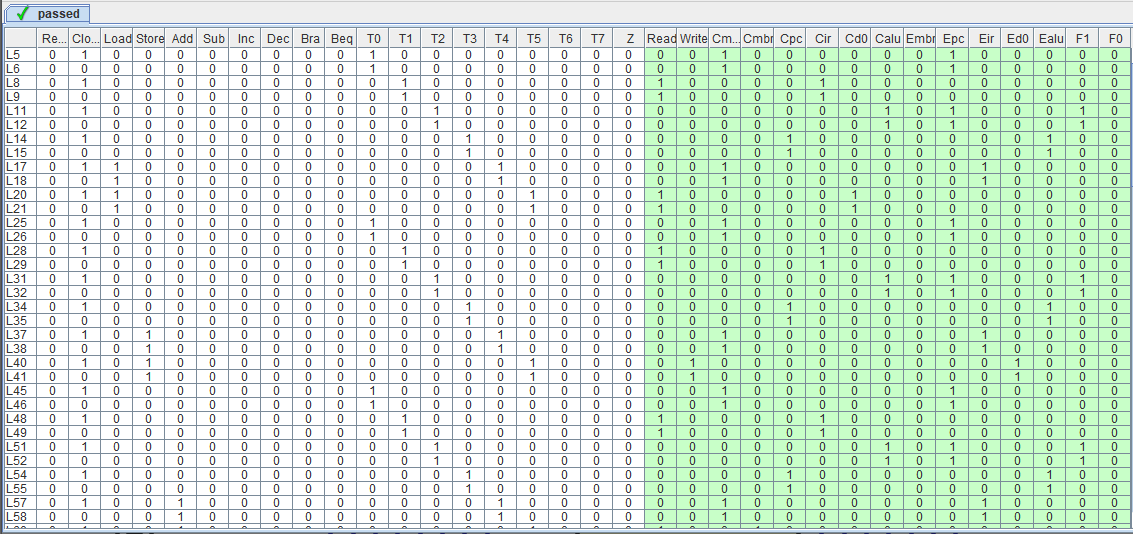


Figure 7: Test Results (Table)

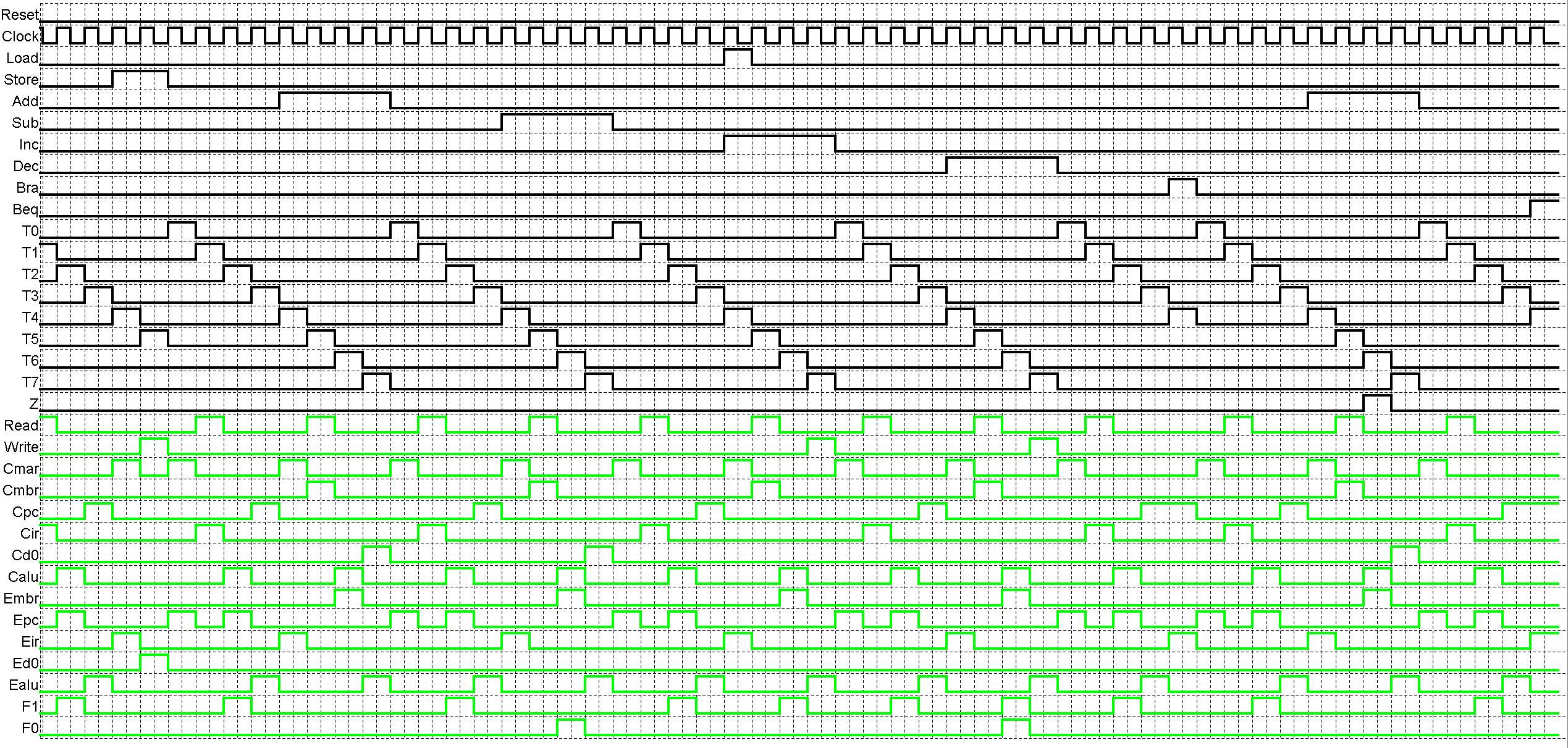


Figure 8: Test Results (Graph)

# 4 Summary

The problem requirement for this assignment was to design circuits to generate the control signals for the Central Processing Unit (CPU), inputs to the designed circuit are analyzed and output as a corresponding command to the CPU. Additionally, the Z input was to be stored during the T6 time period for determining the pursuant of the conditional or unconditional branch.

The truth table and corresponding logical equations were essential to defining functionality and developing a logic expression, that was then used to specify a digital circuit solution. The digital circuit was tested with an extensive set of input vectors (204 tests for 19 inputs) and produced the expected output for each test vector. Therefore, the specified digital circuit design solution satisfies the problem requirements.