ECE 6100 – Programming Assignment 4

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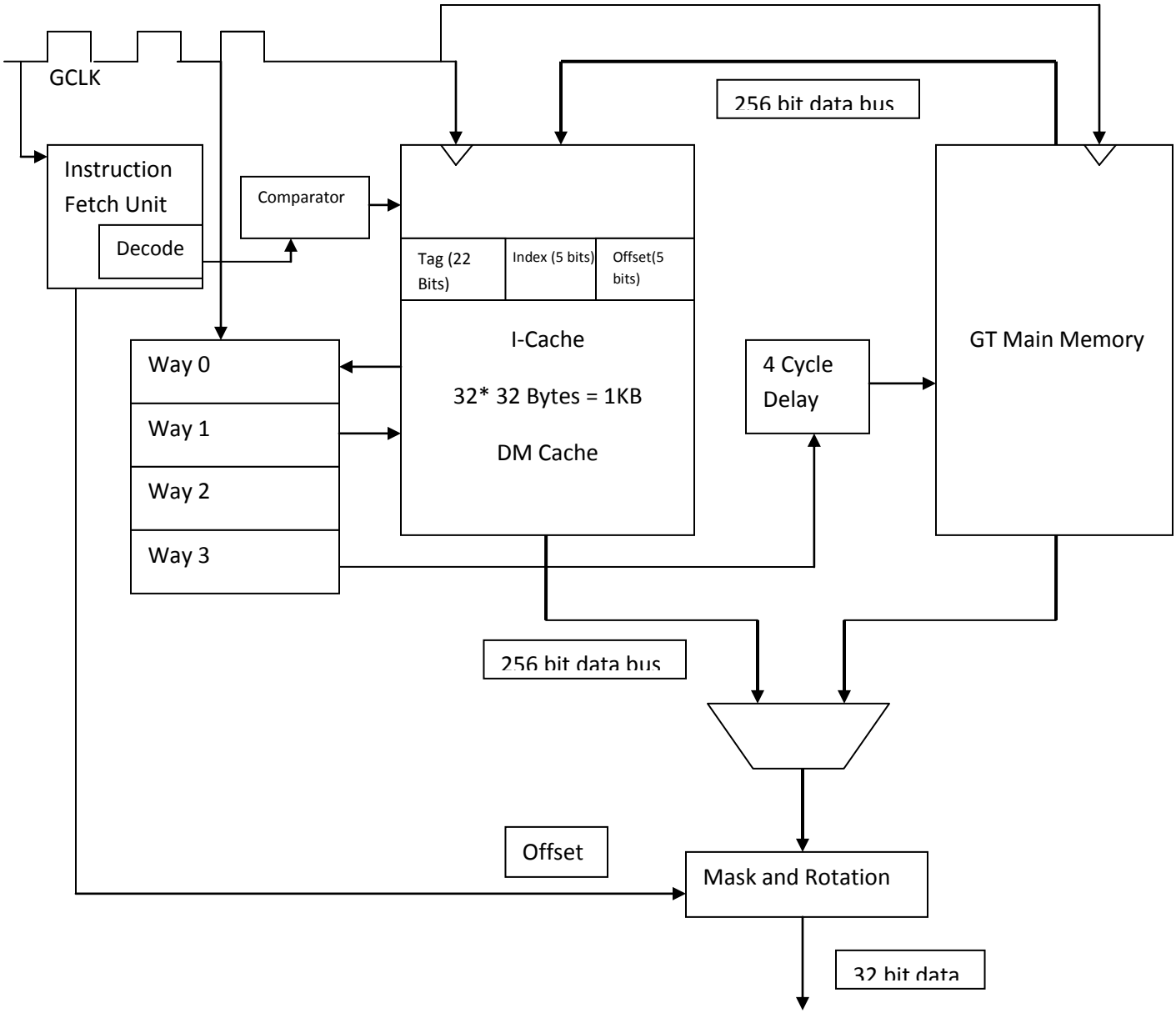
Blocking Instruction Cache

Introduction: In this assignment, we implement a Blocking Instruction Cache . The implementation is done in Verilog (Modelsim v6.6 student edition). The basic functional block diagram of the implementation is as shown below:



- The I-cache structural module follows the following hierarchy:
  - D – Flip Flops
  - Bits – 32
  - Bytes – 32
  - Cache Line (A single line of 32 bytes)
  - I-Cache (A module of Cache Line)

- Similar hierarchy is followed at the tag cache

- Control signals are generated and analyzed in main.v file

- Most of the modules are present in separate files.

- The instruction data stream is delivered from GTIFU module (instruction fetch unit)

- This instruction is sent to a [5:32]decoder whose output is sent to the comparator

- If comparator output is 1, then there is a cache hit and data is sent to the data bus.

- If comparator output is 0, then there is a cache miss and data is searched for in the victim cache

- On victim cache hit, swap procedure takes place

- Else, there is a stall for 4 cycles and data is written into the icache

- The simulation can be run by giving clock stimulus to main.v file