# PIC18F2450/4450

## PIC18F2450/4450 Data Sheet Errata

### Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39760**A**), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F2450/4450 will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

**1. Module: USB**

The USB module for this device incorporates configurable, internal pull-up resistors on the D+ and D- lines. The description and explanation of the pull-ups, however, have been largely omitted from the data sheet.

The following additions are made to **Section 14.0 "Universal Serial Bus (USB)"**:

1. Figure 14-1 is amended to show the internal pull-ups and their control (added detail in dark line, added text in **bold**), as shown below.

> **Note:** Only the upper half of the figure is reproduced for clarity in showing the changes. There are no modifications to the RAM, USB SIE or figure footnotes from the original.

2. In **Section 14.2.2.1 "Internal Transceiver"**, the following paragraph is added immediately following the first paragraph:

The on-chip USB pull-up resistors are controlled by the UPUEN bit (UCFG<4>). They can only be selected when the on-chip transceiver is enabled.

3. A new section is added, following the existing **Section 14.2.2.2 "External Transceiver"**. It reads in its entirety as follows:

#### 14.2.2.3 Internal Pull-up Resistors

The PIC18F2450/4450 devices have built-in pull-up resistors designed to meet the requirements for low-speed and full-speed USB. The UPUEN bit (UCFG<4>) enables the internal pull-ups. Figure 14-1 shows the pull-ups and their control.

The existing subsections 14.2.2.3 and following are renumbered appropriately, starting with **Section 14.2.2.3 "Pull-up Resistors"** (now **Section 14.2.2.4**).

**FIGURE 14-1:** **USB PERIPHERAL AND OPTIONS (PARTIAL REPRESENTATION)**
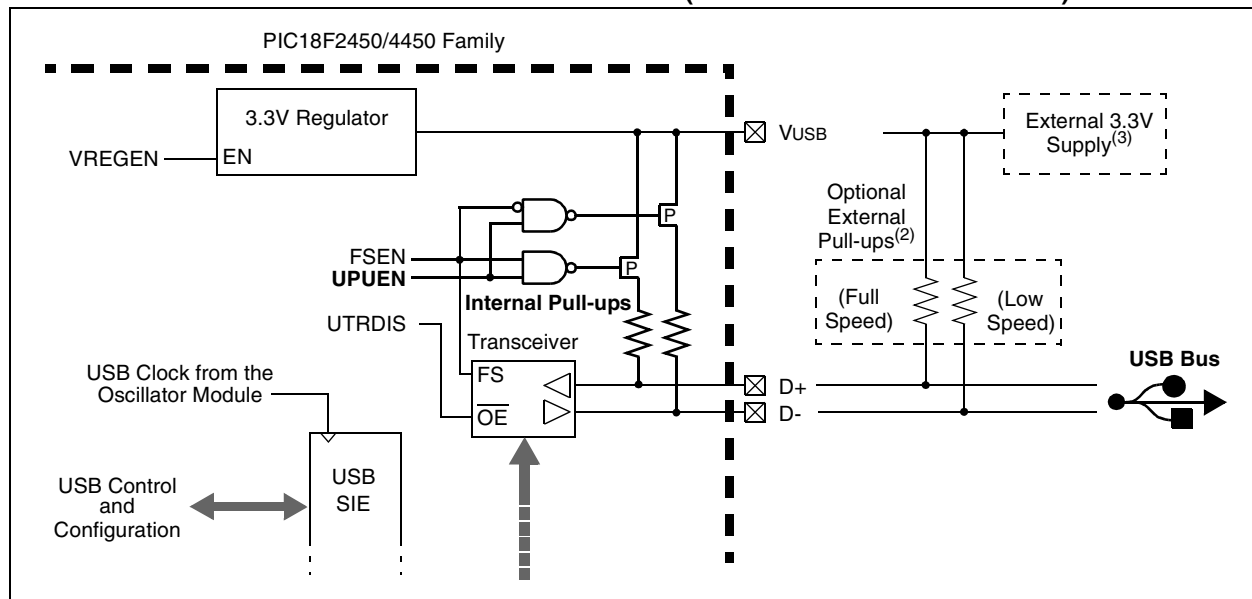
## 2. Module: USB

In **Section 14.4.3 "BD Address Validation"**, the USB RAM address range described in the first paragraph is 400h to 7FFh. The correct range is 400h to **4**FFh.

## 3. Module: USB

In Register 14-5 (BDnSTAT, CPU Mode), the operation of the DSTEN bit is clarified with additional text, shown below in **bold**.

**REGISTER 14-5:** **BDnSTAT: BUFFER DESCRIPTOR n STATUS REGISTER (BD0STAT THROUGH BD63STAT), CPU MODE (PARTIAL REPRESENTATION)**

bit 3      **DTSEN:** Data Toggle Synchronization Enable bit

1 = Data toggle synchronization is enabled; data packets with incorrect Sync value will be ignored **except for a SETUP transaction, which is accepted even if the data toggle bits do not match**

0 = No data toggle synchronization is performed

## 4. Module: USB

In **Section 14.5 "USB Interrupts"**, the following subsection is inserted immediately after **Section 14.5.1 "USB Interrupt Status Register (UIR)"**:

### 14.5.1.1      Bus Activity Detect Interrupt Bit (ACTVIF)

The ACTVIF bit cannot be cleared immediately after the USB module wakes up from Suspend or while the USB module is suspended. A few clock cycles are required to synchronize the internal hardware state machine before the ACTVIF bit can be cleared by firmware. Clearing the ACTVIF bit before the internal hardware is synchronized may not have an effect on the value of ACTVIF. Additionally, if the USB module uses the clock from the 96 MHz PLL source, then after clearing the SUSPND bit, the USB module may not be immediately operational while waiting for the 96 MHz PLL to lock. The application code should clear the ACTVIF bit as shown in Example 14-1.

**EXAMPLE 14-1:      CLEARING ACTVIF BIT (UIR<2>)**

```
Assembly:

        BCF     UCON, SUSPND
LOOP:
        BTFSS   UIR, ACTVIF
        BRA     DONE
        BCF     UIR, ACTVIF
        BRA     LOOP
DONE


C:

UCONbits.SUSPND = 0;
while (UIRbits.ACTVIF){UIRbits.ACTVIF = 0};
```

## 5. Module: Electrical Characteristics

In **Section 21.3 "DC Characteristics"**, the parameters D031 ($V_{IL}$) and D041 ($V_{IH}$) are not valid and are deleted from the table.

## 6. Module: Electrical Characteristics

In **Section 21.4 "AC (Timing) Characteristics"**, the title of Table 21-7 specifies a $V_{DD}$ range of 4.2V to 5.5V for values presented in the table. The correct range is **3.0**V to 5.5V.

## 7. Module: Electrical Characteristics

In **Section 21.4 "AC (Timing) Characteristics"**, Table 21-6 has been updated to reflect the correct range of XT and HSPLL mode operation. The changes are shown below in **bold** text.

**TABLE 21-6: EXTERNAL CLOCK TIMING REQUIREMENTS**

| Param. No. | Symbol | Characteristic | Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| 1A | $F_{OSC}$ | External CLKI Frequency[1] Oscillator Frequency[1] | DC | 48 | MHz | EC, ECIO Oscillator mode |
| | | | **0.2** | **1** | MHz | XT, XTPLL Oscillator mode |
| | | | 4 | 25 | MHz | HS Oscillator mode |
| | | | 4 | **25** | MHz | HSPLL Oscillator mode |
| 1 | $T_{OSC}$ | External CLKI Period[1] Oscillator Period[1] | 20.8 | — | ns | EC, ECIO Oscillator mode |
| | | | **1,000** | **5,000** | ns | XT Oscillator mode |
| | | | **40** | 250 | ns | HS Oscillator mode |
| | | | **40** | 250 | ns | HSPLL Oscillator mode |

# PIC18F2450/4450

## 8. Module: ADC

In **Section 16.2 "Selecting and Configuring Acquisition Time"**, Table 16-1 has been updated to reflect the correct device operating frequencies. The changes are shown in **bold** text.

**TABLE 21-7:** $T_{AD}$ **vs. DEVICE OPERATING FREQUENCIES**

| AD Clock Source ($T_{AD}$) | | Maximum Device Frequency | |
|---|---|---|---|
| Operation | ADCS2:ADCS0 | PIC18FXXXX | PIC18LFXXXX[4] |
| 2 $T_{OSC}$ | 000 | 2.86 MHz | **1.43 MHz** |
| 4 $T_{OSC}$ | 100 | 5.71 MHz | 2.86 MHz |
| 8 $T_{OSC}$ | 001 | 11.43 MHz | 5.72 MHz |
| 16 $T_{OSC}$ | 101 | 22.86 MHz | 11.43 MHz |
| 32 $T_{OSC}$ | 010 | **45.71 MHz** | 22.86 MHz |
| 64 $T_{OSC}$ | 110 | **48.0 MHz** | **45.71 MHz** |
| RC[3] | x11 | 1.00 MHz[1] | 1.00 MHz[2] |

**Note 1:** The RC source has a typical $T_{AD}$ time of 1.2 µs.

**2:** The RC source has a typical $T_{AD}$ time of 2.5 µs.

**3:** For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or the A/D accuracy may be out of specification.

**4:** Low-power devices only.

## 9. Module: USB

In **Section 14.2.2.7 "Internal Regulator"**, the first paragraph after the first note box has been updated. The changes are shown in **bold** text below:

"The regulator is **disabled** by default and can be **enabled** through the VREGEN Configuration bit."

## 10. Module: USB

In **Section 14.2.2.7 "Internal Regulator"**, in the 2nd note box, Note 2 changes as shown in **bold** text below:

"$V_{DD}$ must be greater than **or equal to** $V_{USB}$, even with the regulator disabled."

## REVISION HISTORY

<u>Rev A Document (05/2006)</u>
Original version of this document. Includes clarification issues 1-4 (USB), 5-7 (Electrical Specifications), 8 (ADC) and 9-10 (USB).

**NOTES:**

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