Qualcomm

Qualcomm Technologies, Inc.

Qualcomm® Snapdragon™ 820E Processor (APQ8096SGE)

Device Specification

LM80-P2751-1 Rev. E

February 9, 2018

For additional information or to submit technical questions go to
https://www.96boards.org/product/dragonboard820c/

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.

Revision history

Revision	Date	Description
A	November 12, 2015	Initial release
B	June 2015	■ Section 3.2.1: Removed ■ Table 1.1: Added document number to APQ8096SGE Hardware Register Description ■ Table 1.2: Updated with document numbers ■ Section 1.2: Updated list of Complementary ICs within the APQ8096SGE chipset ■ Figure 4.3: Changed product name to APQ8096SGE
C	January 2016	■ Added Table 7.1: Silicon reliability results ■ Added Table 7.2: Package reliability results
D	August 2016	■ Section 1.2 removed bullet "Chipset and RFFE interfaces" ■ Section 1.3.1 Features integrated into APQ8096 - Updated Bluetooth specification to Bluetooth 4.2 - Removed bullet entry for "Support for LTE-U with PMK8001 and WTR3950 devices" ■ Table 1-3 Summary of APQ8096 device features - corrected video concurrency support ■ Table 1-5 Wireless connectivity summary by standard: Updated Bluetooth specification to Bluetooth 4.2 ■ Section 2.2.2 Pad descriptions - APQ bottom: removed Table 2-11 RF front-end interface functions, and renumbered the tables ■ Table 2-10 Pad descriptions - chipset interface functions: removed the section under subheading Qualcomm RF360 interfaces ■ Table 2-11 Pad descriptions - RF front-end functions: removed this table

Revision	Date	Description
		▪ Table 2-11 Pad descriptions - general-purpose input-output ports: (was Table 2-12) removed entries that showed up in the column Configurable function starting with RFFEn_xxx or GRFC_nn ▪ Section 2.3.1 Pad map - APQ top: correct type from APQ8906 to APQ8096SGE ▪ Section 3.1 Absolute maximum ratings: Added new information ▪ Table 3-1 Absolute maximum ratings: Added new table ▪ Revised VDD_EBI_x values and added SVS2 values in Table 3-2 Operating conditions for voltage rails with AVS Type-1 ▪ Table 3-3 Operating voltages: Revised the VDD_DDR_CORE_1P2 parameter description from 1.155 V to VDD2 ▪ Table 3-8 Digital I/O characteristics for VDD_P7 = 1.8 V nominal (SDC1): Removed the VDD_Px parameter ▪ Table 3-9 Digital I/O characteristics for VDD_P2 = 2.95 V nominal (SDC2): Removed the VDD_Px parameter ▪ Table 3-10 Digital I/O characteristics for VDD_P2 = 1.8 V nominal (SDC2): Removed the VDD_Px parameter ▪ Section 3-11: Changed title to Power management interfaces ▪ Section 3.11.1 RFL front end (RFFE): removed this section ▪ Table 3-11 Digital I/O characteristics for VDD_Px = 2.95 V nominal (UIM1 and UIM2 - Class B): Removed the VDD_Px parameter ▪ Table 3-12 Digital I/O characteristics for VDD_Px = 1.8 V nominal (UIM1 and UIM2 - Class B): Removed the VDD_Px parameter ▪ Table 3-34 Supported RFFE standards and exceptions: removed ▪ Table 7-1 Silicon reliability results: Replaced TBDs with values ▪ Table 7-2 Package reliability results: Revised result details
E	February 2018	▪ Updated the document for language-related changes ▪ Updated the document as per the new branding guidelines

Contents

Figures

Tables

1 Introduction

This document provides a description of chipset capabilities. Not all features are available, nor are all features supported in the software.

> **NOTE:** Enabling some features require additional licensing fees.

1.1 Documentation overview

Technical information for the Qualcomm Technologies, Inc. (QTI) APQ8096SGE device is primarily covered by the documents listed in Table 1-1. All documents must be studied for a thorough understanding of the device and its applications.

Table 1-1   Primary APQ8096SGE documentation

Document number	Title/description
LM80-P2751-1 (this document)	*Qualcomm® Snapdragon™ 820E Processor APQ8096SGE Device Specification* Provides all APQ8096SGE electrical specifications and mechanical information. Additional material includes pad assignments; shipping, storage, and handling instructions; PCB mounting guidelines; and part reliability. This document can be used by company purchasing departments to facilitate procurement.
LM80-P2751-2	*Qualcomm® Snapdragon™ 820E Processor APQ8096SGE Pin Assignment Spreadsheet* A Microsoft Excel spreadsheet listing all APQ8096SGE pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions. This can be used to help build the IC's CAD library symbol, or for quick reference to a particular pad's functional assignment.
LM80-P2751-20	*Qualcomm® Snapdragon™ 820E Processor APQ8096SGE GPIO Configuration Spreadsheet*
LM80-P2751-26	*Qualcomm® Snapdragon™ 820E Processor APQ8096SGE Device Revision Guide* Provides a history of *APQ8096* revisions, explains how to identify the various device revisions, and discusses known issues (or bugs) for each revision and how to work around them.

This APQ8096SGE device specification is organized as follows:

Chapter 1   Provides an overview of the APQ8096SGE documentation, gives a high-level functional description of the device, lists the device features, and defines marking conventions, terms, and acronyms used throughout this document.

Chapter 2   Defines the device pad assignments.

Chapter 3   Defines the device electrical performance specifications, including absolute maximum ratings and operating conditions.

Chapter 4   Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.

Chapter 5   Discusses shipping, storage, and handling of the APQ8096SGE.

Chapter 6   Presents procedures and specifications for mounting the APQ8096SGE onto printed circuit boards (PCBs).

Chapter 7   Presents APQ8096SGE reliability data, including a definition of the qualification samples and a summary of qualification test results.

Table 1-2   Other related documents

Document number	Title / description
LM80-P2751-5	PM8994/8996 Power Management IC Device Specification
LM80-P2751-10	PM8994/8996 Power Management IC Device Revision Guide
LM80-NT441-15	PMI8994/PMI8996 Power Management IC Device Specification
LM80-NT441-17	PMI8994/PMI8996 Device Revision Guide
LM80-P2751-29	WCD9335 Audio Codec Device Specification
LM80-P2751-28	WSA8815/WSA8810 Device Specification
LM80-P2751-24	WSA8815/WSA8810 Device Revision Guide
LM80-P2751-27	Qualcomm Snapdragon 820E CLOCK PLAN

1.2   Introduction

Snapdragon processors were originally designed for hand held devices such as cell phones and tablets, but now can be embedded into virtually anything. Snapdragon processors support high performance, low power consumption, and integrated connectivity to make devices more aware, connected, intelligent and interactive.

Hand held devices such as cell phones and tablets, Internet of Things, and embedded computing devices continue to integrate more and increasingly complex functions while maintaining performance, board space, and cost. These demands are met by the APQ8096SGE device (Figure 1-1) with its processor system that includes a customized 64-bit ARMv8-compliant quad-core applications processor (Qualcomm® Kryo™ CPU), which expands mass market chipset capabilities.

The APQ8096SGE chipset supports high-speed data capabilities over a wide range of air interface standards (listed in Table 1-4 and Table 1-5); the supported radio frequency (RF) operating bands are defined by the chipset's radio frequency integrated circuits (RFIC)s.
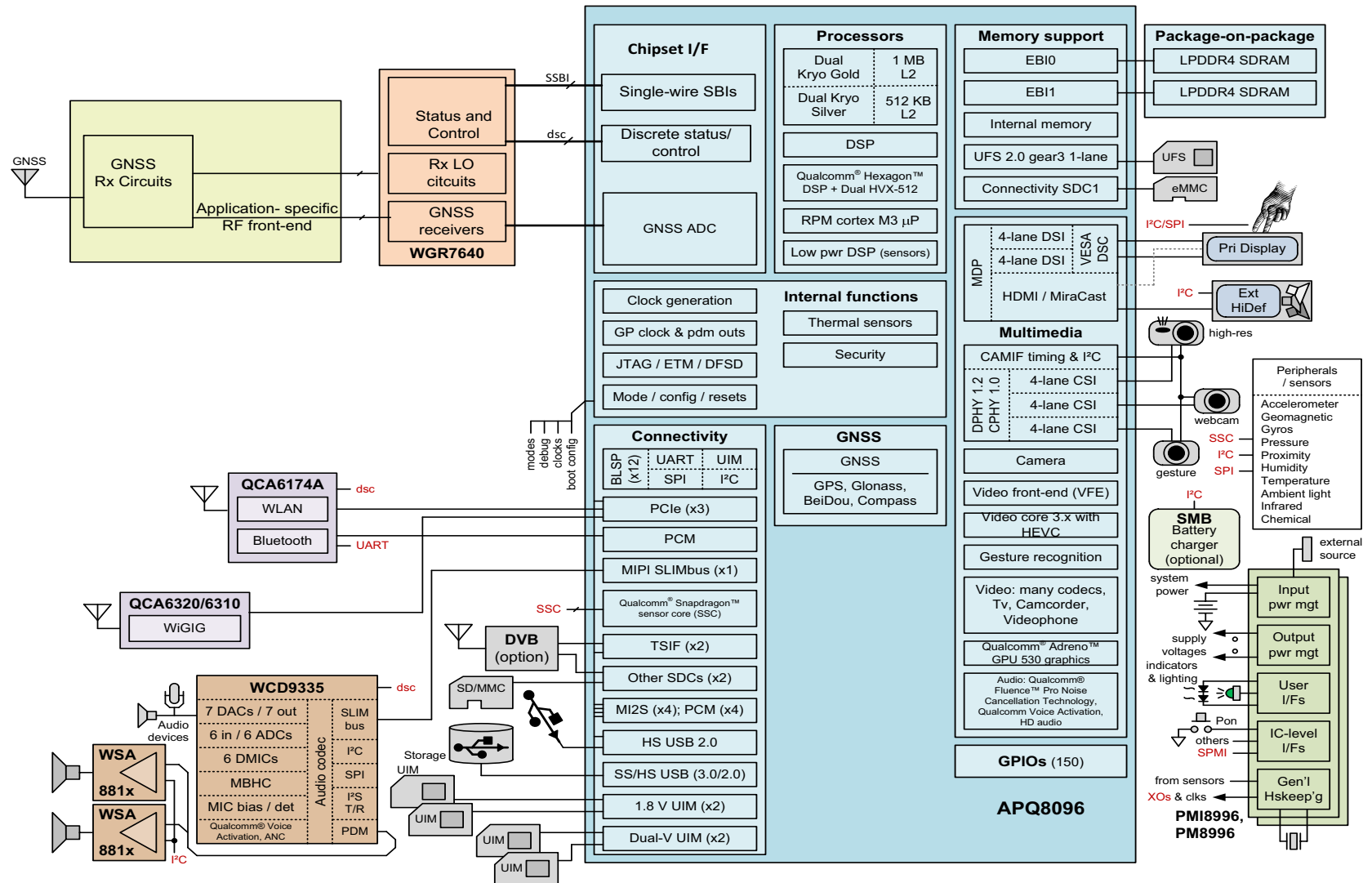
Figure 1-1   APQ8096SGE functional block diagram and example application

The APQ8096SGE device has a high level of integration that reduces the bill-of-material (BoM), and delivers board-area savings. The package-on-package implementation uses LPDDR4 SDRAM memory.

The APQ8096SGE is fabricated using the 14 nm FinFET process. for low active power dissipation and high peak CPU performance. It is available in the 994C MNSP [1], a 15.6 × 15 × 0.64 mm package-on-package (PoP) system (height dimension does not include the memory device). Its bottom footprint is equivalent to a 994-pad nanoscale package (994 NSP), and it accepts memory modules from above that are equivalent to a 387-pad chip-scale package (387 CSP) as specified in *PoP Memory for APQ8094 and APQ8096 Recommendations* (LM80-P2751-15). The bottom includes many ground pads for electrical grounding, mechanical strength, and thermal continuity. See Chapter 2 for pad assignment details and Chapter 4 for mechanical information.

Complementary ICs within the APQ8096SGE chipset include:

- Power management and charger ICs:
    - PM8994/8996 Power Management IC Device Specification
    - PMI8994/8996 Power Management IC Device Revision Guide
    - PM8994/PM8996 AND PMI8994/PMI8992 Power Management ICS Design Guidelines
- Wireless connectivity ICs:
    - QCA6174A Dual-Band 2.2 802.11AC + Bluetooth 4.2 Device Specification
    - QCA6174 WLFC Package Device Specification Addendum
    - QCA6174-1 Device Revision Guide
- Audio ICs:
    - WCD9335 Audio Codec Device Specification
    - WCD9335 Audio Codec Design Guidelines/Training Slides
    - WCD9335 Hardware Register Description
    - WCD9335 Device Revision Guide
    - WGR7640 GNSS RF Receiver IC Device Specification
    - WGR7640 IC GNSS RF Receiver Design Guidelines
    - WGR7640 IC Device Revision Guide
    - WSA8810 Class-D Smart Speaker Amplifier Device Specification
    - WSA8810 Speaker Amplifier Device Revision Guide
    - WSA8815 Class-D Smart Speaker Amplifier Device Specification
    - WSA8815 Speaker Amplifier Device Revision Guide

Since the APQ8096SGE includes many diverse functions, this document describes the major functional blocks individually. The APQ8096SGE Design Guidelines is organized according to the following block partitioning:

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1. The letter 'C' in the package designator (994C MNSP) is used to distinguish this package from other QTI packages that uses the package designator 994 MNSP.

- Architecture and baseband processors

- Memory support

- Air interfaces

- Multimedia

- Connectivity

- Internal functions

- Configurable general-purpose input/output (GPIO) ports

The information contained in this device specification is organized accordingly, including the circuit groupings within its functional block diagram (Figure 1-1), pad descriptions (Chapter 2), and detailed electrical specifications (Chapter 3).

1.3   APQ8096SGE features

NOTE: The hardware features integrated within APQ8096SGE must be enabled by software. Refer to the latest version of the applicable software release notes to identify the enabled APQ8096SGE features.

1.3.1   Features integrated into APQ8096SGE

The following features are integrated into the APQ8096SGE device:

- 14 nm FinFET process for low active power dissipation and high peak CPU performance

- Customized 64-bit ARMv8-compliant quad-core applications processor (Kryo) organized in two clusters

    □ Two high-performance Kryo cores – gold cluster (2.15 GHz)

    □ Two low-power Kryo cores – silver cluster (1.593 GHz)

- Hexagon DSP with dual-Hexagon vector processor (HVX-512) at 825 MHz

- Dual-channel PoP high-speed memory – LPDDR4 SDRAM at 1866 MHz clock rate

- Two 4-lane DSI DPHY 1.2 and HDMI 2.0 (4k60) or 4k30 Miracast

- Display 3840 × 2400 at 60fps, 2560 buffer width (10 layers blending), VESA DSC 1.1

- Complete 4k60 entertainment system (4k60 H.265/VP9 decode with uncompressed 4k display, HDMI 2.0)

    □ Video decode performance – 1080p240/4K60/8x1080p30: H.264, VP8, HEVC 8/10-bit, VP9 1080p60

    □ Video encode performance – 1080p120/4K30/4x1080p30: H.264, VP8, HEVC

    □ Concurrent video performance – 4K60 decode + 4K30 4:2:0 encode, 4K60 decode

- Three 4-lane CSI (4+4+4 or 4+4+2+1) DPHY1.2 at 2.0 Gbps per lane or Three 3-trio CPHY1.0 at 17Gbps

- Dual 14-bit image signal processing (ISP) – 28 MP and 13 MP, 600 MHz; 32 MP 30 ZSL with dual-ISP; 16 MP 30 ZSL with single-ISP; TempNR v2, ASF3, Demosaic, Dual-AF, LTM, CAC, Green Imbalance, Pedestal, stats upgrades, and image quality enhancements

- Adreno 530 (graphics processing unit) with 64-bit addressing at 624 MHz

- Support for UFS2.0 gear 3 (1-lane), eMMC5.1, and SD3.0

- Dedicated low-power SSC with DSP to support always-on use cases

- WLAN 802.11ac and Bluetooth 4.2 supported through QCA6174A; WiGig (802.11ad/ 60 GHz) with QCA6320/QCA6310 – through respective PCIe interfaces

- Three PCIe interfaces

1.3.2   Summary of APQ8096SGE features

Features of the APQ8096SGE device are listed in Table 1-3.

Table 1-3   Summary of APQ8096SGE device features

Feature	APQ8096SGE capability
Processors	
Applications	Customized 64-bit ARMv8-compliant quad-core applications processor (Kryo) ■ Two high-performance Kryo cores – gold cluster (2.15 GHz) ■ Two low-power Kryo cores – silver cluster (1.593 GHz)
Digital signal processing	Hexagon DSP with dual-Hexagon vector processor (HVX-512) (825 MHz)
RPM system	Cortex M3 ■ Suited for code certification and warm boot ■ Brings up secure root of trust (SROT) application processors quickly ■ The only master of the APQ power manager (MPM) ■ MPM coordinates shutdown/wakeup, clock rates, and VDDs
Sensor core	Dedicated low-power Snapdragon sensor core (SSC) with DSP with direct access to internal cores to support always-on low-power use cases.
Memory support	
System memory via PoP and EBI	Dual-channel PoP high-speed memory – LPDDR4 SDRAM at 1866 MHz clock
Internal memory	256 kB OCIMEM 1 MB GMEM for GFX 512 kB VMEM for Video
External memory	
Via UFS	UFS2.0 gear3 – 1 lane
Via SDC1	eMMC5.1 NAND flash device
Air interfaces	
WLAN/Bluetooth	Yes (with QCA6174A)
GNSS – Qualcomm® Location engine	GPS, Glonass, Beidou, and Galileo
Multimedia	
Display support	Up to three concurrent displays; two panels + external
MIPI_DSI	Two; 4-lane + 4-lane; DSI DPHY 1.2; VESA DSC 1.1
HDMI	Yes; v2.0 (4k 60)
Miracast	Yes; v2.0
Example combinations	3840 × 2400 at 60 fps 2560 buffer width (10 layers blending) VESA DSC 1.1
General display features	Color depth – 24-bit pp; TFT, LTPS, CSTN, OLED panels
Camera interfaces	Camera; 1 GP dual ISP

Table 1-3   Summary of APQ8096SGE device features (cont.)

Feature	APQ8096SGE capability
MIPI_CSI	Three 4-lane ■ Legacy mode CSIx_LANEx_P/M (DPHY1.2, Max 8 Gbps 4-lanes) ■ New trio mode with 3-lanes of 3-pads each (CPHY1.0, Max 17 Gbps)
2D performance	■ Dual 14-bit ISP ■ 28 MP + 13 MP, 600 MHz each ■ 28 MP30 ZSL with dual ISP ■ 16 MP30 ZSL with single ISP ■ TempNR v2, ASF3, Demosaic, Dual AF, LTM, CAC, Green Imbalance, Pedestal, statistics upgrades, image quality enhancements
Flexible 3A	Tier 1 customization support, gyro integration
H/W post processor	Hardware temporal NR, zooming, rotator, upscaling
VFE features	No LBC, move LSC, ABF3, demosaic, dual AF, CSC, LTM, gamma, green imbalance, pedestal, stats upgrades, 14-bit pipeline
Mobile display processor	MDP 570
Video applications performance	
Encode	1080p120/4K30/4x 1080p30: H.264, VP8, HEVC
Decode	1080p240/4K60/8x 1080p30: H.264, VP8, HEVC 8/10-bit, VP9
Concurrency	■ 4K30 decode + 4K30 encode ■ 4K60 decode + 1080p60 encode
Graphics	■ Adreno 530 3D graphics accelerator with 64-bit addressing ■ 624 MHz ■ OpenGL ES 3.0/3.1/GEP, GL4.4, DX11.3/4, Path Rendering ■ OpenCL 2.0 Full, Renderscript-Next
Audio	
Codec	Integrated within the Hi-Fi audio codec WCD9335 device: ■ Seven DACs, seven outputs ■ Six differential analog inputs with dedicated ADCs ■ Six digital microphones ■ Snapdragon voice activation (SVA) subsystem for ultra-low voice wake up ■ MBHC, ANC ■ 130 dB dynamic range, 24 bit DAC ■ 44.1 kHz native playback ■ SLIMbus to I2S bridge
Speaker amplifier	Integrated within the WSA8810/WSA8815 class D/G, low noise Smart Amplifier: ■ 4 W output power into 8 Ω load ■ Integrated SmartBoost ■ Integrated feedback speaker protection for excursion and temperature control of the transducers ■ Battery voltage monitoring
Low-power audio	Low-power, low-complexity; 7.1 surround sound
Voice codec support	SILK; QCELP, EVRC, EVRC-B, EVRC-WB; G.711, G.729A/AB; GSM-FR, -EFR, -HR; AMR-NB, -WB

Table 1-3   Summary of APQ8096SGE device features (cont.)

Feature	APQ8096SGE capability
Audio codec support	MP3; AAC, +, eAAC; WMA 9/Pro; Dolby AC-3, eAC-3, DTS
Enhanced audio	■ Surround sound: Dolby True-HD; DTS-HD; DTS express 7.1 ■ Qualcomm® Voice Suite Noise and Echo Cancellation; active speaker protection ■ Enhanced 3D audio solution/Stereo audio expansion feature/Intelligent mixing algorithm
A/V output – HDMI Rev 2.0	Yes ■ Integrated HDMI Tx core and HDMI PHY ■ 1080p at 60 Hz refresh; 24-bit RGB color ■ 4k × 2k at 60 fps + 4k × 2k at 30 fps HDMI ■ Up to 8-channel audio for 7.1 surround sound ■ Dolby Digital Plus, Dolby True-HD, & DTS-HD Master
Digital video broadcast (DVB)	External IC required; dual-TSIF for 12 segment ISDB-T
Connectivity	
BLSP ports	12, 4 bits each; multiplexed serial interface functions
UART	Yes – up to 4 MHz
UIM	Yes – SIM, USIM, CSIM
I2C	Yes – cameras, sensors, near field communicator (NFC), etc.
SPI	Yes – cameras, sensors, etc.
UIM	Two – dual voltage (1.8/2.95 V) Two – 1.8 V only
USB	Two – one USB 2.0 high-speed and one USB 3.0 super-speed/USB 2.0 high-speed compliant
PCIe	Three – PCI-SIG PCIe v2.1 PHY & 2.1 controller
Secure digital interfaces	■ Up to three ports; one 8-bit and two 4-bit; SD 3.0 ■ SDC2 is dual-V ■ SD/MMC card; eMMC NAND; DVB; eSD/eMMC boot
TSIF	Up to two ports; DVB support
Audio interfaces	
SLIMbus	One; highly multiplexed, high-speed; baseline WCD9335
MI2S	■ Full duplex stereo or up to quad channel Tx/Rx MI2S (x3) ■ Up to 8 channel for multi-channel audio applications (x1)
PCM	Short and long sync PCM support
Wireless connectivity	QCA6174A (Wi-Fi + Bluetooth) QCA6320/QCA6310 (802.11ad/60 GHz)
Touchscreen support	Capacitive panels via ext IC (I2C, SPI, and interrupts)
DVB support	Via external DVB device (SDC or TSIF)
Sensors	Snapdragon sensor core (dedicated Q6 low power island with 512 kB)
Configurable GPIOs	

Table 1-3   Summary of APQ8096SGE device features (cont.)

Feature	APQ8096SGE capability
Number of GPIO ports	150 – GPIO_0 to GPIO_149
Input configurations	Pullup, pulldown, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Boot sequence	1) Applications PBL 2) RPM 3) HLOS Emergency boot over USB 3.0
PLLs and clocks	■ Multiple clock regimes; watchdog & sleep timers ■ Inputs: 19.2 MHz CXO, CXO_2 ■ General-purpose outputs: M/N counter, PDM
Resource and power manager	■ Fundamental to power management ■ Key blocks: RPM core, Cortex M3, security controller, MPM ■ Efficiency via clock control, split-rail power collapse and voltage scaling; several low-power sleep modes
Others	Thermal sensors; modes & resets; peripheral subsystem
Chipset interface features	
Power management	2-line SPMI, plus other lines as needed through GPIOs
WCD audio codec	
SLIMbus	Highly MUXed, high-speed audio data plus status and control
Others	Status, control, and clock lines as needed through GPIOs
Wireless connectivity	
WLAN baseband data	PCIe
Bluetooth	PCM and UART interfaces
Fabrication technology and package	
Digital die	14 nm FinFET process for lower active power dissipation, faster peak CPU
NG PoP – small, thermally efficient package	994C MNSP: 15.6 × 15.0 × 0.64 mm (without memory device on top)
Bottom pad array of PoP	Same as 994-pad nanoscale package (994 NSP); 0.4 mm pitch
Top pad array of PoP	Same as 387-pad chipscale package (387 CSP); 0.5 mm pitch

1.3.3   Air interface features

Aspects of the air interface features are listed in Table 1-4 and Table 1-5

Table 1-4   Position location and navigation summary

Standard	Feature descriptions
Qualcomm Location with global navigation satellite system (GNSS) support	
GPS and GLONASS (GNSS), BeiDou/Compass, and Galileo	

Table 1-5   Wireless connectivity summary by standard

Standard	Feature descriptions
WLAN	
With QCA6174A	802.11ac, 2 × 2 MIMO
With QCA6320/QCA6310	WiGIG – 802.11ad, 60 GHz
Bluetooth	
With QCA6174A	Bluetooth 4.2 and earlier

1.4   Terms and acronyms

Table 1-6 defines terms and acronyms commonly used throughout this document.

Table 1-6   Terms and acronyms

Term	Definition
ADC	Analog-to-digital converter
AMR	Adaptive multi-rate codec
ANC	Active noise cancellation
ASF	Adaptive spatial filter
AVS	Adaptive voltage scaling
bps	Bits per second
BLSP	BAM-based low-speed peripheral
CAC	Chromatic aberration correction
CPHY	A MIPI Alliance physical layer standard. The C is a Roman numeral representing 100.
CSC	Clock source control
CSI	Camera serial interface
CSP	Chip scale package
DAC	Digital-to-analog converter
DDR	Double data rate
DVB	Digital video broadcast

Table 1-6   Terms and acronyms (cont.)

Term	Definition
DPHY	A MIPI Alliance physical layer standard. The D is a Roman numeral representing 500.
DRM	Digital Rights Management
DSC	Display stream compression
DSI	Display serial interface
DSP	Digital signal processor
EBI	External bus interface
eMMC	Embedded multimedia card
ETM	Embedded trace macrocell
EVRC	Enhanced variable rate coder
FB	Feedback
FDD	Frequency division duplex
FE	Front-end
GFX	Graphics
GLONASS	Global orbiting navigation satellite system
GNSS	Global navigation satellite system
GPIO	General-purpose input/output
GPS	Global positioning system
GSM	Global system for mobile communications
HB	High band
HDCP	High-bandwidth digital content protection
HDMI	High-definition multimedia interface
HEVC	High Efficiency Video Coding
HSIC	High-speed inter-chip
I^2C	Inter-integrated circuit
I^2S	Inter-IC sound
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group (ANSI/ICEEE Std. 1149.1-1990)
kbps	kilobits per second
LB	Low band
LBC	Linear battery charger
LCD	Liquid crystal display
LPA	Low-power audio
LPDDR	Low-power DDR
LSB	Defines whether the LSB is the least significant bit or least significant byte. All instances of LSB used in this manual are assumed to be LSByte, unless otherwise specified.
LSC	Lens shading correction

Table 1-6   Terms and acronyms (cont.)

Term	Definition
LTM	Local tone map
MB	MegaBytes
MBHC	Multiple button headset control
MI2S	Multiple I^{2}S
MIPI	Mobile industry processor interface
MMC	Multimedia card
MNSP	Package-on-package nano-scale package
MPM	Master power management
MSB	Defines whether the MSB is the most significant bit or most significant byte. All instances of MSB used in this manual are assumed to be MSByte, unless otherwise specified.
MSL	Moisture sensitivity level
NFC	Near field communicator
NSMD	Non-solder mask defined
NSP	Nanoscale package
OCIMEM	On chip internal memory
OLED	Organic light-emitting diode
OMA	Open Mobile Alliance
PA	Power amplifier
PBC	Programmable boot sequence
PBL	Primary boot loader
PCB	Printed circuit board
PCIe	Peripheral component interconnect express
PCM	Pulse-coded modulation
PDM	Pulse-density modulation
PDN	Power Distribution Network
PHY	Physical layer
PLL	Phase lock loop
PM	Power management
PMD	Product material declaration
PoP	Package-on-package
QCELP	Qualcomm code excited linear prediction
QFPROM	Qualcomm fuse programmable read-only memory
QTI	Qualcomm Technologies, Inc.
RFFE	RF front-end
RFIC	Radio frequency integrated circuit
RoHS	Restriction of hazardous substances

Table 1-6   Terms and acronyms (cont.)

Term	Definition
RPM	Resource power manager
SD	Secure digital
SDC	Secure digital controller
SDRAM	Synchronous dynamic random access memory
SFS	Secure file system
SIM	Subscriber identity module
SLIMbus	Serial Low-power Inter-chip Media Bus
SMT	Surface mount technology
SPI	Serial peripheral interface
SPMI	System power management interface
sps	Symbols per second (or samples per second)
SROT	Secure root of trust
SSC	Snapdragon sensor core
SVA	Snapdragon voice activation
SWD	Single Wire Debug
TCXO	Temperature-compensated crystal oscillator
TFT	Thin film transistor
TSIF	Transport stream interface
UART	Universal asynchronous receiver transmitter
UFS	Universal Flash Storage
UICC	Universal integrated circuit card
UIM	User identity module
USB	Universal serial bus
USIM	UMTS subscriber identity module
VDD	System supply voltage
VFE	Video front-end of camera firmware
WAN	Wide area network
WCD	WLP codec device
WCN	Wireless connectivity network
WGR	WLP GPS Receiver
WiGIG	Wireless Gigabit Alliance
WLAN	Wireless local area network
WLP	Wafer-level packaging
WMA	Windows media audio (file type)
XO	Crystal oscillator

1.5   Special marks

Table 1-7 defines special marks used in this document.

Table 1-7   Special marks

Mark	Definition
[ ]	Brackets ([ ]) following a pad, register, or bit name. These brackets enclose a range of numbers. For example, SDC1_DATA[7:4] indicates a range that is 4 bits in length, or DATA[7:0] refers to all eight DATA pads.
_N	A suffix of _N indicates an active low signal. For example, RESIN_N.
0x0000	Hexadecimal numbers are identified with an x in the number (for example, 0x0000). All numbers are decimal (base 10), unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number; for example, 0011 (binary).
|	A grey vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pad definitions

The APQ8096SGE is the lower device within a package-on-package (PoP) system, as illustrated and explained in Figure 2-1.
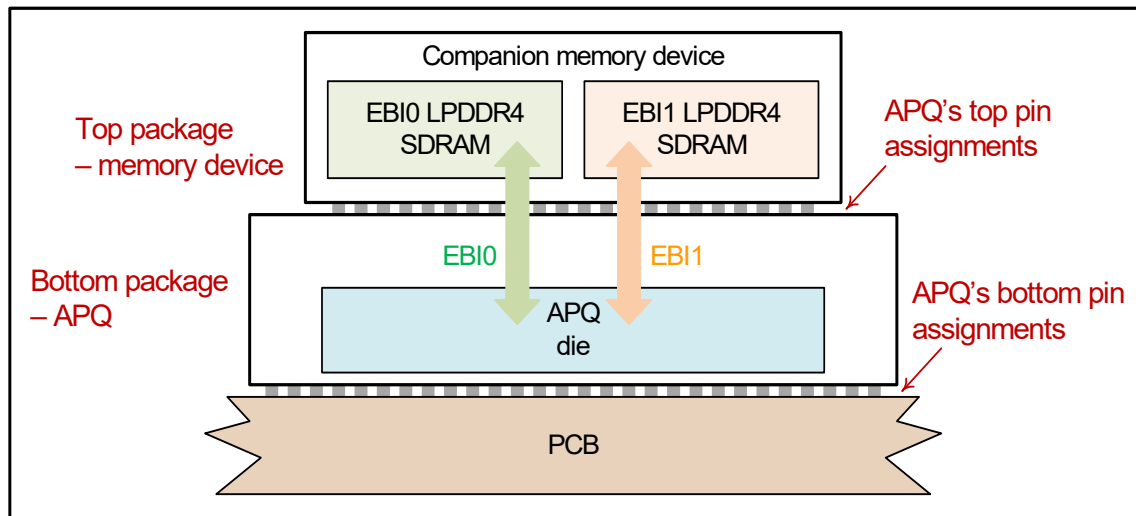
Figure 2-1   Package-on-package system pad assignments

Two sets of pad assignment details are presented in this chapter:

- APQ8096SGE bottom pads (Section 2.2)
- APQ8096SGE top pads (Section 2.3)

2.1 I/O parameter definitions

Table 2-1   I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant

Table 2-1   I/O description (pad type) parameters (cont.)

Symbol	Description
S	Schmitt trigger input
Z	High-impedance (high-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to the list of programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pulldown with programmable options following the colon (:) PU: nppdkp = default pullup with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pullup device
PD	Contains an internal pulldown device
Pad voltage groupings for baseband circuits	
P1	Pad group 1 (EBI pads); tied to VDD_P1 pins (1.1 V only)
P2	Pad group 2 (SDC2); tied to VDD_P2 pins (1.8 V or 2.95 V)
P3	Pad group 3 (peripherals); tied to VDD_P3 pins (1.8 V only)
P5	Pad group 5 (UIM1); tied to VDD_P5 pins (1.8 V or 2.95 V)
P6	Pad group 6 (UIM2); tied to VDD_P6 pins (1.8 V or 2.95 V)
P7	Pad group 7 (SDC1); tied to VDD_P7 pins (1.8 V only)
P9	Pad group 9 (CXO_2 and QREFS_REXT); tied to VDD_P9 pins (1.8 V only)
P10	Pad group 10 (UFS_CLK and UFS_RESET); tied to VDD_P10 pins (1.2 V only)
P11	Pad group 11 (CXO); tied to VDD_P11 pins (1.8 V only)
P12	Pad group 12 (SSC); tied to VDD_P12 pins (1.8 V only)
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_MIPI_CSI (1.8 V only)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_MIPI_DSI (1.8 V only)

Table 2-1   I/O description (pad type) parameters (cont.)

Symbol	Description
Output current drive strength	
EBI pads	Pads for EBI are tailored for 1.1 V interfaces and are source terminated. See Chapter 3 (Section 3.7) for more details.
3.0 V (H) pads	Programmable drive strength, 2–8 mA in 2 mA steps.
1.8 V UIM pads	Programmable drive strength for 1.8 V UIM pads, 2 to 16 mA in 2 mA steps.
Others [1]	Programmable drive strength, 2–16 mA in 2 mA steps.

1. Digital pads other than EBI pads, high-voltage tolerant pads, or 1.8 V UIM pads.

2.2   Pad assignments – APQ bottom

2.2.1   Pad map – APQ bottom

The APQ8096SGE uses the 994B MNSP package; its bottom surface is equivalent to the 994 NSP. See Chapter 4 for package details, and Section 2.3 for information about the top pad assignments. A high-level view of the bottom pad assignments is shown in Figure 2-3. The pins are colored to indicate which function type they support, as defined in Figure 2-2.

Connectivity	Chipset interfaces	GPIOs	Internal functions	Memory support
Multimedia	Ground	DNC, NC, or RSVD	Power	
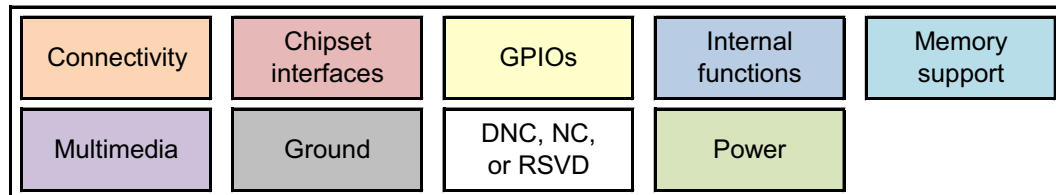
Figure 2-2   APQ8096SGE bottom pad assignments – legend

The text within Figure 2-3 is difficult to read when viewing an 8½" × 11" hard copy. Other viewing options are available:

- Print that one page on a 11" × 17" sheet.

- View the graphic soft copy and zoom in – the resolution is sufficient for comfortable reading.

- Download the *APQ8096 Pin Assignments* (LM80-P2751-2) – this Microsoft Excel spreadsheet lists all APQ8096SGE pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.
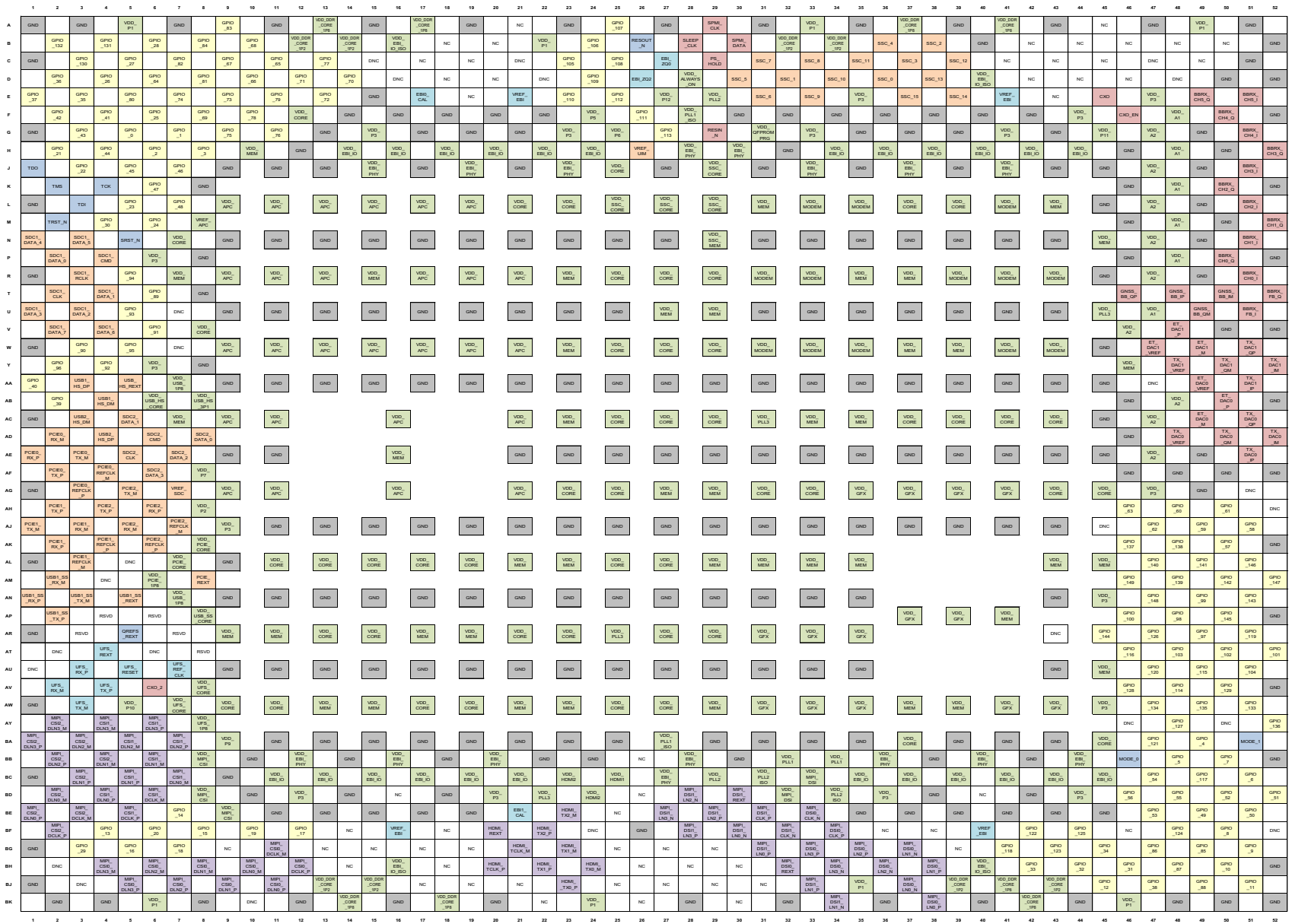
Figure 2-3 High-level view APQ8096SGE bottom pad assignments (from above, through package)

2.2.2 Pad descriptions – APQ bottom

Descriptions of bottom pins are presented in the following tables, organized by functional group:

Table 2-3 Memory support functions

Table 2-4 Multimedia functions

Table 2-5 Connectivity functions

Table 2-7 Internal functions

Table 2-10 Chipset interface functions

Table 2-11 General-purpose input/output ports

Table 2-12 No connection, do not connect, and reserved pins

Table 2-13 Power supply pins

Table 2-14 Ground pins

Table 2-2   Boot configuration GPIOs

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AK50	FORCED_USB_BOOT	GPIO_57	P3	DI B-PD:nppukp	Forced USB boot Configurable I/O
AT52	WDOG_DISABLE	GPIO_101	P3	DI B-PD:nppukp	Watchdog disable Configurable I/O
AT50	BOOT_CONFIG_1	GPIO_102	P3	DI B-PD:nppukp	fast_boot_select bit 0 (configure external boot device) Configurable I/O
AT48	BOOT_CONFIG_2	GPIO_103	P3	DI B-PD:nppukp	fast_boot_select bit 1 (configure external boot device) Configurable I/O
AU51	BOOT_CONFIG_3	GPIO_104	P3	DI B-PD:nppukp	fast_boot_select bit 2 (configure external boot device) Configurable I/O
AV48	BOOT_CONFIG_4	GPIO_114	P3	DI B-PD:nppukp	fast_boot_select bit 3 (configure external boot device) Configurable I/O
AB2	ALL_USE_SERIAL_NUM	GPIO_39	P3	DI B-PD:nppukp	Selects the serial number Configurable I/O
V6	MSA_PK_HASH_IN_FUSE	GPIO_91	P3	DI B-PD:nppukp	Public key hash from fuses for MSA boot segment selected Configurable I/O
Y4	MSA_AUTH_EN	GPIO_92	P3	DI B-PD:nppukp	Selects authentication enable for MSA segments Configurable I/O
U5	AP_PK_HASH_IN_FUSE	GPIO_93	P3	DI B-PD:nppukp	Public key hash from fuse for applications boot segment selected Configurable I/O
Y2	AP_AUTH_EN	GPIO_96	P3	DI B-PD:nppukp	Selects authentication enable for applications segments Configurable I/O
AN49	FORCE_MSA_AUTH_EN	GPIO_99	P3	DI B-PD:nppukp	Force authentication enable for MSA segments Configurable I/O

1.   See Table 2-1 for parameter and acronym definitions.
2.   The boot configuration function of the above GPIOs is sampled at the rising edge of RESOUT_N deassertion.

Table 2-3   Pad descriptions – memory support functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	**Type**	
EBI					
E17	EBI0_CAL	–	–	AI	EBI0 LPDDR4 calibration resistor
BE21	EBI1_CAL	–	–	AI	EBI1 LPDDR4 calibration resistor
E21, E41, BF16, BF40	VREF_EBI	–	–	AI	EBI LPDDR4 DQ and CA reference voltage
C27	EBI_ZQ0	–	–	AI	EBI LPDDR4 ZQ resistor for lower x16 memory
D26	EBI_ZQ2	–	–	AI	EBI LPDDR4 ZQ resistor for upper x16 memory
Universal flash storage (UFS) interface – supports high-density storage					
AU3	UFS_RX_P	–	–	AI	UFS receive – plus
AV2	UFS_RX_M	–	–	AI	UFS receive – minus
AV4	UFS_TX_P	–	–	AO	UFS transmit – plus
AW3	UFS_TX_M	–	–	AO	UFS transmit – minus
AU7	UFS_REF_CLK	–	P10	DOZ-PD:nppukp	UFS reference clock
AU5	UFS_RESET	–	P10	DOZ-PD:nppukp	UFS reset
AT4	UFS_REXT	–	–	AI, AO	UFS external resistor
SDC1 is available for eMMC NAND flash – see Table 2-5					

1. See Table 2-1 for parameter and acronym definitions.

Table 2-4   Pad descriptions – multimedia functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
1 of 3 camera serial interfaces – MIPI_CSI0 – 4-lane differential (plus clock) or 3-lane trio					
BH12	MIPI_CSI0_DCLK_P	DNC	CSI –	AI –	MIPI CSI 0, differential clock – plus Do not connect when CSI0 is configured for CPHY
BG11	MIPI_CSI0_DCLK_M	MIPI_CSI0_TLN0_A	CSI CSI	AI AI, AO	MIPI CSI 0, differential clock – minus MIPI CSI 0, trio lane 0 – A
BJ11	MIPI_CSI0_DLN0_P	MIPI_CSI0_TLN0_B	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 0 – plus MIPI CSI 0, trio lane 0 – B
BH10	MIPI_CSI0_DLN0_M	MIPI_CSI0_TLN0_C	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 0 – minus MIPI CSI 0, trio lane 0 – C
BJ9	MIPI_CSI0_DLN1_P	MIPI_CSI0_TLN1_A	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 1 – plus MIPI CSI 0, trio lane 1 – A
BH8	MIPI_CSI0_DLN1_M	MIPI_CSI0_TLN1_B	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 1 – minus MIPI CSI 0, trio lane 1 – B
BJ7	MIPI_CSI0_DLN2_P	MIPI_CSI0_TLN1_C	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 2 – plus MIPI CSI 0, trio lane 1 – C
BH6	MIPI_CSI0_DLN2_M	MIPI_CSI0_TLN2_A	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 2 – minus MIPI CSI 0, trio lane 2 – A
BJ5	MIPI_CSI0_DLN3_P	MIPI_CSI0_TLN2_B	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 3 – plus MIPI CSI 0, trio lane 2 – B
BH4	MIPI_CSI0_DLN3_M	MIPI_CSI0_TLN2_C	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 3 – minus MIPI CSI 0, trio lane 2 – C
2 of 3 camera serial interfaces – MIPI_CSI1 – 4-lane differential (plus clock) or 3-lane trio					
BE5	MIPI_CSI1_DCLK_P	DNC	CSI –	AI –	MIPI CSI 1, differential clock – plus Do not connect when CSI1 is configured for CPHY
BD6	MIPI_CSI1_DCLK_M	MIPI_CSI1_TLN0_A	CSI CSI	AI AI, AO	MIPI CSI 1, differential clock – minus MIPI CSI 1, trio lane 0 – A
BD4	MIPI_CSI1_DLN0_P	MIPI_CSI1_TLN0_B	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 0 – plus MIPI CSI 1, trio lane 0 – B
BC7	MIPI_CSI1_DLN0_M	MIPI_CSI1_TLN0_C	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 0 – minus MIPI CSI 1, trio lane 0 – C
BC5	MIPI_CSI1_DLN1_P	MIPI_CSI1_TLN1_A	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 1 – plus MIPI CSI 1, trio lane 1 – A
BB6	MIPI_CSI1_DLN1_M	MIPI_CSI1_TLN1_B	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 1 – minus MIPI CSI 1, trio lane 1 – B
BA7	MIPI_CSI1_DLN2_P	MIPI_CSI1_TLN1_C	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 2 – plus MIPI CSI 1, trio lane 1 – C
BA5	MIPI_CSI1_DLN2_M	MIPI_CSI1_TLN2_A	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 2 – minus MIPI CSI 1, trio lane 2 – A
AY6	MIPI_CSI1_DLN3_P	MIPI_CSI1_TLN2_B	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 3 – plus MIPI CSI 1, trio lane 2 – B
AY4	MIPI_CSI1_DLN3_M	MIPI_CSI1_TLN2_C	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 3 – minus MIPI CSI 1, trio lane 2 – C

Table 2-4 Pad descriptions – multimedia functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
3 of 3 camera serial interfaces – MIPI_CSI2 – 4-lane differential (plus clock) or 3-lane trio					
BF2	MIPI_CSI2_DCLK_P	DNC	CSI –	AI –	MIPI CSI 2, differential clock – plus Do not connect when CSI2 is configured for CPHY
BE3	MIPI_CSI2_DCLK_M	MIPI_CSI2_TLN0_A	CSI CSI	AI AI, AO	MIPI CSI 2, differential clock – minus MIPI CSI 2, trio lane 0 – A
BE1	MIPI_CSI2_DLN0_P	MIPI_CSI2_TLN0_B	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 0 – plus MIPI CSI 2, trio lane 0 – B
BD2	MIPI_CSI2_DLN0_M	MIPI_CSI2_TLN0_C	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 0 – minus MIPI CSI 2, trio lane 0 – C
BC3	MIPI_CSI2_DLN1_P	MIPI_CSI2_TLN1_A	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 1 – plus MIPI CSI 2, trio lane 1 – A
BB4	MIPI_CSI2_DLN1_M	MIPI_CSI2_TLN1_B	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 1 – minus MIPI CSI 2, trio lane 1 – B
BB2	MIPI_CSI2_DLN2_P	MIPI_CSI2_TLN1_C	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 2 – plus MIPI CSI 2, trio lane 1 – C
BA3	MIPI_CSI2_DLN2_M	MIPI_CSI2_TLN2_A	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 2 – minus MIPI CSI 2, trio lane 2 – A
BA1	MIPI_CSI2_DLN3_P	MIPI_CSI2_TLN2_B	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 3 – plus MIPI CSI 2, trio lane 2 – B
AY2	MIPI_CSI2_DLN3_M	MIPI_CSI2_TLN2_C	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 3 – minus MIPI CSI 2, trio lane 2 – C
Camera-related timing					
BF4	CAM_MCLK0	GPIO_13	P3	DO B-PD:nppukp	Camera master clock 0 Configurable I/O
BE7	CAM_MCLK1	GPIO_14	P3	DO B-PD:nppukp	Camera master clock 1 Configurable I/O
BF8	CAM_MCLK2	GPIO_15	P3	DO B-PD:nppukp	Camera master clock 2 Configurable I/O
BG5	CAM_MCLK3	GPIO_16	P3	DO B-PD:nppukp	Camera master clock 3 Configurable I/O
1 of 2 display serial interfaces – 4-lane MIPI_DSI0					
BF34	MIPI_DSI0_CLK_P	–	DSI	AO	MIPI display serial interface 0 clock – positive
BE33	MIPI_DSI0_CLK_N	–	DSI	AO	MIPI display serial interface 0 clock – negative
BG33	MIPI_DSI0_LN3_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 3 – positive
BH34	MIPI_DSI0_LN3_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 3 – negative
BG35	MIPI_DSI0_LN2_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 2 – positive
BH36	MIPI_DSI0_LN2_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 2 – negative
BH38	MIPI_DSI0_LN1_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 1 – positive
BG37	MIPI_DSI0_LN1_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 1 – negative
BK38	MIPI_DSI0_LN0_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 0 – positive
BJ37	MIPI_DSI0_LN0_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 0 – negative
BH32	MIPI_DSI0_REXT	–	DSI	AI, AO	MIPI DSI1 external calibration resistor
2 of 2 display serial interfaces – 4-lane MIPI_DSI1					
BE31	MIPI_DSI1_CLK_P	–	DSI	AO	MIPI display serial interface 1 clock – positive

Table 2-4   Pad descriptions – multimedia functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BF32	MIPI_DSI1_CLK_N	–	DSI	AO	MIPI display serial interface 1 clock – negative
BF28	MIPI_DSI1_LN3_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 3 – positive
BE27	MIPI_DSI1_LN3_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 3 – negative
BE29	MIPI_DSI1_LN2_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 2 – positive
BD28	MIPI_DSI1_LN2_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 2 – negative
BJ33	MIPI_DSI1_LN1_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 1 – positive
BK34	MIPI_DSI1_LN1_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 1 – negative
BG31	MIPI_DSI1_LN0_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 0 – positive
BF30	MIPI_DSI1_LN0_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 0 – negative
BD30	MIPI_DSI1_REXT	–	DSI	AI, AO	MIPI DSI0 external calibration resistor
High-definition multimedia interface (HDMI)					
BH20	HDMI_TCLK_P	–	–	AO	HDMI differential clock – plus
BG21	HDMI_TCLK_M	–	–	AO	HDMI differential clock – minus
BF22	HDMI_TX2_P	–	–	AO	HDMI differential transmit 2 – plus
BE23	HDMI_TX2_M	–	–	AO	HDMI differential transmit 2 – minus
BH22	HDMI_TX1_P	–	–	AO	HDMI differential transmit 1 – plus
BG23	HDMI_TX1_M	–	–	AO	HDMI differential transmit 1 – minus
BJ23	HDMI_TX0_P	–	–	AO	HDMI differential transmit 0 – plus
BH24	HDMI_TX0_M	–	–	AO	HDMI differential transmit 0 – minus
BF20	HDMI_REXT	–	–	AI, AO	HDMI external calibration resistor
BH46	HDMI_CEC	GPIO_31	P3	B B-PU:nppdkp	HDMI consumer electronics control Configurable I/O
BH44	HDMI_DDC_CLK	GPIO_32	P3	B B-PU:nppdkp	HDMI display data channel – clock Configurable I/O
BH42	HDMI_DDC_DATA	GPIO_33	P3	B B-PU:nppdkp	HDMI display data channel – data Configurable I/O
BG45	HDMI_HOT_PLUG_DET	GPIO_34	P3	DI B-PD:nppukp	HDMI hot plug detect Configurable I/O
M4	HDMI_RCV_DET	GPIO_30	P3	DO B-PD:nppukp	HDMI receive detection Configurable I/O

Also see Table 2-5 for connectivity ports that are used for multimedia applications:

Audio – SLIMbus, I2S, MI2S, PCM; DVB – TSIF, SDC; controls – I^{2}C, SPI

1.   See Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. See Table 2-11 for a list of all supported functions for each GPIO.

Table 2-5   Pad descriptions – connectivity functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
Super-speed USB 3.0 (USB_SS)					
AN1	USB1_SS_RX_P	–	–	AI	USB super-speed receive – plus
AM2	USB1_SS_RX_M	–	–	AI	USB super-speed receive – minus
AP2	USB1_SS_TX_P	–	–	AO	USB super-speed transmit – plus
AN3	USB1_SS_TX_M	–	–	AO	USB super-speed transmit – minus
AN5	USB1_SS_REXT	–	–	AI, AO	USB super-speed – external resistor
1 of 2 high-speed USB 2.0 (USB1_HS)					
AA3	USB1_HS_DP	–	–	AI, AO	USB high-speed 1 data – plus
AB4	USB1_HS_DM	–	–	AI, AO	USB high-speed 1 data – minus
AA5	USB_HS_REXT	–	–	AI	USB high-speed data – external resistor
2 of 2 high-speed USB 2.0 (USB2_HS)					
AD4	USB2_HS_DP	–	–	AI, AO	USB high-speed 2 data – plus
AC3	USB2_HS_DM	–	–	AI, AO	USB high-speed 2 data – minus
Secure digital controller interfaces – common to all					
AG7	VREF_SDC	–	–	AI	Reference for SDC I/O pads
Secure digital controller 1 (SDC1) interface – supports eMMC NAND					
V2	SDC1_DATA_7	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 7
V4	SDC1_DATA_6	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 6
N3	SDC1_DATA_5	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 5
N1	SDC1_DATA_4	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 4
U1	SDC1_DATA_3	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 3
U3	SDC1_DATA_2	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 2
T4	SDC1_DATA_1	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 1
P2	SDC1_DATA_0	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 0
P4	SDC1_CMD	–	P7	B-PD:nppukp	Secure digital controller 1 command
T2	SDC1_CLK	–	P7	B-NP:pdpukp	Secure digital controller 1 clock
R3	SDC1_RCLK	–	P7	DI-PD:nppukp	Secure digital controller 1 return clock.
Secure digital controller 2 (SDC2) interface – supports dual-voltage SD 3.0					
AA1	SD_WRITE_PROTECT	GPIO_40	P3	DI B-PD:nppukp	Secure digital card write protection Configurable I/O
APQ8096SGE does not include a secure digital controller 3 (SDC3) interface					
Secure digital controller 4 (SDC4) interface – supports SDIO					
Y4	SDC4_DATA_3	GPIO_92	P3	B B-PD:nppukp	Secure digital controller 4 data bit 3 Configurable I/O
R5	SDC4_DATA_2	GPIO_94	P3	B B-PD:nppukp	Secure digital controller 4 data bit 2 Configurable I/O
W5	SDC4_DATA_1	GPIO_95	P3	B B-PD:nppukp	Secure digital controller 4 data bit 1 Configurable I/O
Y2	SDC4_DATA_0	GPIO_96	P3	B B-PD:nppukp	Secure digital controller 4 data bit 0 Configurable I/O

Table 2-5   Pad descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
V6	SDC4_CMD GPIO_91		P3	B B-PD:nppukp	Secure digital controller 4 command Configurable I/O
U5	SDC4_CLK GPIO_93		P3	DO B-PD:nppukp	Secure digital controller 4 clock Configurable I/O
Peripheral component interconnect express 0 (PCIe0) interface					
AE1	PCIE0_RX_P	–	–	AI	PCIe 0 receive – plus
AD2	PCIE0_RX_M	–	–	AI	PCIe 0 receive – minus
AF2	PCIE0_TX_P	–	–	AO	PCIe 0 transmit – plus
AE3	PCIE0_TX_M	–	–	AO	PCIe 0 transmit – minus
AG3	PCIE0_REF_CLK_P	–	–	AO	PCIe 0 reference clock – plus
AF4	PCIE0_REF_CLK_M	–	–	AO	PCIe 0 reference clock – minus
AM8	PCIE_REXT	–	–	AI, AO	PCIe external resistor
D2	PCIE0_CLKREQ_N GPIO_36		P3	DI B-PU:nppdkp	PCIe 0 clock request Configurable I/O
E3	PCIE0_RST_N GPIO_35		P3	DO B-PD:nppukp	PCIe 0 reset Configurable I/O
Peripheral component interconnect express 1 (PCIe1) interface					
AK2	PCIE1_RX_P	–	–	AI	PCIe 1 receive – plus
AJ3	PCIE1_RX_M	–	–	AI	PCIe 1 receive – minus
AH2	PCIE1_TX_P	–	–	AO	PCIe 1 transmit – plus
AJ1	PCIE1_TX_M	–	–	AO	PCIe 1 transmit – minus
AK4	PCIE1_REF_CLK_P	–	–	AO	PCIe 1 reference clock – plus
AL3	PCIE1_REF_CLK_M	–	–	AO	PCIe 1 reference clock – minus
B4	PCIE1_CLKREQ_N GPIO_131		P3	DI B-PU:nppdkp	PCIe 1 clock request Configurable I/O
C3	PCIE1_RST_N GPIO_130		P3	DO B-PD:nppukp	PCIe 1 reset Configurable I/O
Peripheral component interconnect express 2 (PCIe2) interface					
AH6	PCIE2_RX_P	–	–	AI	PCIe 2 receive – plus
AJ5	PCIE2_RX_M	–	–	AI	PCIe 2 receive – minus
AH4	PCIE2_TX_P	–	–	AO	PCIe 2 transmit – plus
AG5	PCIE2_TX_M	–	–	AO	PCIe 2 transmit – minus
AK6	PCIE2_REF_CLK_P	–	–	AO	PCIe 2 reference clock – plus
AJ7	PCIE2_REF_CLK_M	–	–	AO	PCIe 2 reference clock – minus
AU49	PCIE2_CLKREQ_N GPIO_115		P3	DI B-PU:nppdkp	PCIe 2 clock request Configurable I/O
AV48	PCIE2_RST_N GPIO_114		P3	DO B-PD:nppukp	PCIe 2 reset Configurable I/O
Snapdragon sensor core (SSC) pins					
E37	SSC_15	SSC_UART_2_RX SSC_SPI_3_MISO	P12	B-PD:nppukp	Snapdragon sensor core bit 15 SSC UART #2 Receive SSC SPI #3 data master in/slave out

Table 2-5   Pad descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
E39	SSC_14	SSC_UART_2_TX SSC_SPI_3_MOSI	P12	B-PD:nppukp	Snapdragon sensor core bit 14 SSC UART #2 transmit SSC SPI #3 data master out/slave in
D38	SSC_13	SSC_UART_1_RX SSC_SPI_3_CS_N	P12	B-PD:nppukp	Snapdragon sensor core bit 13 SSC UART #1 receive SSC SPI #3 chip select
C39	SSC_12	SSC_UART_1_TX SSC_SPI_3_CLK	P12	B-PD:nppukp	Snapdragon sensor core bit 12 SSC UART #1 transmit SSC SPI #3 clock
C35	SSC_11	SSC_SPI_1_MISO	P12	B-PD:nppukp	Snapdragon sensor core bit 11 SSC SPI #1 data master in/slave out
D34	SSC_10	SSC_SPI_1_MOSI	P12	B-PD:nppukp	Snapdragon sensor core bit 10 SSC SPI #1 data master out/slave in
E33	SSC_9	SSC_SPI_1_CLK SSC_I2C_1_SCL	P12	B-PD:nppukp	Snapdragon sensor core bit 9 SSC SPI #1 clock SSC I^{2}C #1 serial clock
C33	SSC_8	SSC_SPI_1_CS_N SSC_I2C_1_SDA	P12	B-PD:nppukp	Snapdragon sensor core bit 8 SSC SPI #1 chip select 1 SSC I^{2}C #1 serial data
C31	SSC_7	SSC_UART_3_RX SSC_SPI_2_MISO	P12	B-PD:nppukp	Snapdragon sensor core bit 7 SSC UART #3 Receive SSC SPI #2 data master in/slave out
E31	SSC_6	SSC_UART_3_TX SSC_SPI_2_MOSI	P12	B-PD:nppukp	Snapdragon sensor core bit 6 SSC UART #3 transmit SSC SPI #2 data master out/slave in
D30	SSC_5	SSC_I2C_2_SCL SSC_SPI_2_CLK	P12	B-PD:nppukp	Snapdragon sensor core bit 5 SSC I^{2}C #2 serial clock SSC SPI #2 clock
B36	SSC_4	SSC_I2C_2_SDA SSC_SPI_2_CS_N	P12	B-PD:nppukp	Snapdragon sensor core bit 4 SSC I^{2}C #2 serial data SSC SPI #2 chip select
C37	SSC_3	SSC_I2C_3_SCL	P12	B-PD:nppukp	Snapdragon sensor core bit 3 SSC I^{2}C #3 serial clock
B38	SSC_2	SSC_I2C_3_SDA	P12	B-PD:nppukp	Snapdragon sensor core bit 2 SSC I^{2}C #3 serial data
D32	SSC_1	–	P12	B-PD:nppukp	Snapdragon sensor core bit 1 SSC power enable
D36	SSC_0	SSC_SPI_1_CS1_N SYNC_OUT	P12	B-PD:nppukp	Snapdragon sensor core bit 0 SSC SPI #1 chip select 2 Sync signal for sensors
Transport stream interface 1 (TSIF1)					
V6	TSIF1_DATA GPIO_91		P3	DI B-PD:nppukp	Transport stream interface 1 data Configurable I/O
T6	TSIF1_CLK GPIO_89		P3	DI B-PD:nppukp	Transport stream interface 1 clock Configurable I/O
AA1	TSIF1_ERROR GPIO_40		P3	DI B-PD:nppukp	Transport stream interface 1 error Configurable I/O
W3	TSIF1_EN GPIO_90		P3	DI B-PD:nppukp	Transport stream interface 1 enable Configurable I/O

Table 2-5   Pad descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2] Voltage	Type	Functional description
AB2	TSIF1_SYNC	GPIO_39	P3	DI B-PD:nppukp	Transport stream interface 1 sync Configurable I/O
Transport stream interface 2 (TSIF2)					
W5	TSIF2_DATA	GPIO_95	P3	DI B-PD:nppukp	Transport stream interface 2 data Configurable I/O
U5	TSIF2_CLK	GPIO_93	P3	DI B-PD:nppukp	Transport stream interface 2 clock Configurable I/O
Y2	TSIF2_SYNC	GPIO_96	P3	DI B-PD:nppukp	Transport stream interface 2 sync Configurable I/O
R5	TSIF2_EN	GPIO_94	P3	DI B-PD:nppukp	Transport stream interface 2 enable Configurable I/O
Y4	TSIF2_ERROR	GPIO_92	P3	DI B-PD:nppukp	Transport stream interface 2 error Configurable I/O
Audio I2S interface – speaker					
F8	SPKR_I2S_MCLK	GPIO_69	P3	DO B-PD:nppukp	Speaker I2S master clock Configurable I/O
D14	SPKR_I2S_SCK	GPIO_70	P3	B B-PD:nppukp	Speaker I2S bit clock Configurable I/O
D12	SPKR_I2S_DOUT	GPIO_71	P3	DO B-PD:nppukp	Speaker I2S data output Configurable I/O
E13	SPKR_I2S_WS	GPIO_72	P3	B B-PD:nppukp	Speaker I2S word select (L/R) Configurable I/O
Audio MI2S interface #1					
D6	MI2S_1_MCLK	GPIO_64	P3	DO B-PD:nppukp	MI2S #1 master clock Configurable I/O
C11	MI2S_1_SCK	GPIO_65	P3	B B-PD:nppukp	MI2S #1 bit clock Configurable I/O
D10	MI2S_1_WS	GPIO_66	P3	B B-PD:nppukp	MI2S #1 word select (L/R) Configurable I/O
C9	MI2S_1_D0	GPIO_67	P3	B B-PD:nppukp	MI2S #1 serial data channel 0 Configurable I/O
B10	MI2S_1_D1	GPIO_68	P3	B B-PD:nppukp	MI2S #1 serial data channel 1 Configurable I/O
Audio MI2S interface #2					
E11	MI2S_2_MCLK	GPIO_79	P3	DO B-PD:nppukp	MI2S #2 master clock Configurable I/O
E5	MI2S_2_SCK	GPIO_80	P3	B B-PD:nppukp	MI2S #2 bit clock Configurable I/O
D8	MI2S_2_WS	GPIO_81	P3	B B-PD:nppukp	MI2S #2 word select (L/R) Configurable I/O
C7	MI2S_2_D0	GPIO_82	P3	B B-PD:nppukp	MI2S #2 serial data channel 0 Configurable I/O
A9	MI2S_2_D1	GPIO_83	P3	B B-PD:nppukp	MI2S #2 serial data channel 1 Configurable I/O

Table 2-5   Pad descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
Audio MI2S interface #3					
E7	MI2S_3_MCLK	GPIO_74	P3	DO B-PD:nppukp	MI2S #3 master clock Configurable I/O
G9	MI2S_3_SCK	GPIO_75	P3	B B-PD:nppukp	MI2S #3 bit clock Configurable I/O
G11	MI2S_3_WS	GPIO_76	P3	B B-PD:nppukp	MI2S #3 word select (L/R) Configurable I/O
C13	MI2S_3_D0	GPIO_77	P3	B B-PD:nppukp	MI2S #3 serial data channel 0 Configurable I/O
F10	MI2S_3_D1	GPIO_78	P3	B B-PD:nppukp	MI2S #3 serial data channel 1 Configurable I/O
Audio MI2S interface #4					
AK50	MI2S_4_MCLK	GPIO_57	P3	DO B-PD:nppukp	MI2S #4 master clock Configurable I/O
AJ51	MI2S_4_SCK	GPIO_58	P3	B B-PD:nppukp	MI2S #4 bit clock Configurable I/O
AJ49	MI2S_4_WS	GPIO_59	P3	B B-PD:nppukp	MI2S #4 word select (L/R) Configurable I/O
AH48	MI2S_4_D0	GPIO_60	P3	B B-PD:nppukp	MI2S #4 serial data channel 0 Configurable I/O
AH50	MI2S_4_D1	GPIO_61	P3	B B-PD:nppukp	MI2S #4 serial data channel 1 Configurable I/O
AJ47	MI2S_4_D2	GPIO_62	P3	B B-PD:nppukp	MI2S #4 serial data channel 2 Configurable I/O
AH46	MI2S_4_D3	GPIO_63	P3	B B-PD:nppukp	MI2S #4 serial data channel 3 Configurable I/O
Audio PCM interface #1					
C11	PCM1_CLK	GPIO_65	P3	B B-PD:nppukp	Audio PCM clock (port 1) Configurable I/O
D10	PCM1_SYNC	GPIO_66	P3	B B-PD:nppukp	Audio PCM sync (port 1) Configurable I/O
C9	PCM1_DIN	GPIO_67	P3	B B-PD:nppukp	Audio PCM data input (port 1) Configurable I/O
B11	PCM1_DOUT	GPIO_68	P3	B B-PD:nppukp	Audio PCM data output (port 1) Configurable I/O
Audio PCM interface #2					
E5	PCM2_CLK	GPIO_80	P3	B B-PD:nppukp	Audio PCM clock (port 2) Configurable I/O
D8	PCM2_SYNC	GPIO_81	P3	B B-PD:nppukp	Audio PCM sync (port 2) Configurable I/O
C7	PCM2_DIN	GPIO_82	P3	B B-PD:nppukp	Audio PCM data input (port 2) Configurable I/O
A9	PCM2_DOUT	GPIO_83	P3	B B-PD:nppukp	Audio PCM data output (port 2) Configurable I/O
Audio PCM interface #3					

Table 2-5   Pad descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
G9	PCM3_CLK	GPIO_75	P3	B B-PD:nppukp	Audio PCM clock (port 3) Configurable I/O
G11	PCM3_SYNC	GPIO_76	P3	B B-PD:nppukp	Audio PCM sync (port 3) Configurable I/O
C13	PCM3_DIN	GPIO_77	P3	B B-PD:nppukp	Audio PCM data input (port 3) Configurable I/O
F10	PCM3_DOUT	GPIO_78	P3	B B-PD:nppukp	Audio PCM data output (port 3) Configurable I/O
Audio PCM interface #4					
AJ51	PCM4_CLK	GPIO_58	P3	B B-PD:nppukp	Audio PCM clock (port 4) Configurable I/O
AJ49	PCM4_SYNC	GPIO_59	P3	B B-PD:nppukp	Audio PCM sync (port 4) Configurable I/O
AH48	PCM4_DIN	GPIO_60	P3	B B-PD:nppukp	Audio PCM data input (port 4) Configurable I/O
AH50	PCM4_DOUT	GPIO_61	P3	B B-PD:nppukp	Audio PCM data output (port 4) Configurable I/O
Shared audio clock					
F8	AUDIO_REF_CLK	GPIO_69	P3	B B-PD:nppukp	Audio reference clock Configurable I/O
User interface module 1 (UIM1) interfaces – dual-voltage clock, data, and reset; not multiplexed with any BLSP pins					
D24	UIM1_DATA	GPIO_109	P5	B BH-PD:nppukp	UIM1 data (dual-voltage) Configurable I/O
E25	UIM1_PRESENT	GPIO_112	P3	DI B-PD:nppukp	UIM1 presence detection Configurable I/O
F26	UIM1_RESET	GPIO_111	P5	DO BH-PD:nppukp	UIM1 reset (dual-voltage) Configurable I/O
E23	UIM1_CLK	GPIO_110	P5	DO BH-PD:nppukp	UIM1 clock (dual-voltage) Configurable I/O
User interface module 2 (UIM2) interfaces – dual-voltage clock, data, and reset; not multiplexed with any BLSP pins					
C23	UIM2_DATA	GPIO_105	P6	B BH-PD:nppukp	UIM2 data (dual-voltage) Configurable I/O
C25	UIM2_PRESENT	GPIO_108	P3	DI B-PD:nppukp	UIM2 presence detection Configurable I/O
A25	UIM2_RESET	GPIO_107	P6	DO BH-PD:nppukp	UIM2 reset (dual-voltage) Configurable I/O
B24	UIM2_CLK	GPIO_106	P6	DO BH-PD:nppukp	UIM2 clock (dual-voltage) Configurable I/O
User interface module 3 (UIM3) interfaces – 1.8 V interface; multiplexed with BLSP9 pins					
BE49	UIM3_DATA	GPIO_49	P3	B B-PD:nppukp	UIM3 data Configurable I/O
BD50	UIM3_PRESENT	GPIO_52	P3	DI B-PD:nppukp	UIM3 presence detection Configurable I/O
BD52	UIM3_RESET	GPIO_51	P3	DO B-PD:nppukp	UIM3 reset Configurable I/O

Table 2-5   Pad descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
BE51	UIM3_CLK	GPIO_50	P3	DO B-PD:nppukp	UIM3 clock Configurable I/O
User interface module 4 (UIM4) interfaces – 1.8 V interface; multiplexed with BLSP11 pins					
AJ51	UIM4_DATA	GPIO_58	P3	B B-PD:nppukp	UIM4 data Configurable I/O
AH50	UIM4_PRESENT	GPIO_61	P3	DI B-PD:nppukp	UIM4 presence detection Configurable I/O
AH48	UIM4_RESET	GPIO_60	P3	DO B-PD:nppukp	UIM4 reset Configurable I/O
AJ49	UIM4_CLK	GPIO_59	P3	DO B-PD:nppukp	UIM4 clock Configurable I/O
Shared User interface module (UIM) functions					
H26	VREF_UIM		–	AI	Reference for UIM I/O pads
G27	UIM_BATT_ALARM	GPIO_113	P3	DI B-PD:nppukp	UIM battery alarm Configurable I/O
BAM-based low-speed peripheral interface 1 – see Table 2-6 for application-specific pad assignments					
G5	BLSP1_3	GPIO_0	P3	B B-PD:nppukp	BLSP #1 bit 3; SPI, UART, or UIM Configurable I/O
G7	BLSP1_2	GPIO_1	P3	B B-PD:nppukp	BLSP #1 bit 2; SPI, UART, or UIM Configurable I/O
H6	BLSP1_1	GPIO_2	P3	B B-PD:nppukp	BLSP #1 bit 1; SPI, UART, or I^{2}C Configurable I/O
H8	BLSP1_0	GPIO_3	P3	B B-PD:nppukp	BLSP #1 bit 0; SPI, UART, or I^{2}C Configurable I/O
BAM-based low-speed peripheral interface 2 – see Table 2-6 for application-specific pad assignments					
F4	BLSP2_3	GPIO_41	P3	B B-PD:nppukp	BLSP #2 bit 3; SPI, UART, or UIM Configurable I/O
F2	BLSP2_2	GPIO_42	P3	B B-PD:nppukp	BLSP #2 bit 2; SPI, UART, or UIM Configurable I/O
G3	BLSP2_1	GPIO_43	P3	B B-PD:nppukp	BLSP #2 bit 1; SPI, UART, or I^{2}C Configurable I/O
H4	BLSP2_0	GPIO_44	P3	B B-PD:nppukp	BLSP #2 bit 0; SPI, UART, or I^{2}C Configurable I/O
BAM-based low-speed peripheral interface 3 – see Table 2-6 for application-specific pad assignments					
J5	BLSP3_3	GPIO_45	P3	B B-PD:nppukp	BLSP #3 bit 3; SPI, UART, or UIM Configurable I/O
J7	BLSP3_2	GPIO_46	P3	B B-PD:nppukp	BLSP #3 bit 2; SPI, UART, or UIM Configurable I/O
K6	BLSP3_1	GPIO_47	P3	B B-PD:nppukp	BLSP#3 bit 1; SPI, UART, or I^{2}C Configurable I/O
L7	BLSP3_0	GPIO_48	P3	B B-PD:nppukp	BLSP #3 bit 0; SPI, UART, or I^{2}C Configurable I/O
BAM-based low-speed peripheral interface 4 – see Table 2-6 for application-specific pad assignments					
C11	BLSP4_3	GPIO_65	P3	B B-PD:nppukp	BLSP #4 bit 3; SPI, UART, or UIM Configurable I/O

Table 2-5   Pad descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
D10	BLSP4_2	GPIO_66	P3	B B-PD:nppukp	BLSP #4 bit 2; SPI, UART, or UIM Configurable I/O
C9	BLSP4_1	GPIO_67	P3	B B-PD:nppukp	BLSP #4 bit 1; SPI, UART, or I^{2}C Configurable I/O
B10	BLSP4_0	GPIO_68	P3	B B-PD:nppukp	BLSP #4 bit 0; SPI, UART, or I^{2}C Configurable I/O
BAM-based low-speed peripheral interface 5 – see Table 2-6 for application-specific pad assignments					
D8	BLSP5_3	GPIO_81	P3	B B-PD:nppukp	BLSP #5 bit 3; SPI, UART, or UIM Configurable I/O
C7	BLSP5_2	GPIO_82	P3	B B-PD:nppukp	BLSP #5 bit 2; SPI, UART, or UIM Configurable I/O
A9	BLSP5_1	GPIO_83	P3	B B-PD:nppukp	BLSP #5 bit 1; SPI, UART, or I^{2}C Configurable I/O
B8	BLSP5_0	GPIO_84	P3	B B-PD:nppukp	BLSP #5 bit 0; SPI, UART, or I^{2}C Configurable I/O
BAM-based low-speed peripheral interface 6 – see Table 2-6 for application-specific pad assignments					
F6	BLSP6_3	GPIO_25	P3	B B-PD:nppukp	BLSP #6 bit 3; SPI, UART, or UIM Configurable I/O
D4	BLSP6_2	GPIO_26	P3	B B-PD:nppukp	BLSP #6 bit 2; SPI, UART, or UIM Configurable I/O
C5	BLSP6_1	GPIO_27	P3	B B-PD:nppukp	BLSP #6 bit 1; SPI, UART, or I^{2}C Configurable I/O
B6	BLSP6_0	GPIO_28	P3	B B-PD:nppukp	BLSP #6 bit 0; SPI, UART, or I^{2}C Configurable I/O
BAM-based low-speed peripheral interface 7 – see Table 2-6 for application-specific pad assignments					
BE47	BLSP7_3	GPIO_53	P3	B B-PD:nppukp	BLSP #7 bit 3; SPI, UART, or UIM Configurable I/O
BC47	BLSP7_2	GPIO_54	P3	B B-PD:nppukp	BLSP #7 bit 2; SPI, UART, or UIM Configurable I/O
BD48	BLSP7_1	GPIO_55	P3	B B-PD:nppukp	BLSP #7 bit 1; SPI, UART, or I^{2}C Configurable I/O
BD46	BLSP7_0	GPIO_56	P3	B B-PD:nppukp	BLSP #7 bit 0; SPI, UART, or I^{2}C Configurable I/O
BAM-based low-speed peripheral interface 8 – see Table 2-6 for application-specific pad assignments					
BA49	BLSP8_3	GPIO_4	P3	B B-PD:nppukp	BLSP #8 bit 3; SPI, UART, or UIM Configurable I/O
BB48	BLSP8_2	GPIO_5	P3	B B-PD:nppukp	BLSP #8 bit 2; SPI, UART, or UIM Configurable I/O
BC51	BLSP8_1	GPIO_6	P3	B B-PD:nppukp	BLSP #8 bit 1; SPI, UART, or I^{2}C Configurable I/O
BB50	BLSP8_0	GPIO_7	P3	B B-PD:nppukp	BLSP #8 bit 0; SPI, UART, or I^{2}C Configurable I/O
BAM-based low-speed peripheral interface 9 – see Table 2-6 for application-specific pad assignments					
BE49	BLSP9_3	GPIO_49	P3	B B-PD:nppukp	BLSP #9 bit 3; SPI, UART, or UIM Configurable I/O

Table 2-5 Pad descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
BE51	BLSP9_2	GPIO_50	P3	B B-PD:nppukp	BLSP #9 bit 2; SPI, UART, or UIM Configurable I/O
BD52	BLSP9_1	GPIO_51	P3	B B-PD:nppukp	BLSP #9 bit 1; SPI, UART, or I^{2}C Configurable I/O
BD50	BLSP9_0	GPIO_52	P3	B B-PD:nppukp	BLSP #9 bit 0; SPI, UART, or I^{2}C Configurable I/O
BAM-based low-speed peripheral interface 10 – see Table 2-6 for application-specific pad assignments					
BF50	BLSP10_3	GPIO_8	P3	B B-PD:nppukp	BLSP #10 bit 3; SPI, UART, or UIM Configurable I/O
BG51	BLSP10_2	GPIO_9	P3	B B-PD:nppukp	BLSP #10 bit 2; SPI, UART, or UIM Configurable I/O
BH50	BLSP10_1	GPIO_10	P3	B B-PD:nppukp	BLSP #10 bit 1; SPI, UART, or I^{2}C Configurable I/O
BJ51	BLSP10_0	GPIO_11	P3	B B-PD:nppukp	BLSP #10 bit 0; SPI, UART, or I^{2}C Configurable I/O
BAM-based low-speed peripheral interface 11 – see Table 2-6 for application-specific pad assignments					
AJ51	BLSP11_3	GPIO_58	P3	B B-PD:nppukp	BLSP #11 bit 3; SPI, UART, or UIM Configurable I/O
AJ49	BLSP11_2	GPIO_59	P3	B B-PD:nppukp	BLSP #11 bit 2; SPI, UART, or UIM Configurable I/O
AH48	BLSP11_1	GPIO_60	P3	B B-PD:nppukp	BLSP #11 bit 1; SPI, UART, or I^{2}C Configurable I/O
AH50	BLSP11_0	GPIO_61	P3	B B-PD:nppukp	BLSP #11 bit 0; SPI, UART, or I^{2}C Configurable I/O
BAM-based low-speed peripheral interface 12 – see Table 2-6 for application-specific pad assignments					
BG49	BLSP12_3	GPIO_85	P3	B B-PD:nppukp	BLSP #12 bit 3; SPI, UART, or UIM Configurable I/O
BG47	BLSP12_2	GPIO_86	P3	B B-PD:nppukp	BLSP #12 bit 2; SPI, UART, or UIM Configurable I/O
BH48	BLSP12_1	GPIO_87	P3	B B-PD:nppukp	BLSP #12 bit 1; SPI, UART, or I^{2}C Configurable I/O
BJ49	BLSP12_0	GPIO_88	P3	B B-PD:nppukp	BLSP #12 bit 0; SPI, UART, or I^{2}C Configurable I/O
Serial peripheral interface (SPI) extra chip selects (supplements BLSP ports configured for SPI protocol) signals [1]					
W3	BLSP1_SPI_CS1_N	GPIO_90	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP #1 Configurable I/O
M6	BLSP1_SPI_CS2A_N	GPIO_24	P3	DO-Z B-PD:nppukp	Chip select 2A for SPI on BLSP #1 Configurable I/O
B6	BLSP1_SPI_CS2B_N	GPIO_28	P3	DO-Z B-PD:nppukp	Chip select 2B for SPI on BLSP #1 Configurable I/O
C5	BLSP1_SPI_CS3A_N	GPIO_27	P3	DO-Z B-PD:nppukp	Chip select 3A for SPI on BLSP #1 Configurable I/O
L5	BLSP1_SPI_CS3B_N	GPIO_23	P3	DO-Z B-PD:nppukp	Chip select 3B for SPI on BLSP #1 Configurable I/O
F6	BLSP2_SPI_CS1_N	GPIO_25	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP #2 Configurable I/O

Table 2-5   Pad descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
BG3	BLSP2_SPI_CS2_N	GPIO_29	P3	DO-Z B-PD:nppukp	Chip select 2 for SPI on BLSP #2 Configurable I/O
M4	BLSP2_SPI_CS3_N	GPIO_30	P3	DO-Z B-PD:nppukp	Chip select 3 for SPI on BLSP #2 Configurable I/O
BD52	BLSP10_SPI_CS1A_N	GPIO_51	P3	DO-Z B-PD:nppukp	Chip select 1A for SPI on BLSP #10 Configurable I/O
BE49	BLSP10_SPI_CS1B_N	GPIO_49	P3	DO-Z B-PD:nppukp	Chip select 1B for SPI on BLSP #10 Configurable I/O
BD50	BLSP10_SPI_CS2A_N	GPIO_52	P3	DO-Z B-PD:nppukp	Chip select 2A for SPI on BLSP #10 Configurable I/O
BE51	BLSP10_SPI_CS2B_N	GPIO_50	P3	DO-Z B-PD:nppukp	Chip select 2B for SPI on BLSP #10 Configurable I/O
BJ49	BLSP10_SPI_CS3_N	GPIO_88	P3	DO-Z B-PD:nppukp	Chip select 3 for SPI on BLSP #10 Configurable I/O

1. GPIO 'A/B' multiplexing is explained in Figure 2-4.
2. See Table 2-1 for parameter and acronym definitions.

> **NOTE:**   GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. See Table 2-11 for a list of all supported functions for each GPIO.

Twelve 4-pad sets of GPIOs are available as BAM-based low-speed peripheral (BLSP) interface ports that can be configured for UART, UIM, SPI, or I^{2}C operation. Detailed pad assignments are presented in Table 2-6 for each configuration.

Table 2-6   BLSP configurations

Option	Configuration	BLSP bit 3	BLSP bit 2	BLSP bit 1	BLSP bit 0
	BLSP1 GPIO pins =	GPIO_0	GPIO_1	GPIO_2	GPIO_3
	BLSP2 GPIO pins =	GPIO_41	GPIO_42	GPIO_43	GPIO_44
	BLSP3 GPIO pins =	GPIO_45	GPIO_46	GPIO_47	GPIO_48
	BLSP4 GPIO pins =	GPIO_65	GPIO_66	GPIO_67	GPIO_68
	BLSP5 GPIO pins =	GPIO_81	GPIO_82	GPIO_83	GPIO_84
	BLSP6 GPIO pins =	GPIO_25	GPIO_26	GPIO_27	GPIO_28
	BLSP7 GPIO pins =	GPIO_53	GPIO_54	GPIO_55	GPIO_56
	BLSP8 GPIO pins =	GPIO_4	GPIO_5	GPIO_6	GPIO_7
	BLSP9 GPIO pins =	GPIO_49	GPIO_50	GPIO_51	GPIO_52
	BLSP10 GPIO pins =	GPIO_8	GPIO_9	GPIO_10	GPIO_11
	BLSP11 GPIO pins =	GPIO_58	GPIO_59	GPIO_60	GPIO_61
	BLSP12 GPIO pins =	GPIO_85	GPIO_86	GPIO_87	GPIO_88
1	4-pad UART	UART_TX DO 4-pad UART transmit data	UART_RX DI 4-pad UART receive data	UART_CTS_N DI 4-pad UART clear-to-send	UART_RFR_N DO 4-pad UART ready-for-receive
2	2-pad UART + 2-pad I^{2}C	UART_TX DO 2-pad UART transmit data	UART_RX DI 2-pad UART receive data	I2C_SDA B I2C serial data	I2C_SCL B I2C serial clock
3	4-pad SPI	SPI_DATA_MOSI B 4-pad SPI master out/slave in	SPI_DATA_MISO B 4-pad SPI master in/slave out	SPI_CS_N B 4-pad SPI chip select	SPI_CLK B 4-pad SPI clock
4	2-pad UIM + 2-pad I^{2}C	UIM_DATA B UIM data	UIM_CLK DO UIM clock	I2C_SDA B I^{2}C serial data	I2C_SCL B I^{2}C serial clock
5	2-pad UIM + 2 GPIOs	UIM_DATA B UIM data	UIM_CLK DO UIM clock	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O
6	2 GPIOs + 2-pad I^{2}C	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	I2C_SDA B I^{2}C serial data	I2C_SCL B I^{2}C serial clock
7	4 GPIOs	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O
	The three rows within shaded cells list the: 1) pad function; 2) pad type; and 3) functional description.				

As noted throughout these pad definition tables, GPIO assignments must be done carefully to avoid conflicts, and to ensure that the desired functionality is achieved. For GPIOs that can be used as BLSPs, three additional factors must be considered when making functional assignments:

1. BLSP11 has additional GPIO multiplex options for UART and I^{2}C functions:

   □ BLSP11 UART transmit data is also available on GPIO_100

   □ BLSP11 UART receive data is also available on GPIO_101

   □ BLSP11 I^{2}C serial data is also available on GPIO_102

   □ BLSP11 I^{2}C serial clock is also available on GPIO_103

2. Extra chip selects (output only) are available when certain BLSPs are used for serial peripheral interface (SPI):

   □ BLSP1 has extra CS1, CS2A, CS2B, CS3A, and CS3B for its SPI.

   □ BLSP2 has extra CS1, CS2, and CS3 for its SPI.

   □ BLSP10 has extra CS1A, CA1B, CS2A, CS2B, and CS3 for its SPI.

3. Two UIM ports are multiplexed with BLSP pins:

   □ UIM3 is multiplexed with BLSP9.

   □ UIM4 is multiplexed with BLSP11.

4. BLSPs that are configured for SPI or I^{2}C or UART functionality require data mover access to achieve their throughput rates. In any BLSP, the SPI and I^{2}C share the same FIFO/ADM CRCI interface and the UART/UIM share the same FIFO and ADM CRCI interface.

5. I^{2}C can use only BLSP bits [0] and [1]. UIM can use only BLSP bits [2] and [3]. UART_RX and UART_TX are also only available on bits [2] and [3], as shown in Table 2-6. These rules apply across all 12 BLSPs.
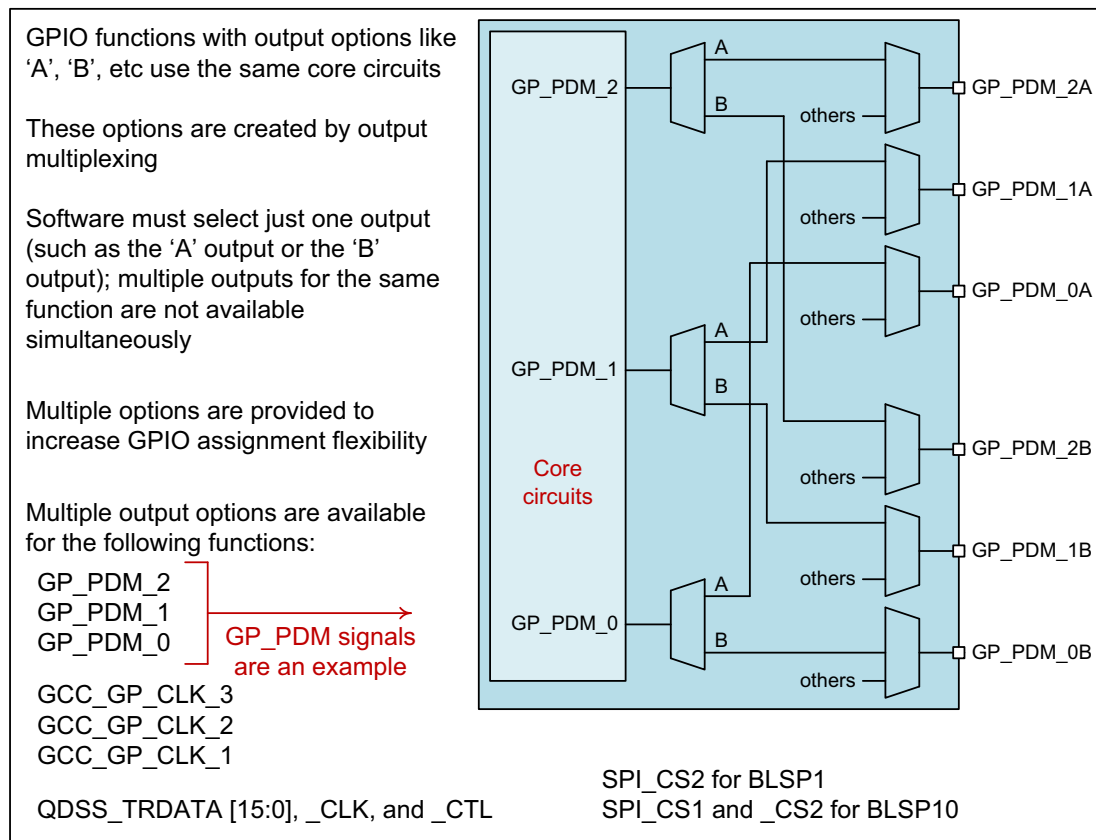
Figure 2-4   GPIO 'A/B' multiplexing

Table 2-7   Pad descriptions – internal functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
Clocks and related signals [1]					
Also see Table 2-10 for clock and related functions that interface with the PMIC (SLEEP_CLK, CXO, CXO_EN)					
AR5	QREFS_REXT	–	–	AI, A0	External resistor for on-die clocking
E25	GP_CLK0	GPIO_112	P3	DO B-PD:nppukp	General-purpose clock 0 output Configurable I/O
G27	GP_CLK1	GPIO_113	P3	DO B-PD:nppukp	General-purpose clock 1 output Configurable I/O
BG3	GP_MN	GPIO_29	P3	DO B-PD:nppukp	General-purpose M/N:D counter output Configurable I/O
W5	GP_PDM_0A	GPIO_95	P3	DO B-PD:nppukp	General-purpose PDM output 0 A Configurable I/O
BC47	GP_PDM_0B	GPIO_54	P3	DO B-PD:nppukp	General-purpose PDM output 0 B Configurable I/O
BG47	GP_PDM_1A	GPIO_86	P3	DO B-PD:nppukp	General-purpose PDM output 1 A Configurable I/O
BF50	GP_PDM_1B	GPIO_8	P3	DO B-PD:nppukp	General-purpose PDM output 1 B Configurable I/O
E11	GP_PDM_2A	GPIO_79	P3	DO B-PD:nppukp	General-purpose PDM output 2 A Configurable I/O
AH46	GP_PDM_2B	GPIO_63	P3	DO B-PD:nppukp	General-purpose PDM output 2 B Configurable I/O
Resets and mode controls – see the list of APQ8096SGE pins (Table 2-8) that can wake up the device (thereby supporting MPM)					
Also see the boot configuration pins listed in Table 2-2 Also see Table 2-10 for reset and mode-control functions that interface with the PMIC (RESIN_N, PS_HOLD)					
BA51	MODE_1	–	P3	DIS-PD	Mode control bit 1 – unconnected for native mode
BB46	MODE_0	–	P3	DIS-PD	Mode control bit 0 – unconnected for native mode
B26	RESOUT_N	–	P3	DO	Reset output

Table 2-7   Pad descriptions – internal functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
JTAG interface					
K4	TCK	–	P3	DI PU	JTAG clock input
L3	TDI	–	P3	DI PU:nppukp	JTAG data input
J1	TDO	–	P3	DO-Z	JTAG data output
K2	TMS	–	P3	DI PU:nppukp	JTAG mode select input
M2	TRST_N	–	P3	DI PD	JTAG reset

1. GPIO 'A/B' multiplexing is explained in Figure 2-4.
2. See Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. See Table 2-11 for a list of all supported functions for each GPIO.

Table 2-8   APQ8096SGE wakeup pins for APQ master power management (MPM)

Pad #	Pad name	Pad characteristics [1]		Additional wakeup function description
		Voltage	Type	
G7	GPIO_1	P3	B-PD:nppukp	General-purpose wakeup
BB48	GPIO_5	P3	B-PD:nppukp	General-purpose wakeup
BG51	GPIO_9	P3	B-PD:nppukp	General-purpose wakeup
BJ51	GPIO_11	P3	B-PD:nppukp	General-purpose wakeup
J3	GPIO_22	P3	B-PD:nppukp	General-purpose wakeup
M6	GPIO_24	P3	B-PD:nppukp	General-purpose wakeup
D4	GPIO_26	P3	B-PD:nppukp	General-purpose wakeup
BG45	GPIO_34	P3	B-PD:nppukp	General-purpose wakeup
D2	GPIO_36	P3	B-PU:nppdkp	General-purpose wakeup
E1	GPIO_37	P3	B-PD:nppukp	PCIe0 wakeup
BJ47	GPIO_38	P3	B-PD:nppukp	General-purpose wakeup
AA1	GPIO_40	P3	B-PD:nppukp	General-purpose wakeup
F2	GPIO_42	P3	B-PD:nppukp	General-purpose wakeup
J7	GPIO_46	P3	B-PD:nppukp	General-purpose wakeup
BE51	GPIO_50	P3	B-PD:nppukp	General-purpose wakeup
BE47	GPIO_53	P3	B-PD:nppukp	General-purpose wakeup
BC47	GPIO_54	P3	B-PD:nppdkp	General-purpose wakeup
BD46	GPIO_56	P3	B-PD:nppukp	General-purpose wakeup
AK50	GPIO_57	P3	B-PD:nppukp	General-purpose wakeup
AJ51	GPIO_58	P3	B-PD:nppukp	SSC_IRQ_0 interrupt

Table 2-8   APQ8096SGE wakeup pins for APQ master power management (MPM) (cont.)

Pad #	Pad name	Pad characteristics [1]		Additional wakeup function description
		Voltage	Type	
AJ49	GPIO_59	P3	B-PD:nppukp	SSC_IRQ_1 interrupt
AH48	GPIO_60	P3	B-PD:nppukp	SSC_IRQ_2 interrupt
AH50	GPIO_61	P3	B-PD:nppukp	SSC_IRQ_3 interrupt
AJ47	GPIO_62	P3	B-PD:nppukp	SSC_IRQ_4 interrupt
AH46	GPIO_63	P3	B-PD:nppukp	SSC_IRQ_5 interrupt
D6	GPIO_64	P3	B-PD:nppukp	General-purpose wakeup
D10	GPIO_66	P3	B-PD:nppukp	General-purpose wakeup
D12	GPIO_71	P3	B-PD:nppukp	General-purpose wakeup
E9	GPIO_73	P3	B-PD:nppukp	General-purpose wakeup
C13	GPIO_77	P3	B-PD:nppukp	General-purpose wakeup
F10	GPIO_78	P3	B-PD:nppukp	SSC_IRQ_6 interrupt
E11	GPIO_79	P3	B-PD:nppukp	SSC_IRQ_7 interrupt
E5	GPIO_80	P3	B-PD:nppukp	SSC_IRQ_8 interrupt
C7	GPIO_82	P3	B-PD:nppukp	General-purpose wakeup
BG47	GPIO_86	P3	B-PD:nppukp	General-purpose wakeup
V6	GPIO_91	P3	B-PD:nppukp	General-purpose wakeup
Y4	GPIO_92	P3	B-PD:nppukp	General-purpose wakeup
W5	GPIO_95	P3	B-PD:nppukp	Secure digital card detect
AR49	GPIO_97	P3	B-PD:nppukp	General-purpose wakeup
AT52	GPIO_101	P3	B-PD:nppukp	General-purpose wakeup
AU51	GPIO_104	P3	B-PD:nppukp	General-purpose wakeup
B24	GPIO_106	P3	BH-PD:nppukp	General-purpose wakeup
C25	GPIO_108	P3	B-PD:nppukp	UIM2 presence detection
E23	GPIO_110	P3	BH-PD:nppukp	General-purpose wakeup
E25	GPIO_112	P3	B-PD:nppukp	UIM1 presence detection
G27	GPIO_113	P3	B-PD:nppukp	UIM battery alarm
AU49	GPIO_115	P3	B-PU:nppdkp	General-purpose wakeup
AT46	GPIO_116	P3	B-PD:nppukp	PCIe2 wakeup
BC49	GPIO_117	P3	B-PD:nppukp	SSC_IRQ_9 interrupt
BG41	GPIO_118	P3	B-PD:nppukp	SSC_IRQ_10 interrupt
AR51	GPIO_119	P3	B-PD:nppukp	SSC_IRQ_11 interrupt
AU47	GPIO_120	P3	B-PD:nppukp	SSC_IRQ_12 interrupt
BA47	GPIO_121	P3	B-PD:nppukp	SSC_IRQ_13 interrupt
BF42	GPIO_122	P3	B-PD:nppukp	SSC_IRQ_14 interrupt
BG43	GPIO_123	P3	B-PD:nppukp	SSC_IRQ_15 interrupt
BF48	GPIO_124	P3	B-PD:nppukp	SSC_IRQ_16 interrupt
BF44	GPIO_125	P3	B-PD:nppukp	SSC_IRQ_17 interrupt
AR47	GPIO_126	P3	B-PD:nppukp	General-purpose wakeup

Table 2-8   APQ8096SGE wakeup pins for APQ master power management (MPM) (cont.)

Pad #	Pad name	Pad characteristics [1]		Additional wakeup function description
		Voltage	Type	
AY48	GPIO_127	P3	B-PD:nppukp	General-purpose wakeup
AV50	GPIO_129	P3	B-PD:nppukp	General-purpose wakeup
B4	GPIO_131	P3	B-PU:nppdkp	General-purpose wakeup
B2	GPIO_132	P3	B-PD:nppukp	PCIe1 wakeup
AW51	GPIO_133	P3	B-PD:nppukp	General-purpose wakeup
AP50	GPIO_145	P3	B-PD:nppukp	General-purpose wakeup
T4	SDC1_DATA_1	P7	B-PD:nppukp	Secure digital controller 1 data bit 1
U1	SDC1_DATA_3	P7	B-PD:nppukp	Secure digital controller 1 data bit 3
AC5	SDC2_DATA_1	P2	BH-PD:nppukp	Secure digital controller 2 data bit 1
AF6	SDC2_DATA_3	P2	BH-PD:nppukp	Secure digital controller 2 data bit 3
AD6	SDC2_CMD	P2	BH-PD:nppukp	Secure digital controller 2 command

1.   See Table 2-1 for parameter and acronym definitions.

Table 2-9   MODE[1:0] settings

MODE[1:0]	Usage
00	Native mode
11	Boundary-scan mode
Others	Test modes

Table 2-10   Pad descriptions – chipset interface functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [3]		Functional description
			Voltage	Type	
WTRs – Rx baseband interfaces					
R51	BBRX_CH0_I	–	–	AI	Baseband receiver input, channel 0, in-phase
P50	BBRX_CH0_Q	–	–	AI	Baseband receiver input, channel 0, quadrature-phase
N51	BBRX_CH1_I	–	–	AI	Baseband receiver input, channel 1, in-phase
M52	BBRX_CH1_Q	–	–	AI	Baseband receiver input, channel 1, quadrature-phase
L51	BBRX_CH2_I	–	–	AI	Baseband receiver input, channel 2, in-phase
K50	BBRX_CH2_Q	–	–	AI	Baseband receiver input, channel 2, quadrature-phase
J51	BBRX_CH3_I	–	–	AI	Baseband receiver input, channel 3, in-phase
H52	BBRX_CH3_Q	–	–	AI	Baseband receiver input, channel 3, quadrature-phase
G51	BBRX_CH4_I	–	–	AI	Baseband receiver input, channel 4, in-phase
F50	BBRX_CH4_Q	–	–	AI	Baseband receiver input, channel 4, quadrature-phase
E51	BBRX_CH5_I	–	–	AI	Baseband receiver input, channel 5, in-phase
E49	BBRX_CH5_Q	–	–	AI	Baseband receiver input, channel 5, quadrature-phase
U51	BBRX_FB_I	–	–	AI	Baseband receiver input, Tx feed back, in-phase
T52	BBRX_FB_Q	–	–	AI	Baseband receiver input, Tx feed back, quadrature phase
Note: For the APQ8096SGE device, the BBRX interface is not available. The pins must be terminated.					
WTRs – GNSS Rx baseband interface					
T48	GNSS_BB_IP	–	–	AI	GNSS receiver baseband input, in-phase plus
T50	GNSS_BB_IM	–	–	AI	GNSS receiver baseband input, in-phase minus
T46	GNSS_BB_QP	–	–	AI	GNSS receiver baseband input, quadrature plus
U49	GNSS_BB_QM	–	–	AI	GNSS receiver baseband input, quadrature minus
WTRs – Tx baseband interfaces					
AE51	TX_DAC0_IP	–	–	AO	Transmitter DAC 0 output, in-phase plus
AD52	TX_DAC0_IM	–	–	AO	Transmitter DAC 0 output, in-phase minus
AC51	TX_DAC0_QP	–	–	AO	Transmitter DAC 0 output, quadrature plus
AD50	TX_DAC0_QM	–	–	AO	Transmitter DAC 0 output, quadrature minus
AD48	TX_DAC0_VREF	–	–	AI	Transmitter DAC 0 voltage reference
AA51	TX_DAC1_IP	–	–	AO	Transmitter DAC 1 output, in-phase plus
Y52	TX_DAC1_IM	–	–	AO	Transmitter DAC 1 output, in-phase minus
W51	TX_DAC1_QP	–	–	AO	Transmitter DAC 1 output, quadrature plus
Y50	TX_DAC1_QM	–	–	AO	Transmitter DAC 1 output, quadrature minus
Y48	TX_DAC1_VREF	–	–	AI	Transmitter DAC 1 voltage reference
Note: For the APQ8096SGE device, the TX_DAC interface is not available. The pins must be terminated.					
WTRs – GSM transmit phase adjust signals					
AW49	GSM_TX_PHASE_D1	GPIO_135	P3	DO B-PD:nppukp	GSM transmit phase adjust data bit 1 for WTR Configurable I/O
AW47	GSM_TX_PHASE_D0	GPIO_134	P3	DO B-PD:nppukp	GSM transmit phase adjust data bit 0 for WTR Configurable I/O
Note: For the APQ8096SGE device, the GSM_TX_PHASE function is not available. The pins can be used as general purpose GPIO pins.					

Table 2-10   Pad descriptions – chipset interface functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [3]		Functional description
			Voltage	Type	
PMIC interfaces					
B28	SLEEP_CLK	–	P3	DI	Sleep clock
E45	CXO	–	P11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
F46	CXO_EN	–	P3	DO	Core crystal oscillator enable
AV6	CXO_2	–	P9	DI	Core crystal oscillator 2 (analog 19.2 MHz system clock)
G29	RESIN_N	–	P3	DI	Reset input
B30	SPMI_DATA	–	P3	B	Slave and PBUS interface for PMICs – data
A29	SPMI_CLK	–	P3	DO	Slave and PBUS interface for PMICs – clock
C29	PS_HOLD	–	P3	DO	Power-supply hold signal to PMIC
QCA6174A WLAN/Bluetooth interfaces					
–	*See Table 2-5 for PCIe and UART interface details.*				
AP50	LTE_COEX_RX	GPIO_145	P3	DI B-PD:nppukp	UART Rx for LTE-WLAN coexistence Configurable I/O
AR45	LTE_COEX_TX	GPIO_144	P3	DO B-PD:nppukp	UART Tx for LTE-WLAN coexistence Configurable I/O
AN51	GNSS_TX_AGGRESSOR	GPIO_143	P3	DI B-PD:nppukp	Tx level which degrades GNSS receiver Configurable I/O
QCA6320/QCA6310 WiGIG interfaces					
–	*See Table 2-5 for PCIe interface details.*				
WCD9335 interfaces					
–	*See Table 2-5 for SLIMbus details; also for I²S and I²C connectivity ports that can be used as an alternative*				
WSA881x interfaces					
–	*See Table 2-5 for I²C interface details.*				
Qualcomm RF360 interfaces [1, 2]					
AB50	ET_DAC0_P	–	–	AO	Envelope tracking DAC0 output, plus
AC49	ET_DAC0_M	–	–	AO	Envelope tracking DAC0 output, minus
AA49	ET_DAC0_VREF	–	–	AI	Envelope tracking DAC0 output, voltage reference
V48	ET_DAC1_P	–	–	AO	Envelope tracking DAC1 output, plus
W49	ET_DAC1_M	–	–	AO	Envelope tracking DAC1 output, minus
W47	ET_DAC1_VREF	–	–	AI	Envelope tracking DAC1 output, voltage reference

1. For the APQ8096SGE device, the ET_DAC interface is not available. The pins must be terminated.
2. For the APQ8096SGE device, the RFFE function is not available. The pins can be used as general purpose GPIO.
3. See Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. See Table 2-11 for a list of all supported functions for each GPIO.

NOTE: System designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

□ GPIO configuration

– Input versus output

– Pull-up or pulldown

□ External connections

– Unused inputs

– Connections to high-impedance (tri-state) outputs

– Connections to external devices

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all APQ8096SGE GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

Table 2-11   Pad descriptions – general-purpose input/output ports

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AP50	GPIO_145	LTE_COEX_RX	P3	B-PD:nppukp DI	Configurable I/O UART Rx for LTE-WLAN coexistence
AR45	GPIO_144	LTE_COEX_TX	P3	B-PD:nppukp DO	Configurable I/O UART Tx for LTE-WLAN coexistence
AN51	GPIO_143	GNSS_TX_AGRESSOR	P3	B-PD:nppukp DI	Configurable I/O Tx level degrades GNSS receiver
AW49	GPIO_135	GSM_TX_PHASE_D1	P3	B-PD:nppukp DO	Configurable I/O GSM transmit phase adjust data bit 1 for WTR
AW47	GPIO_134	GSM_TX_PHASE_D0	P3	B-PD:nppukp DO	Configurable I/O GSM transmit phase adjust data bit 0 for WTR
B2	GPIO_132	–	P3	B-PD:nppukp	Configurable I/O
B4	GPIO_131	PCIE1_CLKREQ_N	P3	B-PU:nppdkp DI	Configurable I/O PCIe 1 clock request
C3	GPIO_130	PCIE1_RST_N	P3	B-PD:nppukp DO	Configurable I/O PCIe 1 reset
AR47	GPIO_126	–	P3	B-PD:nppukp	Configurable I/O
BF44	GPIO_125	–	P3	B-PD:nppukp	Configurable I/O
BF48	GPIO_124	–	P3	B-PD:nppukp	Configurable I/O
BG43	GPIO_123	–	P3	B-PD:nppukp	Configurable I/O
BF42	GPIO_122	–	P3	B-PD:nppukp	Configurable I/O
BA47	GPIO_121	–	P3	B-PD:nppukp	Configurable I/O
AU47	GPIO_120	–	P3	B-PD:nppukp	Configurable I/O
AR51	GPIO_119	–	P3	B-PD:nppukp	Configurable I/O
BG41	GPIO_118	–	P3	B-PD:nppukp	Configurable I/O
BC49	GPIO_117	–	P3	B-PD:nppukp	Configurable I/O

Table 2-11   Pad descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AT46	GPIO_116	PA_INDICATOR	P3	B-PD:nppukp DO	Configurable I/O PA transmit indicator
AU49	GPIO_115	PCIE2_CLKREQ_N	P3	B-PU:nppdkp DI	Configurable I/O PCIe 2 clock request
AV48	GPIO_114	PCIE2_RST_N	P3	B-PD:nppukp DO	Configurable I/O PCIe 2 reset
G27	GPIO_113	UIM_BATT_ALARM GP_CLK1	P3	B-PD:nppukp DI DO	Configurable I/O UIM battery alarm General purpose clock 1
E25	GPIO_112	UIM1_PRESENT GP_CLK0	P3	B-PD:nppukp DI DO	Configurable I/O UIM1 presence detection General purpose clock 0
F26	GPIO_111	UIM1_RESET	P5	BH-PD:nppukp DO	Configurable I/O UIM1 reset (dual-voltage)
E23	GPIO_110	UIM1_CLK	P5	BH-PD:nppukp DO	Configurable I/O UIM1 clock (dual-voltage)
D24	GPIO_109	UIM1_DATA	P5	BH-PD:nppukp B	Configurable I/O UIM1 data (dual-voltage)
C25	GPIO_108	UIM2_PRESENT	P3	B-PD:nppukp DI	Configurable I/O UIM2 presence detection
A25	GPIO_107	UIM2_RESET	P6	BH-PD:nppukp DO	Configurable I/O UIM2 reset (dual-voltage)
B24	GPIO_106	UIM2_CLK	P6	BH-PD:nppukp DO	Configurable I/O UIM2 clock (dual-voltage)
C23	GPIO_105	UIM2_DATA	P6	BH-PD:nppukp B	Configurable I/O UIM2 data (dual-voltage)
AT48	GPIO_103	BLSP11_I2C_SCL_B	P3	B-PD:nppukp B	Configurable I/O BLSP11_I2C_SCL_B (copy)
AT50	GPIO_102	BLSP11_I2C_SDA_B	P3	B-PD:nppukp B	Configurable I/O BLSP11_I2C_SDA_B (copy)
AT52	GPIO_101	BLSP11_UART_RX_B	P3	B-PD:nppukp DI	Configurable I/O BLSP11_UART_RX_B (copy)
AP46	GPIO_100	BLSP11_UART_TX_B	P3	B-PD:nppukp DO	Configurable I/O BLSP11_UART_TX_B (copy)
Y2	GPIO_96	TSIF2_SYNC SDC4_DATA_0	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 2 sync Secure digital controller 4 data bit 0
W5	GPIO_95	TSIF2_DATA SDC4_DATA_1 GP_PDM_0A	P3	B-PD:nppukp DI B DO	Configurable I/O Transport stream interface 2 data Secure digital controller 4 data bit 1 General-purpose PDM output 0 A
R5	GPIO_94	TSIF2_EN SDC4_DATA_2	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 2 enable Secure digital controller 4 data bit 2
U5	GPIO_93	TSIF2_CLK SDC4_CLK	P3	B-PD:nppukp DI DO	Configurable I/O Transport stream interface 2 clock Secure digital controller 4 clock

Table 2-11 Pad descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
Y4	GPIO_92	TSIF2_ERROR SDC4_DATA_3	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 2 error Secure digital controller 4 data bit 3
V6	GPIO_91	TSIF1_DATA SDC4_CMD	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 1 data Secure digital controller 4 command
W3	GPIO_90	TSIF1_EN BLSP1_SPI_CS1_N	P3	B-PD:nppukp DI DO-Z	Configurable I/O Transport stream interface 1 enable Chip select 1 for SPI on BLSP #1
T6	GPIO_89	TSIF1_CLK	P3	B-PD:nppukp DI	Configurable I/O Transport stream interface 1 clock
BJ49	GPIO_88	BLSP12_0 BLSP10_SPI_CS3_N	P3	B-PD:nppukp B DO-Z	Configurable I/O BLSP #12 bit 0; SPI, UART, or I^{2}C Chip select 3 for SPI on BLSP #10
BH48	GPIO_87	BLSP12_1	P3	B-PD:nppukp B	Configurable I/O BLSP #12, bit 1; SPI, UART, or I^{2}C
BG47	GPIO_86	BLSP12_2 GP_PDM_1A	P3	B-PD:nppukp B DO	Configurable I/O BLSP #12, bit 2; SPI, UART, or UIM General-purpose PDM 1 A output
BG49	GPIO_85	BLSP12_3	P3	B-PD:nppukp B	Configurable I/O BLSP #12, bit 3; SPI, UART, or UIM
B8	GPIO_84	BLSP5_0	P3	B-PD:nppukp B	Configurable I/O BLSP #5, bit 0; SPI, UART, or I^{2}C
A9	GPIO_83	BLSP5_1 MI2S_2_D1 PCM2_DOUT	P3	B-PD:nppukp B B B	Configurable I/O BLSP #5, bit 1; SPI, UART, or I^{2}C MI2S #2 serial data channel 1 Audio PCM data output (port 2)
C7	GPIO_82	BLSP5_2 MI2S_2_D0 PCM2_DIN	P3	B-PD:nppukp B B B	Configurable I/O BLSP #5, bit 2; SPI, UART, or UIM MI2S #2 serial data channel 0 Audio PCM data input (port 2)
D8	GPIO_81	BLSP5_3 MI2S_2_WS PCM2_SYNC	P3	B-PD:nppukp B B B	Configurable I/O BLSP #5, bit 3; SPI, UART, or UIM MI2S #2 word select (L/R) Audio PCM sync (port 2)
E5	GPIO_80	MI2S_2_SCK PCM2_CLK	P3	B-PD:nppukp B B	Configurable I/O MI2S #2 bit clock Audio PCM clock (port 2)
E11	GPIO_79	MI2S_2_MCLK GP_PDM_2A	P3	B-PD:nppukp DO DO	Configurable I/O MI2S #2 master clock General-purpose PDM 2 A output
F10	GPIO_78	MI2S_3_D1 PCM3_DOUT	P3	B-PD:nppukp B B	Configurable I/O MI2S #3 serial data channel 1 Audio PCM data output (port 3)
C13	GPIO_77	MI2S_3_D0 PCM3_DIN	P3	B-PD:nppukp B B	Configurable I/O MI2S #3 serial data channel 0 Audio PCM data input (port 3)
G11	GPIO_76	MI2S_3_WS PCM3_SYNC	P3	B-PD:nppukp B B	Configurable I/O MI2S #3 word select (L/R) Audio PCM sync (port 3)

Table 2-11   Pad descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
G9	GPIO_75	MI2S_3_SCK PCM3_CLK	P3	B-PD:nppukp B B	Configurable I/O MI2S #3 bit clock Audio PCM clock (port 3)
E7	GPIO_74	MI2S_3_MCLK	P3	B-PD:nppukp DO	Configurable I/O MI2S #3 master clock
E9	GPIO_73	–	P3	B-PD:nppukp	Configurable I/O
E13	GPIO_72	SPKR_I2S_WS	P3	B-PD:nppukp B	Configurable I/O Speaker I2S word select (L/R)
D12	GPIO_71	SPKR_I2S_DOUT	P3	B-PD:nppukp DO	Configurable I/O Speaker I2S data output
D14	GPIO_70	SPKR_I2S_SCK	P3	B-PD:nppukp B	Configurable I/O Speaker I2S bit clock
F8	GPIO_69	SPKR_I2S_MCLK AUDIO_REF_CLK	P3	B-PD:nppukp DO DI	Configurable I/O Speaker I2S master clock Audio reference clock
B10	GPIO_68	BLSP4_0 MI2S_1_D1 PCM1_DOUT	P3	B-PD:nppukp B B B	Configurable I/O BLSP #4, bit 0; SPI, UART, or I²C MI2S #1 serial data channel 1 Audio PCM data output (port 1)
C9	GPIO_67	BLSP4_1 MI2S_1_D0 PCM1_DIN	P3	B-PD:nppukp B B B	Configurable I/O BLSP #4, bit 1; SPI, UART, or I²C MI2S #1 serial data channel 0 Audio PCM data input (port 1)
D10	GPIO_66	BLSP4_2 MI2S_1_WS PCM1_SYNC	P3	B-PD:nppukp B B B	Configurable I/O BLSP #4, bit 2; SPI, UART, or UIM MI2S #1 word select (L/R) Audio PCM sync (port 1)
C11	GPIO_65	BLSP4_3 MI2S_1_SCK PCM1_CLK	P3	B-PD:nppukp B B B	Configurable I/O BLSP #4, bit 3; SPI, UART, or UIM MI2S #1 bit clock Audio PCM clock (port 1)
D6	GPIO_64	MI2S_1_MCLK	P3	B-PD:nppukp DO	Configurable I/O MI2S #1 master clock
AH46	GPIO_63	MI2S_4_D3 GP_PDM_2B	P3	B-PD:nppukp B DO	Configurable I/O MI2S #4 serial data channel 3 General-purpose PDM output 2 B
AJ47	GPIO_62	MI2S_4_D2	P3	B-PD:nppukp B	Configurable I/O MI2S #4 serial data channel 2
AH50	GPIO_61	BLSP11_0 MI2S_4_D1 PCM4_DOUT UIM4_PRESENT	P3	B-PD:nppukp B B B DI	Configurable I/O BLSP #11, bit 0; SPI, UART, or I²C MI2S #4 serial data channel 1 Audio PCM data output (port 4) UIM4 presence detection
AH48	GPIO_60	BLSP11_1 MI2S_4_D0 PCM4_DIN UIM4_RESET	P3	B-PD:nppukp B B B DO	Configurable I/O BLSP #11, bit 1; SPI, UART, or I²C MI2S #4 serial data channel 0 Audio PCM data input (port 4) UIM4 reset

Table 2-11   Pad descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AJ49	GPIO_59	BLSP11_2 MI2S_4_WS PCM4_SYNC UIM4_CLK	P3	B-PD:nppukp B B B DO	Configurable I/O BLSP #11, bit 2; SPI, UART, or UIM MI2S #4 word select (L/R) Audio PCM sync (port 4) UIM4 clock
AJ51	GPIO_58	BLSP11_3 MI2S_4_SCK PCM4_CLK UIM4_DATA	P3	B-PD:nppukp B B B B	Configurable I/O BLSP #11, bit 3; SPI, UART, or UIM MI2S #4 bit clock Audio PCM clock (port 4) UIM4 data
AK50	GPIO_57	MI2S_4_MCLK	P3	B-PD:nppukp DO	Configurable I/O MI2S #4 master clock
BD46	GPIO_56	BLSP7_0	P3	B-PD:nppukp B	Configurable I/O BLSP #7, bit 0; SPI, UART, or I^2C
BD48	GPIO_55	BLSP7_1	P3	B-PD:nppukp B	Configurable I/O BLSP #7, bit 1; SPI, UART, or I^2C
BC47	GPIO_54	BLSP7_2 GP_PDM_0B	P3	B-PD:nppukp B DO	Configurable I/O BLSP #7, bit 2; SPI, UART, or UIM General-purpose PDM output 0 B
BE47	GPIO_53	BLSP7_3	P3	B-PD:nppukp B	Configurable I/O BLSP #7, bit 3; SPI, UART, or UIM
BD50	GPIO_52	BLSP9_0 UIM3_PRESENT BLSP10_SPI_CS2A_N	P3	B-PD:nppukp B DI DO-Z	Configurable I/O BLSP #9, bit 0; SPI, UART, or I^2C UIM3 presence detection Chip select 2A for SPI on BLSP #10
BD52	GPIO_51	BLSP9_1 UIM3_RESET BLSP10_SPI_CS1A_N	P3	B-PD:nppukp B DO DO-Z	Configurable I/O BLSP #9, bit 1; SPI, UART, or I^2C UIM3 reset Chip select 1A for SPI on BLSP #10
BE51	GPIO_50	BLSP9_2 UIM3_CLK BLSP10_SPI_CS2B_N	P3	B-PD:nppukp B DO DO-Z	Configurable I/O BLSP #9, bit 2; SPI, UART, or UIM UIM3 clock Chip select 2B for SPI on BLSP #10
BE49	GPIO_49	BLSP9_3 UIM3_DATA BLSP10_SPI_CS1B_N	P3	B-PD:nppukp B B DO-Z	Configurable I/O BLSP #9, bit 3; SPI, UART, or UIM UIM3 data Chip select 1B for SPI on BLSP #10
L7	GPIO_48	BLSP3_0	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 0; SPI, UART, or I^2C
K6	GPIO_47	BLSP3_1	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 1; SPI, UART, or I^2C
J7	GPIO_46	BLSP3_2	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 2; SPI, UART, or UIM
J5	GPIO_45	BLSP3_3	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 3; SPI, UART, or UIM
H4	GPIO_44	BLSP2_0	P3	B-PD:nppukp B	Configurable I/O BLSP #2, bit 0; SPI, UART, or I^2C
G3	GPIO_43	BLSP2_1	P3	B-PD:nppukp B	Configurable I/O BLSP #2, bit 1; SPI, UART, or I^2C

Table 2-11   Pad descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
F2	GPIO_42	BLSP2_2	P3	B-PD:nppukp B	Configurable I/O BLSP #2, bit 2; SPI, UART, or UIM
F4	GPIO_41	BLSP2_3	P3	B-PD:nppukp B	Configurable I/O BLSP #2, bit 3; SPI, UART, or UIM
AA1	GPIO_40	SD_WRITE_PROTECT TSIF1_ERROR	P3	B-PD:nppukp DI DI	Configurable I/O Secure digital card write protection Transport stream interface 1 error
AB2	GPIO_39	TSIF1_SYNC	P3	B-PD:nppukp DI	Configurable I/O Transport stream interface 1 sync
BJ47	GPIO_38	–	P3	B-PD:nppukp	Configurable I/O
E1	GPIO_37	–	P3	B-PD:nppukp	Configurable I/O
D2	GPIO_36	PCIE0_CLKREQ_N	P3	B-PU:nppukp DI	Configurable I/O PCIe 0 clock request
E3	GPIO_35	PCIE0_RST_N	P3	B-PD:nppukp DO	Configurable I/O PCIe 0 reset
BG45	GPIO_34	HDMI_HOT_PLUG_DET	P3	B-PD:nppukp DI	Configurable I/O HDMI hot plug detect
BH42	GPIO_33	HDMI_DDC_DATA	P3	B-PU:nppdkp B	Configurable I/O HDMI display data channel – data
BH44	GPIO_32	HDMI_DDC_CLK	P3	B-PU:nppdkp B	Configurable I/O HDMI display data channel – clock
BH46	GPIO_31	HDMI_CEC	P3	B-PU:nppdkp B	Configurable I/O HDMI consumer electronics control
M4	GPIO_30	HDMI_RCV_DET BLSP2_SPI_CS3_N	P3	B-PD:nppukp DO DO-Z	Configurable I/O HDMI receive detection Chip select 3 for SPI on BLSP #2
BG3	GPIO_29	GP_MN BLSP2_SPI_CS2_N	P3	B-PD:nppukp DO DO-Z	Configurable I/O General-purpose M/N:D counter output Chip select 2 for SPI on BLSP #2
B6	GPIO_28	BLSP6_0 BLSP1_SPI_CS2B_N	P3	B-PD:nppukp B DO-Z	Configurable I/O BLSP #6, bit 0; SPI, UART, or I2C Chip select 2B for SPI on BLSP #1
C5	GPIO_27	BLSP6_1 BLSP1_SPI_CS3A_N	P3	B-PD:nppukp B DO-Z	Configurable I/O BLSP #6, bit 1; SPI, UART, or I2C Chip select 3A for SPI on BLSP #1
D4	GPIO_26	BLSP6_2	P3	B-PD:nppukp B	Configurable I/O BLSP #6, bit 2; SPI, UART, or UIM
F6	GPIO_25	BLSP6_3 BLSP2_SPI_CS1_N	P3	B-PD:nppukp B DO-Z	Configurable I/O BLSP #6, bit 3; SPI, UART, or UIM Chip select 1 for SPI on BLSP #2
M6	GPIO_24	BLSP1_SPI_CS2A_N	P3	B-PD:nppukp DO-Z	Configurable I/O Chip select 2A for SPI on BLSP #1
L5	GPIO_23	BLSP1_SPI_CS3B_N	P3	B-PD:nppukp DO	Configurable I/O Chip select 3B for SPI on BLSP #1
BG5	GPIO_16	CAM_MCLK3	P3	B-PD:nppukp DO	Configurable I/O Camera master clock 3
BF8	GPIO_15	CAM_MCLK2	P3	B-PD:nppukp DO	Configurable I/O Camera master clock 2

Table 2-11   Pad descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
BE7	GPIO_14	CAM_MCLK1	P3	B-PD:nppukp DO	Configurable I/O Camera master clock 1
BF4	GPIO_13	CAM_MCLK0	P3	B-PD:nppukp DO	Configurable I/O Camera master clock 0
BJ51	GPIO_11	BLSP10_0	P3	B-PD:nppukp B	Configurable I/O BLSP #10, bit 0; SPI, UART, or I^2C
BH50	GPIO_10	BLSP10_1	P3	B-PD:nppukp B	Configurable I/O BLSP #10, bit 1; SPI, UART, or I^2C
BG51	GPIO_9	BLSP10_2	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 2; SPI, UART, or UIM
BF50	GPIO_8	BLSP10_3 GP_PDM_1B	P3	B-PD:nppukp B DO	Configurable I/O BLSP #10, bit 3; SPI, UART, or UIM General-purpose PDM output 1 B
BB50	GPIO_7	BLSP8_0	P3	B-PD:nppukp B	Configurable I/O BLSP #8, bit 0; SPI, UART, or I^2C
BC51	GPIO_6	BLSP8_1	P3	B-PD:nppukp B	Configurable I/O BLSP #8, bit 1; SPI, UART, or I^2C
BB48	GPIO_5	BLSP8_2	P3	B-PD:nppukp B	Configurable I/O BLSP #8, bit 2; SPI, UART, or UIM
BA49	GPIO_4	BLSP8_3	P3	B-PD:nppukp B	Configurable I/O BLSP #8, bit 3; SPI, UART, or UIM
H8	GPIO_3	BLSP1_0	P3	B-PD:nppukp B	Configurable I/O BLSP #1, bit 0; SPI, UART, or I^2C
H6	GPIO_2	BLSP1_1	P3	B-PD:nppukp B	Configurable I/O BLSP #1, bit 1; SPI, UART, or I^2C
G7	GPIO_1	BLSP1_2	P3	B-PD:nppukp B	Configurable I/O BLSP #1, bit 2; SPI, UART, or UIM
G5	GPIO_0	BLSP1_3	P3	B-PD:nppukp B	Configurable I/O BLSP #1, bit 3; SPI, UART, or UIM

1. See Table 2-1 for parameter and acronym definitions.

Table 2-12   Pad descriptions – no connection, do not connect, and reserved pins

Pad #	Pad name	Functional description
C15, C21, C47, D16, D22, D48, U7, W7, AA47, AG51, AH52, AJ45, AL5, AM4, AR43, AT6, AU1, AT2, AY46, AY50, BF24, BF52, BH2, BJ3, BK10	DNC	Do not connect; connected internally, do not connect externally
A21, A45, B18, B20, B42, B44, B46, B48, B50, C17, C19, C41, C43, C45, C49, D18, D20, D42, D44, D46, E19, E43, BB26, BD16, BD26, BD40, BE25, BF14, BF18, BF36, BF38, BF46, BG9, BG13, BG15, BG17, BG19, BG25, BG27, BG29, BG39, BH14, BH18, BH26, BH28, BH30, BJ17, BJ19, BJ21, BJ25, BJ27, BJ29, BJ31, BK22, BK26, BK30	NC	No connect; not connected internally
AP4, AP6, AR3, AR7, AT8	RSVD	Reserved; connected internally for potential future use, do not connect externally

Table 2-13   Pad descriptions – power supply pads

Pad #	Pad name	Functional description
F48, H48, K48, M48, P48, U47	VDD_A1	Power for analog circuits – low voltage
G47, J47, L47, N47, R47, V46, AB48, AC47, AE47	VDD_A2	Power for analog circuits – high voltage
D28	VDD_ALWAYS_ON	Always-on power domain
L9, L11, L13, L15, L17, L19, R9, R11, R13, R17, R19, R21, W9, W11, W13, W15, W17, W19, W21, AC9, AC11, AC16, AC21, AG9, AG11, AG16, AG21	VDD_APC	Power for Kryo application processor
F12, J25, L21, L23, L37, L39, N7, R25, R27, R29, V8, W25, W27, W29, AC25, AC27, AC29, AC37, AC39, AC41, AC43, AG23, AG25, AG31, AG33, AG43, AG45, AL11, AL13, AL15, AL17, AL19, AL25, AL27, AR13, AR15, AR21, AR23, AR27, AR29, AW9, AW11, AW17, AW19, AW27, BA37, BA45	VDD_CORE	Power for digital core circuits
B12, B14, B32, B34, BJ13, BJ15, BJ39, BJ43	VDD_DDR_CORE_1P2	Power for PoP DDR memory core – 1.2V (top VDD_2)
A13, A17, A37, A41, BJ41, BK14, BK18, BK42	VDD_DDR_CORE_1P8	Power for PoP DDR memory core – 1.8 V (top VDD_1)
H14, H16, H18, H20, H22, H24, H34, H36, H38, H40, H42, H44, BC11, BC13, BC15, BC17, BC19, BC21, BC35, BC37, BC39, BC41, BC43, BC45	VDD_EBI_IO	Power for EBI I/O circuits
B16, D40, BH16, BH40	VDD_EBI_IO_ISO	Power for EBI I/O circuits that need isolated routing on the PCB
H28, H30, J15, J19, J23, J33, J37, J41, BB12, BB16, BB20, BB28, BB36, BB40, BB44, BC27	VDD_EBI_PHY	Power for EBI PHY circuits
AG35, AG37, AG39, AG41, AP37, AP39, AR31, AR33, AR35, AW31, AW33, AW35, AW41, AW43	VDD_GFX	Power for graphics
BC25	VDD_HDMI1	Power for HDMI circuits – low voltage
BC23, BD24	VDD_HDMI2	Power for HDMI circuits – high voltage
H10, L31, L43, N45, R7, R15, R23, R35, R37, U27, U29, W23, W37, W39, Y46, AC7, AC23, AC33, AC35, AE16, AG27, AG29, AL21, AL23, AL29, AL31, AL33, AL35, AL43, AL45, AP41, AR9, AR11, AR17, AR19, AU45, AW13, AW15, AW21, AW23, AW29, AW37, AW39	VDD_MEM	Power for on-chip memory
BB8, BD8, BE9	VDD_MIPI_CSI	Power for MIPI_CSI I/Os and circuits
BC33, BD32	VDD_MIPI_DSI	Reference for MIPI_DSI I/Os and circuits
L33, L35, L41, R31, R33, R39, R41, R43, W31, W33, W35, W41, W43	VDD_MODEM	Power for modem circuits, including the modem DSP
A5, A33, A49, B22, BJ35, BK6, BK24, BK46	VDD_P1	Power for pad group 1 – EBI and DDR I/O pads
AH8	VDD_P2	Power for pad group 2 – SDC2 pads
E35, E47, F44, G15, G23, G33, G41, P6, Y6, AG47, AJ9, AN45, AW45, BD12, BD20, BD36, BD44	VDD_P3	Power for pad group 3 – I/O pads
F24	VDD_P5	Power for pad group 5 – UIM1 pads
G25	VDD_P6	Power for pad group 6 – UIM2 pads
AF8	VDD_P7	Power for pad group 7 – SDC1 pads
BA9	VDD_P9	Power for pad group 9 – CXO_2 pad
AW5	VDD_P10	Power for pad group 10 – UFS pad
G45	VDD_P11	Power for pad group 11 – CXO pad
E27	VDD_P12	Power for pad group 12 – SSC pad
AM6	VDD_PCIE_1P8	Power for PCIe I/O circuitry
AK8, AL7	VDD_PCIE_CORE	Power for PCIe core circuitry
BB32, BB34	VDD_PLL1	Power for PLL circuits – 0.925 V

Table 2-13   Pad descriptions – power supply pads (cont.)

Pad #	Pad name	Functional description
F28, BA27	VDD_PLL1_ISO	Power for PLL circuits – 0.925 V that need isolated routing on the PCB
E29, BC29	VDD_PLL2	Power for PLL circuits – 1.250 V
BC31, BD34	VDD_PLL2_ISO	Power for PLL circuits – 1.250 V that need isolated routing on the PCB
U45, AC31, AR25, BD22	VDD_PLL3	Power for PLL circuits – 1.800 V
G31	VDD_QFPROM_PRG	Power for programming the QFPROM; otherwise, ground
J29, L25, L27, L29	VDD_SSC_CORE	Power for Snapdragon sensor core
N29	VDD_SSC_MEM	Power for Snapdragon sensor core memory
AY8	VDD_UFS_1P8	Power for UFS 1.8 V circuits
AV8, AW7	VDD_UFS_CORE	Power for UFS core circuits
AA7, AN7	VDD_USB_1P8	Power for USB HS1, HS2, and SS – low voltage
AB8	VDD_USB_HS_3P1	Power for USB HS1 and HS2 – high voltage
AB6	VDD_USB_HS_CORE	Power for USB digital core circuits – HS1, HS2
AP8	VDD_USB_SS_CORE	Power for USB digital core circuits – SS1
M8	VREF_APC	Reference voltage for Kryo application processor

Table 2-14   Pad descriptions – ground pads

Pad #	Pad name	Functional description
A1, A3, A7, A11, A15, A19, A23, A27, A31, A35, A39, A43, A47, A51, B40, B52, C1, C51, D50, D52, E15, F14, F16, F18, F20, F22, F30, F32, F34, F36, F38, F40, F42, F52, G1, G13, G17, G19, G21, G35, G37, G39, G43, G49, H12, H32, H46, H50, J9, J11, J13, J17, J21, J27, J31, J35, J39, J43, J45, J49, K8, K46, K52, L1, L45, L49, M46, M50, N9, N11, N13, N15, N17, N19, N21, N23, N25, N27, N31, N33, N35, N37, N39, N41, N43, N49, P8, P46, P52, R1, R45, R49, T8, U9, U11, U13, U15, U17, U19, U21, U23, U25, U31, U33, U35, U37, U39, U41, U43, V50, V52, W1, W45, Y8, AA9, AA11, AA13, AA15, AA17, AA19, AA21, AA23, AA25, AA27, AA29, AA31, AA33, AA35, AA37, AA39, AA41, AA43, AA45, AB46, AB52, AC1, AC45, AD46, AE9, AE11, AE21, AE23, AE25, AE27, AE29, AE31, AE33, AE35, AE37, AE39, AE41, AE43, AE45, AE49, AF46, AF48, AF50, AF52, AG1, AG49, AJ11, AJ13, AJ15, AJ17, AJ19, AJ21, AJ23, AJ25, AJ27, AJ29, AJ31, AJ33, AJ35, AJ37, AJ39, AJ41, AJ43, AK52, AL1, AL9, AN9, AN11, AN13, AN15, AN17, AN19, AN21, AN23, AN25, AN27, AN29, AN31, AN33, AN35, AN43, AP52, AR1, AU9, AU11, AU13, AU15, AU17, AU19, AU21, AU23, AU25, AU27, AU29, AU31, AU33, AU35, AU43, AV52, AW1, BA11, BA13, BA15, BA17, BA19, BA21, BA23, BA25, BA29, BA31, BA33, BA35, BA39, BA41, BA43, BB10, BB14, BB18, BB22, BB24, BB30, BB38, BB42, BB52, BC1, BC9, BD10, BD14, BD18, BD38, BD42, BE11, BE13, BE15, BE17, BE19, BE35, BE37, BE39, BE41, BE43, BE45, BF26, BG1, BH52, BJ1, BK2, BK4, BK8, BK12, BK16, BK20, BK28, BK32, BK36, BK40, BK44, BK48, BK50, BK52	GND	Ground

2.3   Pad assignments – APQ top

2.3.1   Pad map – APQ top

The APQ8096SGE is available in the 994B package-on-package nano-scale package (MNSP). Its top surface is implemented like a 387-pad chip-scale package (387 CSP). See Chapter 4 for package details, and Section 2.2 for information about the bottom pad assignments. A high-level view of the top pad assignments is shown in Figure 2-6. The pins are colored to indicate which function-type they support, as defined in Figure 2-5.

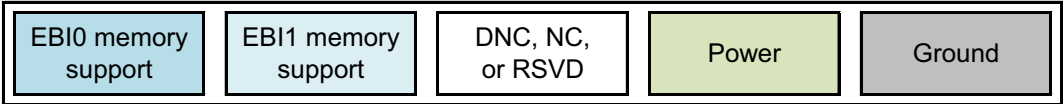| EBI0 memory support	EBI1 memory support	DNC, NC, or RSVD	Power	Ground

Figure 2-5   APQ8096SGE top pad assignments – legend

The text within Figure 2-6 is difficult to read when viewing an 8½" × 11" hard copy. Other viewing options are available and defined in Section 2.2.1.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	NC	VDD_2	GND	VDD_P1	VDD_1	VDD_2	EBI0_CA0_CS0_N	VDD_2	GND	VDD_2	VDD_P1	GND	VDD_P1	VDD_2	GND	VDD_2	VDD_P1	GND	VDD_P1	VDD_1	VDD_2	EBI0_CA1_CS0_N	VDD_2	GND	VDD_2	VDD_P1	GND	VDD_2	NC	A
B	VDD_1	EBI0_DQ_2	EBI0_DQS_0_T	EBI0_DQ_4	GND	EBI0_CA0_0	EBI0_CA0_CS1_N	EBI0_CA0_CK_T	EBI0_CA0_3	VDD_1	EBI0_DQ_13	EBI0_DQS_1_T	EBI0_DQ_11	VDD_1	ZQ2	VDD_1	EBI0_DQ_18	EBI0_DQS_2_T	EBI0_DQ_20	GND	EBI0_CA1_0	EBI0_CA1_CS1_N	EBI0_CA1_CK_T	EBI0_CA1_3	VDD_1	EBI0_DQ_29	EBI0_DQS_3_T	EBI0_DQ_27	VDD_1	B
C	EBI0_DQ_0	GND	EBI0_DQS_0_C	GND	EBI0_DQ_6	GND	VDD_2	EBI0_CA0_CK_C	VDD_2	EBI0_DQ_15	GND	EBI0_DQS_1_C	GND	EBI0_DQ_9	ZQ2	EBI0_DQ_16	GND	EBI0_DQS_2_C	GND	EBI0_DQ_22	GND	VDD_2	EBI0_CA1_CK_C	VDD_2	EBI0_DQ_31	GND	EBI0_DQS_3_C	GND	EBI0_DQ_25	C
D	VDD_P1	EBI0_DQ_3	VDD_P1	EBI0_DQ_5	VDD_P1	EBI0_CA0_1	EBI0_CA0_CKE_0	GND	EBI0_CA0_4	VDD_P1	EBI0_DQ_12	VDD_P1	EBI0_DQ_10	VDD_P1	ZQ0	VDD_P1	EBI0_DQ_19	VDD_P1	EBI0_DQ_21	VDD_P1	EBI0_CA1_1	EBI0_CA1_CKE_0	GND	EBI0_CA1_4	VDD_P1	EBI0_DQ_28	VDD_P1	EBI0_DQ_26	VDD_P1	D
E	EBI0_DQ_1	GND	EBI0_DM_0	EBI0_DQ_7	VDD_2	EBI0_CA0_CKE_1	EBI0_CA0_2	EBI0_CA0_5	EBI0_DQ_14	GND	EBI0_DM_1	EBI0_DQ_8	ZQ0	EBI0_DQ_17	GND	EBI0_DM_2	GND	EBI0_DQ_23	VDD_2	EBI0_CA1_CKE_1	EBI0_CA1_2	EBI0_CA1_5	EBI0_DQ_30	GND	EBI0_DM_3	GND	EBI0_DQ_24			E
F	GND	GND																										GND	GND	F
G	GND	GND																										GND	GND	G
H	GND	GND	DNC	DNC																								GND	GND	H
J	GND	GND	DNC	DNC																								GND	GND	J
K	GND	GND	DNC	DNC																								GND	GND	K
L	GND	GND																										GND	GND	L
M	GND	GND	DNC	DNC																								GND	GND	M
N	GND	GND	DNC	DNC																								GND	GND	N
P	GND	GND	DNC	DNC																								GND	GND	P
R	GND	GND																										GND	GND	R
T	GND	GND	DNC	DNC																								GND	GND	T
U	GND	GND																										GND	GND	U
V	GND	GND	DNC																									GND	GND	V
W	GND	GND	DNC	DNC																								GND	GND	W
Y	GND	GND	DNC	DNC																								GND	GND	Y
AA	GND	GND	DNC	DNC																								GND	GND	AA
AB	GND	GND																										GND	GND	AB
AC	GND	GND																										GND	GND	AC
AD	GND	GND																										GND	GND	AD
AE	EBI1_DQ_1	GND	EBI1_DM_0	GND	EBI1_DQ_7	VDD_2	EBI1_CA0_CKE_1	EBI1_CA0_2	EBI1_CA0_5	EBI1_DQ_14	GND	EBI1_DM_1	GND	EBI1_DQ_8	DDR_RESET_N	EBI1_DQ_17	GND	EBI1_DM_2	GND	EBI1_DQ_23	VDD_2	EBI1_CA1_CKE_1	EBI1_CA1_2	EBI1_CA1_5	EBI1_DQ_30	GND	EBI1_DM_3	GND	EBI1_DQ_24	AE
AF	VDD_P1	EBI1_DQ_3	VDD_P1	EBI1_DQ_5	VDD_P1	EBI1_CA0_1	EBI1_CA0_CKE_0	GND	EBI1_CA0_4	VDD_P1	EBI1_DQ_12	VDD_P1	EBI1_DQ_10	VDD_P1	NC	VDD_P1	EBI1_DQ_19	VDD_P1	EBI1_DQ_21	VDD_P1	EBI1_CA1_1	EBI1_CA1_CKE_0	GND	EBI1_CA1_4	VDD_P1	EBI1_DQ_28	VDD_P1	EBI1_DQ_26	VDD_P1	AF
AG	EBI1_DQ_0	GND	EBI1_DQS_0_C	EBI1_DQ_6	GND	VDD_2	EBI1_CA0_CK_C	VDD_2	EBI1_DQ_15	GND	EBI1_DQS_1_C	GND	EBI1_DQ_9	NC		EBI1_DQ_16	GND	EBI1_DQS_2_C	GND	EBI1_DQ_22	GND	VDD_2	EBI1_CA1_CK_C	VDD_2	EBI1_DQ_31	GND	EBI1_DQS_3_C	GND	EBI1_DQ_25	AG
AH	VDD_1	EBI1_DQ_2	EBI1_DQS_0_T	EBI1_DQ_4	GND	EBI1_CA0_0	EBI1_CA0_CS1_N	EBI1_CA0_CK_T	EBI1_CA0_3	VDD_1	EBI1_DQ_13	EBI1_DQS_1_T	EBI1_DQ_11	VDD_1	NC	VDD_1	EBI1_DQ_18	EBI1_DQS_2_T	EBI1_DQ_20	GND	EBI1_CA1_0	EBI1_CA1_CS1_N	EBI1_CA1_CK_T	EBI1_CA1_3	VDD_1	EBI1_DQ_29	EBI1_DQS_3_T	EBI1_DQ_27	VDD_1	AH
AJ	NC	VDD_2	GND	VDD_P1	VDD_1	VDD_2	EBI1_CA0_CS0_N	VDD_2	GND	VDD_2	VDD_P1	GND	VDD_P1	VDD_2	GND	VDD_2	VDD_P1	GND	VDD_P1	VDD_1	VDD_2	EBI1_CA1_CS0_N	VDD_2	GND	VDD_2	VDD_P1	GND	VDD_2	NC	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Figure 2-6 High-level view of APQ8096SGE top pad assignments (from above)

2.3.2   Pad descriptions – APQ top

Descriptions of top pins are presented in the following tables, organized by functional group:

Table 2-15: Memory support functions

Table 2-16: No connection, do not connect, and reserved pins

Table 2-17: Power-supply pins

Table 2-18: Ground pins

Table 2-15   Pad descriptions – memory support functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
EBI0					
E9	EBI0_CA0_5	–	P1	DO	EBI0 LPDDR4 command/address 0 bit 5
D9	EBI0_CA0_4	–	P1	DO	EBI0 LPDDR4 command/address 0 bit 4
B9	EBI0_CA0_3	–	P1	DO	EBI0 LPDDR4 command/address 0 bit 3
E8	EBI0_CA0_2	–	P1	DO	EBI0 LPDDR4 command/address 0 bit 2
D6	EBI0_CA0_1	–	P1	DO	EBI0 LPDDR4 command/address 0 bit 1
B6	EBI0_CA0_0	–	P1	DO	EBI0 LPDDR4 command/address 0 bit 0
E24	EBI0_CA1_5	–	P1	DO	EBI0 LPDDR4 command/address 1 bit 5
D24	EBI0_CA1_4	–	P1	DO	EBI0 LPDDR4 command/address 1 bit 4
B24	EBI0_CA1_3	–	P1	DO	EBI0 LPDDR4 command/address 1 bit 3
E23	EBI0_CA1_2	–	P1	DO	EBI0 LPDDR4 command/address 1 bit 2
D21	EBI0_CA1_1	–	P1	DO	EBI0 LPDDR4 command/address 1 bit 1
B21	EBI0_CA1_0	–	P1	DO	EBI0 LPDDR4 command/address 1 bit 0
C25	EBI0_DQ_31	–	P1	B	EBI0 LPDDR4 data bit 31
E25	EBI0_DQ_30	–	P1	B	EBI0 LPDDR4 data bit 30
B26	EBI0_DQ_29	–	P1	B	EBI0 LPDDR4 data bit 29
D26	EBI0_DQ_28	–	P1	B	EBI0 LPDDR4 data bit 28
B28	EBI0_DQ_27	–	P1	B	EBI0 LPDDR4 data bit 27
D28	EBI0_DQ_26	–	P1	B	EBI0 LPDDR4 data bit 26
C29	EBI0_DQ_25	–	P1	B	EBI0 LPDDR4 data bit 25
E29	EBI0_DQ_24	–	P1	B	EBI0 LPDDR4 data bit 24
E20	EBI0_DQ_23	–	P1	B	EBI0 LPDDR4 data bit 23
C20	EBI0_DQ_22	–	P1	B	EBI0 LPDDR4 data bit 22
D19	EBI0_DQ_21	–	P1	B	EBI0 LPDDR4 data bit 21
B19	EBI0_DQ_20	–	P1	B	EBI0 LPDDR4 data bit 20
D17	EBI0_DQ_19	–	P1	B	EBI0 LPDDR4 data bit 19
B17	EBI0_DQ_18	–	P1	B	EBI0 LPDDR4 data bit 18
E16	EBI0_DQ_17	–	P1	B	EBI0 LPDDR4 data bit 17
C16	EBI0_DQ_16	–	P1	B	EBI0 LPDDR4 data bit 16
C10	EBI0_DQ_15	–	P1	B	EBI0 LPDDR4 data bit 15

Table 2-15   Pad descriptions – memory support functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1] Voltage	Type	Functional description
E10	EBI0_DQ_14	–	P1	B	EBI0 LPDDR4 data bit 14
B11	EBI0_DQ_13	–	P1	B	EBI0 LPDDR4 data bit 13
D11	EBI0_DQ_12	–	P1	B	EBI0 LPDDR4 data bit 12
B13	EBI0_DQ_11	–	P1	B	EBI0 LPDDR4 data bit 11
D13	EBI0_DQ_10	–	P1	B	EBI0 LPDDR4 data bit 10
C14	EBI0_DQ_9	–	P1	B	EBI0 LPDDR4 data bit 9
E14	EBI0_DQ_8	–	P1	B	EBI0 LPDDR4 data bit 8
E5	EBI0_DQ_7	–	P1	B	EBI0 LPDDR4 data bit 7
C5	EBI0_DQ_6	–	P1	B	EBI0 LPDDR4 data bit 6
D4	EBI0_DQ_5	–	P1	B	EBI0 LPDDR4 data bit 5
B4	EBI0_DQ_4	–	P1	B	EBI0 LPDDR4 data bit 4
D2	EBI0_DQ_3	–	P1	B	EBI0 LPDDR4 data bit 3
B2	EBI0_DQ_2	–	P1	B	EBI0 LPDDR4 data bit 2
E1	EBI0_DQ_1	–	P1	B	EBI0 LPDDR4 data bit 1
C1	EBI0_DQ_0	–	P1	B	EBI0 LPDDR4 data bit 0
C8	EBI0_CA0_CK_C	–	P1	DO	EBI0 CA0 LPDDR4 differential clock (C)
B8	EBI0_CA0_CK_T	–	P1	DO	EBI0 CA0 LPDDR4 differential clock (T)
E7	EBI0_CA0_CKE_1	–	P1	DO	EBI0 CA0 LPDDR4 clock enable 1
D7	EBI0_CA0_CKE_0	–	P1	DO	EBI0 CA0 LPDDR4 clock enable 0
B7	EBI0_CA0_CS1_N	–	P1	DO	EBI0 CA0 LPDDR4 chip select 1
A7	EBI0_CA0_CS0_N	–	P1	DO	EBI0 CA0 LPDDR4 chip select 0
C23	EBI0_CA1_CK_C	–	P1	DO	EBI0 CA1 LPDDR4 differential clock (C)
B23	EBI0_CA1_CK_T	–	P1	DO	EBI0 CA1 LPDDR4 differential clock (T)
E22	EBI0_CA1_CKE_1	–	P1	DO	EBI0 CA1 LPDDR4 clock enable 1
D22	EBI0_CA1_CKE_0	–	P1	DO	EBI0 CA1 LPDDR4 clock enable 0
B22	EBI0_CA1_CS1_N	–	P1	DO	EBI0 CA1 LPDDR4 chip select 1
A22	EBI0_CA1_CS0_N	–	P1	DO	EBI0 CA1 LPDDR4 chip select 0
C27	EBI0_DQS_3_C	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 3 (C)
B27	EBI0_DQS_3_T	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 3 (T)
C18	EBI0_DQS_2_C	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 2 (C)
B18	EBI0_DQS_2_T	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 2 (T)
C12	EBI0_DQS_1_C	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 1 (C)
B12	EBI0_DQS_1_T	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 1 (T)
C3	EBI0_DQS_0_C	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 0 (C)
B3	EBI0_DQS_0_T	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 0 (T)
E27	EBI0_DM_3	–	P1	DO	EBI0 LPDDR4 data mask for byte 3
E18	EBI0_DM_2	–	P1	DO	EBI0 LPDDR4 data mask for byte 2
E12	EBI0_DM_1	–	P1	DO	EBI0 LPDDR4 data mask for byte 1
E3	EBI0_DM_0	–	P1	DO	EBI0 LPDDR4 data mask for byte 0

Table 2-15   Pad descriptions – memory support functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1] Voltage	Type	Functional description
D15, E15	ZQ0	–	–	AI	LPDDR4 ZQ resistor, lower x16 memory (shared by EBIs)
B15, C15	ZQ2	–	–	AI	LPDDR4 ZQ resistor, upper x16 memory (shared by EBIs)
EBI1					
AE9	EBI1_CA0_5	–	P1	DO	EBI1 LPDDR4 command/address 0 bit 5
AF9	EBI1_CA0_4	–	P1	DO	EBI1 LPDDR4 command/address 0 bit 4
AH9	EBI1_CA0_3	–	P1	DO	EBI1 LPDDR4 command/address 0 bit 3
AE8	EBI1_CA0_2	–	P1	DO	EBI1 LPDDR4 command/address 0 bit 2
AF6	EBI1_CA0_1	–	P1	DO	EBI1 LPDDR4 command/address 0 bit 1
AH6	EBI1_CA0_0	–	P1	DO	EBI1 LPDDR4 command/address 0 bit 0
AE24	EBI1_CA1_5	–	P1	DO	EBI1 LPDDR4 command/address 1 bit 5
AF24	EBI1_CA1_4	–	P1	DO	EBI1 LPDDR4 command/address 1 bit 4
AH24	EBI1_CA1_3	–	P1	DO	EBI1 LPDDR4 command/address 1 bit 3
AE23	EBI1_CA1_2	–	P1	DO	EBI1 LPDDR4 command/address 1 bit 2
AF21	EBI1_CA1_1	–	P1	DO	EBI1 LPDDR4 command/address 1 bit 1
AH21	EBI1_CA1_0	–	P1	DO	EBI1 LPDDR4 command/address 1 bit 0
AG25	EBI1_DQ_31	–	P1	B	EBI1 LPDDR4 data bit 31
AE25	EBI1_DQ_30	–	P1	B	EBI1 LPDDR4 data bit 30
AH26	EBI1_DQ_29	–	P1	B	EBI1 LPDDR4 data bit 29
AF26	EBI1_DQ_28	–	P1	B	EBI1 LPDDR4 data bit 28
AH28	EBI1_DQ_27	–	P1	B	EBI1 LPDDR4 data bit 27
AF28	EBI1_DQ_26	–	P1	B	EBI1 LPDDR4 data bit 26
AG29	EBI1_DQ_25	–	P1	B	EBI1 LPDDR4 data bit 25
AE29	EBI1_DQ_24	–	P1	B	EBI1 LPDDR4 data bit 24
AE20	EBI1_DQ_23	–	P1	B	EBI1 LPDDR4 data bit 23
AG20	EBI1_DQ_22	–	P1	B	EBI1 LPDDR4 data bit 22
AF19	EBI1_DQ_21	–	P1	B	EBI1 LPDDR4 data bit 21
AH19	EBI1_DQ_20	–	P1	B	EBI1 LPDDR4 data bit 20
AF17	EBI1_DQ_19	–	P1	B	EBI1 LPDDR4 data bit 19
AH17	EBI1_DQ_18	–	P1	B	EBI1 LPDDR4 data bit 18
AE16	EBI1_DQ_17	–	P1	B	EBI1 LPDDR4 data bit 17
AG16	EBI1_DQ_16	–	P1	B	EBI1 LPDDR4 data bit 16
AG10	EBI1_DQ_15	–	P1	B	EBI1 LPDDR4 data bit 15
AE10	EBI1_DQ_14	–	P1	B	EBI1 LPDDR4 data bit 14
AH11	EBI1_DQ_13	–	P1	B	EBI1 LPDDR4 data bit 13
AF11	EBI1_DQ_12	–	P1	B	EBI1 LPDDR4 data bit 12
AH13	EBI1_DQ_11	–	P1	B	EBI1 LPDDR4 data bit 11
AF13	EBI1_DQ_10	–	P1	B	EBI1 LPDDR4 data bit 10
AG14	EBI1_DQ_9	–	P1	B	EBI1 LPDDR4 data bit 9
AE14	EBI1_DQ_8	–	P1	B	EBI1 LPDDR4 data bit 8

Table 2-15   Pad descriptions – memory support functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AE5	EBI1_DQ_7	–	P1	B	EBI1 LPDDR4 data bit 7
AG5	EBI1_DQ_6	–	P1	B	EBI1 LPDDR4 data bit 6
AF4	EBI1_DQ_5	–	P1	B	EBI1 LPDDR4 data bit 5
AH4	EBI1_DQ_4	–	P1	B	EBI1 LPDDR4 data bit 4
AF2	EBI1_DQ_3	–	P1	B	EBI1 LPDDR4 data bit 3
AH2	EBI1_DQ_2	–	P1	B	EBI1 LPDDR4 data bit 2
AE1	EBI1_DQ_1	–	P1	B	EBI1 LPDDR4 data bit 1
AG1	EBI1_DQ_0	–	P1	B	EBI1 LPDDR4 data bit 0
AG8	EBI1_CA0_CK_C	–	P1	DO	EBI1 CA0 LPDDR4 differential clock (C)
AH8	EBI1_CA0_CK_T	–	P1	DO	EBI1 CA0 LPDDR4 differential clock (T)
AE7	EBI1_CA0_CKE_1	–	P1	DO	EBI1 CA0 LPDDR4 clock enable 1
AF7	EBI1_CA0_CKE_0	–	P1	DO	EBI1 CA0 LPDDR4 clock enable 0
AH7	EBI1_CA0_CS1_N	–	P1	DO	EBI1 CA0 LPDDR4 chip select 1
AJ7	EBI1_CA0_CS0_N	–	P1	DO	EBI1 CA0 LPDDR4 chip select 0
AG23	EBI1_CA1_CK_C	–	P1	DO	EBI1 CA1 LPDDR4 differential clock (C)
AH23	EBI1_CA1_CK_T	–	P1	DO	EBI1 CA1 LPDDR4 differential clock (T)
AE22	EBI1_CA1_CKE_1	–	P1	DO	EBI1 CA1 LPDDR4 clock enable 1
AF22	EBI1_CA1_CKE_0	–	P1	DO	EBI1 CA1 LPDDR4 clock enable 0
AH22	EBI1_CA1_CS1_N	–	P1	DO	EBI1 CA1 LPDDR4 chip select 1
AJ22	EBI1_CA1_CS0_N	–	P1	DO	EBI1 CA1 LPDDR4 chip select 0
AG27	EBI1_DQS_3_C	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 3 (C)
AH27	EBI1_DQS_3_T	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 3 (T)
AG18	EBI1_DQS_2_C	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 2 (C)
AH18	EBI1_DQS_2_T	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 2 (T)
AG12	EBI1_DQS_1_C	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 1 (C)
AH12	EBI1_DQS_1_T	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 1 (T)
AG3	EBI1_DQS_0_C	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 0 (C)
AH3	EBI1_DQS_0_T	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 0 (R)
AE27	EBI1_DM_3	–	P1	DO	EBI1 LPDDR4 data mask for byte 3
AE18	EBI1_DM_2	–	P1	DO	EBI1 LPDDR4 data mask for byte 2
AE12	EBI1_DM_1	–	P1	DO	EBI1 LPDDR4 data mask for byte 1
AE3	EBI1_DM_0	–	P1	DO	EBI1 LPDDR4 data mask for byte 0
AE15	DDR_RESET_N	–	P1	DO	LPDDR4 reset (shared by EBIs)

1. See Table 2-1 for parameter and acronym definitions.

Table 2-16   Pad descriptions – no connection, do not connect, and reserved pins

Pad #	Pad name	Functional description
H3, H4, J3, J3, J4, J4, K3, K3, K4, K4, M3, M3, M4, M4, N3, N3, N4, N4, P3, P3, P4, P4, T3, T3, T4, T4, V3, V3, W3, W3, W4, W4, Y3, Y4, AA3, AA3, AA4, AA4	DNC	Do not connect; connected internally, do not connect externally
A1, A29, AF15, AG15, AH15, AJ1, AJ29	NC	No connect; not connected internally.
–	RSVD	Reserved

Table 2-17   Pad descriptions – power supply pins

Pad #	Pad name	Functional description
A5, A20, B1, B10, B14, B16, B25, B29, AH1, AH10, AH14, AH16, AH25, AH29, AJ5, AJ20	VDD_1	Power for memory core (bottom VDD_DDR_CORE_1P8)
A2, A6, A8, A10, A14, A16, A21, A23, A25, A28, C7, C9, C22, C24, E6, E21, AE6, AE21, AG7, AG9, AG22, AG24, AJ2, AJ6, AJ8, AJ10, AJ14, AJ16, AJ21, AJ23, AJ25, AJ28	VDD_2	Power for memory core (bottom VDD_DDR_CORE_1P2)
A4, A11, A13, A17, A19, A26, D1, D3, D5, D10, D12, D14, D16, D18, D20, D25, D27, D29, AF1, AF3, AF5, AF10, AF12, AF14, AF16, AF18, AF20, AF25, AF27, AF29, AJ4, AJ11, AJ13, AJ17, AJ19, AJ26	VDD_P1	Power for memory I/O pads

Table 2-18   Pad descriptions – ground pins

Pad #	Pad name	Functional description
A3, A9, A123, A15, A18, A24, A27, B5, B20, C2, C4, C6, C11, C13, C17, C19, C21, C26, C28, D8, D23, E2, E4, E11, E13, E17, E19, E26, E28, F1, F2, F28, F29, G1, G2, G28, G29, H1, H2, H28, H29, J1, J2, J28, J29, K1, K2, K28, K29, L1, L2, L28, L29, M1, M2, M28, M29, N1, N2, N28, N29, P1, P2, P28, P29, R1, R2, R28, R29, T1, T2, T28, T29, U1, U2, U28, U29, V1, V2, V28, V29, W1, W2, W28, W29, Y1, Y2, Y28, Y29, AA1, AA2, AA28, AA29, AB1, AB2, AB28, AB29, AC1, AC2, AC28, AC29, AD1, AD2, AD28, AD29, AE2, AE4, AE11, AE13, AE17, AE19, AE26, AE28, AF8, AF23, AG2, AG4, AG6, AG11, AG13, AG17, AG19, AG21, AG26, AG28, AH5, AH20, AJ3, AJ9, AJ12, AJ15, AJ18, AJ24, AJ27	GND	Ground

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings in Table 3-1 reflect the stress levels that, if exceeded, will cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1   Absolute maximum ratings

Power supply	Description	Min	Max	Unit
VDD_CORE	APQ digital core	-0.3	1.177	V
VDD_MEM VDD_USB_HS_CORE	APQ on chip memory Power for USB digital core circuits - HS1, HS2	-0.3	1.177	V
VDD_GFX	APQ graphics core	-0.3	1.177	V
VDD_APC	Power for quad Kryo applications microprocessors	-0.3	1.353	V
VDD_MODEM	Power for modem circuits, including the two QDSP6s	-0.3	1.177	V
VDD_A1	Power for analog circuits - low voltage	-0.3	1.43	V
VDD_A2	Power for analog circuits - high voltage	-0.3	2.079	V
VDD_QFPROM_PRG	Power for programming the QFPROM			
VDD_EBI_PHY	Power for EBI PHY circuits	-0.3	1.177	V
VDD_EBI_IO	Power for EBI IO circuits			
VDD_EBI_IO_ISO	Power for EBI IO circuits that need isolated routing on the PCB			
VDD_SSC_CORE	Power for Snapdragon sensor core	-0.3	1.074	V
VDD_SSC_MEM	Power for Snapdragon sensor core memory	-0.3	1.074	V
VDD_PLL1	Power for PLL circuits - 0.925 V	-0.3	1.051	V
VDD_PLL1_ISO	Power for PLL circuits - 0.925 V that need isolated routing on the PCB			
VDD_HDMI1	Power for HDMI circuits - low voltage			
VDD_PCIE_CORE	Power for PCIe core circuitry			
VDD_UFS_CORE	Power for UFS core circuits			
VDD_USB_SS_CORE	Power for USB digital core circuits - SS			
VDD_PLL2	Power for PLL circuits - 1.250 V	-0.3	1.419	V

Table 3-1   Absolute maximum ratings

Power supply	Description	Min	Max	Unit
VDD_PLL2_ISO	Power for PLL circuits - 1.250 V that need isolated routing on the PCB			
VDD_MIPI_CSI	Power for MIPI_CSI IOs			
VDD_MIPI_DSI	Reference for MIPI_DSI IOs and circuits			
VDD_PLL3	Power for PLL circuits - 1.800 V	-0.3	2.09	V
VDD_P9	Power for pad group 9 - CXO_2 pad			
VDD_HDMI2	Power for HDMI circuits - high voltage			
VDD_UFS_IP8	Power for UFS 1.8 V circuits			
VDD_USB_1P8	Power for USB HS1, HS2, and SS - low voltage			
VDD_PCIE_1P8	Power for PCIe IO circuitry			
VDD_P11	Power for pad group 11 - CXO pad			
VDD_P1	Power for pad group 1 - EBI1 pads and DDR memory IO pads	-0.3	1.287	V
VDD_DDR_CORE_1P2	Power for PoP DDR memory core - for VDD2			
VDD_P2	Power for pad group 2 - SDC2 pads	-0.3	3.344	V
VDD_P3	Power for pad group 3 - IO pads	-0.3	2.09	V
VDD_DDR_CORE_1P8	Power for PoP DDR memory core - for VDD1			
VDD_P7	Power for pad group 7 - SDC1 pads			
VDD_P5	Power for pad group 5 - UIM1 pads	-0.3	3.344	V
VDD_P6	Power for pad group 6 - UIM2 pads	-0.3	3.344	V
VDD_P10	Power for pad group 10 - UFS pad	-0.3	1.375	V
VDD_P12	Power for pad group 12 - SSC pad	-0.3	2.09	V
VDD_USB_HS_3P1	Power for USB HS1 and HS2 - high voltage	-0.3	3.52	V

3.2   Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-2 and Table 3-3). The APQ8096SGE meets all performance specifications when used within the operating conditions (provided the absolute maximum ratings have never been exceeded).

Table 3-2   Operating conditions for voltage rails with AVS Type-1

Parameter [1]		Min	Max	Unit
VDD_CORE	APQ digital core			
	Turbo	0.795	1.07	V
	Nominal	0.705	0.976	V
	SVS	0.59	0.8	V
	Low SVS	0.515	0.717	V
VDD_MEM	APQ on-chip memory			
VDD_USB_HS_CORE	Power for USB digital core circuits – HS1, HS2			
	Turbo	0.795	1.07	V
	Nominal	0.785	1.025	V
	SVS [2]	0.785	0.915	V
	Low SVS [2]	0.785	0.915	V
VDD_GFX	APQ graphics core			
	Turbo	0.795	1.07	V
	Nominal L1	0.744	1.036	V
	Nominal	0.705	0.976	V
	SVS L1	0.643	0.888	V
	SVS	0.59	0.8	V
	Low SVS	0.515	0.717	V
	Min SVS	0.545	0.64	V
VDD_APC	Power for quad Kryo applications microprocessors			
	Turbo	0.79	1.23	V
	Nominal	0.695	0.976	V
	SVS	0.59	0.8	V
	Min SVS	0.54	0.646	V
VDD_MODEM	Power for modem circuits			
	Turbo	0.795	1.07	V
	Nominal	0.705	0.976	V
	SVS	0.59	0.8	V
	Low SVS	0.515	0.717	V

Table 3-2   Operating conditions for voltage rails with AVS Type-1 (cont.)

Parameter [1]		Min	Max	Unit
VDD_EBI_PHY	Power for EBI PHY circuits			
VDD_EBI_IO	Power for EBI I/O circuits			
VDD_EBI_IO_ISO	Power for EBI I/O circuits that need isolated routing on the PCB			
	Turbo	0.815	1.07	V
	Nominal	0.7	0.97	V
	SVS	0.675	0.915	V
	Low SVS	0.633	0.778	V
VDD_SSC_CORE	Power for Snapdragon sensor core			
	Turbo	0.795	1.07	V
	Nominal	0.705	0.976	V
	SVS	0.59	0.8	V
	Low SVS	0.515	0.717	V
VDD_SSC_MEM	Power for Snapdragon sensor core memory			
	Turbo	0.795	1.07	V
	Nominal	0.785	1.025	V
	SVS [2]	0.785	0.915	V
	Low SVS [2]	0.785	0.915	V

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. The voltage setting at the PMIC for SVS and low SVS modes for this core is a static 0.85 V. There is no scaling.

Table 3-3   Operating voltages

Parameter		Min	Typ [2]	Max	Unit
Power supply voltages					
VDD_A1	Power for analog circuits – low voltage	1.15	1.225	1.3	V
VDD_A2 VDD_QFPROM_PRG	Power for analog circuits – high voltage Power for programming the QFPROM	1.71	1.8	1.89	V
VDD_PLL1	Power for PLL circuits – 0.925 V	0.885	0.925	0.955	V
VDD_PLL1_ISO	Power for PLL circuits – 0.925 V that need isolated routing on the PCB				
VDD_HDMI1	Power for HDMI circuits – low voltage				
VDD_PCIE_CORE	Power for PCIe core circuitry				
VDD_UFS_CORE	Power for UFS core circuits				
VDD_USB_SS_CORE	Power for USB digital core circuits – SS				

Table 3-3   Operating voltages (cont.)

Parameter		Min	Typ [2]	Max	Unit
VDD_PLL2	Power for PLL circuits – 1.250 V	1.21	1.25	1.29	V
VDD_PLL2_ISO	Power for PLL circuits – 1.250 V that need isolated routing on the PCB				
VDD_MIPI_CSI	Power for MIPI_CSI I/Os				
VDD_MIPI_DSI	Reference for MIPI_DSI I/Os and circuits				
VDD_PLL3	Power for PLL circuits – 1.800 V	1.7	1.8	1.9	V
VDD_P9	Power for pad group 9 – CXO_2 pad				
VDD_HDMI2	Power for HDMI circuits – high voltage				
VDD_UFS_1P8	Power for UFS 1.8 V circuits				
VDD_USB_1P8	Power for USB HS1, HS2, and SS – low voltage				
VDD_PCIE_1P8	Power for PCIe I/O circuitry				
VDD_P11	Power for pad group 11 – CXO pad				
VDD_P1	Power for pad group 1 – EBI1 pads and DDR memory I/O pads	1.07	1.125	1.17	V
VDD_DDR_CORE_1P2	Power for PoP DDR memory core – VDD2 for DDR memory				
VDD_P2	Power for pad group 2 – SDC2 pads	1.7/2.7	1.8/2.95	1.9/3.04	V
VDD_P3	Power for pad group 3 – I/O pads	1.7	1.8	1.9	V
VDD_DDR_CORE_1P8	Power for PoP DDR memory core – 1.8 V for VDD1				
VDD_P7	Power for pad group 7 – SDC1 pads				
VDD_P5	Power for pad group 5 – UIM1 pads	1.7/2.7	1.8/2.95	1.9/3.04	V
VDD_P6	Power for pad group 6 – UIM2 pads	1.7/2.7	1.8/2.95	1.9/3.04	V
VDD_P10	Power for pad group 10 – UFS pad	1.15	1.2	1.25	V
VDD_P12	Power for pad group 12 – SSC pad	1.7	1.8	1.9	V
VDD_USB_HS_3P1	Power for USB HS1 and HS2 – high voltage	2.98	3.075	3.2	V
Thermal conditions					
T_C	Device operating temperature (case)	-30	+25	+85	°C
	Fuse programming temperature (case)	+10	+25	+85	°C
T_A [1]	3GPP2-mode operating temperature (ambient)	-30	+25	+60	°C
	3GPP-mode operating temperature (ambient)	-20	+25	+60	°C

1. These temperature ranges are defined by the 3GPP and 3GPP2 system specifications.
2. Typical voltages represent the recommended output settings of the companion PMIC device.

3.3   Power distribution network

The impedances of the distribution networks that deliver power to the APQ device are critical to its supply voltages, not just at DC but over a wide range of frequencies. The PDN must meet the minimum/maximum values listed in Table 3-4 and Table 3-5. Table 3-6 lists the power distribution network (PDN) maximum impedance specifications.

Table 3-4   APQ8096SGE PDN specifications – lumped

Power domain	Maximum impedance (mΩ)		Pad number of positive port	Pad number of negative port
	DC–10 Hz	10 Hz–25 MHz		
VDD_APC	2	15	All VDD_APC pins	All GND pins
VDD_GFX	3	25	All VDD_GFX pins	All GND pins
VDD_MODEM	10	30	All VDD_MODEM pins	All GND pins
VDD_CORE	8	–	All VDD_CORE pins	All GND pins
VDD_MEM	8	–	All VDD_MEM pins	All GND pins
VDD_SSC_CORE	50	85	J29, L25, L27, L29	J27, J31, N23, N25, N27, N31
VDD_SSC_MEM	150	200	N29	N27, N31

Table 3-5   APQ8096SGE PDN specifications – distributed

Power domain	Maximum impedance (mΩ)	Port number	Pad number of positive port	Pad number of negative port
	10 Hz–25 MHz			
VDD_APC	64	1	R9, R11, R13	N9, N11, N13, N15, P8, T8, U9, U11, U13, U15
	64	2	R17, R19, R21	N15, N17, N19, N21, N23, U15, U17, U19, U21, U23
	64	3	AC9, AC11, AG9, AG11	Y8, AA9, AA11, AE9, AE11, AJ11
	64	4	AC16, AC21, AG16, AG21	AA15, AA17, AA19, AA21, AE21, AE23, AJ15, AJ17, AJ19, AJ21, AJ23
VDD_GFX	64	1	AW31, AW33, AW35	AU29, AU31, AU33, AU35, BA31, BA33, BA35
	64	2	AW41, AW43	AU43, BA41, BA43, BB42
VDD_MODEM	64	1	L33, L35	J31, J35, N31, N33, N35, N37
	85	2	L41	J39, J43, N39, N41, N43
	70	3	R39, R41, R43	N37, N39, N41, N43, U37, U39, U41
	70	4	W41, W43	U39, U41, AA39, AA41, AA43

Table 3-5　APQ8096SGE PDN specifications – distributed (cont.)

Power domain	Maximum impedance (mΩ) 10 Hz–25 MHz	Port number	Pad number of positive port	Pad number of negative port
VDD_CORE	90	1	F12	F14, G13, H12, J11, J13
	64	2	J25, L21, L23	J21, J27, N19, N21, N23, N25
	80	3	L37, L39	J35, J39, N35, N37, N39, N41
	64	4	N7, V8	N9, P8, T8, U9, Y8
	35	5	R25, R27, R29	N23, N25, N27, N31, U23, U25, U31
	40	6	W25, W27, W29, AC25, AC27, AC29, AG23, AG25, AG31, AG33, AL25, AL27	U23, U25, U31, AA25, AA27, AA29, AE21, AE23, AE25, AE27, AE29, AE31, AE33, AJ21, AJ23, AJ25, AJ27, AJ29, AJ31, AJ33
	64	7	AC37, AC39, AC41, AC43, AG43, AG45	AA35, AA37, AA39, AA41, AA43, AC45, AE35, AE37, AE39, AE41, AE43, AE45, AF46, AJ43
	64	8	AL11, AL13, AL15, AL17, AL19, AR13, AR15	AJ11, AJ13, AJ15, AJ17, AJ19, AJ21, AL9, AN9, AN11, AN13, AN15, AN17, AN19, AN21, AU11, AU13, AU15, AU17
	64	9	AR21, AR23	AN19, AN21, AN23, AU19, AU21, AU23, AU25
	64	10	AR27, AR29	AN29, AN31, AU25, AU27, AU29, AU31
	64	11	AW9, AW11	AU9, AU11, AU13, BA11, BB10, BC9
	64	12	AW17, AW19	AU15, AU17, AU19, AU21, BA15, BA17, BA19, BA21, BB18
	64	13	AW25, AW27	AU23, AU25, AU27, AU29, BA23, BA25, BA29, BB24, BB30
	100	14	BA37	BA35, BA39, BB38
	100	15	BA45	BA41, BA43, BB42

Table 3-5   APQ8096SGE PDN specifications – distributed (cont.)

Power domain	Maximum impedance (mΩ) 10 Hz–25 MHz	Port number	Pad number of positive port	Pad number of negative port
VDD_MEM	90	1	H10	H12, J9, J11
	85	2	L31	H32, J31, N31
	80	3	L43	J43, N41, N43
	80	4	R7	N9, P8, T8, U9
	64	5	R15	N13, N15, N17, U13, U15, U17
	64	6	R23	N21, N23, N25, U21, U23, U25
	50	7	R35, R37, U27, U29, W37, W39, AC33, AC35	N33, N35, N37, N39, U25, U31, U33, U35, U37, U41, AA35, AA37, AA39, AA41, AE31, AE33, AE35, AE37
	90	8	AC7	Y8, AA9, AE9
	64	9	AC23	AA21, AA25, AE21, AE23, AE25
	70	10	AE16	AA15, AA17, AJ15, AJ17
	64	11	AG27, AG29	AE25, AE27, AE29, AE31, AJ25, AJ27, AJ29, AJ31
	64	12	AL21, AL23, AR17, AR19	AJ19, AJ21, AJ23, AJ25, AN15, AN17, AN19, AN21, AN23, AU15, AU17, AU19, AU21
	64	13	AL29, AL31, AL33, AL35	AJ27, AJ29, AJ31, AJ33, AJ35, AN27, AN29, AN31, AN33, AN35
	64	14	AL43, AL45, AU45	AJ41, AJ43, AN43, AU43
	80	15	AP41	AN43, AU43
	64	16	AR9, AR11	AN9, AN11, AN13, AU9, AU11, AU13
	64	17	AW13, AW15	AU11, AU13, AU15, AU17, BA11, BA13, BA15, BA17
	64	18	AW21, AW23	AU19, AU21, AU23, AU25, BA19, BA21, BA23, BA25, BB22, BB24
	64	19	AW29	AU27, AU29, AU31, BA29, BA31, BB30
	64	20	AW37, AW39	AU35, BA35, BA39, BA41, BB38

Table 3-6   APQ8096SGE PDN specifications – EBI

Power domain	Maximum impedance (mΩ)		Maximum effective impedance (mΩ)					Port number	Pad number of positive port	Pad number of negative port
	Lumped DC	*Distributed DC*	*1 MHz*	*5 MHz*	*9 MHz*	*25 MHz*	*300 MHz*			
VDD_EBI_PHY [1]	20	53	1000	200	200	481	5448	1	J15	E15, F14, F16, F18, F20, F22, G13, G17, G19, G21, H12, J11, J17, J21
			1000	200	200	481	5448	2	J19	E15, F14, F16, F18, F20, F22, G13, G17, G19, G21, H12, J11, J17, J21
			1000	200	200	481	5448	3	J23	E15, F14, F16, F18, F20, F22, G13, G17, G19, G21, H12, J11, J17, J21
		53	1000	200	200	481	5448	4	J33	F32, F34, F36, F38, F40, F42, G35, G37, G39, G43, H32, J35, J39, J43, J45
			1000	200	200	481	5448	5	J37	F32, F34, F36, F38, F40, F42, G35, G37, G39, G43, H32, J35, J39, J43, J45
			1000	200	200	481	5448	6	J41	F32, F34, F36, F38, F40, F42, G35, G37, G39, G43, H32, J35, J39, J43, J45
		53	1000	200	200	481	5448	7	BB12	BA11, BA13, BA15, BA17, BA19, BA21, BB10, BB14, BB18, BB22, BC9, BD10, BD14, BD18, BE11, BE13, BE15, BE17, BE19
			1000	200	200	481	5448	8	BB16	BA11, BA13, BA15, BA17, BA19, BA21, BB10, BB14, BB18, BB22, BC9, BD10, BD14, BD18, BE11, BE13, BE15, BE17, BE19
			1000	200	200	481	5448	9	BB20	BA11, BA13, BA15, BA17, BA19, BA21, BB10, BB14, BB18, BB22, BC9, BD10, BD14, BD18, BE11, BE13, BE15, BE17, BE19

Table 3-6   APQ8096SGE PDN specifications – EBI (cont.)

Power domain	Maximum impedance (mΩ)		Maximum effective impedance (mΩ)					Port number	Pad number of positive port	Pad number of negative port
	Lumped DC	*Distributed DC*	*1 MHz*	*5 MHz*	*9 MHz*	*25 MHz*	*300 MHz*			
VDD_EBI_PHY [1] (cont.)	20	53	1000	200	200	481	5448	10	BB36	BA35, BA39, BA41, BA43, BB38, BB42, BD38, BD42, BE35, BE37, BE39, BE41, BE43, BE45
			1000	200	200	481	5448	11	BB40	BA35, BA39, BA41, BA43, BB38, BB42, BD38, BD42, BE35, BE37, BE39, BE41, BE43, BE45
			1000	200	200	481	5448	12	BB44	BA35, BA39, BA41, BA43, BB38, BB42, BD38, BD42, BE35, BE37, BE39, BE41, BE43, BE45
	Lumped DC	*Distributed DC*	*1 MHz*	*5 MHz*	*10 MHz*	*25 MHz*	*300 MHz*			
VDD_EBI_IO [1]	9	38	972	199	199	356	4325	1	H14, H16	E15, F14, F16, F18, F20, F22, G13, G17, G19, G21, H12, J11, J17, J21
			972	199	199	356	4325	2	H18, H20	E15, F14, F16, F18, F20, F22, G13, G17, G19, G21, H12, J11, J17, J21
			972	199	199	356	4325	3	H22, H24	E15, F14, F16, F18, F20, F22, G13, G17, G19, G21, H12, J11, J17, J21
		38	972	199	199	356	4325	4	H34, H36	F32, F34, F36, F38, F40, F42, G35, G37, G39, G43, H32, J35, J39, J43, J45
			972	199	199	356	4325	5	H38, H40	F32, F34, F36, F38, F40, F42, G35, G37, G39, G43, H32, J35, J39, J43, J45
			972	199	199	356	4325	6	H42, H44	F32, F34, F36, F38, F40, F42, G35, G37, G39, G43, H32, J35, J39, J43, J45

Table 3-6   APQ8096SGE PDN specifications – EBI (cont.)

Power domain	Maximum impedance (mΩ)		Maximum effective impedance (mΩ)					Port number	Pad number of positive port	Pad number of negative port
	Lumped DC	*Distributed DC*	*1 MHz*	*5 MHz*	*10 MHz*	*25 MHz*	*300 MHz*			
VDD_EBI_IO [1] (cont.)	9	38	972	199	199	356	4325	7	BC11, BC13	BA11, BA13, BA15, BA17, BA19, BA21, BB10, BB14, BB18, BB22, BC9, BD10, BD14, BD18, BE11, BE13, BE15, BE17, BE19
			972	199	199	356	4325	8	BC15, BC17	BA11, BA13, BA15, BA17, BA19, BA21, BB10, BB14, BB18, BB22, BC9, BD10, BD14, BD18, BE11, BE13, BE15, BE17, BE19
			972	199	199	356	4325	9	BC19, BC21	BA11, BA13, BA15, BA17, BA19, BA21, BB10, BB14, BB18, BB22, BC9, BD10, BD14, BD18, BE11, BE13, BE15, BE17, BE19
		38	972	199	199	356	4325	10	BC35, BC37	BA35, BA39, BA41, BA43, BB38, BB42, BD38, BD42, BE35, BE37, BE39, BE41, BE43, BE45
			972	199	199	356	4325	11	BC39, BC41	BA35, BA39, BA41, BA43, BB38, BB42, BD38, BD42, BE35, BE37, BE39, BE41, BE43, BE45
			972	199	199	356	4325	12	BC43, BC45	BA35, BA39, BA41, BA43, BB38, BB42, BD38, BD42, BE35, BE37, BE39, BE41, BE43, BE45
	DC		*1 MHz*	*3 MHz*	*10 MHz*	*25 MHz*	*300 MHz*			
VDD_EBI_IO_ISO	60		804	196	196	388	5087	1	B16	A15
	60		804	196	196	388	5087	2	D40	B40
	60		804	196	196	388	5087	3	BH16	BK16
	60		804	196	196	388	5087	4	BH40	BK40

1. Meeting both lumped and distributed DC specifications is required.

3.4 Power sequencing

The PMIC includes power on circuits that provide the proper power sequencing for the entire APQ8096SGE chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of PMIC pins. There will be a hardware default sequence that can be used. The programmable boot sequence (PBS) module of the PMIC allows for programming of the sequence required. Refer to the appropriate PMIC device specification for details, such as the *PM8994/PM8996 PMI8994/PMI8996 Power Management IC Device Specification* (LM80-P2751-5).

A high-level summary of the required default power on sequence:

1. VDD_MEM (on-chip memory), VDD_USB_HS_CORE (USB digital core circuits – HS1, HS2)

2. VDD_EBI_PHY, VDD_EBI_IO, and VDD_EBI_IO_ISO (EBI0/1 circuits)

3. VDD_CORE (digital core circuits)

4. VREF_SDC/VREF_UIM/VREF_APC (SDC/UIM reference voltage)

5. VDD_P3 (I/Os), VDD_P7 (SDC1), and VDD_DDR_CORE_1P8 (DDR memory core 1.8 V)

6. SLEEP_CLK (32.768 MHz)

7. VDD_PLL3 (PLL circuitry 1.8 V), VDD_UFS_1P8 (UFS 1.8 V circuits), VDD_USB_1P8 (USB 1.8 V circuits), VDD_PCIE_1P8 (PCIe I/O circuits), VDD_HDMI2 (HDMI 1.8 V circuits), VDD_P9 (CXO_2), and VDD_P11 (CXO)

8. VDD_P1 (EBI and DDR I/Os), VDD_DDR_CORE_1P1 (DDR core 1.1 V), and VREF_EBI (EBI0 and EBI1 DQ and CA reference voltage)

9. VDD_USB_HS_3P1 (USB 3 V circuits)

10. VDD_P10 (UFS I/O)

11. VDD_PLL2 and VDD_PLL2_ISO (PLL circuitry 1.25 V), VDD_MIPI_CSI, and VDD_MIPI_DSI

12. VDD_PLL1 and VDD_PLL1_ISO (PLL circuitry 0.925 V), VDD_HDMI1 (HDMI 0.925 V circuits), VDD_PCIE_CORE (PCIe core circuits), VDD_UFS_CORE (UFS core circuits), and VDD_USB_SS_CORE (USB digital core circuits – SS)

13. VDD_P2 (SDC2 I/O)

14. CXO (19.2 MHz for digital circuits)

15. VDD_APC0 (applications processor cluster 0)

16. CXO_2 (19.2 MHz for analog circuits)

Comments regarding this sequence:

- The core voltage (VDD_CORE) needs to power up before the pad circuits (VDD_PX), so that the internal circuits can take control of the I/Os and pads.

- If pad voltages power up first, the output drivers might be stuck in unknown states, and might cause large leakage currents until VDD_CORE powers on.

- The general-purpose pad voltage (VDD_P3) needs to precede the analog voltages (VDD_AX).

■ Supplies can be powered on by software after the sequence is completed.

■ Each domain needs to reach its 90% value before the next domain starts ramping up. For example, when VDD_CORE reaches 90% of its value, the VDD_P3 supply can start ramping up.

3.5 Digital logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

■ Specifications are not provided for interfaces that are dedicated for interconnections between the APQ device and ICs within the QTI chipset.

■ Specifications defined by existing standards, such as I^{2}C and SPI are not provided. QTI devices comply with those standards.

Table 3-7   DC specification of VDD_P3 = 1.8 V GPIOs

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt, (hihys_en = LOW)	0.65 × VDD_Px	VDD_Px + 0.3 V	V
VIL	Low-level input voltage, CMOS/Schmitt, (hihys_en = LOW)	-0.3 V	0.35 × VDD_Px	V
VIH	High-level input voltage, CMOS/Schmitt, (hihys_en = HIGH)	0.7 × VDD_Px	VDD_Px + 0.3 V	V
VIL	Low-level input voltage, CMOS/Schmitt, (hihys_en = HIGH)	-0.3 V	0.3 × VDD_Px	V
VSHYS	Schmitt hysteresis voltage, (hihys_en = LOW)	100	–	mV
VSHYS	Schmitt hysteresis voltage, (hihys_en = HIGH)	300	–	mV
IIH	Input high leakage current (note1)	–	1	µA
IIL	Input low leakage current (note1)	-1	–	µA
IIHPD	Input high leakage current with pull-down	27.5 (60 K)	97.5 (20 K)	µA Ω
IILPU	Input low leakage current with pull-up	-97.5 (20 K)	-27.5 (60 K)	µA Ω
IOZH	High-level, tri-state leakage current (note1)	–	1	µA
IOZL	Low-level, tri-state leakage current (note1)	-1	–	µA
IOZHPD	High-level, tri-state leakage current with pulldown	27.5 (60 K)	97.5 (20 K)	µA Ω
IOZLPU	Low-level, tri-state leakage current with pullup	97.5 (20 K)	27.5 (60 K)	µA Ω
IOZHKP	High-level, tri-state leakage current with keeper (note2)	-22.5 (20 K)	-7.5 (60 K)	µA Ω

Table 3-7   DC specification of VDD_P3 = 1.8 V GPIOs

Parameter	Description	Min	Max	Units
IOZLKP	Low-level, tri-state leakage current with keeper (note2)	7.5 (60 K)	22.5 (20 K)	µA Ω
VOH	High-level output voltage, CMOS	VDD_Px - 0.45	VDD_Px	V
VOL	Low-level output voltage, CMOS	0.0	0.45	V

1. Pad voltage = VDD_Px maximum. For keeper pins, pad voltage = VDD_Px maximum - 0.45 V.
2. Pad voltage = GND and supply = VDD_Px maximum. For keeper pins, pad voltage = 0.45 V and supply = VDD_Px maximum.

Table 3-8   Digital I/O characteristics for VDD_P7 = 1.8 V nominal (SDC1)

Parameter	VDDP	Min	Typ	Max
VOH	1.8 V	VDD_Px - 0.45 V	–	–
VOL	1.8 V	--	–	0.45 V
VIH	1.8 V	0.65 × VDD_Px	–	VDD_Px + 0.3 V
VIL	1.8 V	-0.3 V	–	0.35 × VDD_Px

Table 3-9   Digital I/O characteristics for VDD_P2 = 2.95 V nominal (SDC2)

Parameter	Description	Min	Typ	Max	Units
VIH	High-level input voltage	0.625 × VDD_Px	–	VDD_P + 0.3	V
VIL	Low-level input voltage	-0.3	–	0.25 × VDD_Px	V
VHYS	Schmitt hysteresis voltage	100	–	–	mV
IIH	Input high leakage current	–	–	10	µA
IIL	Input low leakage current	-10	–	–	µA
IOZH	High-level, tri-state leakage current	–	–	10	µA
IOZL	Low-level, tri-state leakage current	-10	–	–	µA
Rpullup	Pull-up resistance	10 K	–	100 K	Ω
Rpulldown	Pull-down resistance	10 K	–	100 K	Ω
Rkeeperup	Keeper-up resistance	10 K	–	100 K	Ω
Rkeeperdown	Keeper-down resistance	10 K	–	100 K	Ω
VOH	High-level output voltage	0.75 × VDD_Px	–	VDD_Px	V
VOL	Low-level output voltage	0.0	–	0.125 × VDD_Px	V

Table 3-10   Digital I/O characteristics for VDD_P2 = 1.8 V nominal (SDC2)

Parameter	Description	Min	Typ	Max	Units
VIH	High-level input voltage	1.27	–	2	V
VIL	Low-level input voltage	-0.3	–	0.58	V
VHYS	Schmitt hysteresis voltage	100	–	–	mV
IIH	Input high leakage current	–	–	5	µA
IIL	Input low leakage current	-5	–	–	µA
IOZH	High-level, tri-state leakage current	-	–	5	µA
IOZL	Low-level, tri-state leakage current	-5	–	–	µA
Rpullup	Pull-up resistance	10 K	–	100 K	Ω
Rpulldown	Pull-down resistance	10 K	–	100 K	Ω
Rkeeperup	Keeper-up resistance	10 K	–	100 K	Ω
Rkeeperdown	Keeper-down resistance	10 K	–	100 K	Ω
VOH	High-level output voltage(note2)	1.4	–	–	V
VOL	Low-level output voltage	–	–	0.45	V

Table 3-11   Digital I/O characteristics for VDD_Px = 2.95 V nominal (UIM1 & UIM2 – Class B)

Parameter	Description	Min	Typ	Max	Units
VIH	High-level input voltage [1]	0.7 × VDD_Px	–	VDD_Px + 0.3	V
VIL	Low-level input voltage [1]	-0.3	–	0.2 × VDD_Px	V
VHYS	Schmitt hysteresis voltage [1]	100	–	–	mV
IIH	Input high leakage current	-20	–	20	µA
IIL	Input low leakage current		–	1000	µA
IOZH	High-level, tri-state leakage current	-	–	10	µA
IOZL	Low-level, tri-state leakage current	-10	–	–	µA
Rpullup	Pull-up resistance	10 K	–	100 K	Ω
Rpulldown	Pull-down resistance	10 K	–	100 K	Ω
Rkeeperup	Keeper-up resistance	10 K	–	100 K	Ω
Rkeeperdown	Keeper-down resistance	10 K	–	100 K	Ω
VOH	High-level output voltage [2]	0.8 × VDD_Px	–	VDD_Px	V
VOL	Low-level output voltage [2]	0.0	–	0.4	V

1. VIH and VIL are only applicable for I/O signal.
2. UICC specifies VOL = 0.2 × VDD_Px (RST, CLK) and 0.4 V (I/O) and VOH = 0.8 × VDD_Px (RST) and 0.7 × VDD_Px (CLK, I/O). The worst-case VOL and VOH are used in the table.

Table 3-12   Digital I/O characteristics for VDD_Px = 1.8 V nominal (UIM1 & UIM2 –Class B)

Parameter	Description	Min	Typ	Max	Units
VIH	High-level input voltage [1]	0.7 × VDD_Px	–	VDD_Px + 0.3	V
VIL	Low-level input voltage [1]	-0.3	–	0.2 × VDD_Px	V
VHYS	Schmitt hysteresis voltage [1]	100	–	–	mV
IIH	Input high leakage current	-20	–	20	µA
IIL	Input low leakage current		–	1000	µA
IOZH	High-level, tri-state leakage current	-	–	5	µA
IOZL	Low-level, tri-state leakage current	-5	–	–	µA
Rpullup	Pull-up resistance	10 K	–	100 K	Ω
Rpulldown	Pull-down resistance	10 K	–	100 K	Ω
Rkeeperup	Keeper-up resistance	10 K	–	100 K	Ω
Rkeeperdown	Keeper-down resistance	10 K	–	100 K	Ω
VOH	High-level output voltage [2]	0.8 × VDD_Px	–	VDD_Px	V
VOL	Low-level output voltage [2]	0.0	–	0.4	V

1. VIH, VIL are only applicable for I/O signal.
2. UICC specifies VOL = 0.2 × VDD_Px (RST, CLK) and 0.4 V (I/O) and VOH = 0.8 × VDD_Px (RST) and 0.7 × VDD_Px (CLK, I/O). The worst-case VOL and VOH are used in the table.

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (Figure 3-1) with respect to the drive current (drive currents are given in Table 2-1). They can be calculated using these relationships:

$$Vol[\max] = \frac{\%drive \times 450}{100} mV$$

$$Voh[\min] = Vdd\_px - \left(\frac{\%drive \times 450}{100}\right) mV$$
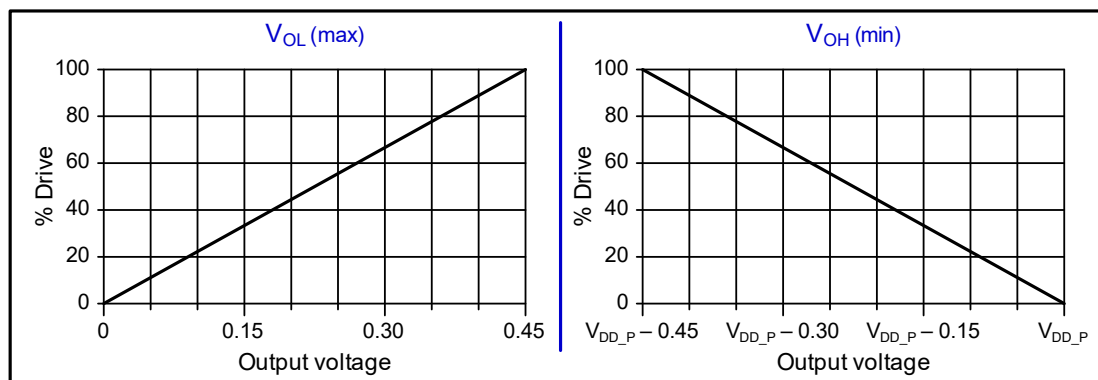
Figure 3-1   IV curve for V_{OL} and V_{OH} (valid for all V_{DD_Px})

3.6   Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its performance specifications. General comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE: All APQ8096SGE devices are characterized with actively terminated loads; all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.6.2.

3.6.1   Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-2.

Waveform	Description
	Don't care or bus is driven
	Signal is changing from low to high
	Signal is changing from high to low
	Bus is changing from invalid to valid
Keeper	Bus is changing from valid to keeper
	Bus is changing from Hi-Z to valid
	Denotes multiple clock periods

Figure 3-2   Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.

- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.

- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:

  □ For a bus type signal (multiple bits), the processor or external interface is driving a value, but the validity of the value is unknown.

  □ For a single signal, this indicates don't care.

3.6.2   Rise and fall time specifications

The testers that characterize APQ8096SGE devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-3.
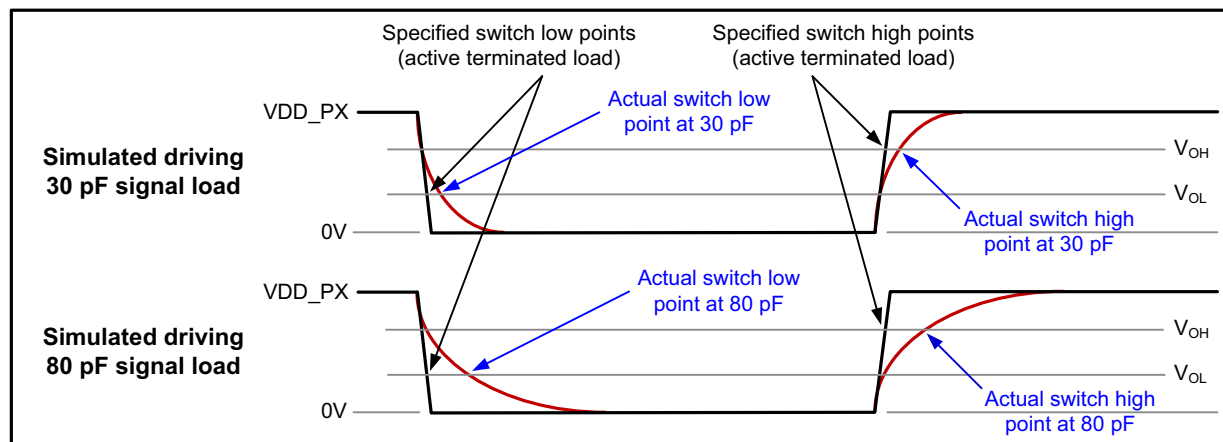
Figure 3-3   Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the APQ device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.6.3   Pad design methodology

The APQ8096SGE device uses a generic CMOS pad driver design. The intent of the pad design is to create pad response and behavior that is symmetric with respect to the associated V_{DD_PX} supply (Figure 3-4). The input switch point for pure input-only pads is designed to be $V_{DD\_PX}/2$ (or 50% of V_{DD_PX}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DD_PX} for V_{IL} and 65% of V_{DD_PX} for V_{IH}.
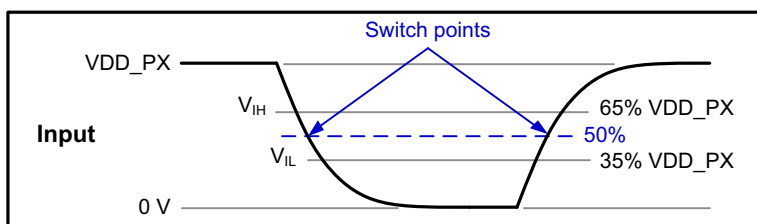
Figure 3-4   Digital input-signal switch points

Outputs (address, chip selects, clocks, etc.) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-5) are CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- $V_{OH} \sim V_{DD\_PX}$ - 50 mV or more

- $V_{OL} \sim$ 50 mV or less
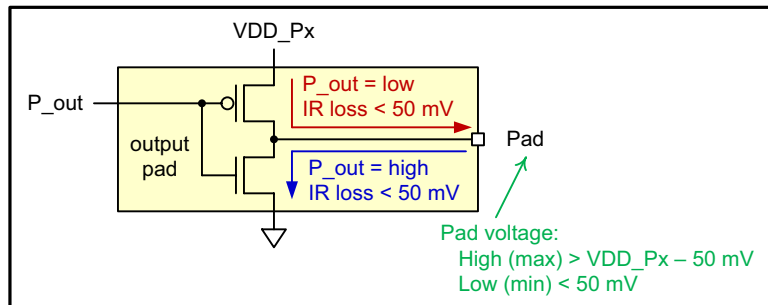
Figure 3-5   Output pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DD_PX} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at $2/3 \times [V_{OL}$ (max) - 50 mV], and 1.5 mA or more at $1/3 \times [V_{OL}$ (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at $\frac{1}{2} \times [V_{DD\_PX}$ - 50 mV + V_{OH} (min)].

The output pads are CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (**t**(r)) and fall time (**t**(f)) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described above.

3.7   Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup-time numbers will degrade and hold time numbers will increase.

3.7.1 EBI0 and EBI1 memory support

The EBI0 and EBI1 ports are dedicated to the PoP LPDDR4 SDRAM memory that is attached to the top of the APQ8096SGE chipset. The memory pinout and package requirements are specified in *PoP Memory for APQ8094 and APQ8096 Recommendations* (LM80-P2751-15).

3.7.2 eMMC on SDC1

The eMMC NAND flash can be supported through the SDC1 port. See Section 3.9.1 for secure digital interface details.

3.7.3 NOR memory on SPI

SPI can be used to support NOR memory devices with appropriate user-modified software. See Section 3.9.12 for serial peripheral interface details.

3.8 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.8.1 Camera interfaces

The APQ8096SGE device supports up to three 4-lane camera interfaces or up to four (two 4-lane and two 1-lane) camera interfaces.

Table 3-13 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification for CSI-2 v1.3	RAW7 not supported DPCM predictor 2 not supported	None
MIPI Alliance Specification for DPHY v1.2	None	None
MIPI Alliance Specification for CPHY v1.0	None	None

3.8.2 Audio support

The APQ8096SGE supports the WCD9335 audio codec IC to provide the system's audio functions. The APQ audio-related interface options with the WCD include:

- SLIMbus: Section 3.9.6
- I^2S: Section 3.9.7
- PCM: Section 3.9.8
- I^2C: Section 3.9.11

Refer to the *WCD9335 Audio Codec Device Specification* (LM80-P2751-6) for its performance characteristics.

The APQ8096SGE also supports the audio portion of HDMI using APQ-internal connections; see Section 3.8.4 for supported HDMI specifications.

3.8.3   Display support

The APQ8096SGE device supports two 4-lane MIPI_DSI interfaces.

Table 3-14   Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification for Display Serial Interface	None	None
MIPI Alliance Specification for D-PHY V1.2	None	None

3.8.4   A/V outputs

The HDMI port is supported by the APQ8096SGE.

Table 3-15   Supported HDMI standards and exceptions

Applicable standard	Feature exceptions	APQ variations
HDMI Specification Version 2.0	None	None

3.8.5   Digital video broadcast support

The APQ8096SGE supports an external digital video broadcast (DVB) solution using the following interface options:

- TSIF: Section 3.9.9
- SD: Section 3.9.1

3.9   Connectivity

The connectivity functions supported by the APQ8096SGE that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- Peripheral Component Interconnect Express (PCIe) interfaces
- User integrated module (UIM) ports, including dual-voltage options
- Serial low-power inter-chip media bus (SLIMbus) interface
- Inter-IC sound (I^2S) interfaces

- Pulse-coded modulation (PCM) interfaces

- Transport stream interface (TSIF) interfaces

- Touch screen connections

- Through proper configuration of the twelve BLSP ports:

    □ Universal asynchronous receiver/transmitter (UART) ports

    □ User identity module (UIM) ports, including dual-voltage options

    □ Inter-integrated circuit (I^2C) interfaces

    □ Serial peripheral interface (SPI) ports

Pertinent specifications for these functions are detailed in the following subsections.

NOTE: In addition to the following hardware specifications, consult the latest software release notes for software-based performance features or limitations.

3.9.1   Secure digital interfaces

Table 3-16   Supported SD standards and exceptions

Applicable standard	Feature exceptions	APQ variations
Embedded Multimedia Card (eMMC) Specification version 5.1	None	Timing specifications – see Figure 3-6
Secure Digital: Physical Layer Specification version 3.0	None	
SDIO Card Specification version 3.0	None	

Single data rate – SDR mode
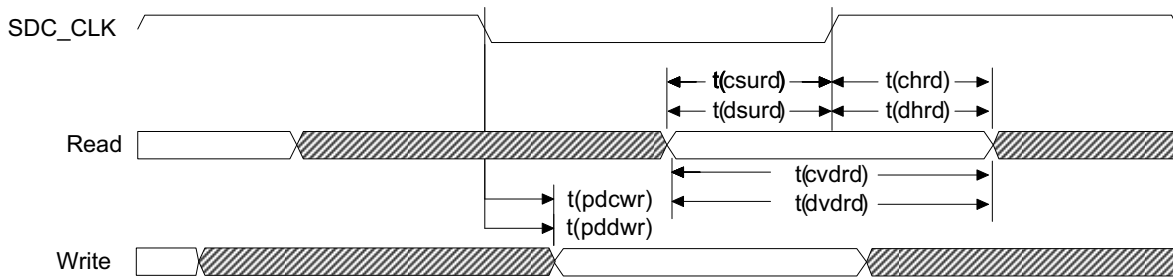
Double data rate – DDR mode
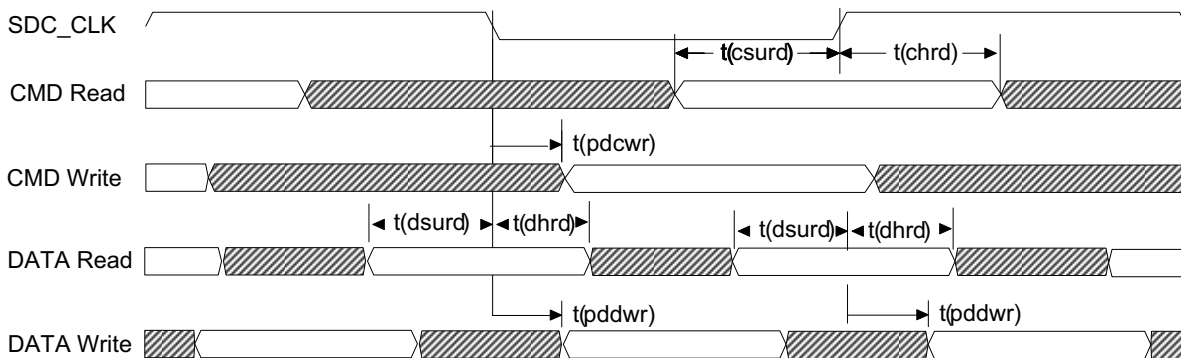
HS400 mode input timing
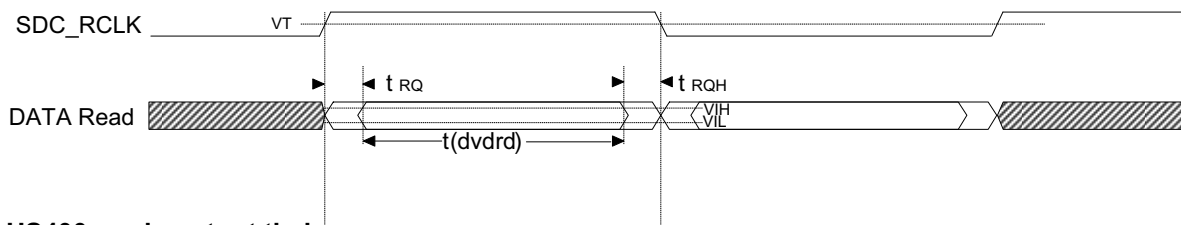
HS400 mode output timing
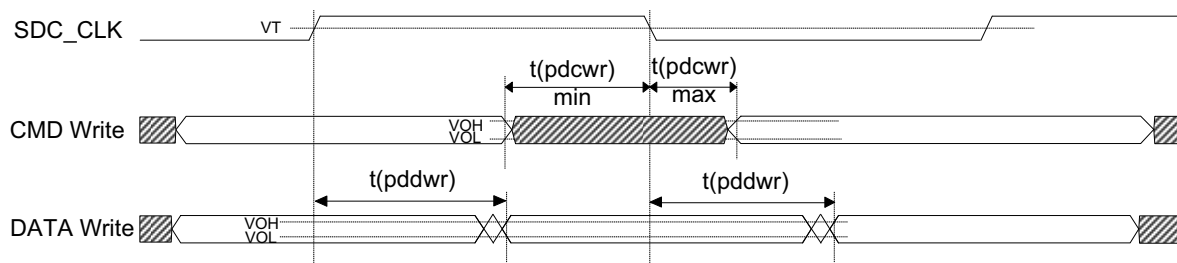
Figure 3-6   SD interface timing

3.9.2   USB interfaces

Table 3-17   Supported USB standards and exceptions

Applicable standard	Feature exceptions	APQ variations
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2	Operating voltages, system clock, and VBUS
UTMI + Low Pin Interface (ULPI) Specification (October 20, 2004 Revision 1.1 or later)	None	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	None	None

3.9.3   PCIe interface

APQ8096SGE does not support PCIe hot plug.

Table 3-18   Supported PCIe standards and exceptions

Applicable standard	Feature exceptions	APQ variations
PCI Express Specification, Revision 2.1 (March 4, 2009 or later)	None	None

3.9.4   UFS interface

Table 3-19   Supported UFS standards and exceptions

Applicable standard	Feature exceptions	APQ variations
Universal Flash Storage (UFS), Version 2.0	None	None

3.9.5   UICC interface

Table 3-20   Supported UICC standards and exceptions

Applicable standard	Feature exceptions	APQ variations
ISO/IEC 7816-3	None	None

3.9.6   SLIMbus interface

Table 3-21   Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None	None

3.9.7   I^{2}S interfaces

There are two I^{2}S interface types supported by the APQ8096SGE:

- Legacy I^{2}S interfaces for primary and secondary microphones and speakers.

- The multiple I^{2}S (MI^{2}S) interface for microphone and speaker functions, including 7.1 audio for HDMI.

The following information applies to both interface types.

Table 3-22   Supported I^{2}S standards and exceptions

Applicable standards	Feature exceptions	APQ variations
Philips I2S Bus Specifications revised June 5, 1996	None	When an external SCK clock is used, a duty cycle between 45% to 55% is required.
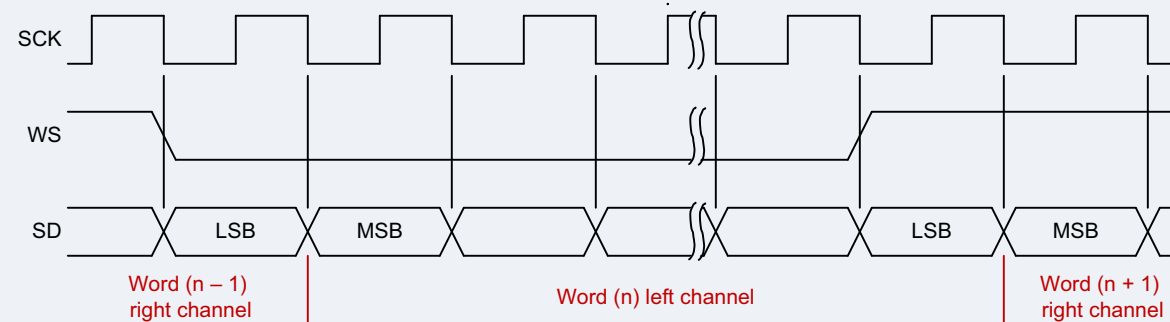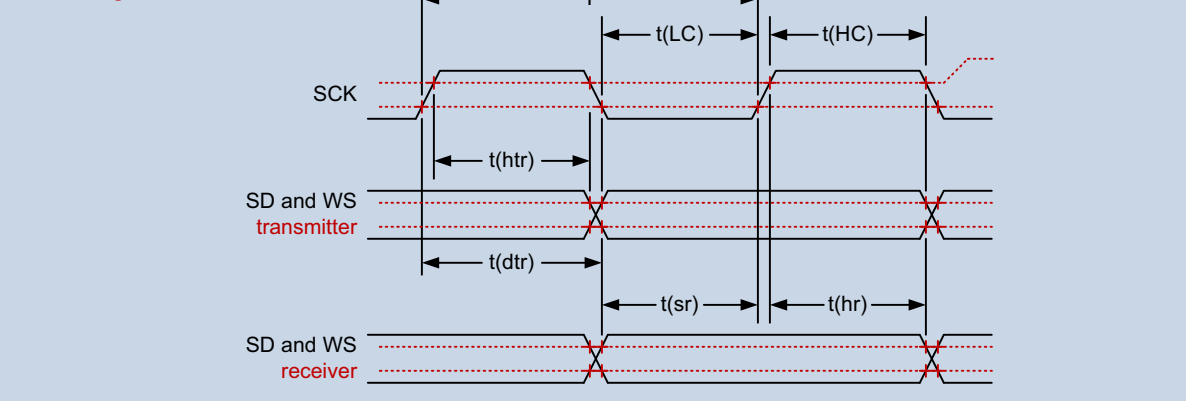
Figure 3-7   I^{2}S timing diagram

Table 3-23   I2S interface timing

Parameter		Comments [1]	Min	Typ	Max	Unit
Using internal SCK						
Frequency		–	–	–	12.288	MHz
T	Clock period	–	81.380	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	16.276	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	65.100	ns
t(htr)	SD and WS output hold time	–	0	–	–	ns
Using external SCK						
Frequency		–	–	–	12.288	MHz
T	Clock period	–	81.380	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	16.276	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	65.100	ns
t(htr)	SD and WS output hold time	–	0	–	–	ns

1. Load capacitance between 10 to 40 pF.

3.9.8   External-codec PCM interface

### 3.9.8.1   Primary PCM interface (2048 kHz clock)
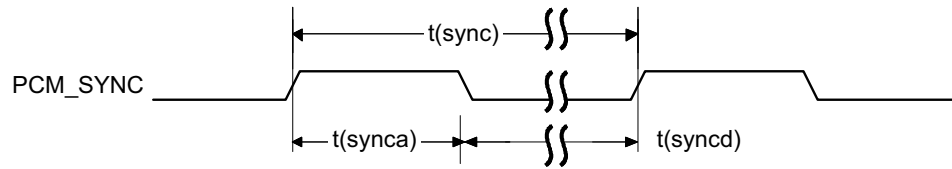
Figure 3-8   PCM_SYNC timing
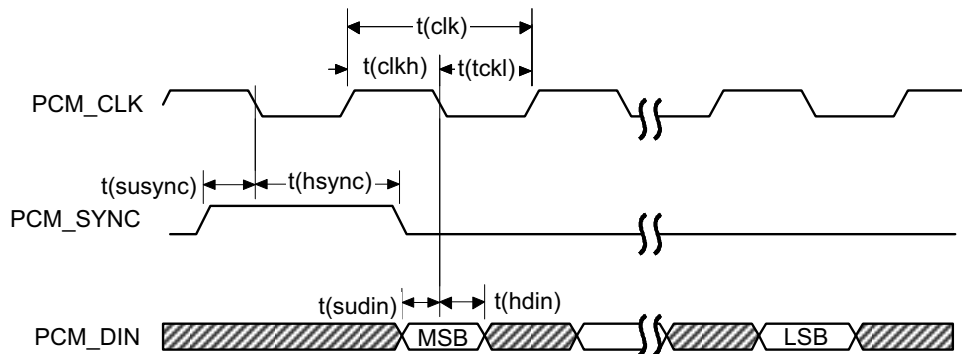
Figure 3-9   PCM_CODEC to APQ timing
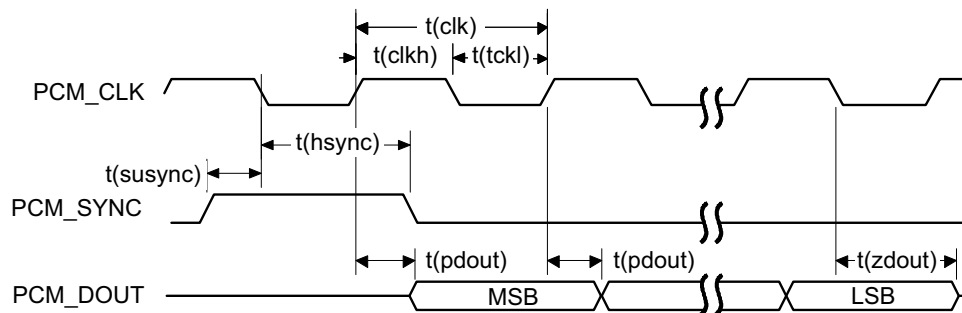
Figure 3-10   APQ to PCM_CODEC timing

Table 3-24   PCM_CODEC timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(sync)	PCM_SYNC cycle time	–	–	125	–	µs
t(synca)	PCM_SYNC asserted time	–	–	488	–	ns
t(syncd)	PCM_SYNC de-asserted time	–	–	124.5	–	µs
t(clk)	PCM_CLK cycle time	–	–	488	–	ns
t(clkh)	PCM_CLK high time	–	–	244	–	ns
t(clkl)	PCM_CLK low time	–	–	244	–	ns

Table 3-24   PCM_CODEC timing parameters (cont.)

Parameter		Comments	Min	Typ	Max	Unit
t(susync)	PCM_SYNC offset time to PCM_CLK falling	–	–	122	–	ns
t(sudin)	PCM_DIN setup time to PCM_CLK falling	–	60	–	–	ns
t(hdin)	PCM_DIN hold time after PCM_CLK falling	–	10	–	–	ns
t(pdout)	Delay from PCM_CLK rising to PCM_DOUT valid	–	–	–	350	ns
t(zdout)	Delay from PCM_CLK falling to PCM_DOUT HIGH-Z	–	–	160	–	ns

3.9.8.2   Auxiliary PCM interface (128 kHz clock)
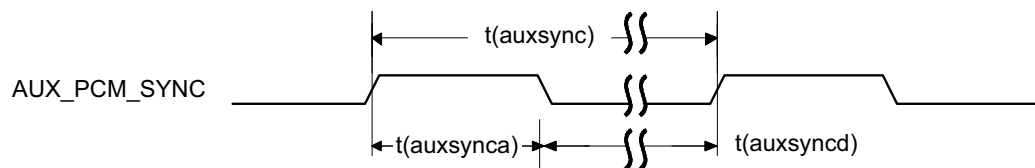
Figure 3-11   AUX_PCM_SYNC timing
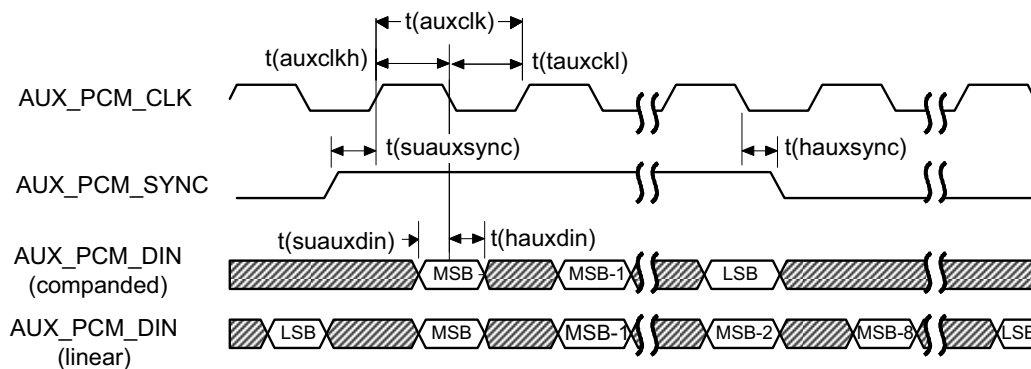
Figure 3-12   AUX_PCM_CODEC to APQ timing
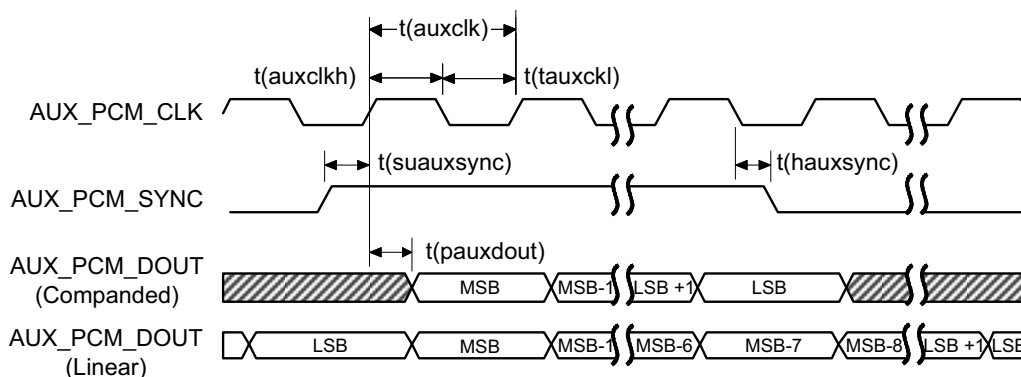
Figure 3-13   APQ to AUX_PCM_CODEC timing

Table 3-25   AUX_PCM_CODEC timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(auxsync) [1]	AUX_PCM_SYNC cycle time	–	–	125	–	µs
t(auxsynca) [1]	AUX_PCM_SYNC asserted time	–	62.4	62.5	–	µs
t(auxsyncd) [1]	AUX_PCM_SYNC de-asserted time	–	62.4	62.5	–	µs
t(auxclk) [1]	AUX_PCM_CLK cycle time	–	–	7.8	–	µs
t(auxclkh) [1]	AUX_PCM_CLK high time	–	3.8	3.9	–	µs
t(auxclkl) [1]	AUX_PCM_CLK low time	–	3.8	3.9	–	µs
t(suauxsync)	AUX_PCM_SYNC setup time to AUX_PCM_CLK rising	–	1.95	–	–	ns
t(hauxsync)	PCM_SYNC hold time after AUX_PCM_CLK rising	–	1.95	–	–	ns
t(suauxdin)	AUX_PCM_DIN setup time to AUX_PCM_CLK falling	–	70	–	–	ns
t(hauxdin)	AUX_PCM_DIN hold time after AUX_PCM_CLK falling	–	20	–	–	ns
t(pauxdout)	Delay from AUX_PCM_CLK to AUX_PCM_DOUT valid	–	–	–	50	ns

1. These values require that the CODEC_CTL is not being used to override the codec clock and sync operation.

3.9.9   TSIF

Table 3-26   Supported TSIF standards and exceptions

Applicable standard	Feature exceptions	APQ variations
ITU-T H.222.0 Transport Stream (HTS); also known as ISO/IEC 13818-1	None	None

3.9.10   Touch screen connections

Touch screen panels are supported using I^{2}C busses (Section 3.9.11) and GPIOs configured as discrete digital inputs (Section 3.5). Additional specifications are not required.

3.9.11   I^{2}C interface

Table 3-27   Supported I^{2}C standards and exceptions

Applicable standard	Feature exceptions	APQ variations
I2C Specification, version 3.0	None	HS mode, slave mode, and 10-bit addressing are not supported.

3.9.12 Serial peripheral interface

The APQ8096SGE supports serial peripheral interface (SPI) as a master only. Any one of the 12 BLSP ports can be configured as an SPI master.
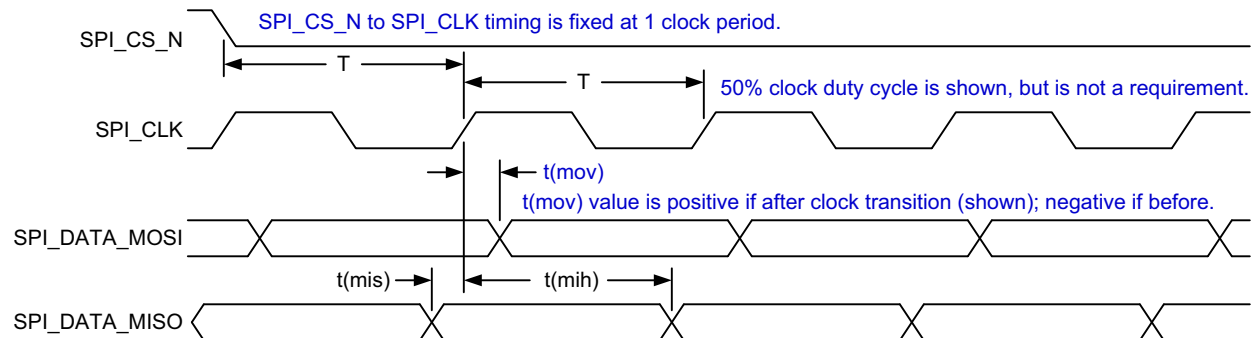

Figure 3-14   SPI master timing diagram

Table 3-28   SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	50 MHz maximum	20	–	–	ns
t(ch)	Clock HIGH	8	–	–	ns
t(cl)	Clock LOW	8	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

3.10 Internal functions

Internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.10.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified in this section.

3.10.1.1   19.2 MHz CXO input
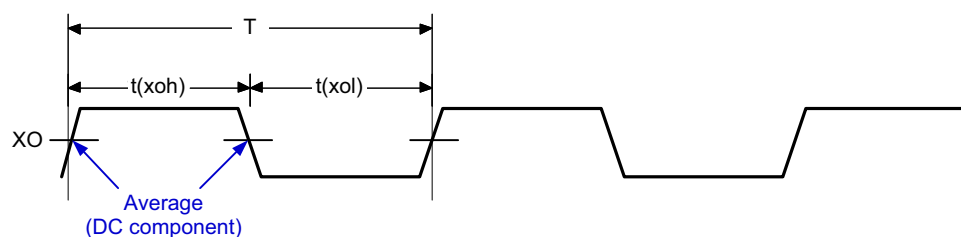
Figure 3-15   XO timing parameters

Table 3-29   XO timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	22.6	–	29.5	ns
t(xol)	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. Refer to *GPS Quality, 19.2 MHz 2016 Package Size, TH+XTAL Mini-Specification* (LM80-P2751-19) documents for more information.

3.10.1.2   CXO_2 specification
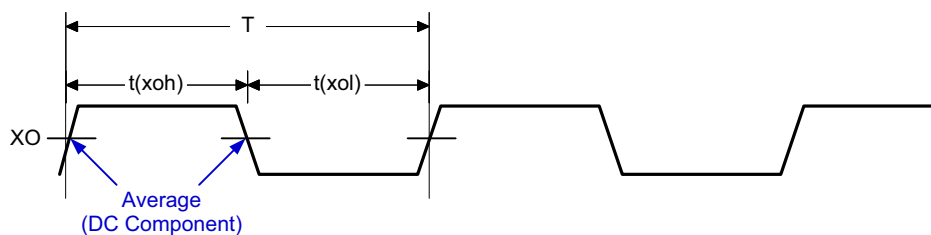
Figure 3-16   CXO_2 timing parameters

Table 3-30   CXO_2 timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	XO logic high		22.6	–	29.5	ns
t(xol)	XO logic low		22.6	–	29.5	ns
T	XO clock period		–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used	–	19.2	–	MHz

1.

3.10.1.3　Sleep clock
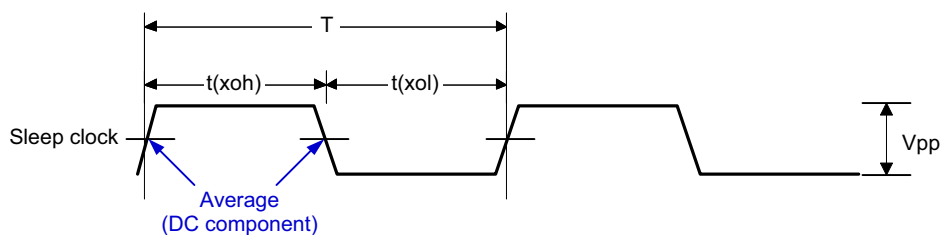
Figure 3-17　Sleep-clock timing parameters

Table 3-31　Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.518	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.10.2　Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.6.

3.10.3   JTAG
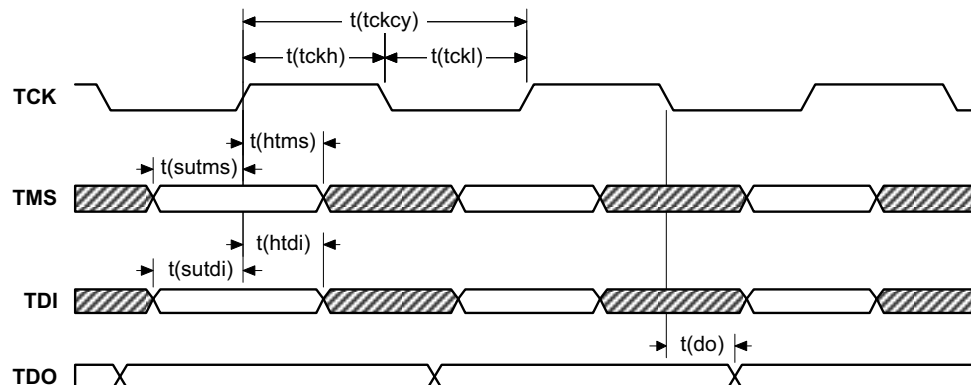
Figure 3-18   JTAG interface timing diagram

Table 3-32   JTAG interface timing characteristics

Parameter		Comments	Min	Typ	Max	Unit
t(tckcy)	TCK period	–	50	–	–	ns
t(tckh)	TCK pulse width high	–	20	–	–	ns
t(tckl)	TCK pulse width low	–	20	–	–	ns
t(sutms)	TMS input setup time	–	5	–	–	ns
t(htms)	TMS input hold time	–	20	–	–	ns
t(sutdi)	TDI input setup time	–	5	–	–	ns
t(htdi)	TDI input hold time	–	20	–	–	ns
t(do)	TDO data output delay	–	–	–	15	ns

3.10.4   Single Wire Debug (SWD)
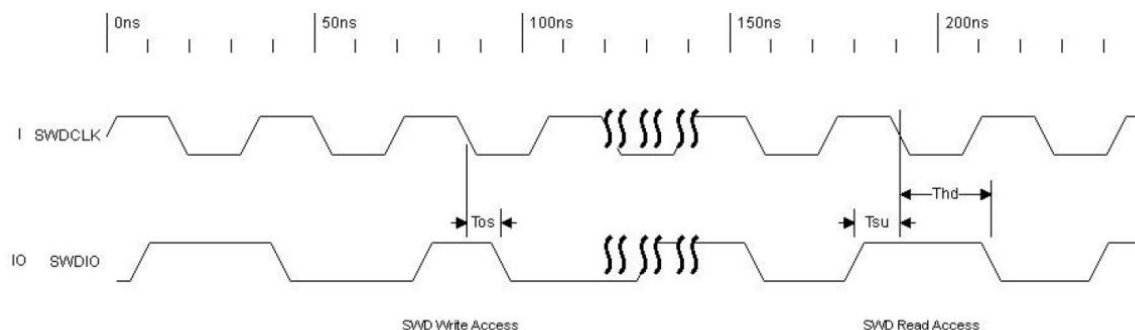
Figure 3-19   SWD write and read AC timing diagram

Table 3-33   AC timing parameters

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to falling edge of SWDCLK	0	17.5	ns
T_{su}	Input setup time between SWDIO and rising edge of SWDCLK	4	--	ns
T_{hd}	Input hold time between SWDIO and rising edge of SWDCLK	1	--	ns

3.11 Power management interfaces

The supported chipset interfaces are listed in Table 3-34. The digital I/Os must meet the logic-level requirements specified in Section 3.5. The Rx and Tx baseband interfaces are proprietary, and are not specified.

3.11.1   System power management interface (SPMI)

Table 3-34   Supported SPMI standards and exceptions

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None	None

4   Mechanical information

4.1   Device physical dimensions

The APQ8096SGE device is available in the 994C MNSP [1], a 15.6 × 15 × 0.64 mm PoP system (height dimension does not include the memory device). Its bottom footprint is equivalent to a 994-pad nanoscale package (994 NSP), and it accepts memory modules from above that are equivalent to a 387-pad chip-scale package (387 CSP). The bottom includes many ground pins for electrical grounding, mechanical strength, and thermal continuity. Pad A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the 994C MNSP outline drawing is shown in Figure 4-1.

---

1. The letter 'C' in the package designator (994C MNSP) is used to distinguish this package from another QTI package that uses the package designator '994 MNSP'.

Figure 4-1   994C MNSP (15.6 × 15 × 0.64 mm) outline drawing
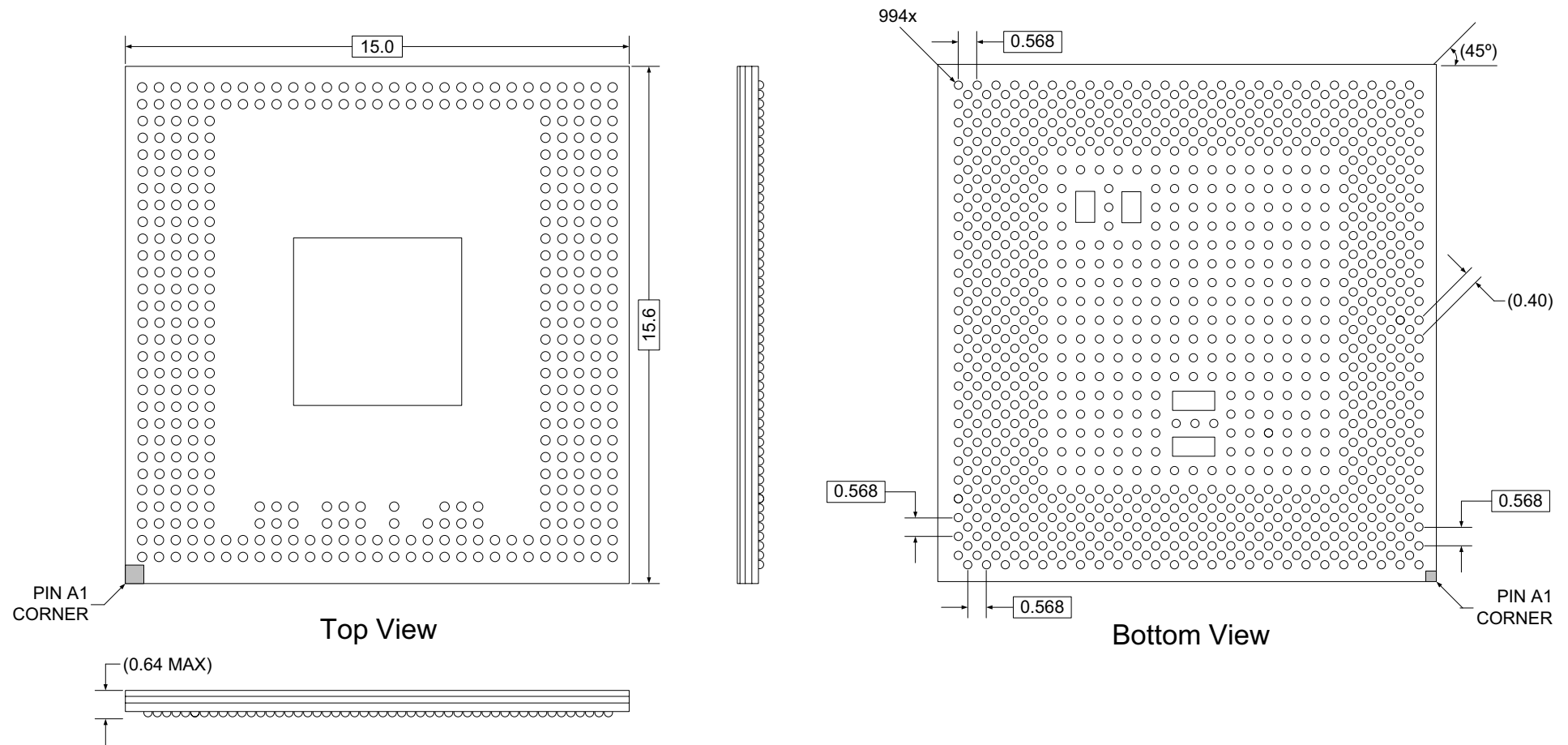
NOTE: This is a simplified outline drawing.

NOTE: The co-planarity specification for the APQ8096SGE bottom package is 130 μm.

4.2   APQ8096SGE part marking
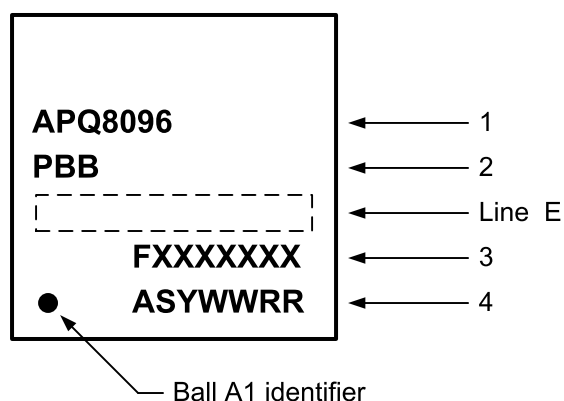
Figure 4-2   APQ8096SGE device marking (top view, not to scale)

Table 4-1   APQ8096SGE marking line definitions

Line	Marking	Description
1	APQ8096SGE	QTI product name
2	PBB	P = product configuration code ■ See Table 4-3 for assigned values. BB = feature code ■ See Table 4-3 for assigned values.
E	Blank or random	Additional content as necessary
3	FXXXXXXX	F = supply source code ■ F = J (Samsung) ■ XXXXXXX = traceability number
4	AXYWWRR	A = assembly site code ■ A = C (Amkor, South Korea) ■ A = X (Amkor, Japan) S = traceability number Y = single-digit year WW = work week (based on calendar year) RR = product revision (See Table 4-3 for assigned values)

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Figure 4-3, and explained below.

Device ID code ▶	AAA-AAAA	— P	— CCC	DDDD	— EE	— RR	— S	— BB
Symbol definition ▶	Product name	Config code	Number of pins	Package type	Shipping package	Product revision	Source code	Feature code
Example ▶	MSM-8996	— 0	— 994	CMNSP	— TR	— 02	— 0	— AB

Feature code (BB) is not always included when identifying older devices.

Figure 4-3 Device identification code

Device identification details for all samples available to date are summarized in Table 4-2.

Table 4-2 APQ8096SGE device identification details [1]

Device	Product configuration code (*P*)	Product revision (*RR*)	Hardware revision number	Sample type	BB value	Feature ID	Comments
APQ8096SGE	1	02	0x2 003E 0E1	ES2.1	AB	00	APQ8096SGE 994C MNSP, Kryo CPU, A530 GPU SSC, HVX
APQ8096SGE	1	03	0x3 003E 0E1	ES3.0	AB	00	APQ8096SGE 994C MNSP, Kryo CPU, A530 GPU SSC, HVX
APQ8096SGE	1	04	0x4 003E 0E1	ES3.1	AB	00	APQ8096SGE 994C MNSP, Kryo Gold 2.15 GHz, A530 GPU: 624 MHz: SSC, HVX
APQ8096SGE	1	04	0x4 003E 0E1	ES3.1.3/CS	AB	14	APQ8096SGE 994C MNSP, Kryo Gold 2.15 GHz, A530 GPU: 624 MHz: SSC, HVX

1. APQ8096SGE devices with date code YWW ≥ 543 are CS parts.

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-3.

Table 4-3   MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	$\leq$ 30°C/85% RH
2	1 year	$\leq$ 30°C/60% RH
2a	4 weeks	$\leq$ 30°C/60% RH
3	168 hours	$\leq$ 30°C/60% RH; **APQ8096SGE rating**
4	72 hours	$\leq$ 30°C/60% RH
5	48 hours	$\leq$ 30°C/60% RH
5a	24 hours	$\leq$ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	$\leq$ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The Qualcomm® Snapdragon™ 820 Processor APQ8096SGE devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) must not be confused with the peak temperature within the recommended solder reflow profile; see Section 6.2 for more details.

5 Carrier, handling, and storage information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the APQ8096SGE tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.
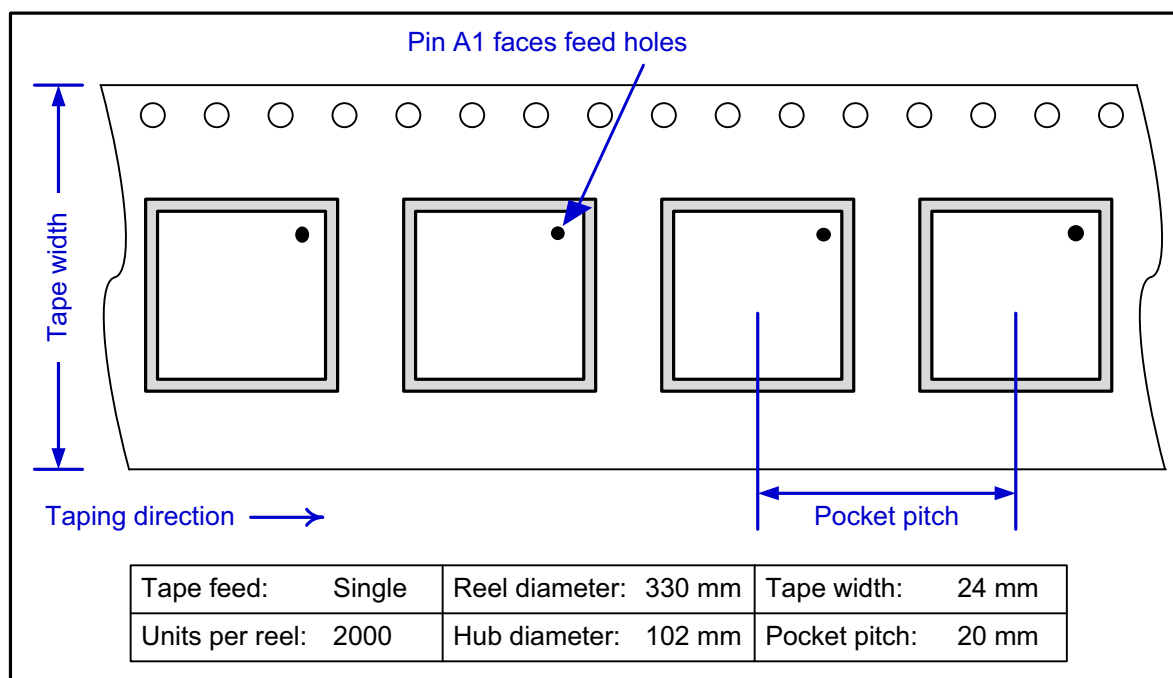

Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	102 mm	Pocket pitch:	20 mm

Figure 5-1   Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

Handle only at the edges
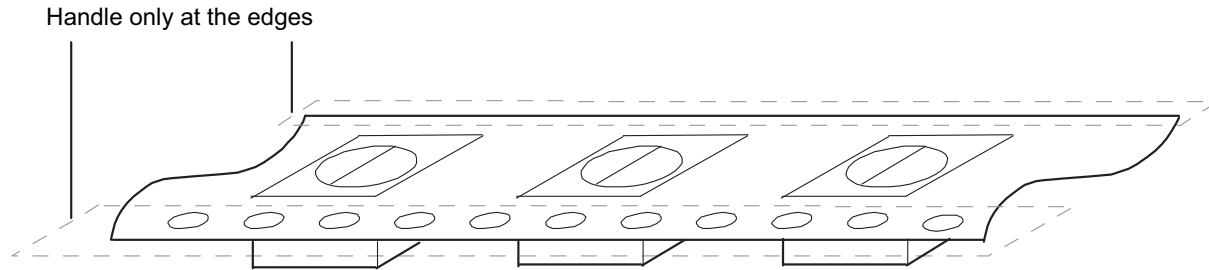
Figure 5-2   Tape handling

5.2   Storage

5.2.1   Bagged storage conditions

APQ8096SGE devices delivered in tape and reel carriers must be stored in sealed, moisture-barrier, anti-static bags.

5.2.2   Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3   Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1   Baking

It is **not necessary** to bake the APQ8096SGE if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the APQ8096SGE if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices must not be baked in tape and reel carriers at any temperature.

5.3.2   Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage will result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

See Chapter 7 for the APQ8096SGE ESD ratings.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS (restriction of hazardous substances) directive. Its SnAgCu solder balls use SAC305 composition on the top and SAC125/Ni on the bottom. A product material declaration (PMD), which provides RoHS and other product environmental governance information, will be published when the data is available.

6.2 Surface mount technology parameters

This section describes QTI board-level characterization process parameters. This information is included to assist customers with their surface mount technology (SMT) process development, but it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

The land pattern and stencil recommendations presented in this section are based on QTI internal characterizations for lead-free solder pastes on an eight-layer PCB, built primarily to the specifications described in JEDEC JESD22-B111.

QTI recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

General land pattern guidelines:

- Non-solder mask defined (NSMD) pads provide the best reliability.
- Keep the solderable area consistent for each pad, especially when mixing via-in-pad and non-via-in-pad in the same array.
- Avoid large solder mask openings over ground planes.
- Traces for external routing are recommended to be less than or equal to half the pad diameter, to ensure consistent solder-joint shapes.

6.2.2 Stacked-package dip process

The APQ8096SGE is a PoP device, which requires the memory package to be assembled using a paste or flux dip process; based on internal development results, the flux dip process is recommended. For production assembly, single-pass reflow is preferred over pre-stacking the devices. The flux film depth must be adjusted to achieve a target thickness of at least 50% of the solder-ball height (Figure 6-1). The film thickness must be set based on empirical measurement rather than machine set points. QTI internal characterizations were performed using a flux film thickness of 150 microns.
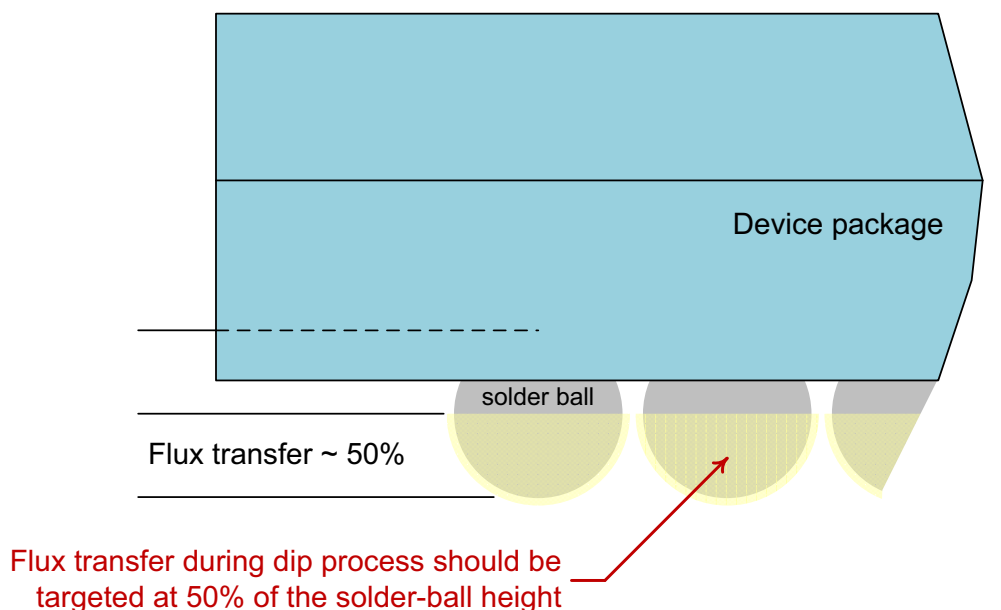

Device package

solder ball

Flux transfer ~ 50%

Flux transfer during dip process should be targeted at 50% of the solder-ball height

Figure 6-1 Flux transfer during dip process

6.2.3 Reflow profile

Reflow profile conditions typically used by QTI for lead-free systems are listed in Table 6-1, and are shown in Figure 6-2.

Table 6-1 QTI typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temperature range	Condition
Preheat	Initial ramp	< 150°C	3°C/s maximum
Soak	Flux activation	150–190°C	60 to 75 s
Ramp	Transition to liquidus (solder-paste melting point)	190–220°C	< 30 s
Reflow	Time above liquidus	220–245°C [1]	50–70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/s maximum

1. During the reflow process, the recommended peak temperature is 245°C (minimum). This temperature must not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.4.
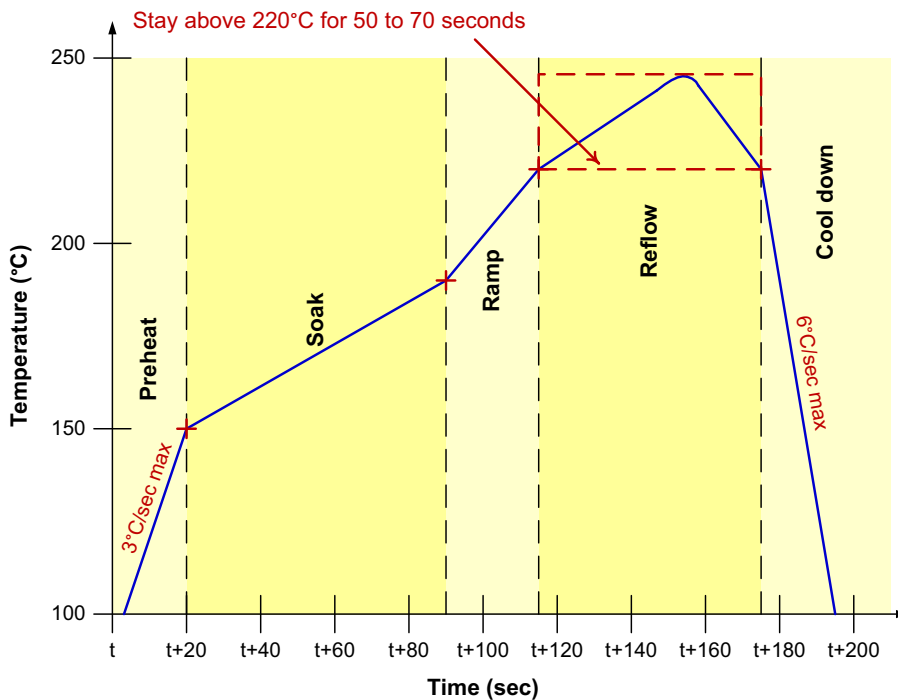
Figure 6-2   QTI typical SMT reflow profile

6.2.4   SMT peak package-body temperature

This document states a peak package-body temperature in three other places within this document. The three places are listed below, along with an explanation of the stated value and its meaning within that section's context.

- Section 4.4: Device moisture sensitivity level

  APQ8096SGE devices are classified as MSL3 at 260°C +0/-5°C. The temperature included in this designation is the lower limit of the range stated for moisture resistance testing during the device qualification process, as explained immediately below.

- Chapter 7: Reliability qualifications summary

  One of the tests conducted for device qualification is the moisture resistance test. QTI follows J-STD-020-C, and hits a peak reflow temperature that falls within the range of 260°C +0/-5°C (255°C to 260°C).

- Section 6.2.3: Reflow profile

  During a production board's reflow process, the temperature experienced by the package must be controlled. Obviously, the temperature must be high enough to melt the solder and provide reliable connections, but it must not go so high that the device can be damaged. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more).

6.2.5   SMT process verification

QTI recommends verification of the SMT process prior to high-volume board assembly, including:

- In-line solder-paste deposition monitoring
- Reflow profile measurement and verification
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder-ball shape, and voiding

6.3   Board-level reliability

QTI conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing: optional (JESD22-B113)

7 Part reliability

7.1 Reliability qualifications summary

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108-A Total samples from three different wafer lots	> 1000	Pass DPPM < 1000
HTOL in FIT ($ƒÜ$) failure in billion device hours HTOL: JESD22-A108-A Total samples from three different wafer lots	> 1000	Pass FIT < 50
Mean time to failure (MTTF) t = 1/$ƒÜ$ in million hours Total samples from three different wafer lots	> 1000	> 20
ESD – Human-body model (HBM) rating JESD22-A114-F Target 1000 V Total samples from one wafer lot	3	±1000 V
ESD – Charge-device model (CDM) rating JESD22-C101-D Target 250 V Total samples from one wafer lot	3	±250 V
Latch-up (I-test): EIA/JESD78C Trigger current: ±100 mA; temperature: 85°C Total samples from one wafer lot	6	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78C Trigger voltage: stress at 1.5 × Vdd maximum per device specification; temperature: 85°C Total samples from one wafer lot	6	Pass

Table 7-2   Package reliability results

Tests, standards, and conditions	Amkor, South Korea sample size	Amkor, Japan sample size	Result
Moisture resistance test (MRT): J-STD-020-C Reflow @ 260 +0/-5°C, MSL3 Total samples from three different assembly lots	462	462	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8-10 minutes Cycle rate: 2 cycles per hour (CPH) Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	231	231	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hours duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	231	231	Pass
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, and 1000 hours Total samples from three different assembly lots	231	231	Pass
Flammability: UL-STD-94 Flammability test – not required Qualcomm's ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, provided the devices are mounted on materials rated V-1. In general, PWBs onto which Qualcomm's ICs are mounted are rated V-0 (better than V-1).	–	–	See note under test column
Physical dimensions: JESD22-B100-B Case outline drawing: Qualcomm internal document Total samples from three different assembly lots	75	75	Pass
Solder ball shear: JESD22-B117A Total samples from three different assembly lots	30	30	Pass
Internal/external visual Ball diameter, height, and x-ray Total samples from three different assembly lots	30	30	Pass

7.2 Qualification sample description

Device characteristics

Device name: APQ8096SGE

Package type: 994C MNSP

Package body size: 15.6 mm × 15 mm × 0.64 mm

Fab process: 14 nm FinFET

Fab sites: Samsung

Assembly sites: Amkor

Solder ball pitch: 0.4 mm

EXHIBIT 1

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    1.5   LIMITATION OF LIABILITY. IN NO EVENT SHALL QTI, QTI'S AFFILIATES OR ITS LICENSORS BE LIABLE TO YOU FOR ANY INCI-DENTAL, CONSEQUENTIAL OR SPECIAL DAMAGES, INCLUDING BUT NOT LIMITED TO ANY LOST PROFITS, LOST SAVINGS, OR OTHER INCI-DENTAL DAMAGES, ARISING OUT OF THE USE OR INABILITY TO USE, OR THE DELIVERY OR FAILURE TO DELIVER, ANY OF THE MATERIALS, OR ANY BREACH OF ANY OBLIGATION UNDER THIS AGREEMENT, EVEN IF QTI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. THE FOREGOING LIMITATION OF LIABILITY SHALL REMAIN IN FULL FORCE AND EFFECT REGARDLESS OF WHETHER YOUR REMEDIES HERE-UNDER ARE DETERMINED TO HAVE FAILED OF THEIR ESSENTIAL PURPOSE. THE ENTIRE LIABILITY OF QTI, QTI's AFFILIATES AND ITS LICEN-SORS, AND THE SOLE AND EXCLUSIVE REMEDY OF YOU, FOR ANY CLAIM OR CAUSE OF ACTION ARISING HEREUNDER (WHETHER IN CONTRACT, TORT, OR OTHERWISE) SHALL NOT EXCEED US$10.

2.   COMPLIANCE WITH LAWS; APPLICABLE LAW.

Any litigation or other dispute resolution between You and Us arising out of or relating to this Agreement, or Your relationship with Us will take place in the Southern District of California, and You and QTI hereby consent to the personal jurisdiction of and exclusive venue in the state and federal courts within that District with respect any such litigation or dispute resolution. This Agreement will be governed by and construed in accordance with the laws of the United States and the State of California, except that body of California law concerning conflicts of law. This Agreement shall not be governed by the United Nations Convention on Contracts for the Interna-tional Sale of Goods, the application of which is expressly excluded.

3.   CONTRACTING PARTIES. If the Materials are downloaded on any computer owned by a corporation or other legal entity, then this Agreement is formed by and between QTI and such entity. The individual accepting the terms of this Agreement represents and warrants to QTI that they have the authority to bind such entity to the terms and conditions of this Agreement.

4.   MISCELLANEOUS PROVISIONS. This Agreement, together with all exhibits attached hereto, which are incorporated herein by this reference, constitutes the entire agreement between QTI and You and supersedes all prior negotiations, representations and agreements between the parties with respect to the subject matter hereof. No addition or modification of this Agreement shall be effective unless made in writing and signed by the respective representatives of QTI and You. The restrictions, limitations, exclusions and conditions set forth in this Agreement shall apply even if QTI or any of its affiliates becomes aware of or fails to act in a manner to address any violation or failure to comply therewith. You hereby acknowledge and agree that the restrictions, limitations, conditions and exclusions imposed in this Agreement on the rights granted in this Agreement are not a derogation of the benefits of such rights. You further acknowledges that, in the absence of such restrictions, limitations, conditions and exclusions, QTI would not have entered into this Agreement with You. Each party shall be responsible for and shall bear its own expenses in connection with this Agreement. If any of the provisions of this Agreement are determined to be invalid, illegal, or otherwise unenforceable, the remaining provi-sions shall remain in full force and effect. This Agreement is entered into solely in the English language, and if for any reason any other language version is prepared by any party, it shall be solely for convenience and the English version shall govern and control all aspects. If You are located in the province of Quebec, Canada, the following applies: The Parties hereby confirm they have requested this Agreement and all related documents be prepared in English.