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Recent developments in the CBC3, a CMS micro-strip readout ASIC for track-trigger modules at the HL-LHC

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Abstract

The CMS Binary Chip (CBC) is the front-end readout ASIC planned for the outermost layers of the CMS Phase 2 silicon outer tracker. Results from an extensive irradiation campaign carried out on the CBC3, the first version of the ASIC to include the full trigger logic circuitry, have demonstrated that the chip is capable of withstanding the levels of radiation expected at the HL-LHC, with only a slight (< 1%) increase in power consumption. Results from the irradiation campaign, and details of the novel damage model developed to describe the measurements and extrapolate to the final operating conditions, will be presented.

Keywords: Tracking detectors, Radiation Effects, Total Ionizing Dose, ASICs
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1. Introduction

The Phase-2 CMS silicon tracker upgrade [1] will have to provide high-quality physics data while operating at the extreme beam intensities and particle collision rates foreseen at the high-luminosity upgrade of the Large Hadron Collider (HL-LHC). The outer tracker (OT) will be built from double-layered modules, each consisting of two strip (2S), or one pixel and one strip (PS) silicon sensors.

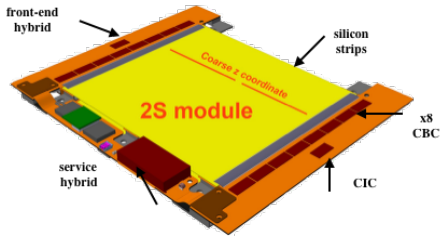

Figure 1: Conceptual diagram of a 2S module: two front-end hybrids containing sixteen CBC3s will read out the full module and perform the stub finding for the L1 trigger. A single service hybrid will provide power and data connectivity.

A single module can identify high transverse momentum tracks by looking for a pair of coincident hits (a stub) in nearby channels in the two closely separated sensors. Stubs from different layers can then be combined into tracks in off-detector electronics. The CMS Binary Chip (CBC) is a 254-channel front-end ASIC manufactured in 130 nm CMOS technology for the readout of the 2S modules (shown in fig. 1). The CBC3 [2], manufactured in a 130 nm CMOS technology, is the final prototype of the ASIC and the first to include the full logic circuitry required for stub finding.

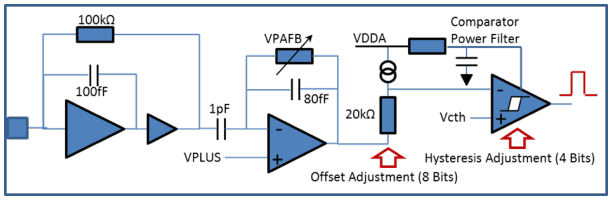

Figure 2: Simplified block diagrams describing the CBC3's analogue front-end.

Total ionizing dose (TID) tests performed on the previous prototype [3] of the CBC showed a large increase in current and corresponding disruption of the internal test-pulse circuitry [4]. These were attributed to radiation-induced leakage in the

SRAM block of the pipeline logic, motivating the decision to modify the SRAM block in the CBC3.

In this report the results of an X-ray irradiation campaign measuring the radiation-tolerance of the CBC3 are reported. A radiation damage model, developed to extrapolate the results to HL-LHC operating conditions, will also be described.

2. Experimental Procedure

Nine CBC3 chips were irradiated at a variety of dose rates (0.11 ± 0.02 kGy/h to 23.0 ± 4.6 kGy/h) and temperatures (-20 °C to 5 °C). All irradiations were performed using the CERN Seifert RP149 X-ray machine. The machine's high-power cooling system was used to control the temperature of the chips, monitored using a thermocouple placed close to the chip, during irradiation. The dose rates were measured, with an uncertainty of 20%, using a calibrated PIN diode connected to a source-measure unit with a high-precision ammeter.

To replicate realistic operating conditions, a prototype DAQ system was used to provide the 320 MHz system clock, slow-control I2C commands, and clock-synchronous fast commands such as triggers and resets. The chips were wire-bonded to carrier boards plugged into an interface card, which provided the low voltage (1.25V) and level translation to interface to the DAQ. The interface card also provided monitoring of the digital and analogue currents, and the on-chip analogue bias signals (via an on-chip 17:1 analogue multiplexer).

3. Results

3.1. Current Consumption

The current consumption of the digital and analogue circuits recorded during the irradiation of a CBC3 at 23 kGy/h is shown in Figure 3.

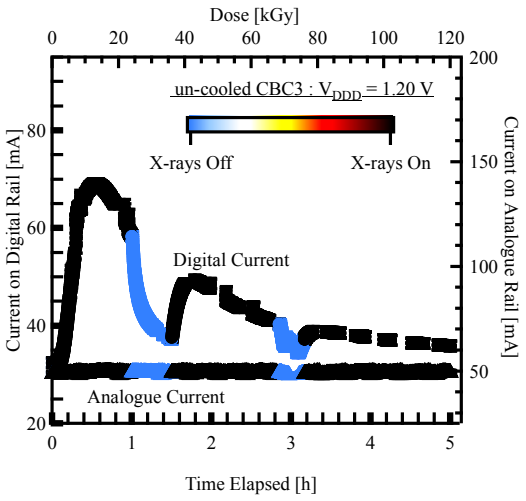

Figure 3: Measured CBC3 digital (left axis) and analogue (right axis) currents during exposure to X-rays at the CERN X-ray irradiation facility. The color of the marker indicates the state of the X-ray machine during the measurement.

The radiation-induced leakage current observed in the previous version of the chip is still present in the CBC3. The current consumed, by the digital circuitry on the ASIC, begins to increase after a few kGy of ionizing dose. It continues to increase up to a dose of approximately 15 kGy , beyond which it decreases exponentially towards the initial value.

The initial irradiation was performed at a dose rate ten thousand times higher than that expected for the 2S modules closest to the interaction point, and a temperature 47 °C warmer than that expected in chips deployed in the Phase-2 OT. Determining the magnitude of the current increase under realistic HL-LHC operating conditions therefore requires an understanding of the effect of temperature and dose rate on the radiation induced leakage current. This motivated the undertaking of the series of measurements at different temperatures and dose rates summarized in Figure 4.

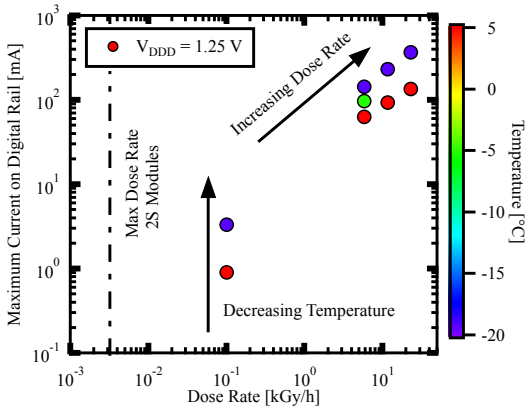

Figure 4: The (maximum) measured current consumption on the CBC3's digital rail as a function of dose rate. The color of the markers indicates the temperature at which the irradiation took place. All measurements were performed using a bias voltage of 1.25 V.

Figure 4 demonstrates that the radiation induced increase in current rises for decreasing temperatures and increasing dose rates. The temperature of the CBCs when deployed in the Phase-2 OT is expected to range from -17 °C to -9 °C ; and the expected dose rate, indicated by a dashed line in Figure 4, is approximately $1/50^{\text{th}}$ of the lowest dose rate reached in the X-ray irradiations.

3.2. Analogue Front-End Performance

To verify the robustness of the CBC3's analogue front-end against damage from ionizing radiation all parameters critical to its operation were monitored throughout the irradiation periods. This included checking the behavior of the analogue bias registers, verification of the on-chip pipeline by measuring the response of the chip to the internal test pulse, and continuous monitoring of the pedestal and the noise.

Of the analogue biases monitored during the X-ray irradiations two are considered the most important: the output of the band-gap reference (V_{BG}) circuit and the comparator threshold

voltage (V_{cth}). V_{BG} because it is the reference for all on-chip analogue biases, and V_{cth} because it determines the global comparator threshold (shown in Figure 2). The resolution of V_{th}, provided by a 10 bit resistor ladder digital to analogue converter (DAC) with reference voltages provided by the analogue supply rail (V_{DDA}) and the on-chip ground (GND), is given by

$$V_{cth}\ [\frac{\text{mV}}{\text{DAC units}}] = \frac{V_{DDA} - GND}{1024} = \frac{2V_{BG} - GND}{1024}, \quad (1)$$

where V_{DDA} is twice V_{BG}.

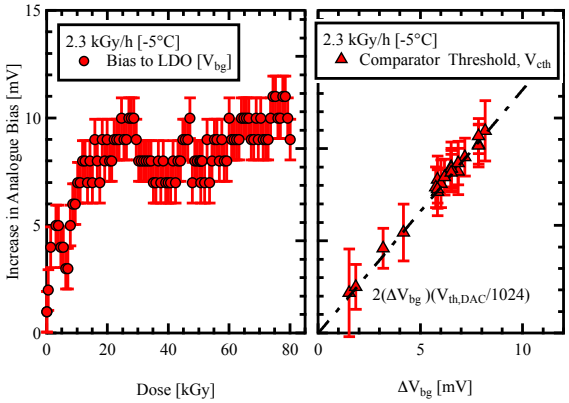

Figure 5: Two of the on-chip analogue biases during irradiation; the bias to the on-chip Low Dropout Regulator (LDO) powers the analogue front-end circuits on the CBC3, and the comparator threshold corresponds to the output of the bias DAC at the nominal threshold setting of ≈580 DAC units.

The evolution of the band-gap reference voltage during irradiation, and the corresponding change in V_{cth}, for a chip irradiated at 2.3 kGy/h and a temperature of -5 °C is shown in Figure 5. It shows that the measured 10 mV increase ($O(2\%)$) in the band-gap reference voltage of the chip is within the expected range (±12 mV) for the standardized circuit used in the CBC3 [5]; and the measured increase in the threshold voltage is as expected from Equation (1).

The noise and pedestal in a binary system such as the CBC3 must be inferred from an S-curve which shows the fraction of events, for a fixed number of triggers, in which a hit is detected as a function of the comparator threshold V_{cth}. Examples of S-curves collected during an irradiation are shown in Figure 6. Fitting the S-curve with a sigmoid of the form :

$$f(x, \mu, \sigma) = \frac{1}{2}[1 + \text{erf}(\frac{x - \mu}{\sqrt{2}\sigma})], \quad (2)$$

returns the pedestal (μ) and noise (σ). S-curves were also used to test the response of the CBC3 to the internal test pulse, by using the on-chip test pulse to inject charge into all 254 input channels on the CBC3. As Figure 6 shows, the CBC3 remains responsive to the test pulse in the presence of a large leakage current (≈ 200 mA). This indicates that enclosing the pipeline logic in this iteration of the chip mitigated the effects observed in the previous version. The noise and pedestals measured for different dose rates are shown in Figure 7. It shows

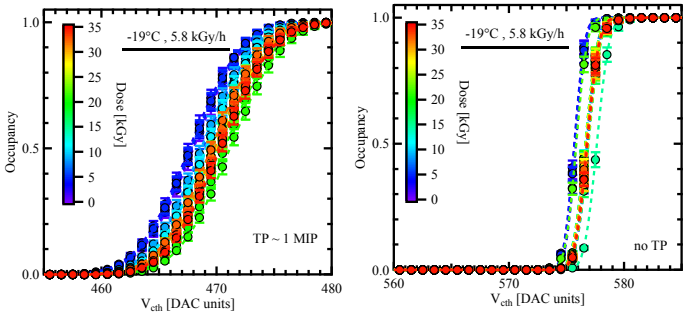

Figure 6: S-curves measured during the irradiation period: (left) using the on-chip test pulse to inject charge equivalent to 1 MIP, and (right) with no charge injected.The color of the markers indicates the dose received at the time of measurement, and the dashed lines the result of the fit using Equation (2).

that the increase in noise observed during irradiation at high dose rate is correlated with the radiation induced leakage current; no change in the noise is observed as long as the increase in current remains below 10 mA .

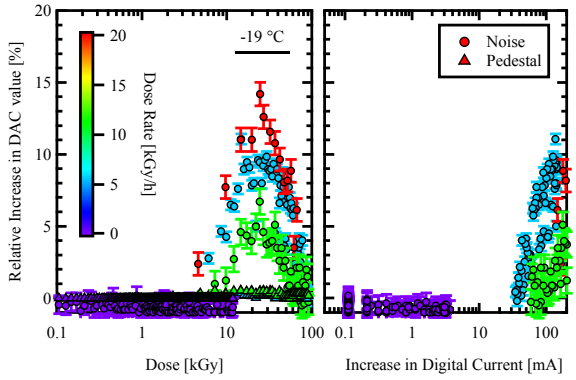

Figure 7: Noise and pedestal measured for different dose rates: (left) both as a function of dose, and (right) correlation between noise and increase in digital current.The color of the markers indicates the dose rate at which the irradiation took place.

4. Radiation Damage Model

The data collected with the CERN X-ray source (Figure 4) was used to develop a model capable of predicting an upper limit for the expected current increase in a 2S module under HL-LHC operating conditions. The model is an expansion upon the leakage current model proposed by Backhaus et al [6], where the leakage current is attributed to the creation of leakage paths between source and drain via the inversion layer. The leakage current paths are described as parasitic transistors, each with a transfer characteristic given by

$$I_D \approx 0 \quad : N_{\text{eff}} < N_{\text{thr}} \quad (3)$$

$$I_D \approx K_0\,(N_{\text{eff}} - N_{\text{thr}})^2 \quad : N_{\text{eff}} \geq N_{\text{thr}}, \quad (4)$$

where N_{eff} is the effective number of charges located in the inversion layer created in the silicon by the build-up of positive charge in the oxide, N_{thr} is the threshold number of charges required to activate the transistor, and K_0 is a proportionality constant.

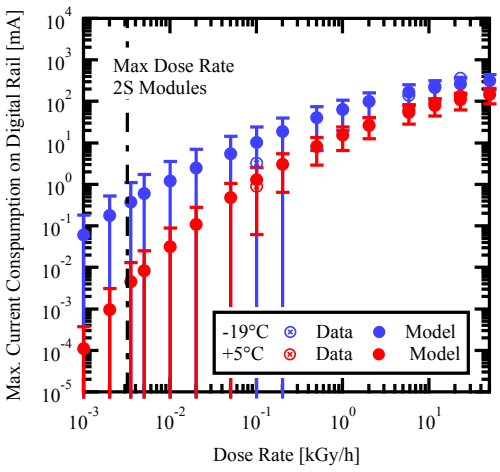

Figure 8: The size of reconstructed clusters in strips (635 μm strip pitch) for both readout coordinates of the central detector.

The effective number of charges in the transistor can be expressed as

$$N_{\text{eff}} = N_{\text{OT}} - N_{\text{IT}}. \tag{5}$$

where N_{OT} and N_{IT} are the positive trapped charge and interface traps created [7] when electron-hole pairs (ehps) generated by ionizing radiation interact with existing defects and impurities in the oxide. Holes that survive the initial prompt recombination can move throughout the oxide bulk using existing defect sites. As they travel they may be trapped by deep traps located in the oxide which creates trapped positive charge N_{OT}; depending on the energy level(s) of the traps and the temperature of the device during irradiation trapped holes have a finite probability of escaping. Holes not trapped by defect sites are free to interact with hydrogen containing defects ($D^{'}H$) introduced in the oxide during its growth. The simplest of these interactions acts to release a proton (H^{+}) from the defect site. Interface traps are created when a proton produced by such a reaction reaches the Si-SiO_2 interface and removes a hydrogen molecule (H_2) from a hydrogen passivated dangling bond (SiH); thus creating an interface trap.

The rate of creation of trapped positive charge in the oxide can therefore be given by

$$\dot{N}_{\text{OT}} = f_{\text{OT}} k_0 \dot{D} (N_{\text{OT,max}} - N_{\text{OT}}) - r_{\text{OT}} N_{\text{OT}}, \tag{6}$$

where f_{OT} is a deep trap's hole trapping probability, k_0 is a constant proportional to the introduction rate of holes in the oxide, r_{OT} is the de-trapping rate of holes, $N_{\text{OT,max}}$ is the maximum number of deep trapping sites in the oxide, and $\dot{D}$ is the dose rate. In addition, the rate of proton release can expressed as

$$\dot{p} = f_p (k_0 \dot{D} - \dot{N}_{\text{OT}}) (N_p - p), \tag{7}$$

where f_p is a hydrogen containing defect's proton trapping a hole, $(k_0 \dot{D} - \dot{N}_{\text{OT}})$ describes the number of holes available to participate in this process, and N_p is the maximum number of available hydrogen containing defects in the oxide. Finally, the rate of interface trap creation can be modeled by

$$\dot{N}_{\text{IT}} = f_I (N_{\text{SiH}} - N_{\text{IT}}) \dot{p}, \tag{8}$$

where f_I is the probability that an available dangling bond captures the free proton, and N_{SiH} is the number of hydrogen passivated dangling bonds present in the un-irradiated oxide. An analytical description for the number of fixed positive charges N_{OT} and interface traps N_{IT} created during an irradiation can be found by solving the system of coupled differential equations described by Equations (6) to (8). The solution for the case where the irradiation starts at $t = 0$ is given by

$$N_{\text{IT}} = N_{\text{SiH}} [1 - e^{-p(t)}] \tag{9}$$

$$N_{\text{OT}} = N_{\text{OT,max}} \frac{f_{\text{OT}} k_0 \dot{D}}{f_{\text{OT}} k_0 \dot{D} + r_{\text{OT}}} [1 - e^{-(f_{\text{OT}} k_0 \dot{D} + r_{\text{OT}}) t}] \tag{10}$$

$$p(t) = f_I N_p [1 - e^{-f_p k_0 \dot{D} t + f_p N_{\text{OT}}(t)}]. \tag{11}$$

A simultaneous fit of the parametrized damage model to the data collected for each set of four chips irradiated at −19 °C and 5 °C was used to extract the dose-rate dependence of the model parameters. The predicted current increase at the expected HL-LHC dose rate and −19 °C , shown in Figure 8, is assumed to be a conservative upper limit on the current increase expected in the 2S modules due to radiation induced leakage in the CBC3s.

5. Conclusion

An extensive irradiation campaign was carried out on the CBC3 has shown to be capable of withstanding the levels of radiation expected at the HL-LHC, albeit with an expected slight increase in power consumption due to irradiation induced leakage paths in the digital circuitry of the chip.

A radiation damage model has been developed, using the data collected during the irradiation campaign, to predict the expected increase in power consumption for operating conditions at the HL-LHC. The maximum expected current increase in the CBCs would increase the power consumption of a 2S module by approximately 20 mW (given that there are ×16 CBCs per 2S module) which corresponds to a smaller than one percent increase in the total power consumption of a module.

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