Experiment 4

VLSI

4 Bit Carry Save Array Based Multiplier

Shashank Sharma

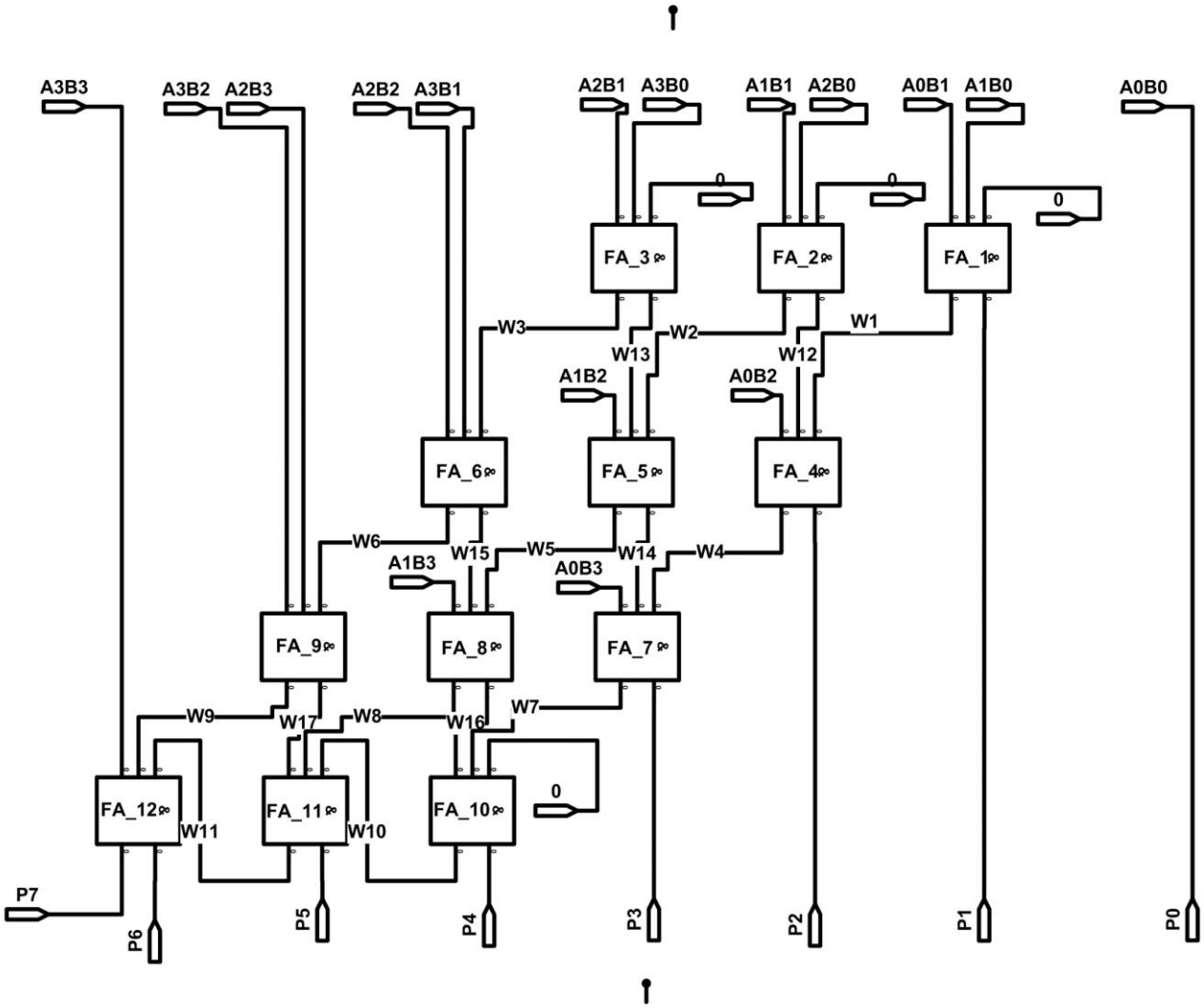
15BEE0270

L47+L48

Objective:

To design, implement and test 4 Bit Carry Save Array Based Multiplier circuit using Xilinx ISE Tool.

Circuit Diagram:



Design code:

```
module csa_4bit(
   input [3:0] a,b,
   output [7:0]p
   );
        supply0 zero;
        wire[17:1]w;
        assign p[0]=a[0]&b[0];

        fa_df fa1(a[1]&b[0],a[0]&b[1],zero,p[1],w[1]);
        fa_df fa2(a[2]&b[0],a[1]&b[1],zero,w[12],w[2]);
        fa_df fa3(a[3]&b[0],a[2]&b[1],zero,w[13],w[3]);

        fa_df fa4(w[12],a[0]&b[2],w[1],p[2],w[4]);
        fa_df fa5(w[13],a[1]&b[2],w[2],w[14],w[5]);
        fa_df fa6(a[3]&b[1],a[2]&b[2],w[3],w[15],w[6]);

        fa_df fa7(w[14],a[0]&b[3],w[4],p[3],w[7]);
        fa_df fa8(w[15],a[1]&b[3],w[5],w[16],w[8]);
        fa_df fa9(a[3]&b[2],a[2]&b[3],w[6],w[17],w[9]);

        fa_df fa10(w[16],w[7],zero,p[4],w[10]);
        fa_df fa11(w[10],w[17],w[8],p[5],w[11]);
        fa_df fa12(a[3]&b[3],w[9],w[11],p[6],p[7]);
endmodule
```

Test Bench Code:

```
module csa_4bit_test;
	reg [3:0] a;
	reg [3:0] b;
	// Outputs
	wire [7:0] p;
	reg [7:0]check;
	// Instantiate the Unit Under Test (UUT)
	csa_4bit uut (
		.a(a),
		.b(b),
		//.w(w),
		.p(p)
	);
	initial repeat(20) begin
		// Initialize Inputs
		a = $random;
		b = $random;
		check=a*b;
		// Wait 100 ns for global reset to finish
		#10 $display($time,"%d*%d=%d(%d)",a,b,p,check);
	end
endmodule
```

Result:

Successfully designed, implemented and tested 4 Bit Carry Save Array Based Multiplier circuit using Xilinx ISE Tool.

Device utilization summary:

Selected Device : 3s500efg320-4

Number of Slices:	15	out of	4656	0%
Number of 4 input LUTs:	26	out of	9312	0%
Number of IOs:	16			
Number of bonded IOBs:	16	out of	232	6%

Timing Summary:

Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 11.618ns