Experiment 5

VLSI

Wallace Tree Multiplier

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15BEE0270

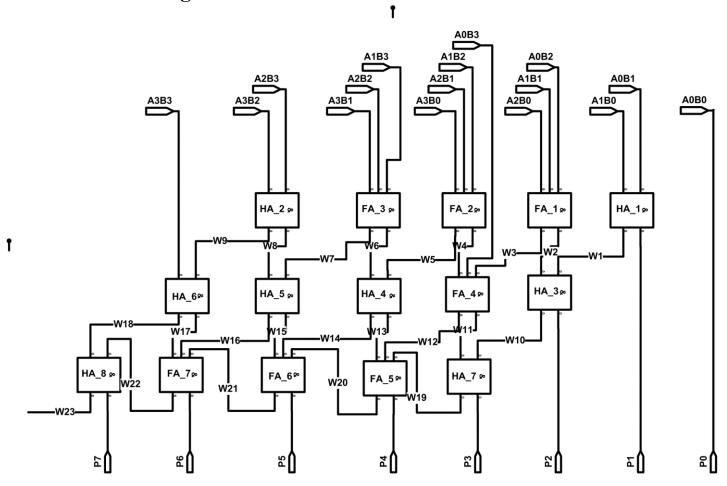
L47+L48

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Objective:

To design, implement and test Wallace Tree Multiplier circuit using Xilinx ISE Tool.

Circuit Diagram:



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Design code:

```
module wt_4bit_mul(
  input [3:0] a,
  input [3:0] b,
  output [7:0] p);
wire [23:1] w;
assign p[0]=a[0]\&b[0];
ha_df ha1(a[1]&b[0],a[0]&b[1],p[1],w[1]);
fa_df fa_1(a_2)&b_0,a_1)&b_1,a_0&b_2,w_2,w_3);
fa_df fa2(a[3]&b[0],a[2]&b[1],a[1]&b[2],w[4],w[5]);
fa_df fa3(a[3]&b[1],a[2]&b[2],a[1]&b[3],w[6],w[7]);
ha_df ha2(a[3]&b[2],a[2]&b[3],w[8],w[9]);
ha_df ha3(w[2],w[1],p[2],w[10]);
fa_df fa4(a[0]&b[3],w[4],w[3],w[11],w[12]);
ha_df ha4(w[5],w[6],w[13],w[14]);
ha_df ha5(w[7],w[8],w[15],w[16]);
ha_df ha6(a[3]&b[3],w[9],w[17],w[18]);
ha_df ha7(w[10],w[11],p[3],w[19]);
fa_df fa5(w[12],w[13],w[19],p[4],w[20]);
fa_df fa6(w[14],w[15],w[20],p[5],w[21]);
fa_df fa7(w[16],w[17],w[21],p[6],w[22]);
ha_df ha8(w[18],w[22],p[7],w[23]);
endmodule
```

Test Bench Code:

```
module wt_4bit_mul_test;
       // Inputs
       reg [3:0] a;
       reg [3:0] b;
       // Outputs
       wire [7:0] p;
       reg[7:0] check;
       // Instantiate the Unit Under Test (UUT)
       wt_4bit_mul uut (
              .a(a),
              .b(b),
              .p(p)
       );
       initial repeat(20) begin
              // Initialize Inputs
              a = \$random;
              b = $random;
              check=a*b;
              // Wait 100 ns for global reset to finish
              #10 $display($time,"%d*%d=%d(%d)",a,b,p,check);
       end
endmodule
```

Result:

Successfully designed, implemented and tested Wallace Tree Multiplier circuit using Xilinx ISE Tool.

Device utilization summary:

Selected Device: 3s500efg320-4

Number of Slices: 18 out of 4656 0%

Number of 4 input LUTs: 32 out of 9312 0%

Number of IOs: 16

Number of bonded IOBs: 16 out of 232 6%

Timing Summary:

Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 15.104ns

