# Experiment 1

# VLSI

# 4 Bit Ripple Carry Adder

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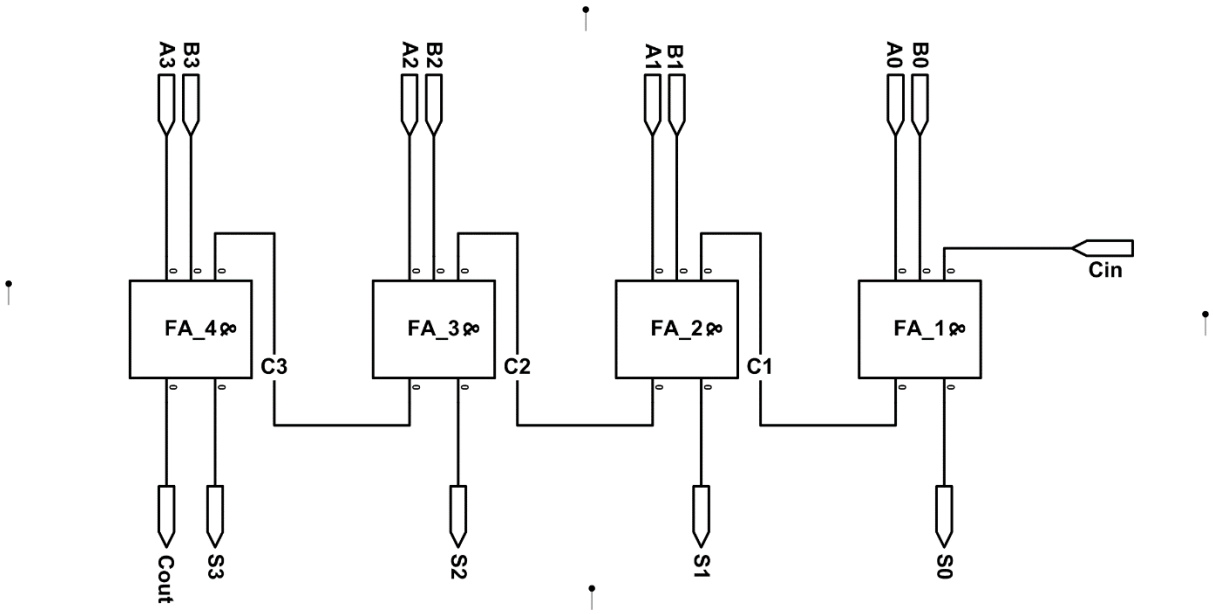
## Objective:

To design, implement and test 4 Bit Ripple Carry Adder circuit using Xilinx ISE Tool.

## Circuit Diagram:



## Design code:

```
module Ripple_Counter(
   input [3:0]a,b,
   input Cin,
   output [3:0]S,
   output Cout
   );
wire c1,c2,c3;
fa_df fa1(a[0],b[0],Cin,S[0],c1);
fa_df fa2(a[1],b[1],c1,S[1],c2);
fa_df fa3(a[2],b[2],c2,S[2],c3);
fa_df fa4(a[3],b[3],c3,S[3],Cout);
endmodule
```

## Test Bench Code

```
module Ripple_Counter_test;
        // Inputs
        reg [3:0] a;
        reg [3:0] b;
        reg Cin;

        // Outputs
        wire [3:0] S;
        wire Cout;
        reg [4:0] check;
```

```
// Instantiate the Unit Under Test (UUT)
	Ripple_Counter uut (
		.a(a),
		.b(b),
		.Cin(Cin),
		.S(S),
		.Cout(Cout)
	);
	initial repeat(20) begin
		// Initialize Inputs
		a = $random;
		b = $random;
		Cin = $random;
		check=a+b+Cin;
		// Wait 100 ns for global reset to finish
		#10 $display($time, " %d+%d+%d=%d(%d)", a,b,Cin,{Cout,S},check)
	end
endmodule
```

# Result

Successfully designed, implemented and tested 4 Bit Ripple Carry Adder circuit using Xilinx ISE Tool.

Device utilization summary:

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Selected Device : 3s500efg320-4

| | | | | |
|---|---|---|---|---|
| Number of Slices: | 4 | out of | 4656 | 0% |
| Number of 4 input LUTs: | 8 | out of | 9312 | 0% |
| Number of IOs: | 14 | | | |
| Number of bonded IOBs: | 14 | out of | 232 | 6% |

Timing Summary:

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Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.926ns