Experiment 2

VLSI

4 Bit Carry Look Ahead Adder

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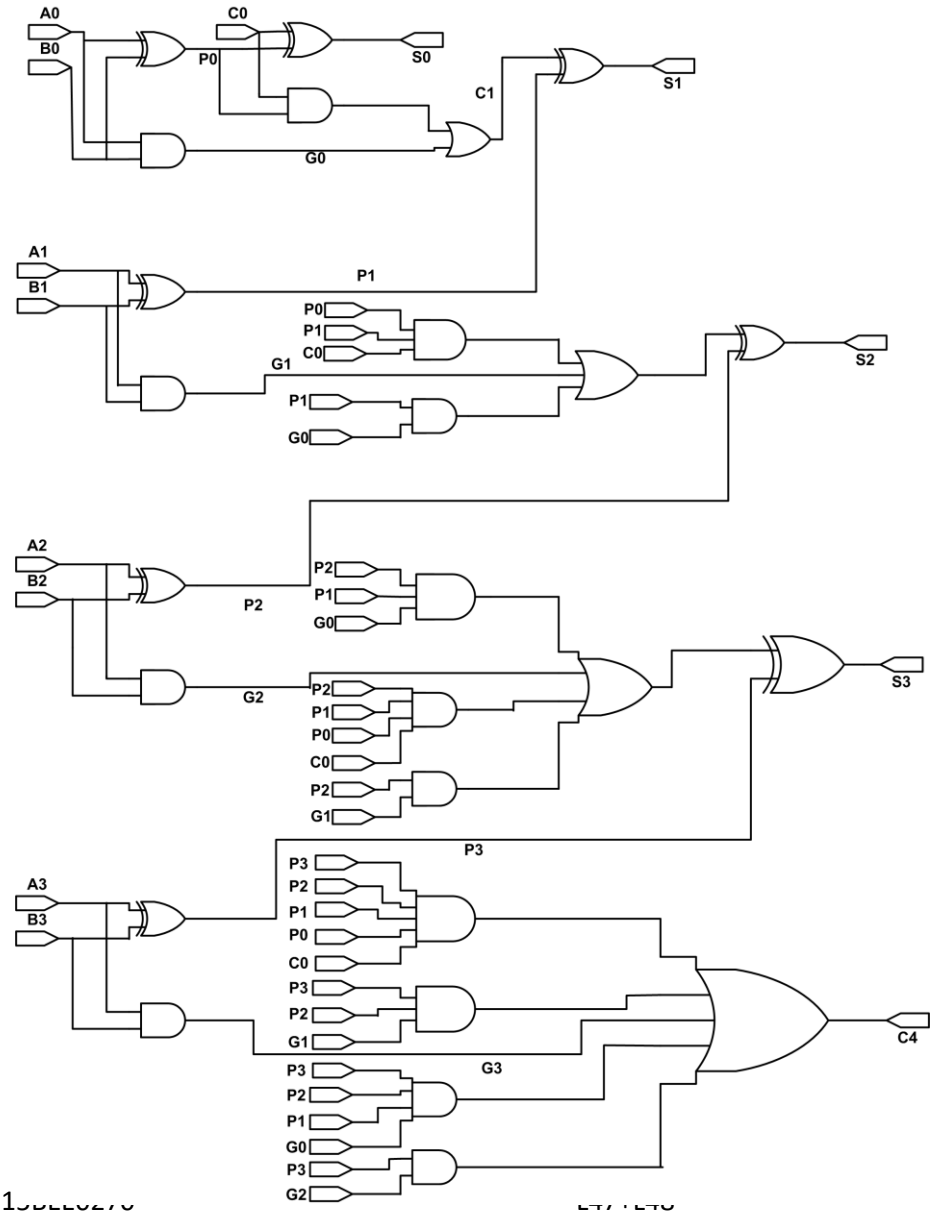
L47+L48

Objective:

To design implement and test 4 Bit Carry Look Ahead Adder circuit using Xilinx ISE Tool.

Circuit Diagram:



Design code:

```
module CLA_4bit(
   input [3:0]a,b,
   input Cin,
   output [3:0] S,
   output Cout
   );
        wire [3:0]p;
        wire [3:0]g;
        wire [4:0]c;
        assign c[0]=Cin;
        assign p[0]=a[0]^b[0];
        assign g[0]=a[0]&b[0];
        assign c[1]=(p[0]&c[0])|g[0];

        assign p[1]=a[1]^b[1];
        assign g[1]= a[1]&b[1];
        assign c[2]=(p[1]&p[0]&c[0])|(p[1]&g[0])|g[1];

        assign p[2]=a[2]^b[2];
        assign g[2]=a[2]&b[2];
        assign c[3]=(p[2]&p[1]&p[0]&c[0])|(p[2]&p[1]&g[0])|(p[2]&g[1])|g[2];

        assign p[3]=a[3]^b[3];
        assign g[3]=a[3]&b[3];
        assign c[4]=
(p[3]&p[2]&p[1]&p[0]&c[0])|(p[3]&p[2]&p[1]&g[0])|(p[3]&p[2]&g[1])|(p[3]&g[2])|g[3];
```

```
        assign Cout=c[4];


        assign S[0]=p[0]^c[0];
        assign S[1]=p[1]^c[1];
        assign S[2]=p[2]^c[2];
        assign S[3]=p[3]^c[3];
endmodule
```

Test Bench Code:

```
module cla_4bit_test;
        // Inputs
        reg [3:0] a;
        reg [3:0] b;
        reg Cin;
        // Outputs
        wire [3:0] S;
        wire Cout;
        reg [4:0]check;
        // Instantiate the Unit Under Test (UUT)
        CLA_4bit uut (
                .a(a),
                .b(b),
                .Cin(Cin),
                .S(S),
                .Cout(Cout)
        );
```

```
        initial repeat(20) begin
                // Initialize Inputs
                a = $random;
                b = $random;
                Cin = $random;
                check=a+b+Cin;

                // Wait 100 ns for global reset to finish
                #10 $display($time,"%d+%d+%d=%d(%d)",a,b,Cin,{Cout,S},check);

                // Add stimulus here

        end

endmodule
```

Result:

Successfully designed, implemented and tested 4 Bit Carry Look Ahead Adder circuit using Xilinx ISE Tool.

Device utilization summary:

Selected Device : 3s500efg320-4

Number of Slices:	4	out of 4656	0%
Number of 4 input LUTs:	8	out of 9312	0%
Number of IOs:	14		
Number of bonded IOBs:	14	out of 232	6%

Timing Summary:

Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.882ns