Experiment 6

VLSI

4 Bit Dadda-Tree Multiplier

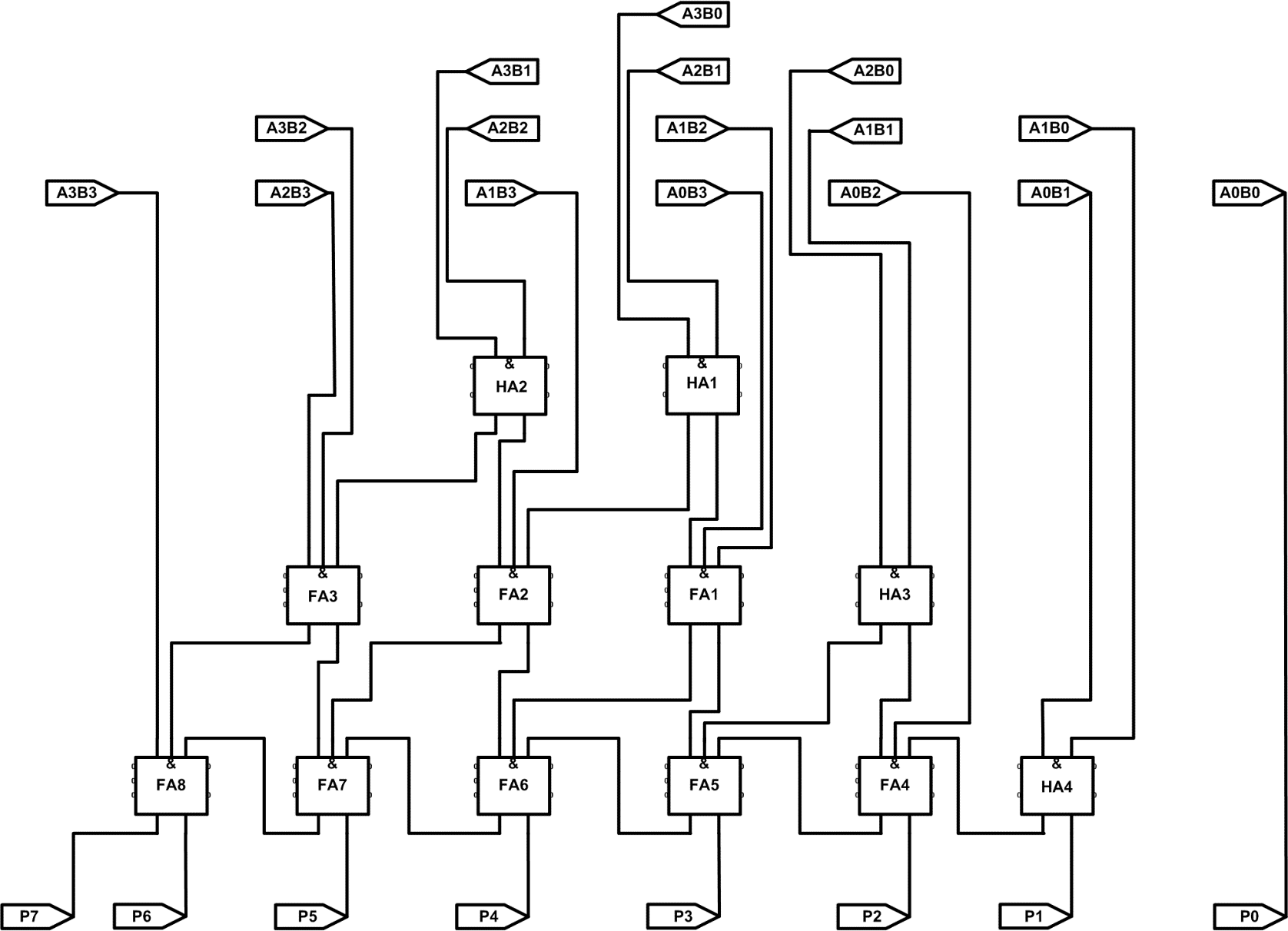
Shashank Sharma

15BEE0270

L47+L48

**Objective:**

To design, implement and test 4 Bit Dadda Tree Multiplier circuit using Xilinx ISE Tool.

**Circuit Diagram:**

**Design code:**

module dadda\_tree(

input [3:0] a,

input [3:0] b,

output [7:0] p

);

wire[17:1]w;

assign p[0]=a[0]&b[0];

ha\_df ha1(a[3]&b[0],a[2]&b[1],w[1],w[2]);

ha\_df ha2(a[3]&b[1],a[2]&b[2],w[3],w[4]);

ha\_df ha3(a[2]&b[0],a[1]&b[1],w[5],w[6]);

fa\_df fa1(a[1]&b[2],a[0]&b[3],w[1],w[7],w[8]);

fa\_df fa2(a[1]&b[3],w[2],w[3],w[9],w[10]);

fa\_df fa3(a[3]&b[2],a[2]&b[3],w[4],w[11],w[12]);

ha\_df ha4(a[1]&b[0],a[0]&b[1],p[1],w[13]);

fa\_df fa4(a[0]&b[2],w[5],w[13],p[2],w[14]);

fa\_df fa5(w[6],w[7],w[14],p[3],w[15]);

fa\_df fa6(w[8],w[9],w[15],p[4],w[16]);

fa\_df fa7(w[10],w[11],w[16],p[5],w[17]);

fa\_df fa8(a[3]&b[3],w[12],w[17],p[6],p[7]);

endmodule

**Test Bench Code:**

module dadda\_tree\_test;

// Inputs

reg [3:0] a;

reg [3:0] b;

// Outputs

wire [7:0] p;

reg[7:0] check;

// Instantiate the Unit Under Test (UUT)

dadda\_tree uut (

.a(a),

.b(b),

.p(p)

);

initial repeat(20) begin

// Initialize Inputs

a = $random;

b = $random;

check=a\*b;

// Wait 100 ns for global reset to finish

#10 $display($time,"%d\*%d=%d(%d)",a,b,p,check);

// Add stimulus here

end

endmodule

**Result**

Successfully designed, implemented and tested 4 Bit Dadda Tree Multiplier circuit using Xilinx ISE Tool.

Device utilization summary:

---------------------------

Selected Device: 3s500efg320-4

Number of Slices: 16 out of 4656 0%

Number of 4 input LUTs: 27 out of 9312 0%

Number of IOs: 16

Number of bonded IOBs: 16 out of 232 6%

Timing Summary:

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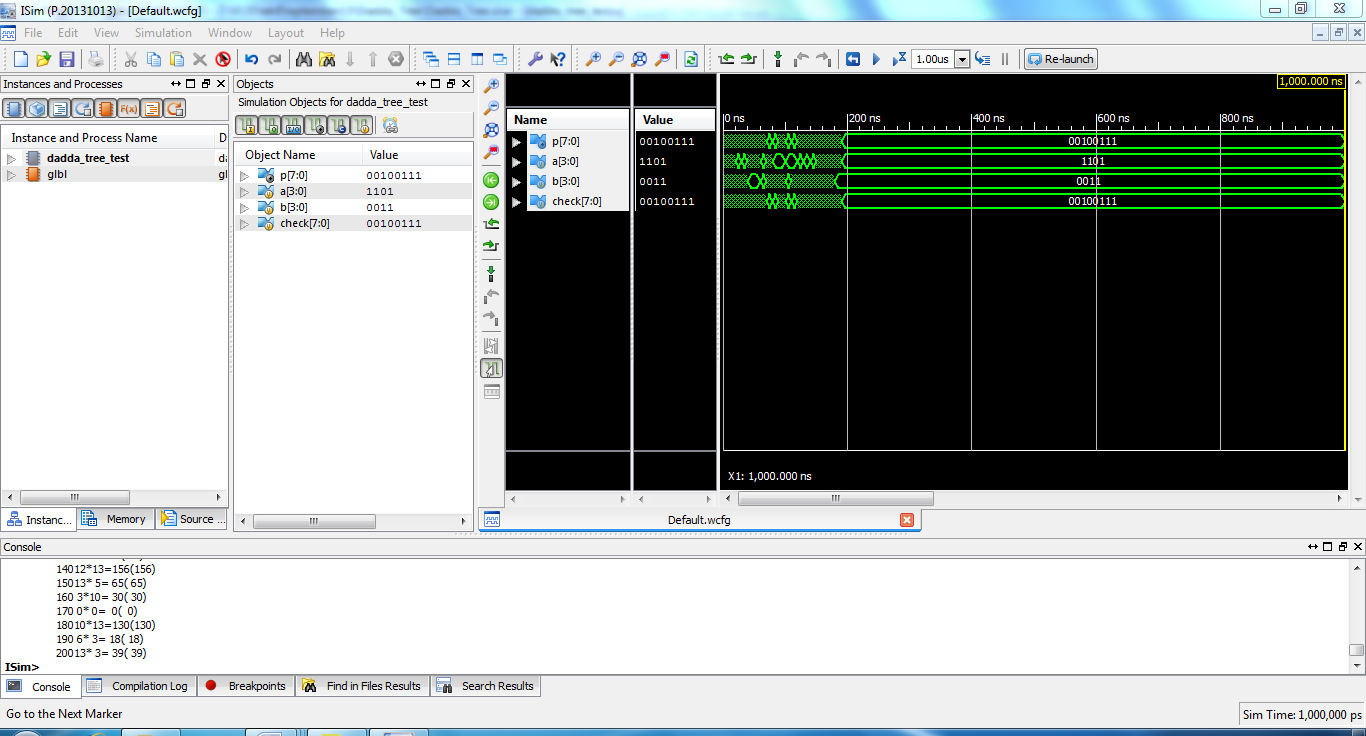
Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 12.629ns



Experiment 7

VLSI

4 Bit Bough Wooley Array Multiplier

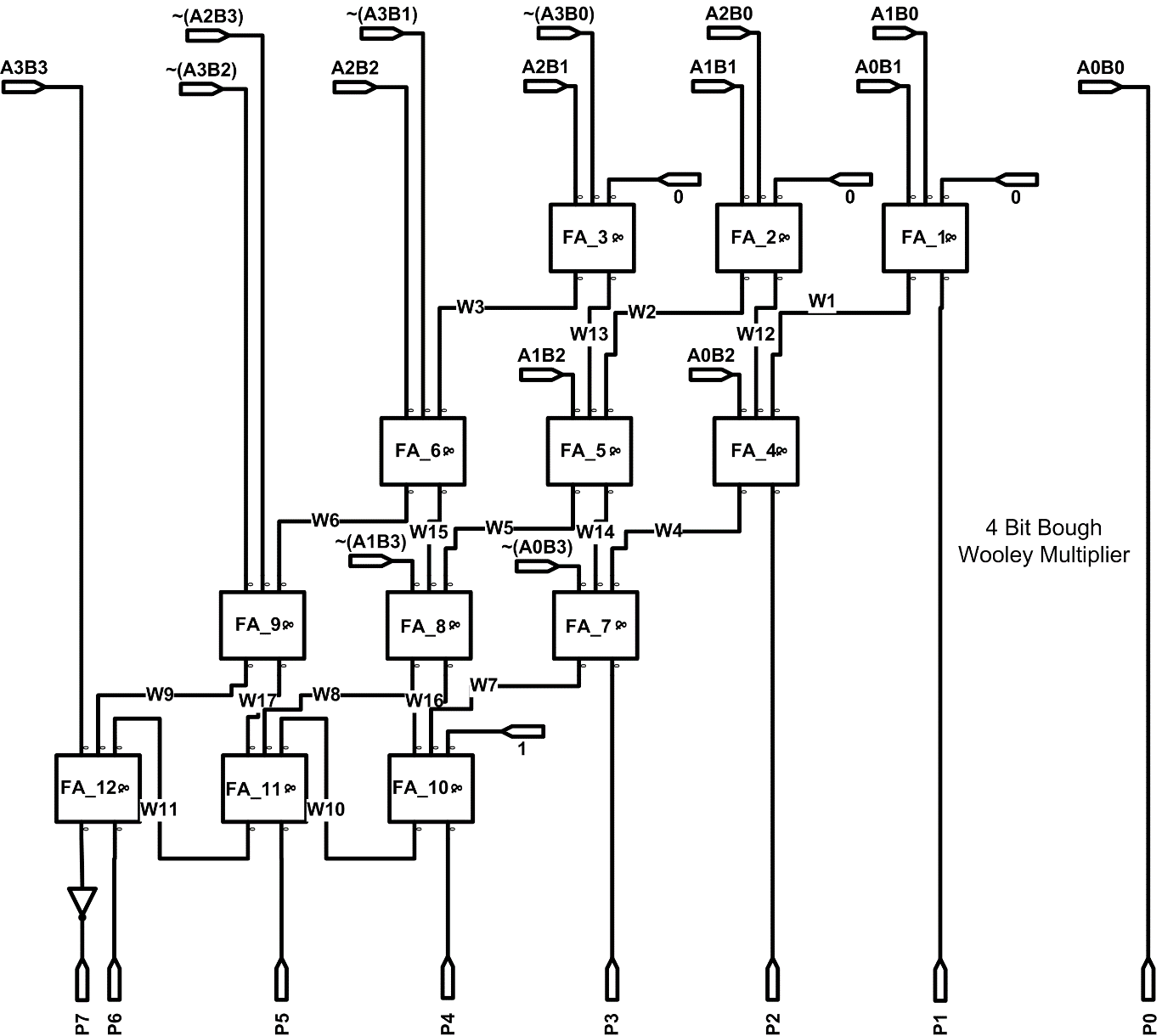
Shashank Sharma

15BEE0270

L47+L48

**Objective:**

To design, implement and test 4 Bit Bough Wooley Array Multiplier circuit using Xilinx ISE Tool.

**Circuit Diagram:**

**Design code:**

module bwy\_4bit\_mul(

input signed[3:0] a,b,

output signed[7:0] p

);

supply0 zero;

supply1 one;

wire[18:1]w;

assign p[0]=a[0]&b[0];

fa\_df fa1(a[1]&b[0],a[0]&b[1],zero,p[1],w[1]);

fa\_df fa2(a[2]&b[0],a[1]&b[1],zero,w[12],w[2]);

fa\_df fa3(~(a[3]&b[0]),a[2]&b[1],zero,w[13],w[3]);

fa\_df fa4(w[12],a[0]&b[2],w[1],p[2],w[4]);

fa\_df fa5(w[13],a[1]&b[2],w[2],w[14],w[5]);

fa\_df fa6(~(a[3]&b[1]),a[2]&b[2],w[3],w[15],w[6]);

fa\_df fa7(w[14],~(a[0]&b[3]),w[4],p[3],w[7]);

fa\_df fa8(w[15],~(a[1]&b[3]),w[5],w[16],w[8]);

fa\_df fa9(~(a[3]&b[2]),~(a[2]&b[3]),w[6],w[17],w[9]);

fa\_df fa10(w[16],w[7],one,p[4],w[10]);

fa\_df fa11(w[10],w[17],w[8],p[5],w[11]);

fa\_df fa12(a[3]&b[3],w[9],w[11],p[6],w[18]);

assign p[7]=~w[18];

endmodule

**Test Bench Code:**

module bwy\_mul\_test1;

reg signed [3:0] a;

reg signed[3:0] b;

// Outputs

wire signed [7:0] p;

reg signed [7:0]check;

// Instantiate the Unit Under Test (UUT)

bwy\_4bit\_mul uut (

.a(a),

.b(b),

.p(p)

);

initial repeat(20) begin

// Initialize Inputs

a = $random;

b = $random;

check=a\*b;

// Wait 100 ns for global reset to finish

#10 $display($time,"%d\*%d=%d(%d)",a,b,p,check);

// Add stimulus here

end

endmodule

**Result**

Successfully designed, implemented and tested 4 Bit Bough Wooley Array Multiplier circuit using Xilinx ISE Tool.

Device utilization summary:

---------------------------

Selected Device : 3s500efg320-5

Number of Slices: 15 out of 4656 0%

Number of 4 input LUTs: 26 out of 9312 0%

Number of IOs: 16

Number of bonded IOBs: 16 out of 232 6%

Timing Summary:

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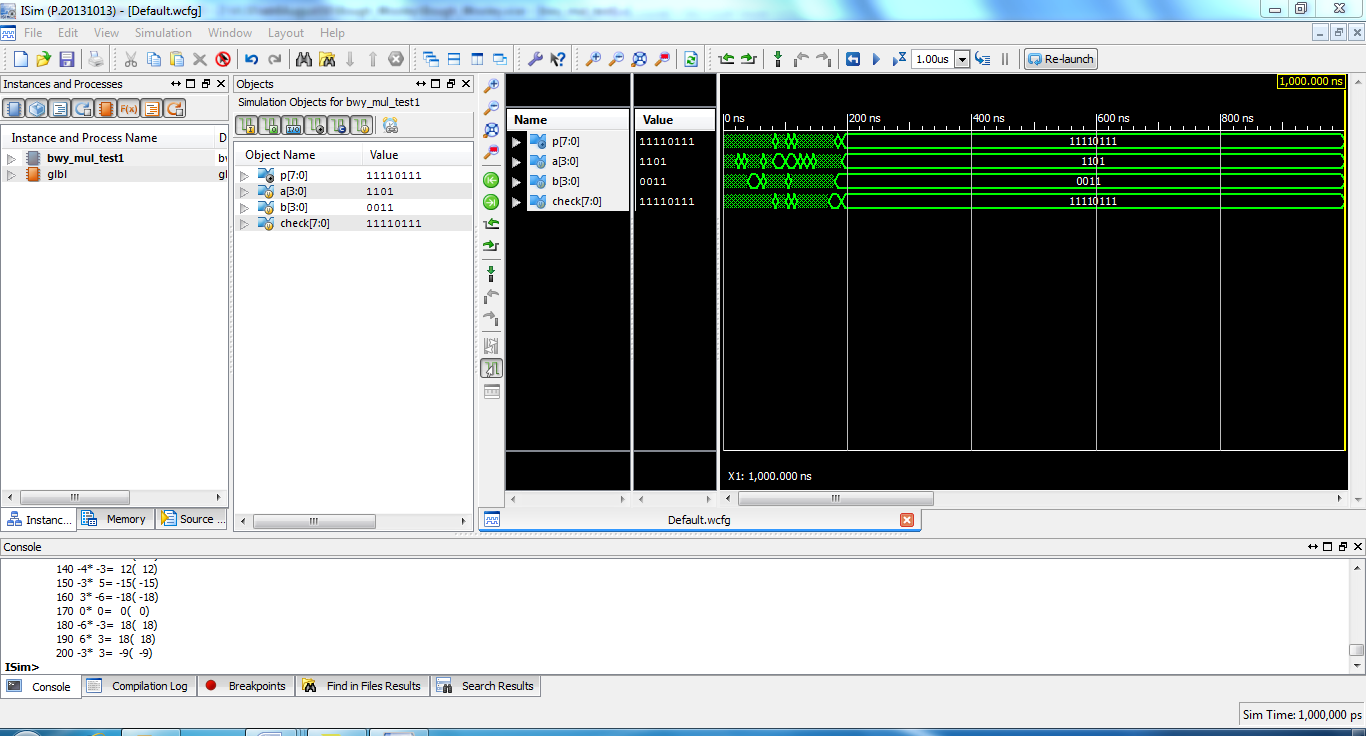
Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 10.425ns

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Experiment 8

VLSI

4 Bit Squarer Design

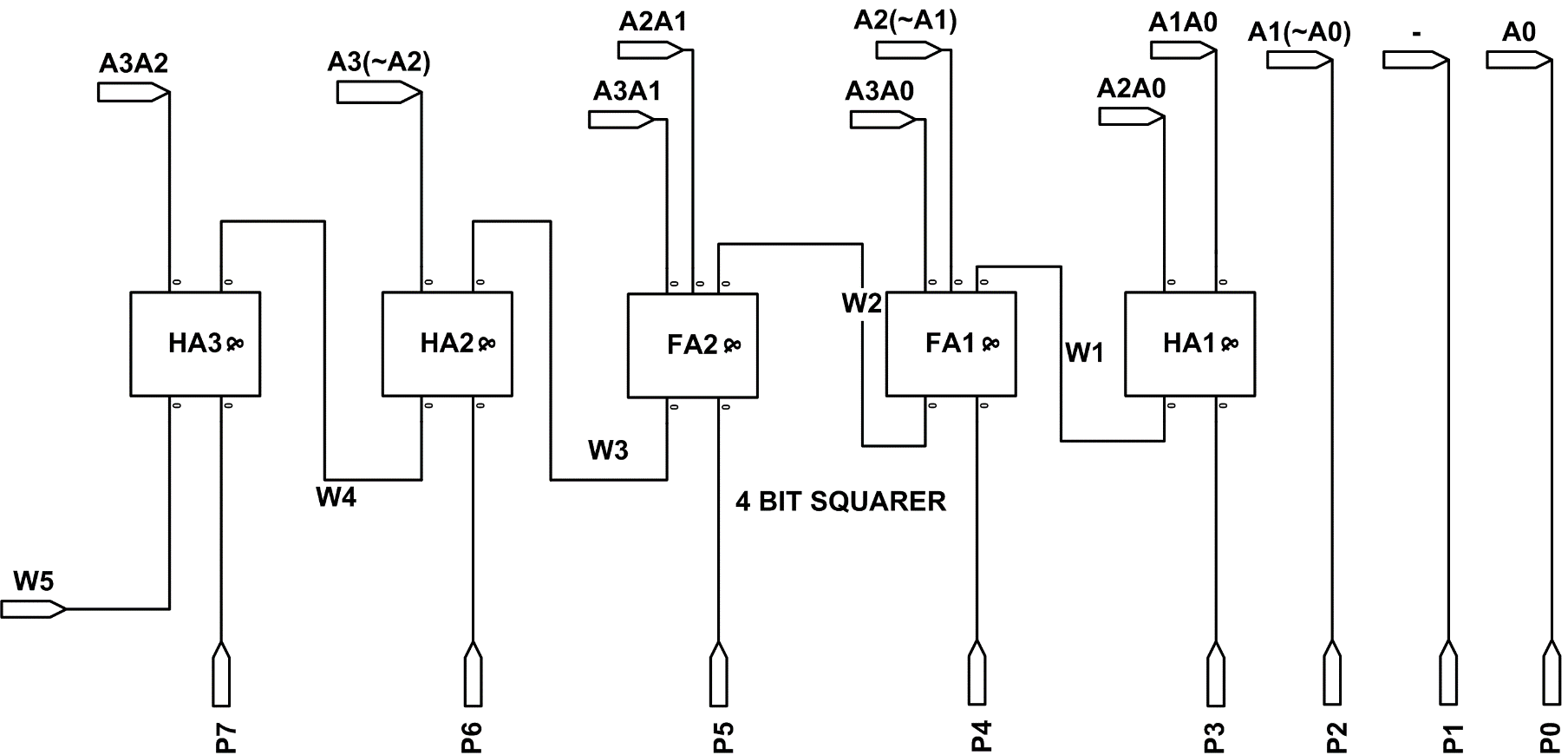
Shashank Sharma

15BEE0270

L47+L48

**Objective:**

To design, implement and test 4 Bit squarer design circuit using Xilinx ISE Tool.

**Circuit Diagram:**

**Design code:**

module four\_bit\_squarer(

input [3:0] a,

output [7:0] p

);

supply0 zero;

wire [5:1] w;

assign p[0]=a[0];

assign p[1]=zero;

assign p[2]=(a[1]&~a[0]);

ha\_df ha1(a[1]&a[0],a[2]&a[0],p[3],w[1]);

fa\_df fa1(a[3]&a[0],a[2]&~a[1],w[1],p[4],w[2]);

fa\_df fa2(a[2]&a[1],a[3]&a[1],w[2],p[5],w[3]);

ha\_df ha2(a[3]&~a[2],w[3],p[6],w[4]);

ha\_df ha3(a[3]&a[2],w[4],p[7],w[5]);

endmodule

**Test Bench Code:**

module four\_bit\_squarer\_test;

// Inputs

reg [3:0] a;

// Outputs

wire [7:0] p;

reg[7:0] check;

// Instantiate the Unit Under Test (UUT)

four\_bit\_squarer uut (

.a(a),

.p(p)

);

initial repeat(20) begin

// Initialize Inputs

a = $random;

check=a\*a;

// Wait 100 ns for global reset to finish

#10 $display($time,"%d\*%d=%d(%d)",a,a,p,check);

// Add stimulus here

end

endmodule

**Result**

Successfully designed, implemented and tested 4 Bit Squarer Design circuit using Xilinx ISE Tool.

Device utilization summary:

Selected Device: 3s500efg320-4

Number of Slices: 3 out of 4656 0%

Number of 4 input LUTs: 6 out of 9312 0%

Number of IOs: 12

Number of bonded IOBs: 12 out of 232 5%

Timing Summary:

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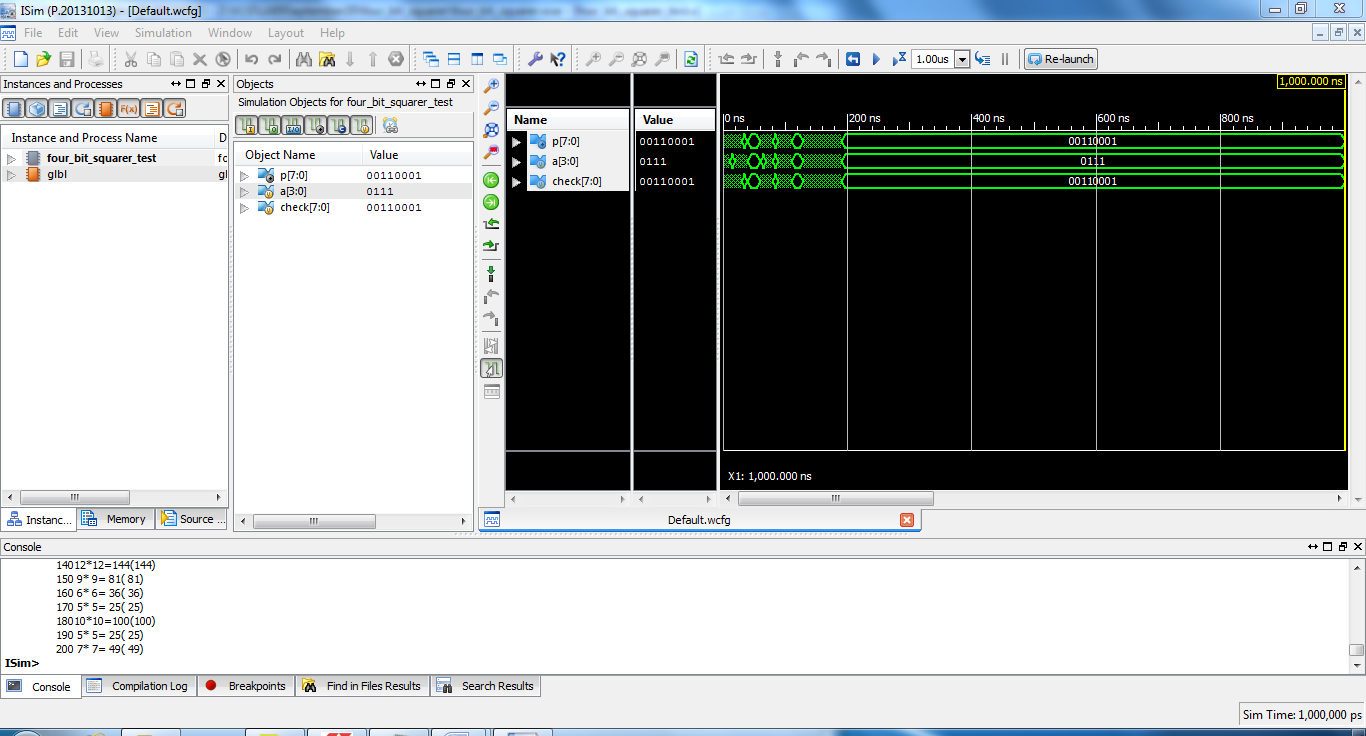
Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 6.422ns



Experiment 9

VLSI

MAC Design

Shashank Sharma

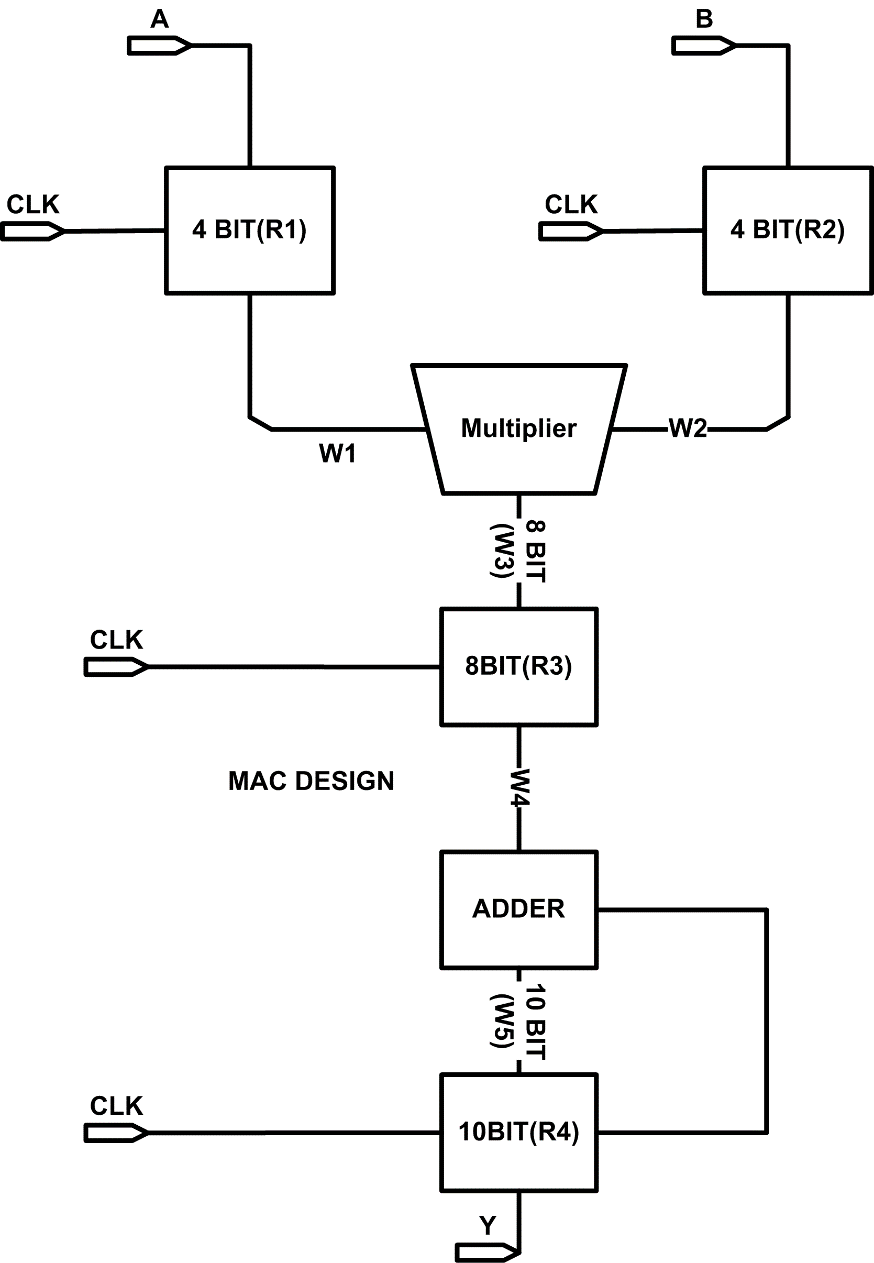
15BEE0270

L47+L48

**Objective:**

To design, implement and test MAC Design using Xilinx ISE Tool.

**Circuit Diagram:**

****

**Design code:**

**Pipo 4 Bit:**

module pipo\_4bit(

input [3:0] d,

input Clk, rst,

output reg [3:0] q

);

always@(posedge Clk or negedge rst)

if(!rst)

q<=4'b0000;

else

q<=d;

endmodule

**Pipo 8 Bit:**

module pipo\_8bit(

input [7:0] d,

input Clk, rst,

output reg [7:0] q

);

always@(posedge Clk or negedge rst)

if(!rst)

q<=8'b00000000;

else

q<=d;

endmodule

**Pipo 10 Bit:**

module pipo\_10bit(

input [9:0] d,

input Clk, rst,

output reg [9:0] q

);

always@(posedge Clk or negedge rst)

if(!rst)

q<=10'b0000000000;

else

q<=d;

endmodule

**Verilog Code of MAC:**

module MAC(

input [3:0] a,

input [3:0] b,

input Clk, rst,

output [9:0] y

);

wire [3:0]w1,w2;

wire [7:0]w3,w4;

wire [9:0]w5,w6;

pipo\_4bit R1(a,Clk,rst,w1);

pipo\_4bit R2(b,Clk,rst,w2);

pipo\_8bit R3(w3,Clk,rst,w4);

pipo\_10bit R4(w5,Clk,rst,w6);

assign w3=w1\*w2;

assign w5=w4+w6;

assign y=w6;

endmodule

**Test Bench Code:**

module MAC\_Test;

// Inputs

reg [3:0] a;

reg [3:0] b;

reg Clk;

reg rst;

// Outputs

wire [9:0] y;

// Instantiate the Unit Under Test (UUT)

MAC uut (

.a(a),

.b(b),

.Clk(Clk),

.rst(rst),

.y(y)

);

initial begin

// Initialize Inputs

a = 4'b0000;

b = 4'b0000;

Clk = 1'b0;

rst = 1'b0;

// Wait 100 ns for global reset to finish

#100;

a=4'b0101;

b=4'b0100;

rst=1'b1;

// Add stimulus here

end

always #50 Clk=~Clk;

endmodule

**Result**

Successfully designed, implemented and tested MAC Design using Xilinx ISE Tool.

Device utilization summary:

---------------------------

Selected Device : 3s500efg320-4

Number of Slices: 14 out of 4656 0%

Number of Slice Flip Flops: 26 out of 9312 0%

Number of 4 input LUTs: 11 out of 9312 0%

Number of IOs: 20

Number of bonded IOBs: 20 out of 232 8%

Number of MULT18X18SIOs: 1 out of 20 5%

Number of GCLKs: 1 out of 24 4%

Timing Summary:

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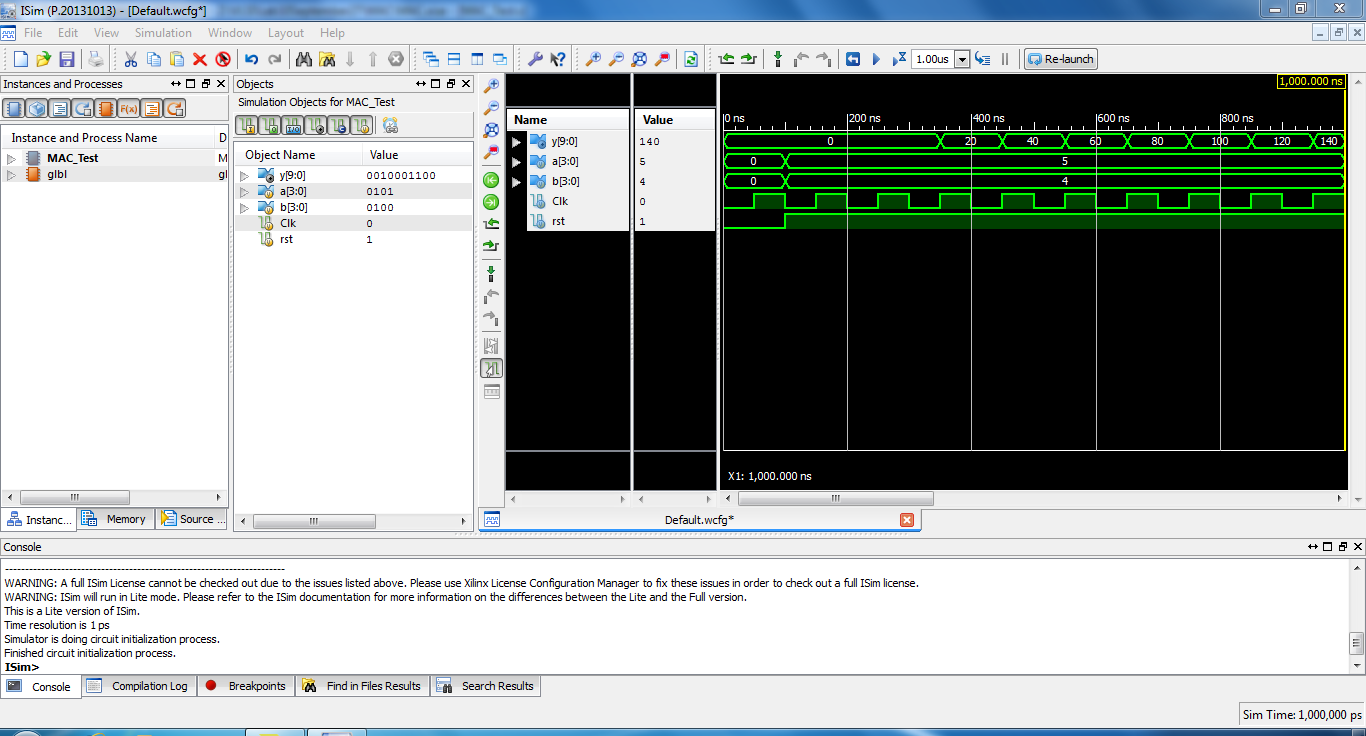
Speed Grade: -4

Minimum period: 6.083ns (Maximum Frequency: 164.393MHz)

Minimum input arrival time before clock: 1.946ns

Maximum output required time after clock: 4.310ns

Maximum combinational path delay: No path found



Experiment 10

VLSI

FIR Filter Design

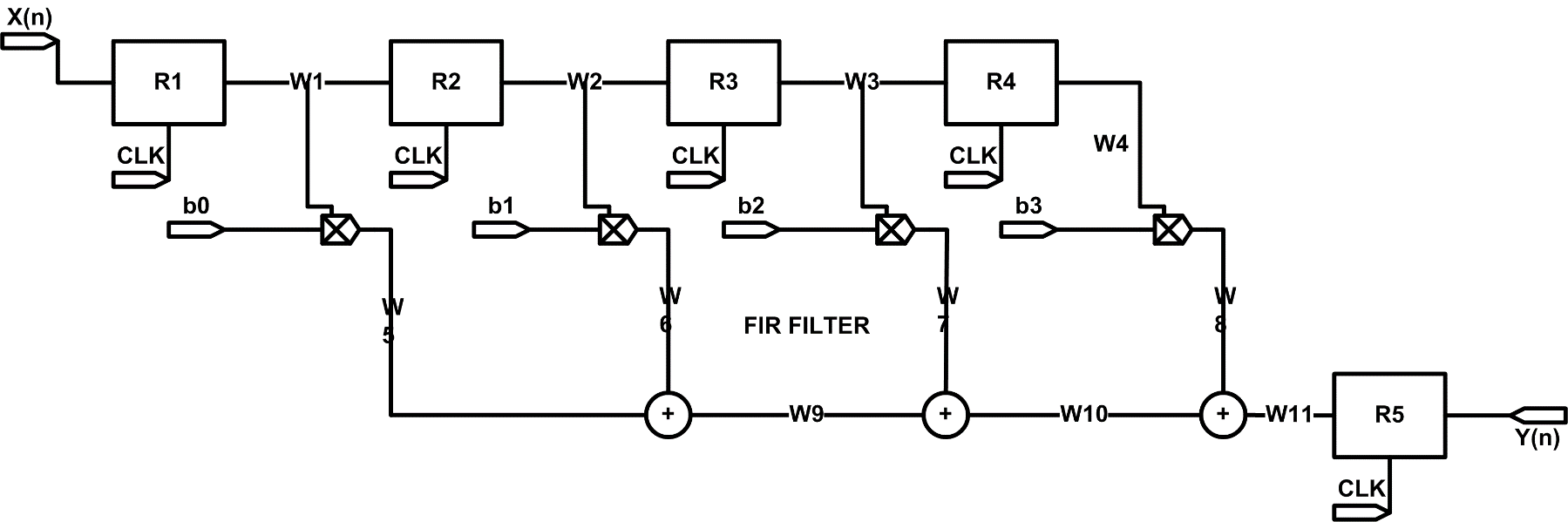
Shashank Sharma

15BEE0270

L47+L48

**Objective:**

To design, implement and test FIR Filter Design using Xilinx ISE Tool.

**Circuit Diagram:**

**Design code:**

**Pipo 4 Bit:**

module pipo\_4bit(

input [3:0] d,

input Clk, rst,

output reg [3:0] q

);

always@(posedge Clk or negedge rst)

if(!rst)

q<=4'b0000;

else

q<=d;

endmodule

**Verilog Code of FIR Filter Design:**

module fir(

input [3:0] x,

input Clk,

input rst,

output [10:0] q

);

wire [3:0]w1,w2,w3,w4;

wire [7:0]w5,w6,w7,w8;

wire [9:0]w9,w10;

wire[10:0]w11;

parameter b0=4'b0001;

parameter b1=4'b0010;

parameter b2=4'b0011;

parameter b3=4'b0100;

pipo\_4bit R1(x,Clk,rst,w1);

pipo\_4bit R2(w1,Clk,rst,w2);

pipo\_4bit R3(w2,Clk,rst,w3);

pipo\_4bit R4(w3,Clk,rst,w4);

assign w5=b0\*w1;

assign w6=b1\*w2;

assign w7=b2\*w3;

assign w8=b3\*w4;

assign w9=w5+w6;

assign w10=w9+w7;

assign w11=w10+w8;

assign q=w11;

endmodule

**Test Bench Code:**

module fir\_test\_1;

// Inputs

reg [3:0] x;

reg Clk;

reg rst;

// Outputs

wire [10:0] q;

// Instantiate the Unit Under Test (UUT)

fir uut (

.x(x),

.Clk(Clk),

.rst(rst),

.q(q)

);

initial begin

// Initialize Inputs

x = 4'b0000;

Clk = 1'b0;

rst = 1'b0;

// Wait 100 ns for global reset to finish

#100;

x = 4'b0001;

rst=1'b1;

#100;

x=4'b0010;

#100

x=4'b0011;

#100;

x=4'b0100;

#100;

x=4'b0000;

rst=1'b1;

end

always #50 Clk=~Clk;

endmodule

**Result**

Successfully designed, implemented and tested FIR Filter Design using Xilinx ISE Tool.

Device utilization summary:

---------------------------

Selected Device : 3s500efg320-4

Number of Slices: 15 out of 4656 0%

Number of Slice Flip Flops: 16 out of 9312 0%

Number of 4 input LUTs: 21 out of 9312 0%

Number of IOs: 17

Number of bonded IOBs: 17 out of 232 7%

Number of GCLKs: 1 out of 24 4%

Timing Summary:

---------------

Speed Grade: -4

Minimum period: 1.607ns (Maximum Frequency: 622.278MHz)

Minimum input arrival time before clock: 1.946ns

Maximum output required time after clock: 12.186ns

Maximum combinational path delay: No path found

