Shabnam Sheikhha — Computer Science

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Research Interests

RTL Simulation, Computer Architecture, Computer Systems

Education

◇ **Massachusetts Institute of Technology**, MA, USA Sep. 2021 - present (Exp. May 2027)
Ph.D., Electrical Engineering and Computer Science, **Overall GPA: 5.0/5.0**

◇ **Sharif University of Technology**, Tehran, Iran Sep. 2016 - Feb . 2021
B.Sc., Computer Engineering, Major Degree, **Overall GPA: 18.97/20**
B.Sc., Mathematics, Minor Degree, **Overall GPA: 18.62/20**

Relevant courses **(GPA: 19.67/20)**: Advanced Computer Architecture (18.8/20, *graduate*), Multicore Computing (19.4/20), Computer Networks (19.4/20), Operating Systems (20/20), Embedded Systems (19.7/20), Digital Systems Design (19.9/20), Linear Algebra (19.4/20), Data Analysis (20/20), Statistics and Applications (20/20)

◇ **Farzanegan High School**, Yazd, Iran Sep. 2012 - May 2016
Affiliated with National Organization for Development of Exceptional Talents (NODET)
Diploma in Mathematics and Physics, **Overall GPA: 19.85/20**

Honors and Awards

◇ **ACM Student Research Competition**, MICRO'21 Oct. 2021
- Ranked 2^{nd} in the Undergraduate category

◇ **Best Paper Award**, FPGA'20 Feb. 2020

◇ **National Elite Foundation Fellowship** Sep. 2015 - Sep. 2021

◇ **National University Entrance Exams (Konkur)** Dec. 2015
- Ranked 29^{th} among 162 000+ in Mathematics and Physics
- Ranked 4^{th} among 6 000+ in English Language

Publication

◇ Josipovic, L., **Sheikhha, S.**, Guerrieri, A., Ienne, P., Cortadella, J. Buffer Placement and Sizing for High-Performance Dataflow Circuits. *28th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA'20)*, 2020. **Best Paper Award.**

Research Experience

◇ **Massachusetts Institute of Technology**, MA, USA Sep. 2021 - present
Computer Science and Artificial Intelligence Laboratory (CSAIL)
Ph.D. Advisor: Prof. Daniel Sanchez

Fast simulation of digital circuits is crucial to build modern chips. But RTL (Register-Transfer-Level) simulators are slow, as they cannot exploit multicores well. Slow simulation lengthens chip design time and makes bugs more frequent. Our research focuses on accelerating RTL simulation with hardware-software co-design.

◇ **Barcelona Supercomputing Center**, Barcelona, Spain Oct. 2020 - Aug. 2021
Computer Architecture for Parallel Paradigms
Research Supervisor: Prof. Osman Unsal

The aim of the project was to propose a hardware accelerator tailored to applications with irregular memory access patterns such as sparse matrix computations. Our goal was to address two main bottlenecks: irregular memory accesses and index matching. I worked remote until May 2021, after which I moved to Barcelona and started work in person.

◇ **École Polytechnique Fédérale de Lausanne**, Lausanne, Switzerland Jul. - Dec. 2019
Processor Architecture Lab (LAP)
Summer@EPFL Program
Research Supervisor: Prof. Paolo Ienne

The aim of the project was performance optimization and resource utilization in dataflow circuits. My main focus was implementing strategic buffer placement to reduce the critical path delay and

increase the throughput (*published in FPGA'20*). I continued remote work, focusing on detecting memory dependencies to minimize the use of Load-Store Queues.

◇ **Sharif University of Technology**, Tehran, Iran
High Performance Computing Architectures and Networks (HPCAN)
Research Assistant under the supervision of Prof. Hamid Sarbazi-Azad Dec. 2018 - present

The aim of the project is to conduct a comprehensive study on the limitations and strengths of linear algebraic kernels in graph processing on GPUs. My main focus is implementing linear algebraic GPU kernels using CUDA, profiling these kernels, and analyzing profiling results.

Work Experience

◇ **Hamravesh Co.**, Tehran, Iran
University Internship Course: Software Engineering Intern at Updamus Feb. - Jun. 2020

Updamus is a website monitoring service offering performance metrics, such as uptime, apdex, response time, etc. My main focus was data visualization and analysis.

University Course Projects

◇ **Smart City Light Poles to Reduce Energy Consumption** Fall 2019
Embedded Systems — Using an Arduino board in Proteus Design Suit, we simulated smart light poles turning on/off based on a cost function operating according to vehicle location and velocity.

◇ **Parallel Implementation of K-means Clustering** Spring 2019
Multicore Computing — Using CUDA programming, I implemented a version of K-means clustering to partition n-dimensional observations that is parallelizable for any number of n.

◇ **PintOS Enhancement to Support Various OS Concepts** Fall 2018
Operating Systems — Based on the course project for CS162@Berkeley, we strengthened PintOS' support for kernel thread scheduling, user program execution, and file systems.

◇ **An Analysis of Timss and Pirls Contest** Spring 2018
Data Analysis — Using R programming language, we conducted a comprehensive analysis on the impact of student, school, and teacher background on test scores.

◇ **RTL to Verilog Converter** Spring 2018
Advanced Logic Design — Using Java, I implemented a converter taking an input RTL description and outputting the behavioral Verilog code.

◇ **JVM Emulator** Spring 2018
Computer Architecture — Using Java, we implemented an emulator taking IJVM input code, showing the inner workings of the microarchitecture. We used this emulator to profile the runtime of a IJVM program, reporting metrics such as resource utilization, throughput, and cache status.

Teaching Experience

◇ **Multicore Computing (Head TA)**, Instructor: Dr. M. Sadrosadati Spring 2020

◇ **Computer Structure and Language**, Instructor: Prof. H. Asadi Fall 2018, 2019

◇ **Computer Structure and Language**, Instructor: Prof. H. Sarbazi-Azad Fall 2019

◇ **Probability and Statistics**, Instructor: Prof. A. Sharifi-Zarchi Fall 2018, 2019

◇ **Introduction to Bioinformatics**, Instructor: Prof. A. Sharifi-Zarchi Spring 2019

◇ **Data Structures and Algorithms**, Instructor: Prof. A. Sharifi-Zarchi Spring 2019

◇ **Data Structures and Algorithms**, Instructor: Prof. M. Ghodsi Fall 2018

Organization Experiences

◇ **HardWar: Sharif Hardware Contest** May 2019
As a key member of the scientific staff, I contributed to designing a Minesweeper game and preparing the infrastructure for the Verilog section.

◇ **Data Days Machine Learning and Data Science Competition** Dec. 2018
As a key member of the scientific staff, I designed the majority of the data analysis tasks and judged the contestants' results and methods.

Languages

Persian (native), **English** (native, born in England), **Arabic** (familiar), **French** (familiar)

Test Scores

◇ **TOEFL iBT**: 117 (Reading: 30, Listening: 30, Speaking: 29, Writing: 28)

◇ **GRE General Test**: 331 (Verbal: 161, Quantitative: 170, Analytical Writing: 4)

Technical Skills

◇ **Software**: Quartus, ModelSim, VPR, git, LaTeX, Proteus, Arduino IDE, Adobe Photoshop

◇ **Programming, HDL, and API**: C/C++, CUDA, OpenMP, R, Python, Java, Verilog, MIPS Assembly, x86 Assembly

Interests

Piano, Violin, Cello: I have 15+ years of experience in recitals and group concerts.