Shabnam Sheikhha

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RESEARCH INTERESTS	High-Performance Computing, Computer Architecture, Hardware Reliability

EDUCATION

◇ **Sharif University of Technology**, Tehran, Iran　　　　　Sep. 2016 - Expected Sep. 2021
B.Sc., Computer Engineering, Major Degree, **Overall GPA: 19.02/20**
B.Sc., Mathematics, Minor Degree, **Overall GPA: 18.62/20**

Relevant courses (**GPA: 19.67/20**): Advanced Computer Architecture (18.8/20, *graduate*), Multicore Computing (19.4/20), Data and Network Security (20/20), Computer Networks (19.4/20), Operating Systems (20/20), Embedded Systems (19.7/20), Digital Systems Design (19.9/20), Linear Algebra (19.4/20), Data Analysis (20/20), Statistics and Applications (20/20)

◇ **Farzanegan High School**, Yazd, Iran　　　　　　　　　　Sep. 2012 - May 2016
Affiliated with National Organization for Development of Exceptional Talents (NODET)
Diploma in Mathematics and Physics, **Overall GPA: 19.85/20**

HONORS AND AWARDS

◇ **Best Paper Award**, FPGA'20　　　　　　　　　　　　　　　　Feb. 2020

◇ **National Elite Foundation Fellowship**　　　　　　　　　　2015 - present

◇ **National University Entrance Exams (Konkur)**
 - Ranked 29th among 162 000+ in Mathematics and Physics　　　Dec. 2015
 - Ranked 4th among 6 000+ in English Language　　　　　　　　Dec. 2015

PUBLICATION

◇ Josipovic, L., **Sheikhha, S.**, Guerrieri, A., Ienne, P., Cortadella, J. Buffer Placement and Sizing for High-Performance Dataflow Circuits. *28th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA'20)*, 2020. **Best Paper Award.**

RESEARCH EXPERIENCE

◇ **Barcelona Supercomputing Center**, Barcelona, Spain
Computer Architecture for Parallel Paradigms
Remote Intern under the supervision of Prof. Osman Unsal　　　Oct. 2020 - present

The aim of the project is to propose a hardware accelerator tailored to applications with irregular memory access patterns such as sparse matrix computations. Our goal is to address two main bottlenecks: irregular memory accesses and index matching.

◇ **École Polytechnique Fédérale de Lausanne (EPFL)**, Lausanne, Switzerland
Processor Architecture Lab (LAP)
Summer@EPFL Program Intern under the supervision of Prof. Paolo Ienne　　Jul. - Dec. 2019

The aim of the project was performance optimization and resource utilization in dataflow circuits. My main focus was implementing strategic buffer placement to reduce the critical path delay and increase the throughput (*published in FPGA'20*). I continued remote work, focusing on detecting memory dependencies to minimize the use of Load-Store Queues.

◇ **Sharif University of Technology**, Tehran, Iran
High Performance Computing Architectures and Networks (HPCAN)
Research Assistant under the supervision of Prof. Hamid Sarbazi-Azad　　Dec. 2018 - present

The aim of the project is to conduct a comprehensive study on the limitations and strengths of linear algebraic kernels in graph processing on GPUs. My main focus is implementing linear algebraic GPU kernels using CUDA, profiling these kernels, and analyzing profiling results.

WORK EXPERIENCE

◇ **Hamravesh Co.**, Tehran, Iran
University Internship Course: Software Engineering Intern at Updamus　　Feb. - Jun. 2020

Updamus is a website monitoring service offering performance metrics, such as uptime, apdex, response time, etc. My main focus was data visualization and analysis.

UNIVERSITY COURSE PROJECTS	⬦ **Smart City Light Poles to Reduce Energy Consumption**	Fall 2019

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Embedded Systems — Using an Arduino board in Proteus Design Suit, we simulated smart light poles turning on/off based on a cost function operating according to vehicle location and velocity.

⬦ **Parallel Implementation of K-means Clustering** — Spring 2019
Multicore Computing — Using CUDA programming, I implemented a version of K-means clustering to partition n-dimensional observations that is parallelizable for any number of n.

⬦ **PintOS Enhancement to Support Various OS Concepts** — Fall 2018
Operating Systems — Based on the course project for CS162@Berkeley, we strengthened PintOS' support for kernel thread scheduling, user program execution, and file systems.

⬦ **An Analysis of Timss and Pirls Contest** — Spring 2018
Data Analysis — Using R programming language, we conducted a comprehensive analysis on the impact of student, school, and teacher background on test scores.

⬦ **RTL to Verilog Converter** — Spring 2018
Advanced Logic Design — Using Java, I implemented a converter taking an input RTL description and outputting the behavioral Verilog code.

⬦ **JVM Emulator** — Spring 2018
Computer Architecture — Using Java, we implemented an emulator taking IJVM input code, showing the inner workings of the microarchitecture. We used this emulator to profile the runtime of a IJVM program, reporting metrics such as resource utilization, throughput, and cache status.

TEACHING EXPERIENCE

⬦ **Multicore Computing (Head TA)**, Instructor: Dr. M. Sadrosadati — Spring 2020

⬦ **Computer Structure and Language**, Instructor: Prof. H. Asadi — Fall 2018, 2019

⬦ **Computer Structure and Language**, Instructor: Prof. H. Sarbazi-Azad — Fall 2019

⬦ **Probability and Statistics**, Instructor: Prof. A. Sharifi-Zarchi — Fall 2018, 2019

⬦ **Introduction to Bioinformatics**, Instructor: Prof. A. Sharifi-Zarchi — Spring 2019

⬦ **Data Structures and Algorithms**, Instructor: Prof. A. Sharifi-Zarchi — Spring 2019

⬦ **Data Structures and Algorithms**, Instructor: Prof. M. Ghodsi — Fall 2018

ORGANIZATION EXPERIENCES

⬦ **HardWar: Sharif Hardware Contest** — May 2019
As a key member of the scientific staff, I contributed to designing a Minesweeper game and preparing the infrastructure for the Verilog section.

⬦ **Data Days Machine Learning and Data Science Competition** — Dec. 2018
As a key member of the scientific staff, I designed the majority of the data analysis tasks and judged the contestants' results and methods.

LANGUAGES
Persian (native), **English** (native, born in England), **Arabic** (familiar), **French** (familiar)

TEST SCORES

⬦ **TOEFL iBT**: 117 (Reading: 30, Listening: 30, Speaking: 29, Analytical Writing: 28)

⬦ **GRE General Test**: Verbal: 161, Quantitative: 170, Writing: 4

TECHNICAL SKILLS

⬦ **Software**: Quartus, ModelSim, VPR, git, LaTeX, Proteus, Arduino IDE, Adobe Photoshop

⬦ **Programming, HDL, and API**: C/C++, CUDA, OpenMP, R, Python, Java, Verilog, MIPS Assembly, x86 Assembly

INTERESTS
Piano, Violin, Cello: I have 13+ years of experience in recitals and group concerts.