# Lab 4: Single-Cycle CPU

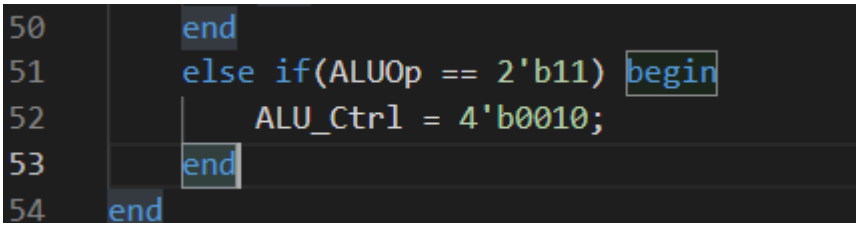
| Instr | RW | B | J | WB | MR | MW | Src | Op |
|---|---|---|---|---|---|---|---|---|
| R-type | 1 | 0 | 0 | 00 | 0 | 0 | 00 | 10 |
| addi | 1 | 0 | 0 | 00 | 0 | 0 | X | 11 |
| Load | 1 | 0 | 0 | 01 | 1 | 0 | X | 00 |
| Store | 0 | 0 | 0 | XX | 0 | 1 | X | 00 |
| Branch | 0 | 1 | 0 | XX | 0 | 0 | 00 | 01 |
| JAL | 1 | 0 | 1 | 1X | 0 | 0 | 0X | XX |
| JALR | 1 | 0 | 1 | 1X | 0 | 0 | 1X | XX |

## What's the problem you encounter?

- I found it very difficult to debug, because there is no easy way of printing the values out.

## Your implement detail.

- The difference in instruction type that requires alu form last time is addi that has opcode == 0010011, so I defined an ALUop == 11,so that the alu knows to do addition when the addi instruction comes in.




The rest is not much different from last time.

## Anything you want to say.

- Why do we have to register our group for every lab,because me and my friend just assumed that the group will stay the same so both of us didn’t register to a group so we’re on our own this time.There’s nothing wrong with registering for every lab, I'm just curious.