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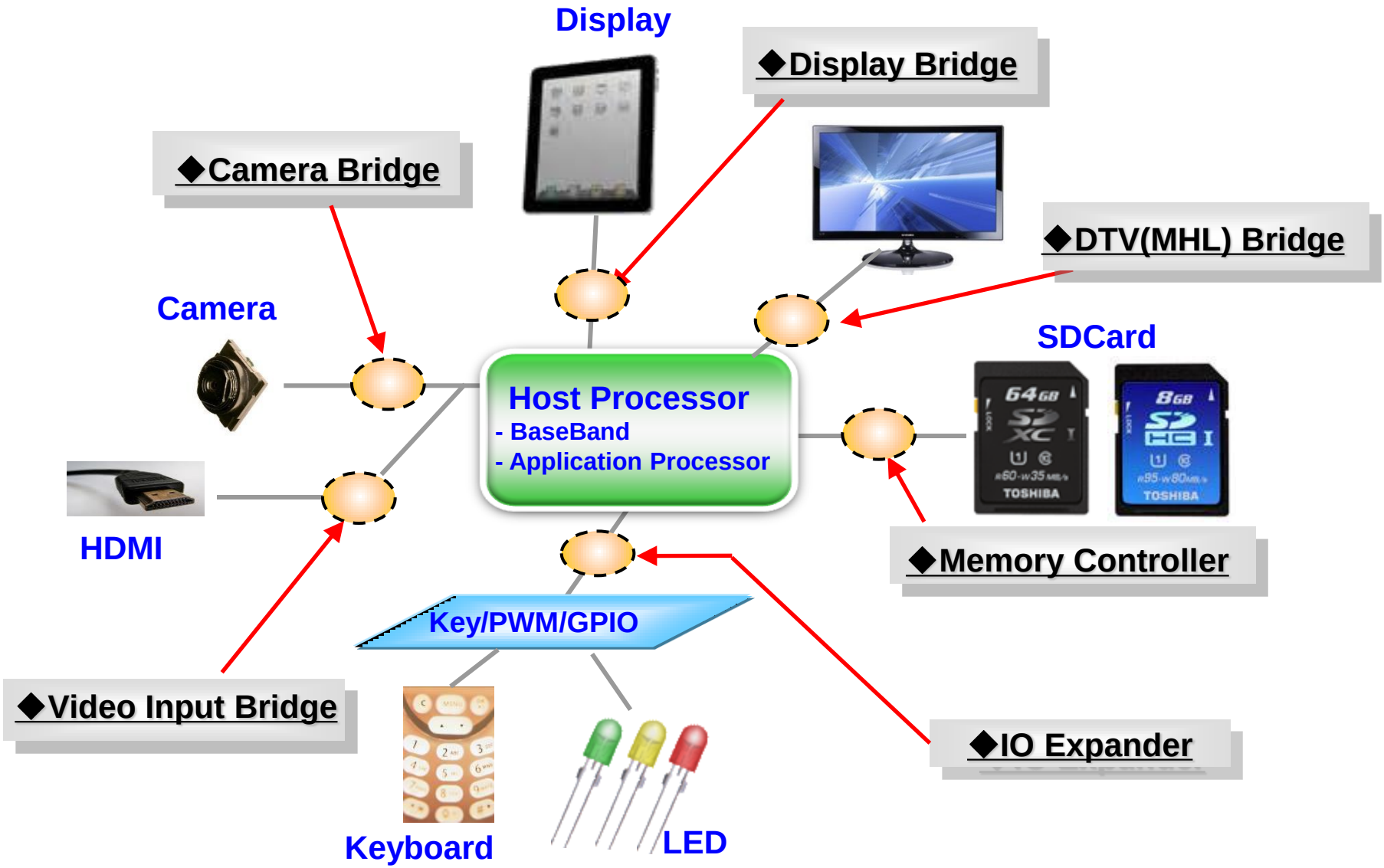
TOSHIBA
Mobile Peripheral Devices (MPD)

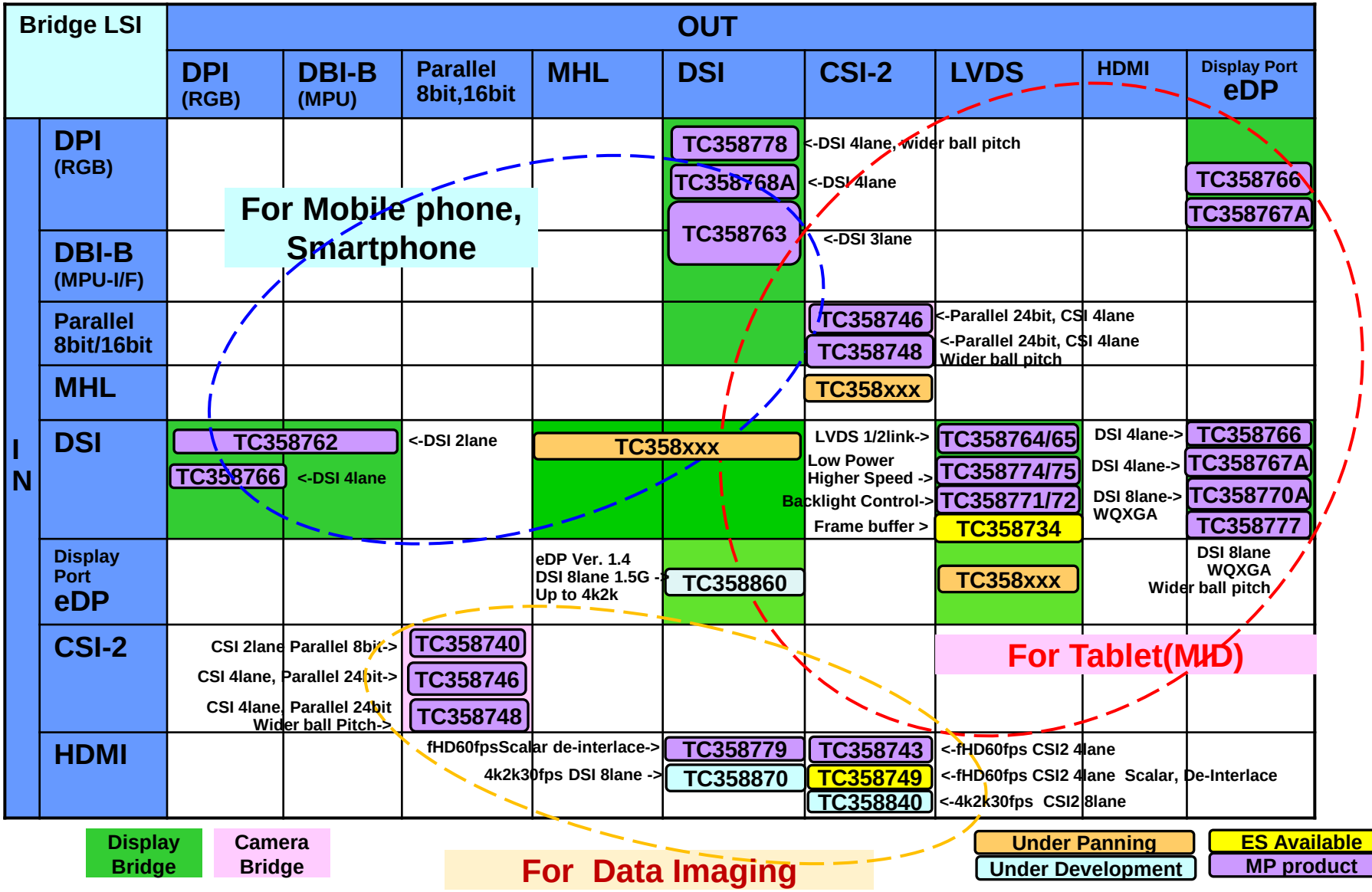
Mar, 2014 (v02wPIF)

TOSHIBA Semiconductor & Storage Products Company

Product Area of MPD



TOSHIBA I/F Bridge LSI Input/Output matrix



Use Cases

Key word:

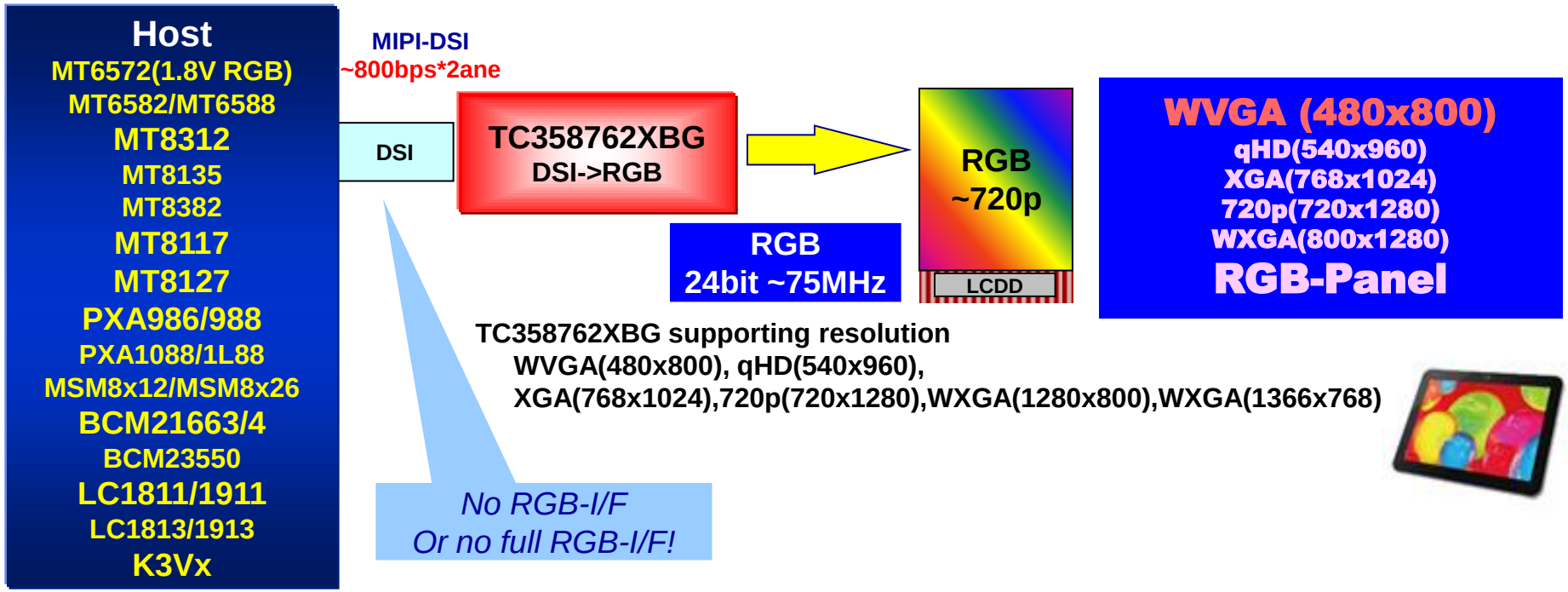
MID, iPad mini, Retina, MIPI, LVDS, eDP, HDMI

[MID] Connection to RGB Display

Several Mobile PFs tend to delete RGB interface to realize smaller die and smaller package.

However still need of RGB display exists for low tier application

-> DSI-> RGB conversion is required.



Low Tier MID

[MID] Connection to LVDS Display

Most common panel for 7”, 10” or bigger is LVDS panel.

Several APPs don’t have LVDS interface.
-> Bridge function is required

Host
MT6572(1.8V RGB)
MT6582/MT6588
MT8312/MT8382
MT8392/MT8395
PXA986/988
PXA1088/1L88
MSM8x25Q/MSM8x30
MSM8x12/MSM8x26
BCM21663/4
BCM23550
LC1911/1913
CloverTrail+(Z25xx)
BayTrail-T(Z3xxx)
BayTrail-T Entry
K3Vx

No LVDS I/F!

DSI

TC358764/65XBG
DSI->LVDS
or
TC358774/75XBG
DSI->LVDS
or
TC358771/72XBG
DSI->LVDS

LVDS
1link(764/774/771)
2link(765/775/772)

LVDS
WSVGA
XGA,WXGA
LCDD

Low Power Version

Low Power Version + Adaptive Backlight Control

WSVGA(1024x600)
XGA(1024x768)
720p(1280x720)
WXGA(1280x800)
WXGA(1366x768)
1080p(1920x1080)
WUXGA(1920x1200)
LVDS-Panel

Connection to LVDS Panel

TC358764/774/771XBG supporting resolution
~WSVGA(1024x600), XGA(1024x768),WXGA(1280x800,1366x768)

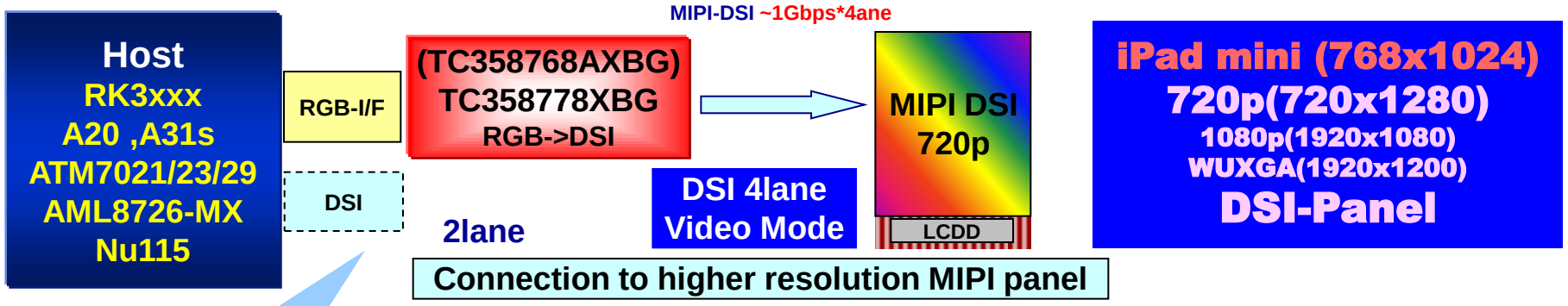
TC358765/775/772XBG supporting resolution ~WUXGA(1920x1200)

MID

[MID]Connection to DSI Display

MIPI-DSI is defacto Standard in mobilephone. MID market also starts following this trend.

A certain APP only has 2lane DSI or no DSI.
-> 720p panel needs 4lanes.
For 4lane connection, bridge function is required



2lane only or no DSI! Cannot connect to 4lane panel

TC358768AXBG/TC358778XBG supporting resolution
~720p(720x1280),WXGA(1280x800),WXGA(1366x768), FullHD(1920x1080), WUXGA(1920x1200)

"iPad mini" type MID

[MID] Connection to Display Port(eDP)

Interface of Note PC LCD is changing to eDP. MID also starts using eDP LCD panel.

However several APPs don't have Display Port Interface.
-> Bridge function is required

Host
MT6589/8389
MT8125/8135
MT8312/8382
MT6592/MT8392
ATM7039
A31
PXA1088/1L88
MSM8x12/MSM8x26
BCM21663/4, 23550
LC1911/1913/1960
CloverTrail+(Z25xx)
K3Vx

MIPI-DSI ~1Gbps*4lane*1link
Stream Mode

Support ASSR for eDP panel

DSI

TC358770(A)XBG
TC358777XBG
DSI->DP

Display Port 1.62/2.7G * 4channel

Display Port
~1920x1200
LCDD

1366x768
1920x1080
1920x1200
eDP Panel

Max resolution 1920x1200, 24bpp@60fps

Host
RK3xxx
A20 ,A31s
ATM7021/23/29
AML8726-MX
Nu115

RGB 24bit, PCLK max 154MHz
60fps

RGB

TC358766/67AXBG
RGB->DP

Display Port 1or 2chnnel

Display Port
~WUXGA
LCDD

1 panel mode
Video data coming from DPI

1366x768
1920x1080
1920x1200
eDP Panel

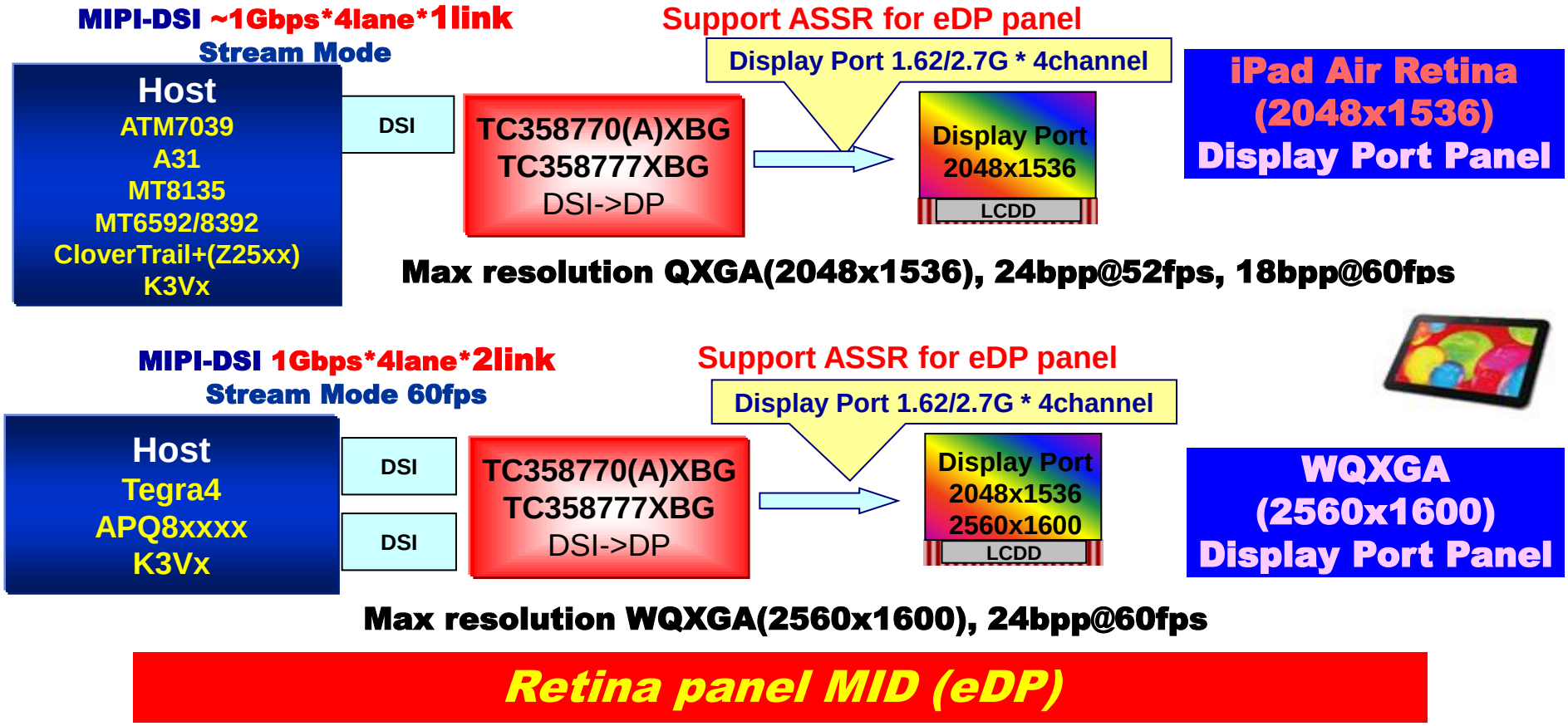
Max resolution 1920x1200, 24bpp@60fps

MID using Note PC panel (eDP)

[MID] Connection to Display Port(eDP)

Interface of High Resolution (WQXGA) Display for MID and Ultra book will be Display Port (eDP)

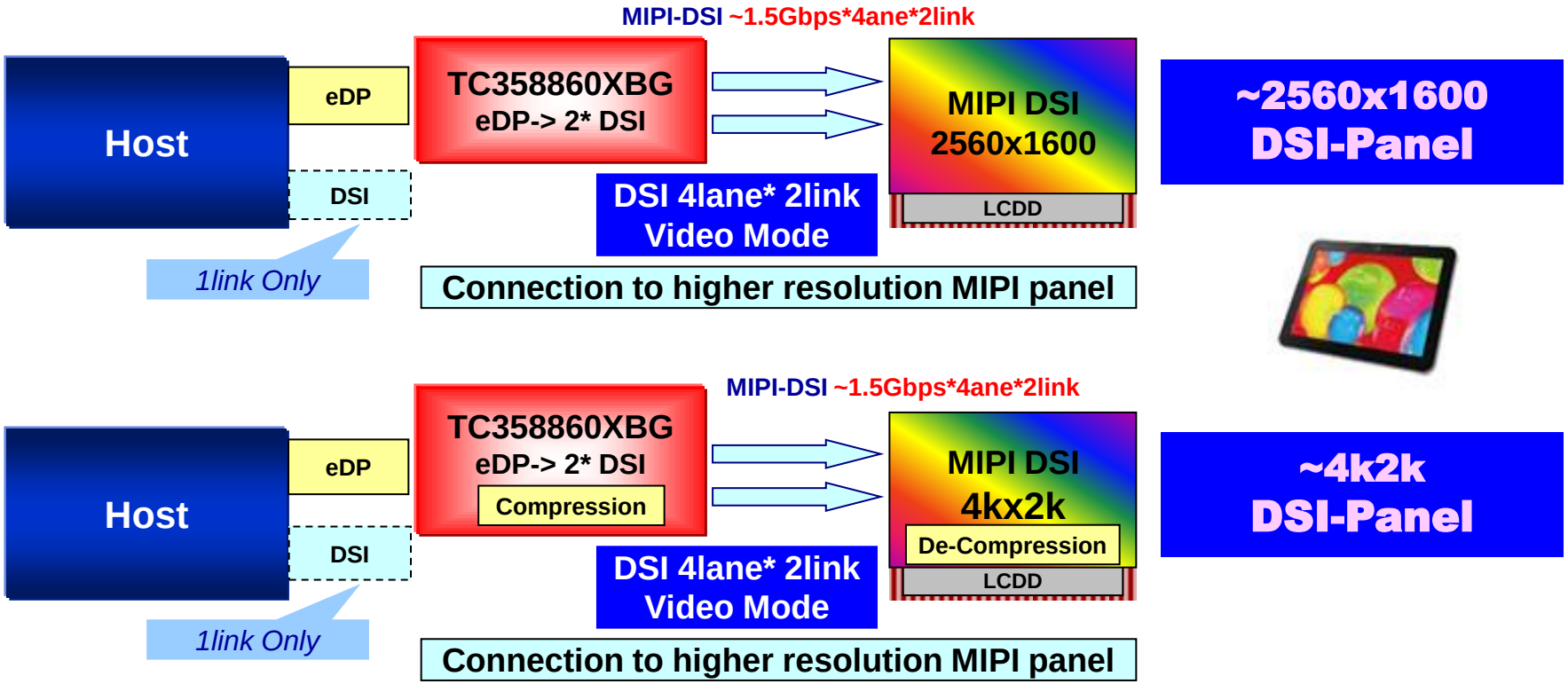
Several APPs don't have Display Port Interface.
-> Bridge function is required



Retina panel MID (eDP)

[MID] Connection to Hi Reso MIPI Display

DSI * 2link High Resolution LCD is one of the trend in mobile market. APPs having 2link DSI are not many and limited.
On the other hand, APPs embedding eDP for High Resolution application are increasing.
-> eDP to 2link DSI conversion is expected.

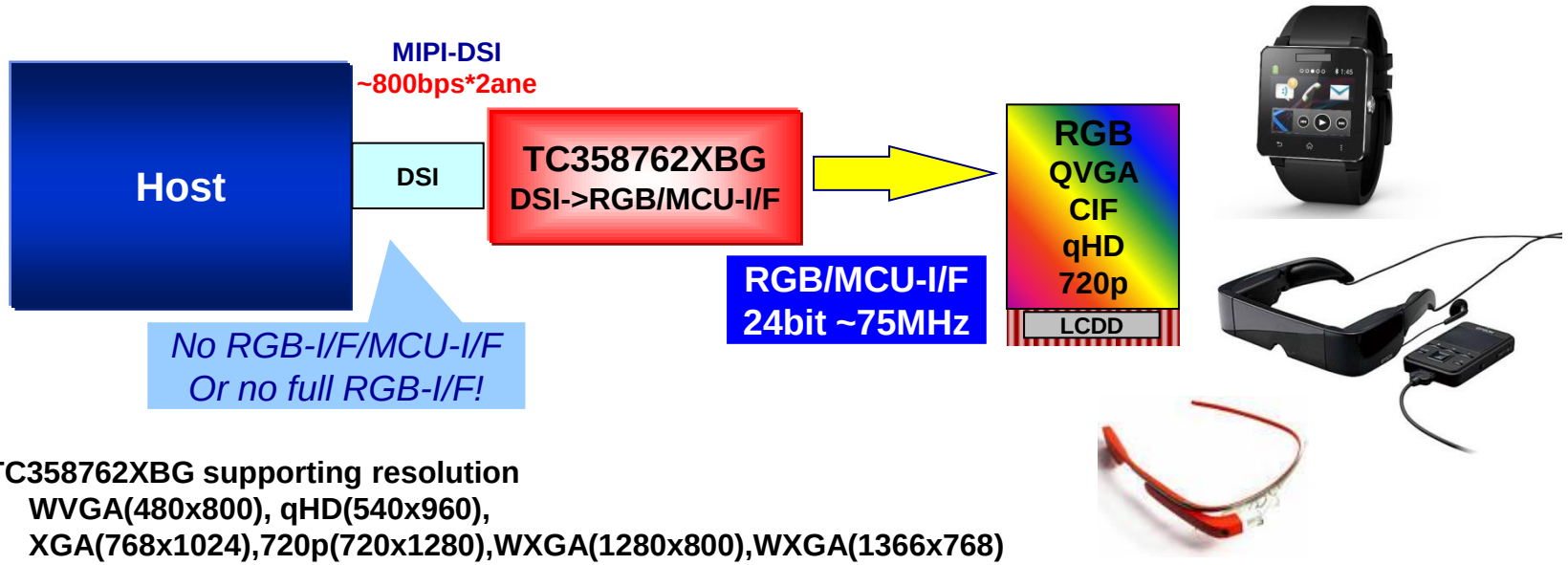


"2560x1600" , 4k2k MID

[Smart watch, HMD] Connection to RGB/MCU-I/F Display

New devices such as Smart watch, Head Mount Display use small size special LCDs. Special LCDs normally adopt RGB I/F, MCU-I/F.

However latest PF deleted RGB-I/F/MCU-I/F.
For connection to latest PF
-> DSI-> RGB/MCU-I/F conversion is required.

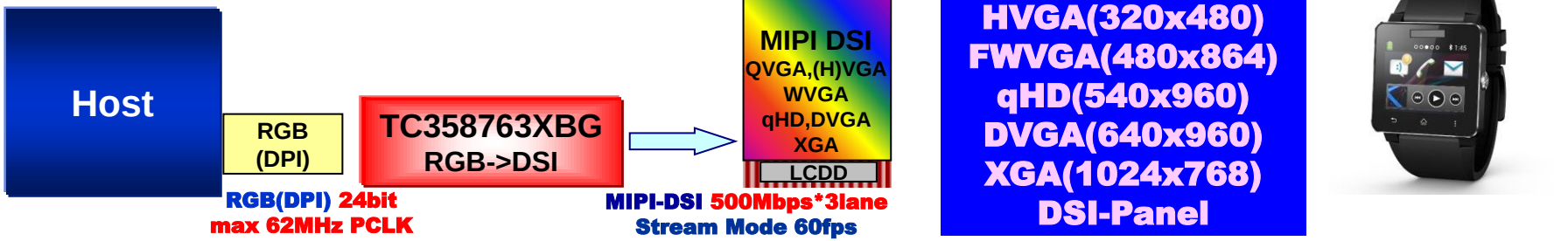


TC358762XBG supporting resolution
WVGA(480x800), qHD(540x960),
XGA(768x1024),720p(720x1280),WXGA(1280x800),WXGA(1366x768)

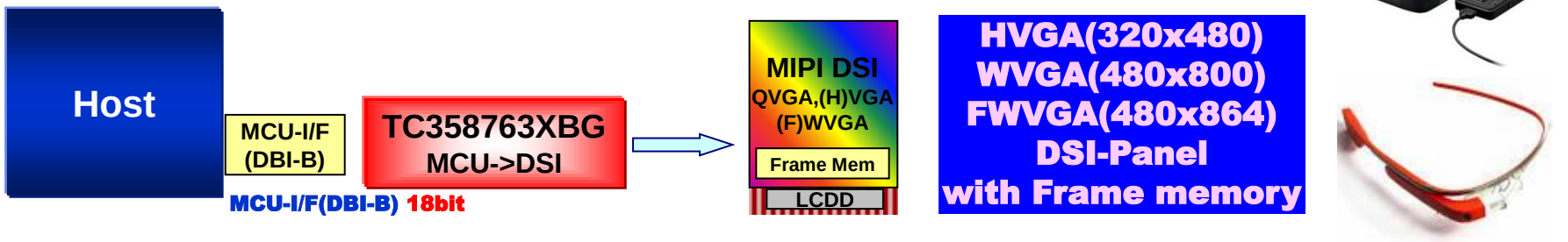
Smart watch, Head Mount Display(HMD) with latest PF

[Smart watch, HMD] Connection to DSI Display

New devices such as Smart watch, Head Mount Display use small size LCDs. Some LCD adopt MIPI DSI as interface.
However, PF used for wearable equipment sometimes doesn't have MIPI DSI interface.
-> RGB/MCU-> DSI conversion is required.

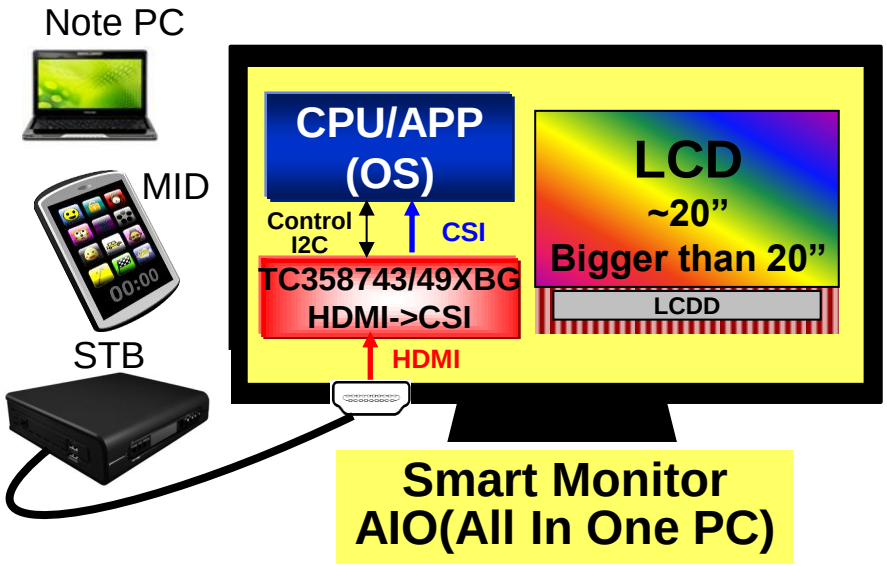


Max resolution XGA(1024x768), 24bpp



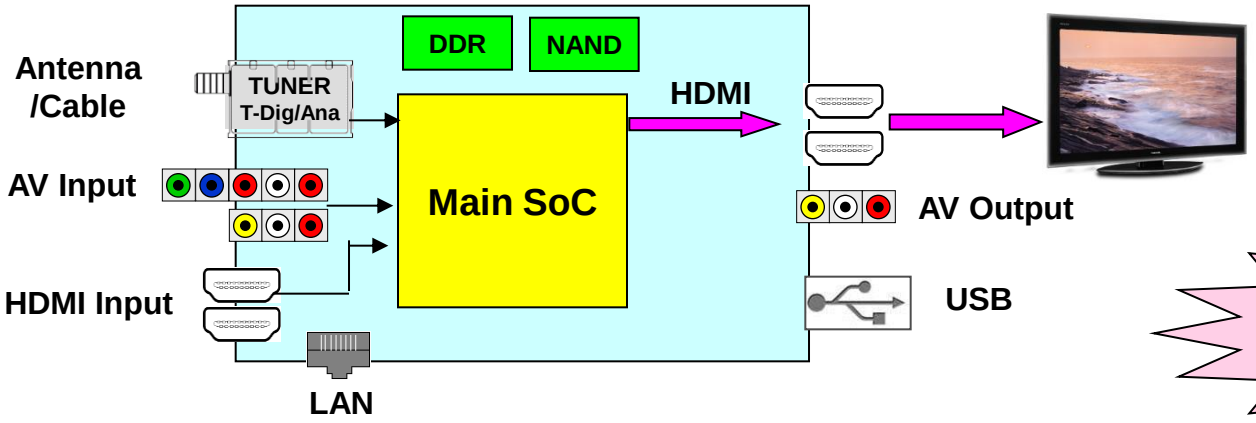
Smart watch, Head Mount Display(HMD) using MIPI LCD

[Smart Monitor, AIO(All In One PC)] HDMI to CSI2



[Smart STB] HDMI to CSI2

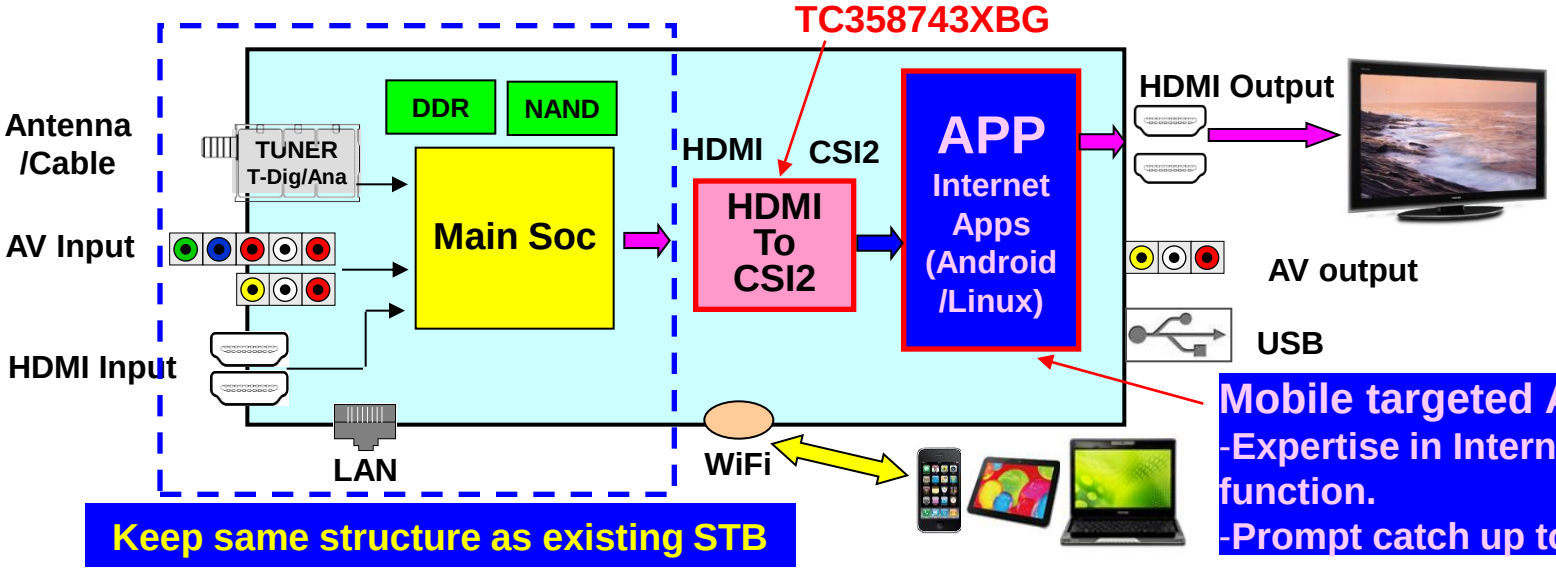
＜Existing STB Solution＞ No internet/PC related function



Adding internet/PC related function

＜Smart STB Solution＞

Adding Internet/PC related function based on Android/linux



Smart STB

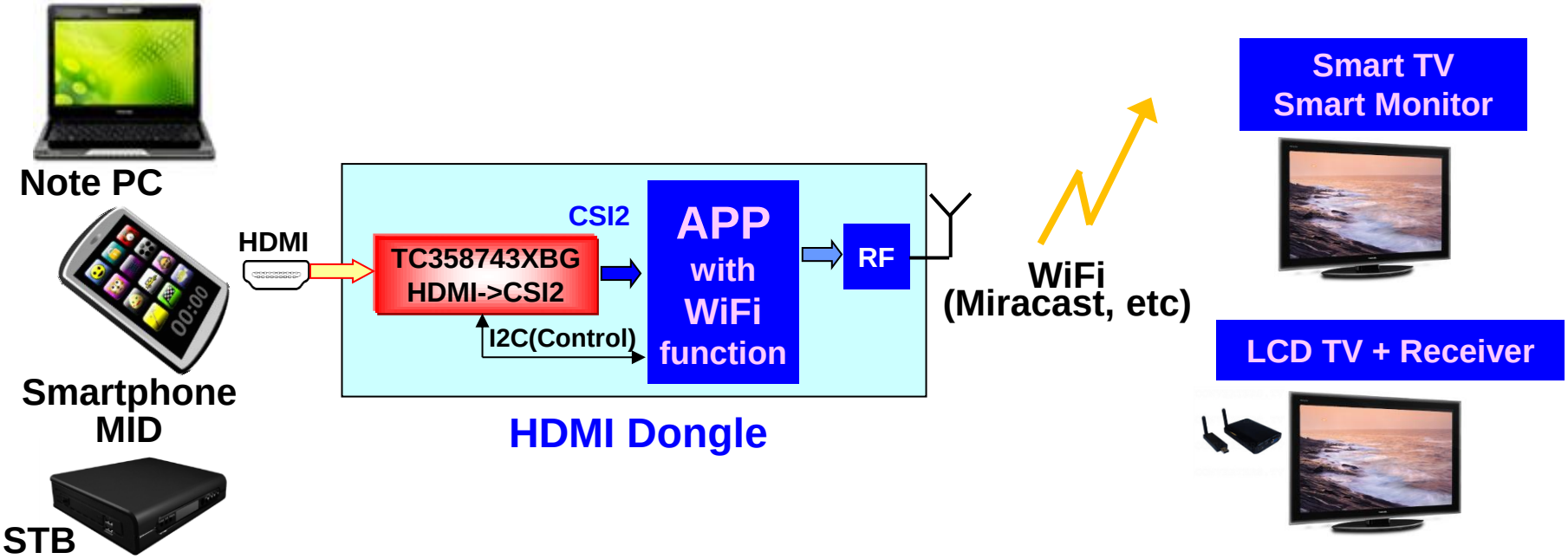
Keep same structure as existing STB

Mobile targeted APP
-Expertise in Internet/PC related function.
-Prompt catch up to latest OS

[Wireless HDMI] HDMI to CSI2

Make HDMI interface wireless

Any equipment having HDMI output can have wireless visual connection to TV/Monitor

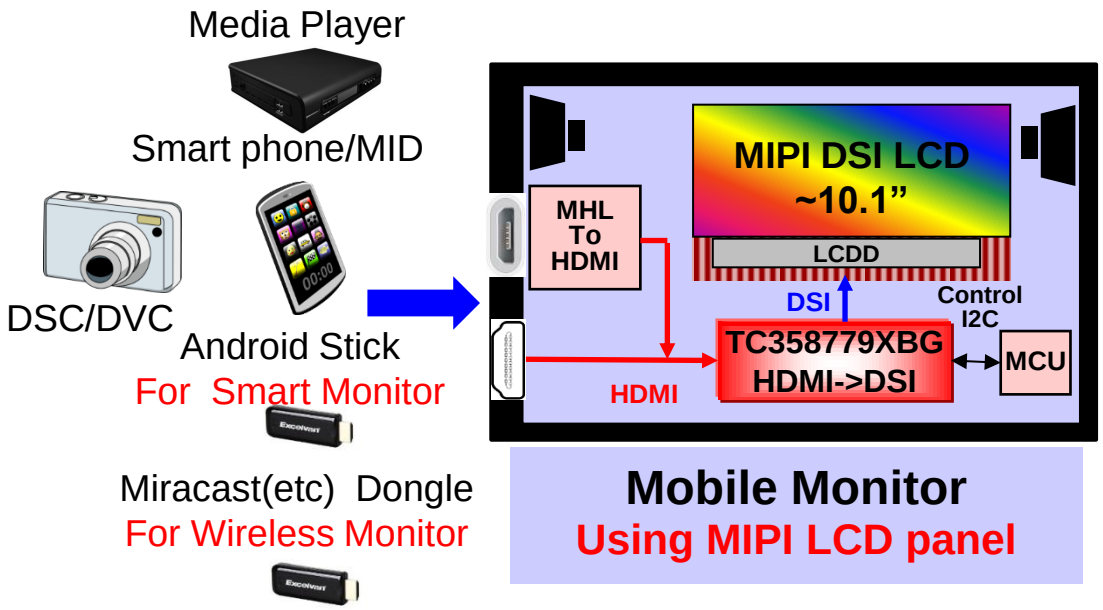


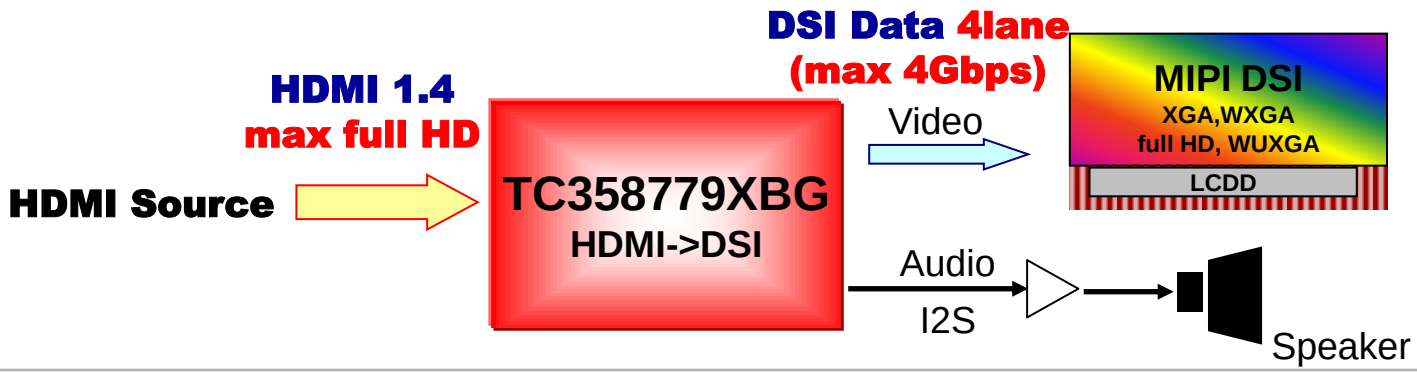
[Mobile Monitor] HDMI->DSI(TC358779XG)

MIPI Panel is very common in mobile market

Can select from many variety.

Can get with cheaper price



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Other Use Cases

Connection to DSI Display (Use Case2)

For APPs which don't have MIPI-DSI
(LCD resolution: smaller than 720p)

Max resolution DVGA(640x960), 18bpp

HVGA(320x480)
FWVGA(480x864)
qHD(540x960)
DVGA(640x960)
DSI-Panel

Max resolution XGA(1024x768), 24bpp

HVGA(320x480)
FWVGA(480x864)
qHD(540x960)
DVGA(640x960)
XGA(1024x768)
DSI-Panel

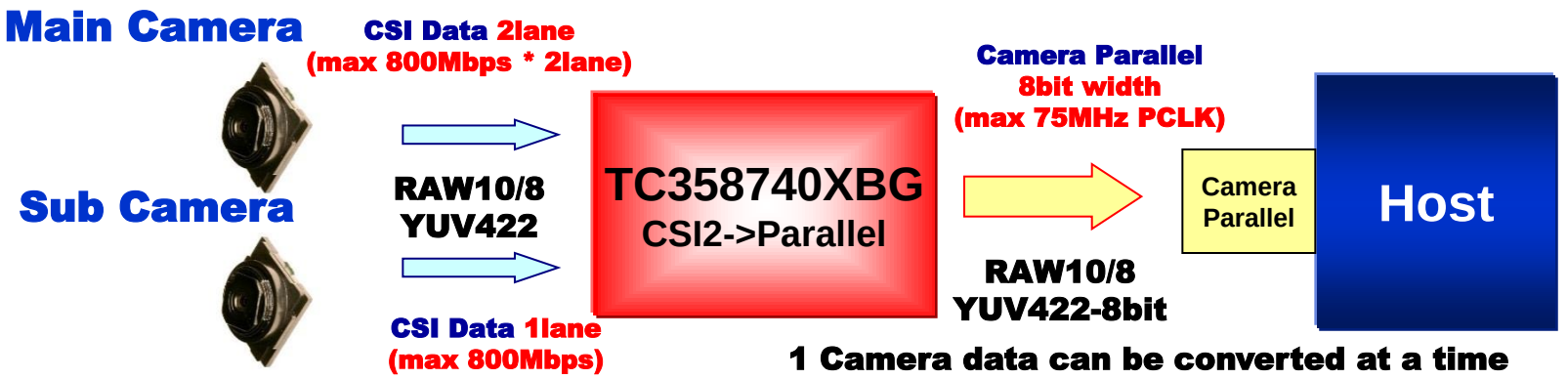
Max resolution FWVGA(480x864)

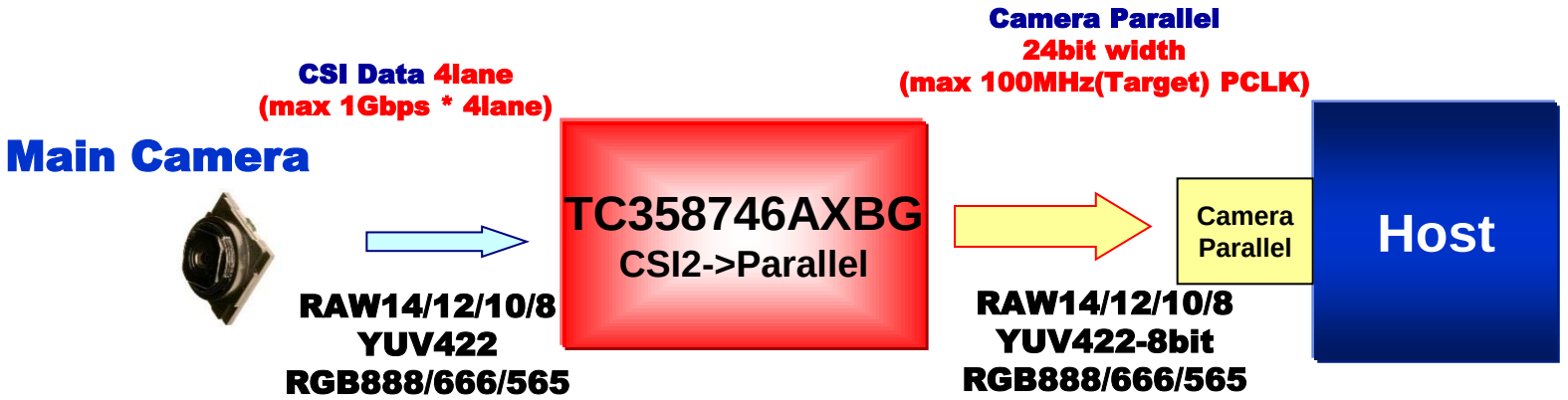
HVGA(320x480)
WVGA(480x800)
FWVGA(480x864)
DSI-Panel
with Frame memory

Camera Bridge Solution(1) (MIPI-CSI->Parallel)

Connection to MIPI-CSI2 Camera

~ Host doesn't have CSI2. Host has only parallel I/F ~

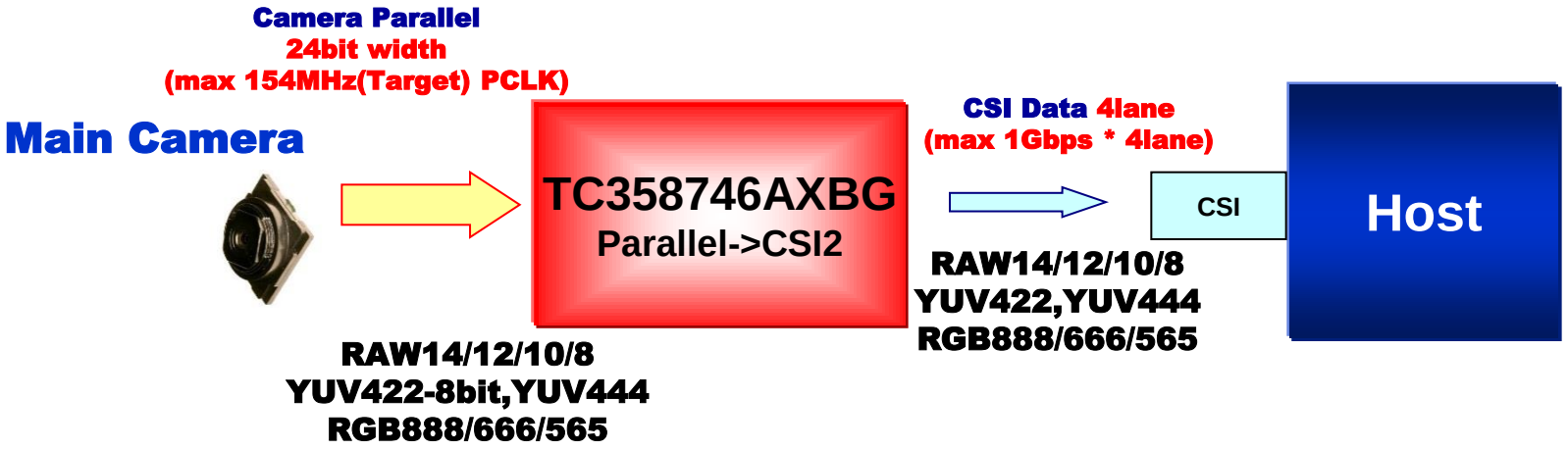




Camera Bridge Solution(2) (MIPI-CSI->Parallel)

Connection to Parallel I/F Camera

~ Want to use Parallel I/F camera, but Host doesn't have parallel I/F ~



Product Detail

Display Bridge Product Table (1)

	TC358760	TC358762	TC358763
Input	MDDI 1.2 Type1	MIPI DSI 2 Lanes x 1ch	MIPI DPI(24bit) MIPI DBI-B(18bit)
Output	MIPI DSI 3Lanes x 1ch.	MIPI DPI/DBI -B (24bit)	MIPI DSI 3Lanes x 1ch
Resolution	DVGA(640x960) @18bit	WXGA(1366x768) @18bit	XGA(1024 x 768) @24bit
Note	---	---	---
PKG	VFBGA49 3.5mm x 3.5mm 0.4mm pitch	VFBGA64 5mm x 5mm 0.5mm pitch	VFBGA72 4.5mm x 4.5mm 0.4mm pitch
ES	Available	Available	Available
MP	Available	Available	Available

Display Bridge Product Table (2)

	TC358768A	TC358778	TC358764	TC358765	TC358774	TC358775	TC358771	TC358772
Input	MIPI DPI (24bit)	MIPI DPI (24bit)	MIPI DSI 4 Lanes x 1ch.	MIPI DSI 4 Lanes x 1ch.	MIPI DSI 4 Lanes x 1ch	MIPI DSI 4 Lanes x 1ch	MIPI DSI 4 Lanes x 1ch.	MIPI DSI 4 Lanes x 1ch.
Output	MIPI DSI 4 Lanes x 1ch.	MIPI DSI 4 Lanes x 1ch.	LVDS Single Link (5 pairs/ link)	LVDS Dual Link (5 pairs / link)	LVDS Single Link (5 pairs/ link	LVDS Dual Link (5 pairs / link)	LVDS Single Link (5 pairs / link)	LVDS Dual Link (5 pairs / link)
Reso-lution	WUXGA 1920x1200 @24bit	WUXGA 1920x1200 @24bit	WSXGA 1440x900 @24bit	WUXGA 1920x1200 @18bit	UXGA 1600x1200 @24bit	WUXGA 1920x1200 @24bit	UXGA 1600X1200 @24bi	WUXGA 1920x1200 @24bit
Note	---	For Non HDI PCB	---	---	Low Power (1.8V LVDS) 135M LVDS Clk	Low Power (1.8V LVDS) 135M LVDS Clk	Adaptive Back Light Control	Adaptive Back Light Control
PKG	VFBGA72 4.5mmx4.5mm 0.4mm pitch	TFBGA80 7mmx7mm 0.65mm pitch	TFBGA49 5mm x 5mm 0.65mm pitch	TFBGA64 6mm x 6mm 0.65mm pitch	TFBGA49 5mm x 5mm 0.65mm pitch	TFBGA64 6mm x 6mm 0.65mm pitch	TFBGA49 5mm x 5mm 0.65mm pitch	TFBGA64 6mm x 6mm 0.65mm pitch
ES	Available	Available	Available	Available	Available	Available	Available	Available
MP	Available	Available	Available	Available	Available	Available	Available	Available

Display Bridge Product Table (3)

	TC358766	TC358767A	TC358770A	TC358777	TC358779	TC358860	
Input	MIPI DSI 4 Lanes x 1ch. / MIPI DPI (24bit)	MIPI DSI 4 Lanes x 1ch.	MIPI DSI 4 Lanes x 2ch	MIPI DSI 4 Lanes x 2ch	HDMI 1.4a	eDP 4ch 1.62G/2.7G/5,4G	
Output	Display Port x 2 Ports / MIPI DPI (24bit)	Display Port x 2 Ports	Display Port x 4Ch	Display Port x 4Ch	MIPI DSI 4 Lanes x 1ch	MIPI DSI(1.5G) 4 Lanes x 2ch	
Reso-lution	WUXGA 1920 x 1200 @24bit	WUXGA 1920 x 1200 @24bit	WQXGA 2560 x 1600@24bit	WQXGA 2560 x 1600@24bit	Full HD 1920x1080@24bit	2560x1600 4k2k with comprewssion	
Note	---	---	-Audio Support -Support ASSR	-For Non HDI PCB -Wider ball pitch version of TC358770A	-Audio Support -Scalar -De-Interlace	Compression function for 4K2K LCD	
PKG	VFBGA120 6mm x 6mm 0.5mm pitch	VFBGA81 5mm x 5mm 0.5mm pitch	VFBGA100 5mm x 5mm 0.4mm pitch	TFBGA80 7mmx7mm 0.65mm pitch	TFBGA80 7mmx7mm 0.65mm pitch	VFPGA64 5,mmx5mm 0.5mm pitch (Tentative)	
ES	Available	Available	Available	Available	Available	2014/Q2	
MP	Available	Available	Available	Available	Available	2014/Q4	

MIPI CSI2 bridge Product Table

	TC358740	TC358746A	TC358748	TC358743	TC358749
Input	MIPI CSI2 RX 2 Data Lanes x 1ch, 1 Data lanes x1ch	- MIPI CSI2-RX 4Data LanesX1ch - Parallel input 24bit@154MHz	- MIPI CSI2 RX 4 Data Lanes x 1ch - Parallel input 24bit@154MHz	HDMI 1.4a	HDMI 1.4a
Output	- MDDI1.2 - Parallel 8bit@70MHz	- Parallel output 24bit@100MHz - MIPI CSI2-TX 4Data LanesX1ch	- Parallel output 24bit@100MHz - MIPI CSI2-TX 4Data LanesX1ch	- MIPI CSI2-TX 4Data LanesX1ch	- MIPI CSI2-TX 4 Data Lanes x 1ch
Note	-	-	- For Non HDI PCB - Wider ball pitch version of TC358746A	Audio Support	-Audio Support -Scalar -De-Interlace
PKG	VFBGA49 3.5mm x 3.5mm 0.4mm pitch	VFBGA72 4.5mm x 4.5mm 0.4mm pitch	TFBGA80 7mmx7mm 0.65mm pitch	TFBGA64 6mm x 6mm 0.65mm pitch	TFBGA80 7mmx7mm 0.65mm pitch
ES	Available	Available	Available	Available	Available
MP	Available	Available	Available	Available	Q3,2014

TC358774/75XBG
(MIPI->LVDS Low Power Bridge)

Comparison between 764/65 and 774/75

		TC358764XBG	TC358765XBG	TC358774XBG	TC358775XBG
Input	DSI	MIPI DSI 4 lane	MIPI DSI 4 lane	MIPI DSI 4 lane	MIPI DSI 4 lane
Output	LVDS	1-link	2-link	1 link	2 link
Video Format	DSI	RGB565,RGB666, RGB666 (loosely packed) RGB888	RGB565,RGB666, RGB666 (loosely packed) RGB888	RGB565,RGB666, RGB666 (loosely packed) RGB888	RGB565,RGB666, RGB666 (loosely packed) RGB888
	LVDS	RGB565, RGB666, RGB888	RGB565, RGB666, RGB888	RGB565, RGB666, RGB888	RGB565, RGB666, RGB888
Video Size	LVDS	~WXGA 1280x800,1366x768@24bit	WUXGA1920x1200@18bit	1600x1200@24bit	WUXGA 1920x1200@24bit
Link Speed	DSI	Up to 800Mbps/Lane	Up to 800Mbps/Lane	Up to 1 Gbps/lane	Up to 1 Gbps/lane
	LVDS	85 MHz	170 MHz	135 MHz	270 MHz
I2C(100K/400KHz)		Slave/Master	Slave/Master	Slave/Master	Slave/Master
Power Supply		1.2V/1.8V ~ 3.3V/3.3V	1.2V/1.8V ~ 3.3V/3.3V	1.2V/1.8V	1.2V/1.8V
Power Consumption		75MHz LVDS (Single LVDS link) 160 mW	1920x1080 24bit @60fps (Dual LVDS link) 275mW	1366x1080 18bit@60fps (Single LVDS link) 68mW	1920x1080 18bit @60fps (Dual LVDS link) 95mW
Stand-by sate by STBY pin		-	-	By STBY pin control VDDIO=ON, VDDC=OFF state is possible	By STBY pin control VDDIO=ON, VDDC=OFF state is possible
Package		5.0mmx5.0mmx1.2mm, BGA49 0.65mm Pitch	6.0mmx6.0mmx1.20mm BGA 64 0.65mm Pitch	5.0mmx5.0mmx1.2mm, BGA49 0.65mm Pitch	6.0mmx6.0mmx1.20mm BGA 64 0.65mm Pitch
Status		MP	MP	MP	MP

Advantage of TC358774/75

- Low Power Consumption

1.8V LVDS PHY is adopted.

1920x1080 18bit @60fps
TC358765XBG(Current Product) -> 275mW
TC358775XBG -> 95mW **cutting off 65% power**

- 1Gbps DSI input support

1Gbps/lane D-PHY is adopted.
1920x1200, 24bit 60fps is supported.

- High Speed LVDS Clock support

135MHz LVDS clock is supported.
Certain vender's LCD panel needs over 100MHz LVDS clock.

-Stand-by operation

Stand-by state -> Keep I/O power on and cut off core power is possible.
TC358774/75XBG can share LDO used for Host I/O.

Difference between 764/765 and 774/775

- Common level of LVDS signal

TC358765XBG(Current Product) -> 1125mV~1375mV
TC358774/75XBG -> 800mV~1000mV

- STBY signal

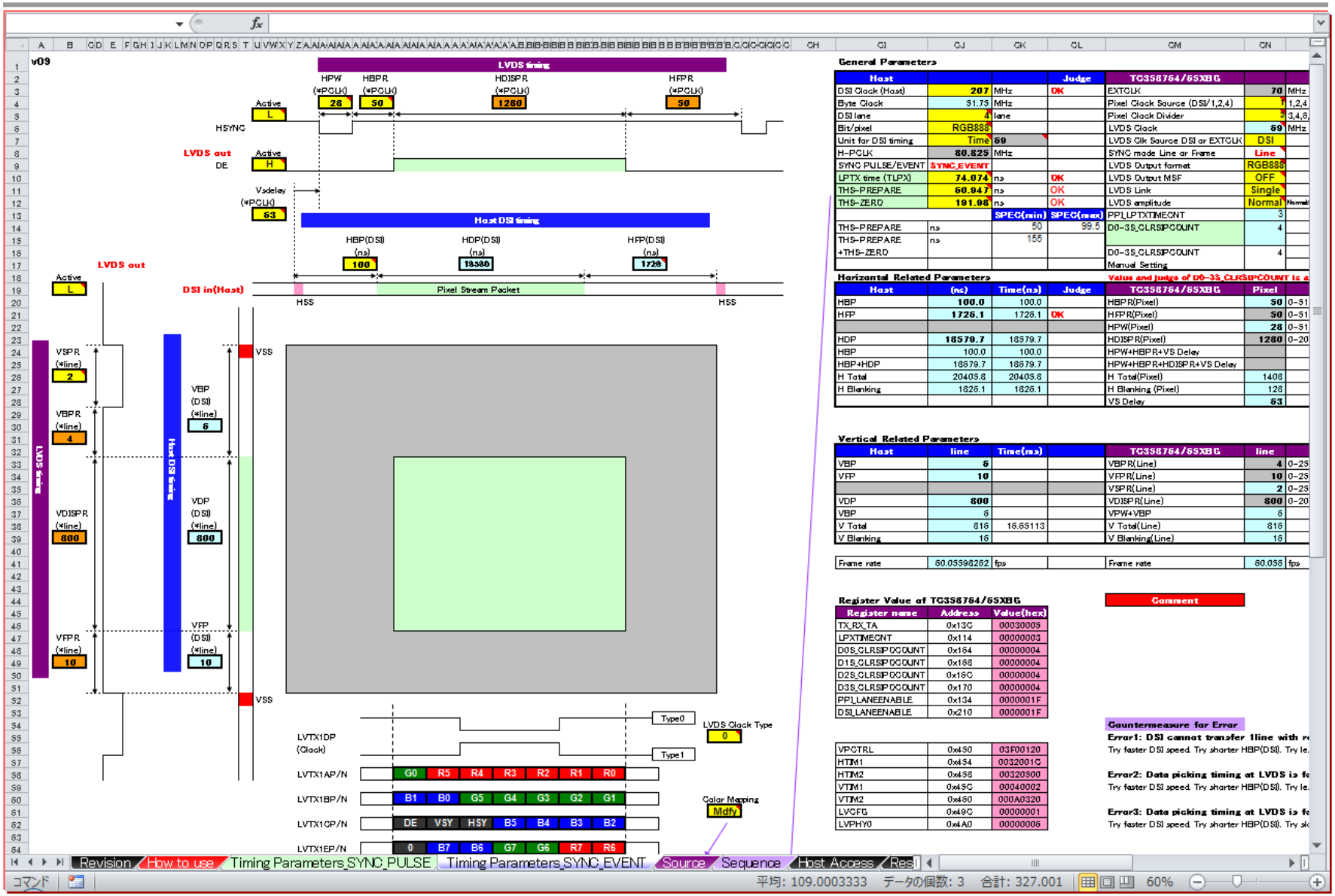
TC358774/75XBG
-> STBY pin is mapped to GPIO pin of TC358764/65XBG (GPIO4)

- Voltage for LVDS part

TC358765XBG(Current Product) -> 3.3V (VDD_LVDS*_33)
TC358774/75XBG -> 1.8V (VDD_LVDS*_18)

* Pin distribution diagram of TC358764/65XBG and TC358774/75XBG is the same except for special function (STBY) added on GPIO4 pin.

TC358774/75XBG Setting Sequence generation tool (1)



Host			Judge	TC358764/65XBG		
DSI Clock (Host)	207	MHz	OK	EXTCLK	70	MHz
Byte Clock	51.75	MHz		Pixel Clock Source (DSI/1,2,4)	1	1,2,4
DSI lane	4	lane		Pixel Clock Divider	3	3,4,6,
Bit/pixel	RGB888			LVDS Clock	69	MHz
Unit for DSI timing	Time	69		LVDS Clk Source DSI or EXTCLK	DSI	
H-PCLK	80.825	MHz		SYNC mode Line or Frame	Line	
SYNC PULSE/EVENT	SYNC_EVENT			LVDS Output format	RGB888	
LPTX time (TLPX)	74.074	ns	OK	LVDS Output MSF	OFF	
THS-PREPARE	60.947	ns	OK	LVDS Link	Single	
THS-ZERO	191.98	ns	OK	LVDS amplitude	Normal	Normal
		SPEC(min)	SPEC(max)	PPI_LPTXTIMECNT	3	
THS-PREPARE	ns	50	99.5	D0-3S_CLRSIPCOUNT	4	
THS-PREPARE +THS-ZERO	ns	155				
				D0-3S_CLRSIPCOUNT Manual Setting	4	

Value and Judge of D0-3S_CLRSIPCOUNT is a

Host	(ns)	Time(ns)	Judge	TC358764/65XBG	Pixel	
HBP	100.0	100.0		HBPR(Pixel)	50	0-31
HFP	1726.1	1726.1	OK	HFPR(Pixel)	50	0-31
				HPW(Pixel)	28	0-31
HDP	18579.7	18579.7		HDISPR(Pixel)	1280	0-20
HBP	100.0	100.0		HPW+HBPR+VS Delay		
HBP+HDP	18679.7	18679.7		HPW+HBPR+HDISPR+VS Delay		
H Total	20405.8	20405.8		H Total(Pixel)	1408	
H Blanking	1825.1	1825.1		H Blanking (Pixel)	128	
				VS Delay	53	

Host	line	Time(ms)		TC358764/65XBG	line	
VBP	6			VBPR(Line)	4	0-25
VFP	10			VFPR(Line)	10	0-25
				VSPR(Line)	2	0-25
VDP	800			VDISPR(Line)	800	0-20
VBP	6			VPW+VBP	6	
V Total	816	16.65113		V Total(Line)	816	
V Blanking	16			V Blanking(Line)	16	
Frame rate	60.05398252	fps		Frame rate	60.056	fps

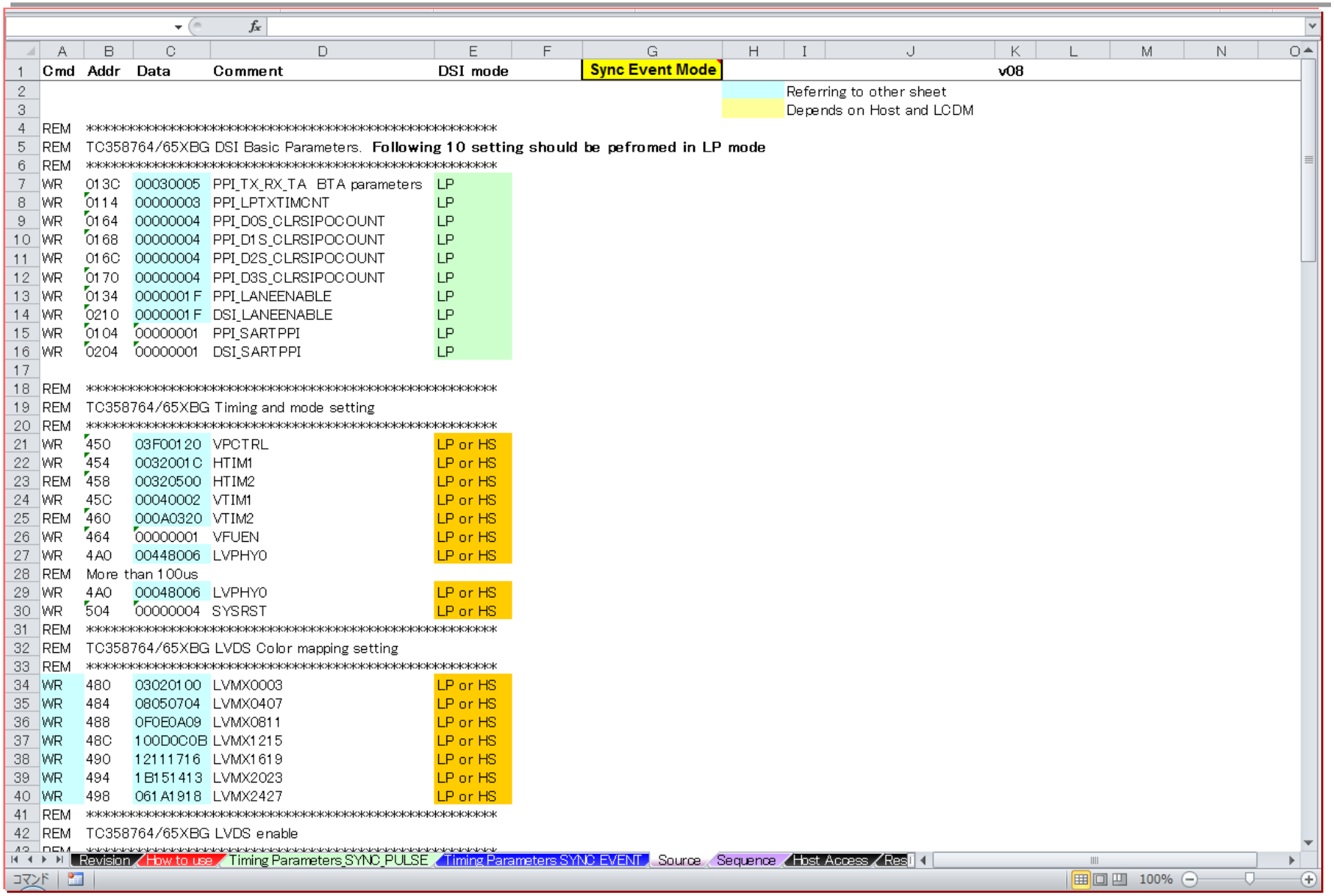
Register name	Address	Value(hex)
TX_RX_TA	0x13C	00030003
LPXTIMECNT	0x114	00000003
D0S_CLRSIPCOUNT	0x164	00000004
D1S_CLRSIPCOUNT	0x168	00000004
D2S_CLRSIPCOUNT	0x16C	00000004
D3S_CLRSIPCOUNT	0x170	00000004
PPI_LANEENABLE	0x134	0000001F
DSI_LANEENABLE	0x210	0000001F
VPCTRL	0x450	03F00120
HTIM1	0x454	0032001C
HTIM2	0x458	00320500
VTIM1	0x45C	00040002
VTIM2	0x460	000A0320
LVCFG	0x49C	00000001
LVPHY0	0x4A0	00000008

Error1: DSI cannot transfer 1line with r
Try faster DSI speed. Try shorter HBP(DSI). Try le.

Error2: Data picking timing at LVDS is fa
Try faster DSI speed. Try shorter HBP(DSI). Try le.

Error3: Data picking timing at LVDS is fa
Try faster DSI speed. Try shorter HBP(DSI). Try sl

TC358774/75XBG Setting Sequence generation tool (2)



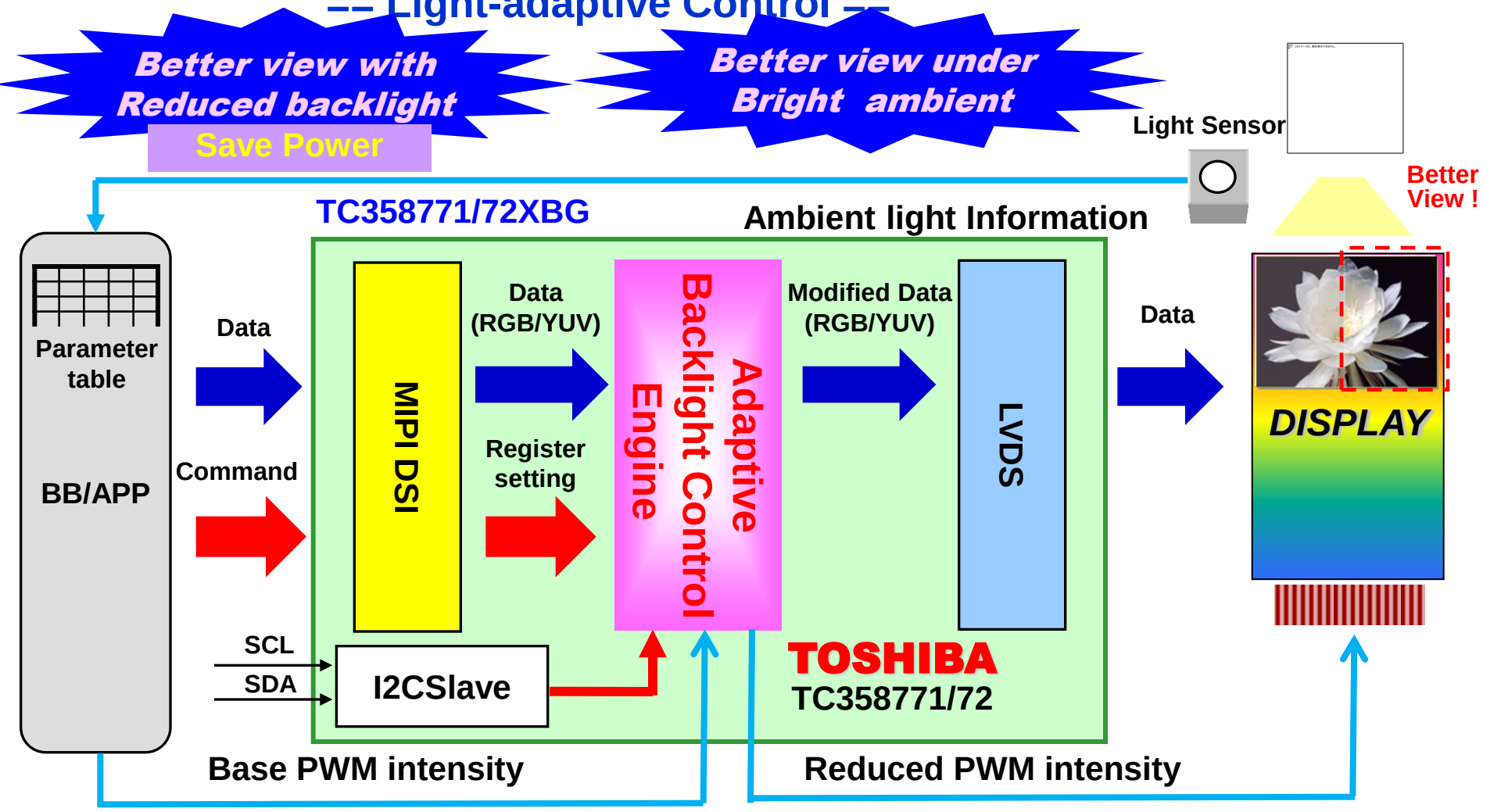
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1	Cmd	Addr	Data	Comment	DSI mode		Sync Event Mode				v08				
2										Referring to other sheet					
3										Depends on Host and LCDM					
4	REM	**********													
5	REM	TC358764/65XBG DSI Basic Parameters. **Following 10 setting should be pefromed in LP mode**													
6	REM	**********													
7	WR	013C	00030005	PPI_TX_RX_TA BTA parameters	LP										
8	WR	0114	00000003	PPI_LPTXTIMCNT	LP										
9	WR	0164	00000004	PPI_D0S_CLRSIPOCOUNT	LP										
10	WR	0168	00000004	PPI_D1S_CLRSIPOCOUNT	LP										
11	WR	016C	00000004	PPI_D2S_CLRSIPOCOUNT	LP										
12	WR	0170	00000004	PPI_D3S_CLRSIPOCOUNT	LP										
13	WR	0134	0000001F	PPI_LANEENABLE	LP										
14	WR	0210	0000001F	DSI_LANEENABLE	LP										
15	WR	0104	00000001	PPI_SARTPPI	LP										
16	WR	0204	00000001	DSI_SARTPPI	LP										
17															
18	REM	**********													
19	REM	TC358764/65XBG Timing and mode setting													
20	REM	**********													
21	WR	450	03F00120	VPCTRL	LP or HS										
22	WR	454	0032001C	HTIM1	LP or HS										
23	REM	458	00320500	HTIM2	LP or HS										
24	WR	45C	00040002	VTIM1	LP or HS										
25	REM	460	000A0320	VTIM2	LP or HS										
26	WR	464	00000001	VFUEN	LP or HS										
27	WR	4A0	00448006	LVPHY0	LP or HS										
28	REM	More than 100us													
29	WR	4A0	00048006	LVPHY0	LP or HS										
30	WR	504	00000004	SYSRST	LP or HS										
31	REM	**********													
32	REM	TC358764/65XBG LVDS Color mapping setting													
33	REM	**********													
34	WR	480	03020100	LVMX0003	LP or HS										
35	WR	484	08050704	LVMX0407	LP or HS										
36	WR	488	0F0E0A09	LVMX0811	LP or HS										
37	WR	48C	100D0C0B	LVMX1215	LP or HS										
38	WR	490	12111716	LVMX1619	LP or HS										
39	WR	494	1B151413	LVMX2023	LP or HS										
40	WR	498	061A1918	LVMX2427	LP or HS										
41	REM	**********													
42	REM	TC358764/65XBG LVDS enable													

Revision | How to use | Timing Parameters SYNC_PULSE | Timing Parameters SYNC_EVENT | Source | Sequence | Host Access | Res

TC358771/72XBG
(MIPI->LVDS Bridge with Adaptive Backlight Control)

Display Bridge with Adaptive Backlight Control

== Light-adaptive Control ==



■ Keeping Pin Compatibility with 774/775 except for PWM pin. TC358772 MP
Saving power without a modification of the substrate circuit. TC358771 MP

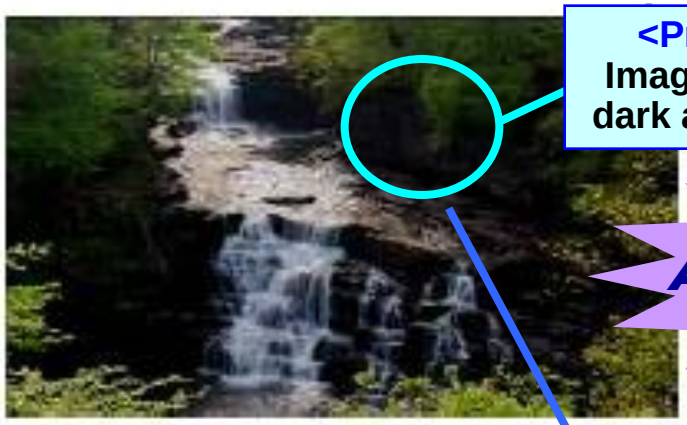
Effect of Adaptive Backlight Control(1)

For power save

For better view at bright ambient

BL (dark)

BL (bright)



<Problem>
Image detail in dark area is lost

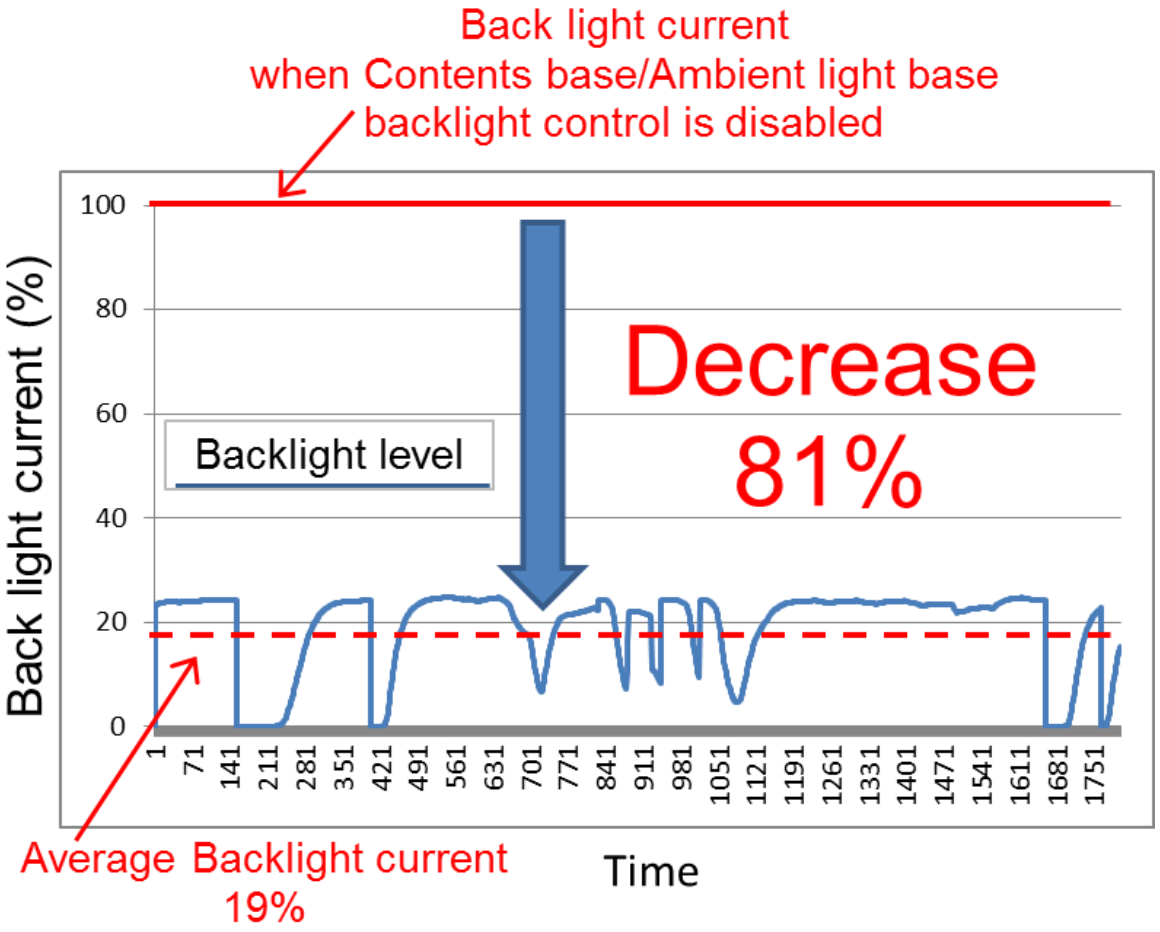
<Problem>
Image detail in bright area is lost

Without Adaptive backlight Control

<Adaptive Backlight Control>

By using region-by-region (16 region) tone adjustment, good image quality can be kept in optimized Back Light

Effect of Adaptive Backlight Control(2)



Contents Base
BL control
Enabled

Ambient Light
Base BL control
Enabled

Contents: Movie

Feature of Display Bridge with Adaptive Back-light Control

(1) Focusing on Backlight power which is most effective to total current consumption.

(2) Based on TOSHIBA Digital TV technology

(3) Cheaper than buffer solution by line buffer structure

(4) Proven bridge structure by several APP venders

(5) Easy to change from current product

<Main backlight control functions>

DRE function: Automatically control backlight level based on image contents

BLC function: Automatically control backlight level based on ambient light

GLB function: Adjust image contents based on target backlight level

H/W difference between DSI->LVDS Bridge chip

	TC358764/65	TC358774/75	TC358771/772
Feature	Base Product	-Low Power LVDS core	-Low Power LVDS core -Adaptive Backlight Control
Package		Same as 764/765	Same as 764/765
Pin function Difference	GPIO[4:0]	-GPIO4 is used as STBY input	-GPIO4 is used as STBY input -GPIO3 is uses as PWM control output
Power	LVDS Core Power =3.3V	LVDS Core Power =1.8V	LVDS Core Power =1.8V

TC358734XBG
(DSI->LVDS Buffer with Adaptive Backlight Control)

<Key word>

DSI -> LVDS

Embedded Frame memory

Adaptive Backlight Controller

WSVGA, XGA, WXGA, WUXGA

Feature of TC358734

<Function>

MIPI DSI -> LVDS conversion

18.5Mbit Frame memory

Adaptive back light control

<DSI-RX>

1Gbps/lane * 4lane (1/2/3/4 lane operation is possible)
Support up to 1920x1200 x 24bit

<LVDS-TX>

Supports single-link/dual-link
Maximum LVDS clock frequency of 135MHz

<Adaptive back light control>

Provides a proper backlight parameter to the environment light

<Power>

1.8V (Embedded Regulator)

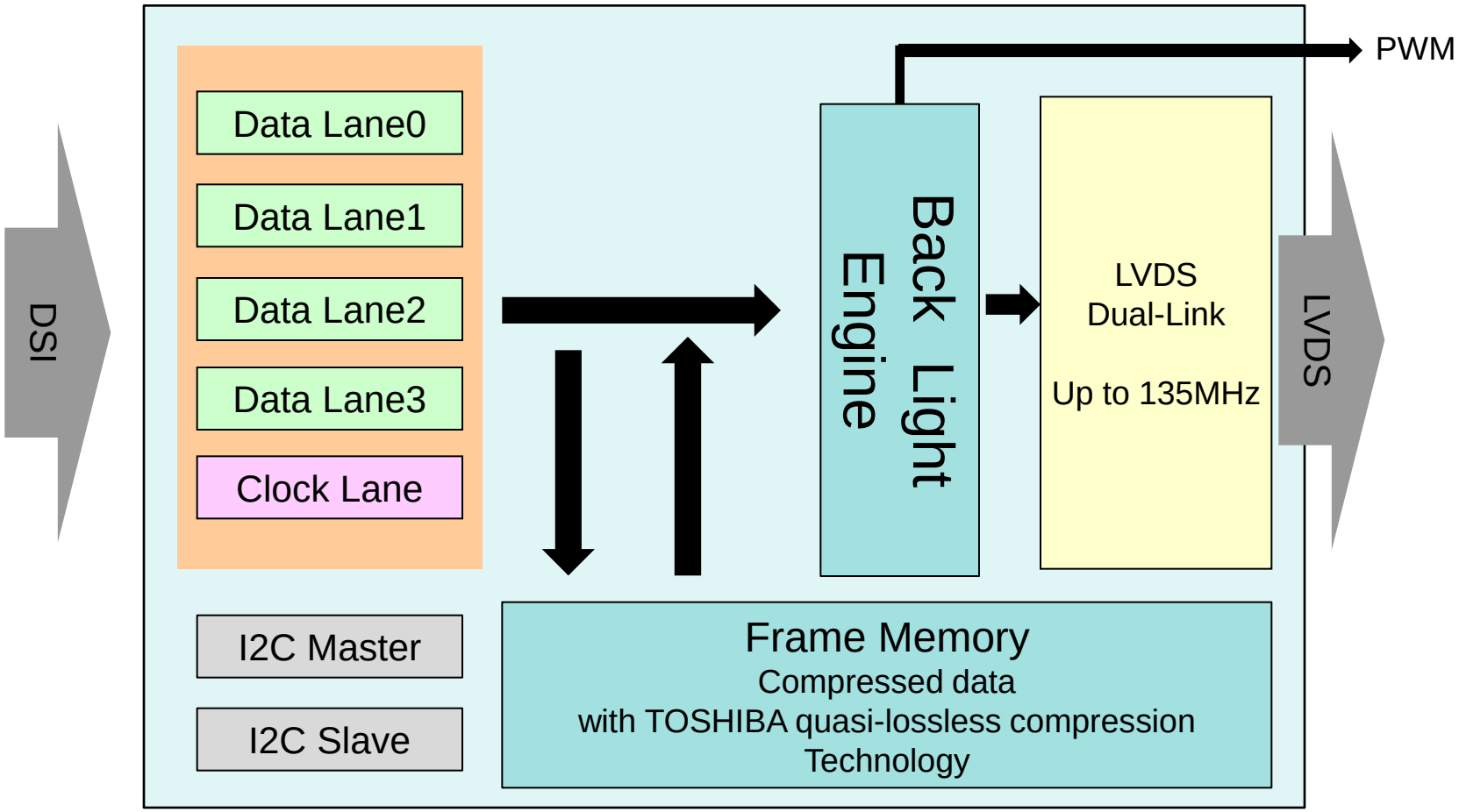
<Package>

7.0mm x 7.0mm 0.65mm pitch 80balls BGA

<Schedule>

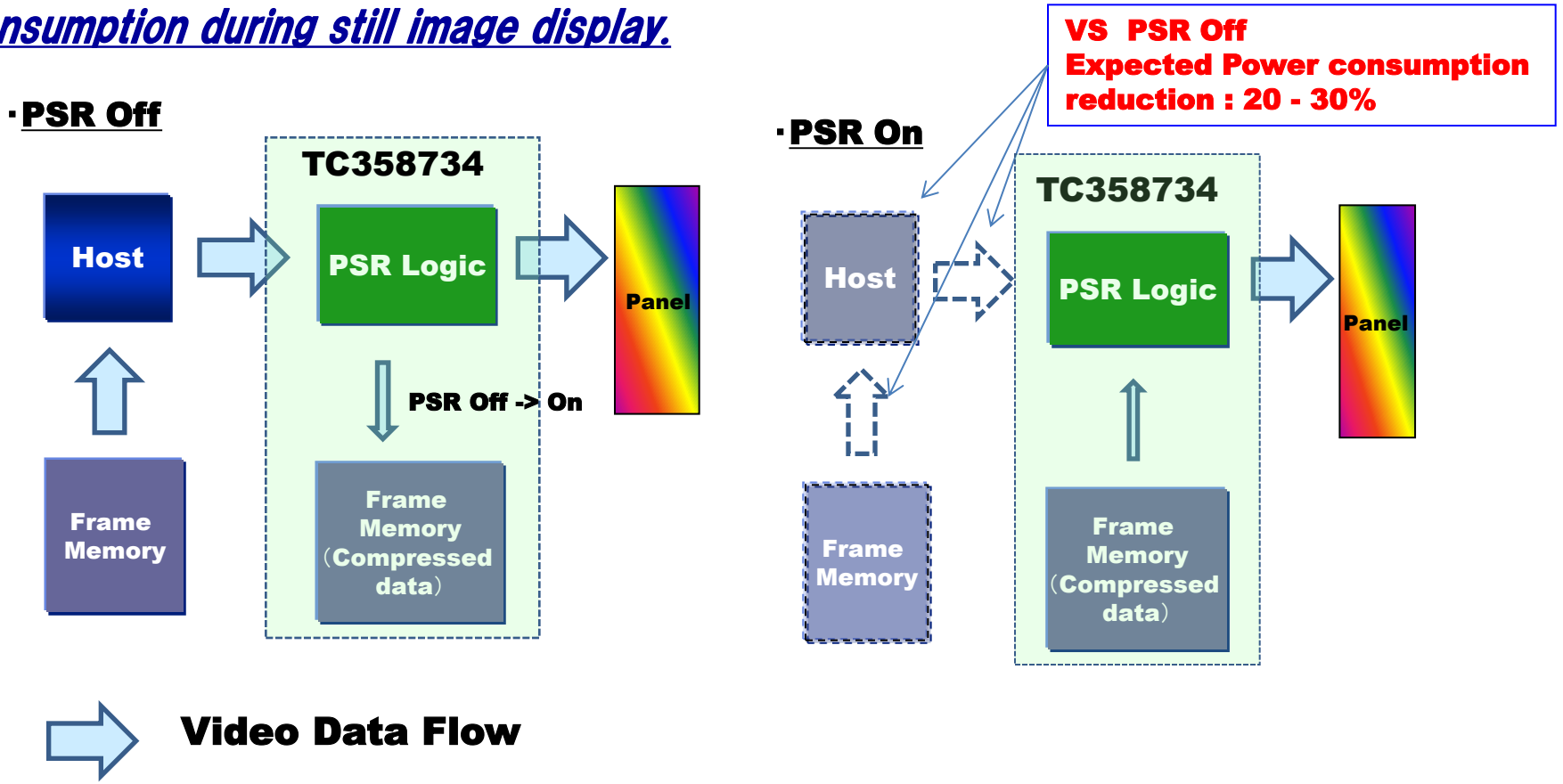
ES : Available, MP : 2014/Q3

Block Diagram



What is PSR?

PSR is an effective method to reduce power consumption during still image display.



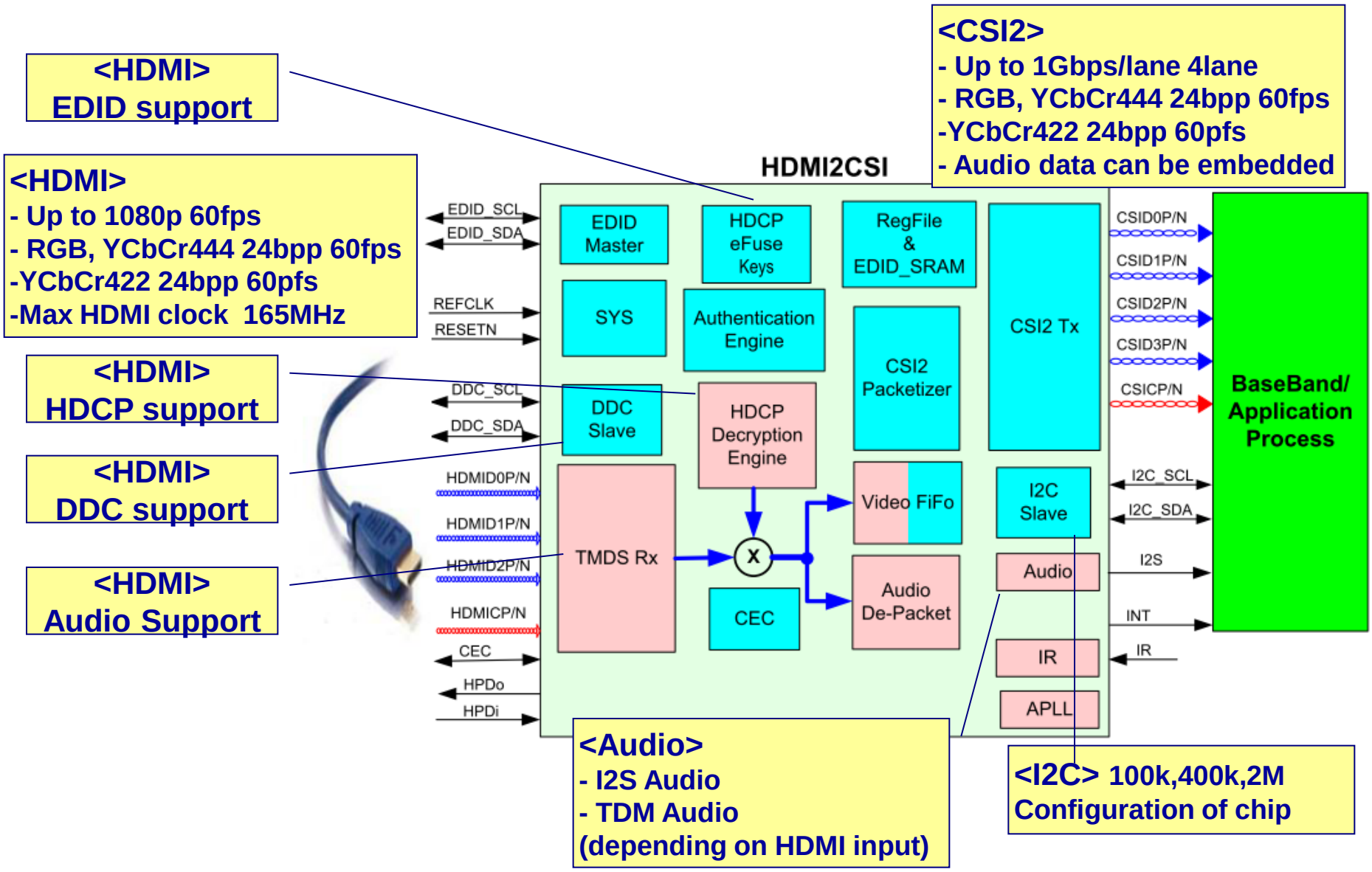
Required Frame Memory size for PSR

WUXGA(1920x1200) : 52.7Mbit => 18.5Mbit(1/3 Comp)

WQXGA(2560x1600) : 93.8Mbit => 15.6Mbit(1/6 Comp)

TC358743XBG (HDMI->MIPI-CSI2)

TC358743XBG Block Diagram



Feature of TC358743XBG (1)

<Function> HDMI -> MIPI CSI2 conversion

<HDMI-RX>

HDMI 1.4

<Resolution, Format>

- Up to 1080p 60fps
- RGB, YCbCr444 24bpp 60fps, YCbCr422 24bpp 60pfs
- Max HDMI clock 165MHz
- 3D support

<HDCP> HDCP support

<Audio> Internal audio PLL tracks N/CTS value transmitted by ACR packet

<DDC, EDID> DDC, EDID support

<CSI2-TX>

MIPI-CSI2 Version 1.01 Rev.0.04

- Up to 1Gbps/lane 4lane
- RGB, YCbCr444 24bpp 60fps,YCbCr422 24bpp 60pfs
- Audio data can be embedded

Feature of TC358743XBG (2)

<Audio-output>

I2S, TDM (depending on HDMI input)

<Host-I/F>

I2C: For Configuration of chip

100k, 400k, 2M, 7bit slave address

<Power>

Core and MIPI: 1.2V

HDMI: 3.3V

APLL: 3.3V/2.5V

I/O: 1.8V~3.3V

* HDMI power is independent from other power.

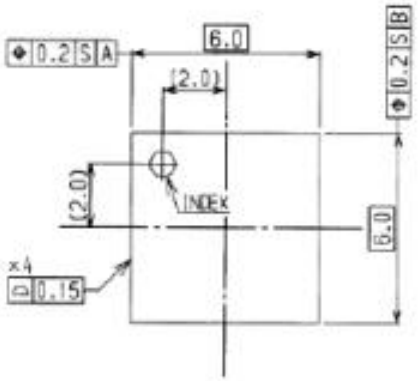
Keep HDMI power-on while other powers shut down is possible.

* HDI(Hot Plug Detect Input) and DDC I2C are 5V tolerant.

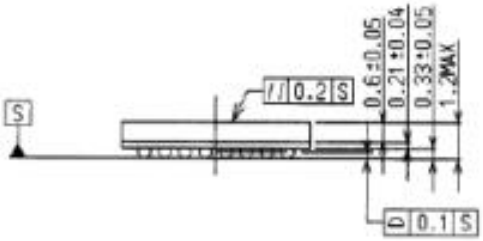
<Package>

6mm x 6mm BGA,   0.65mm pitch 64 balls.

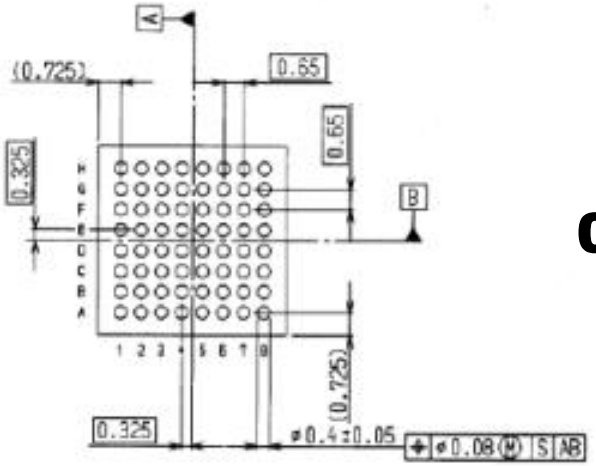
TC358743XBG Package



6mm x 6mm body



1.2mm(max) height



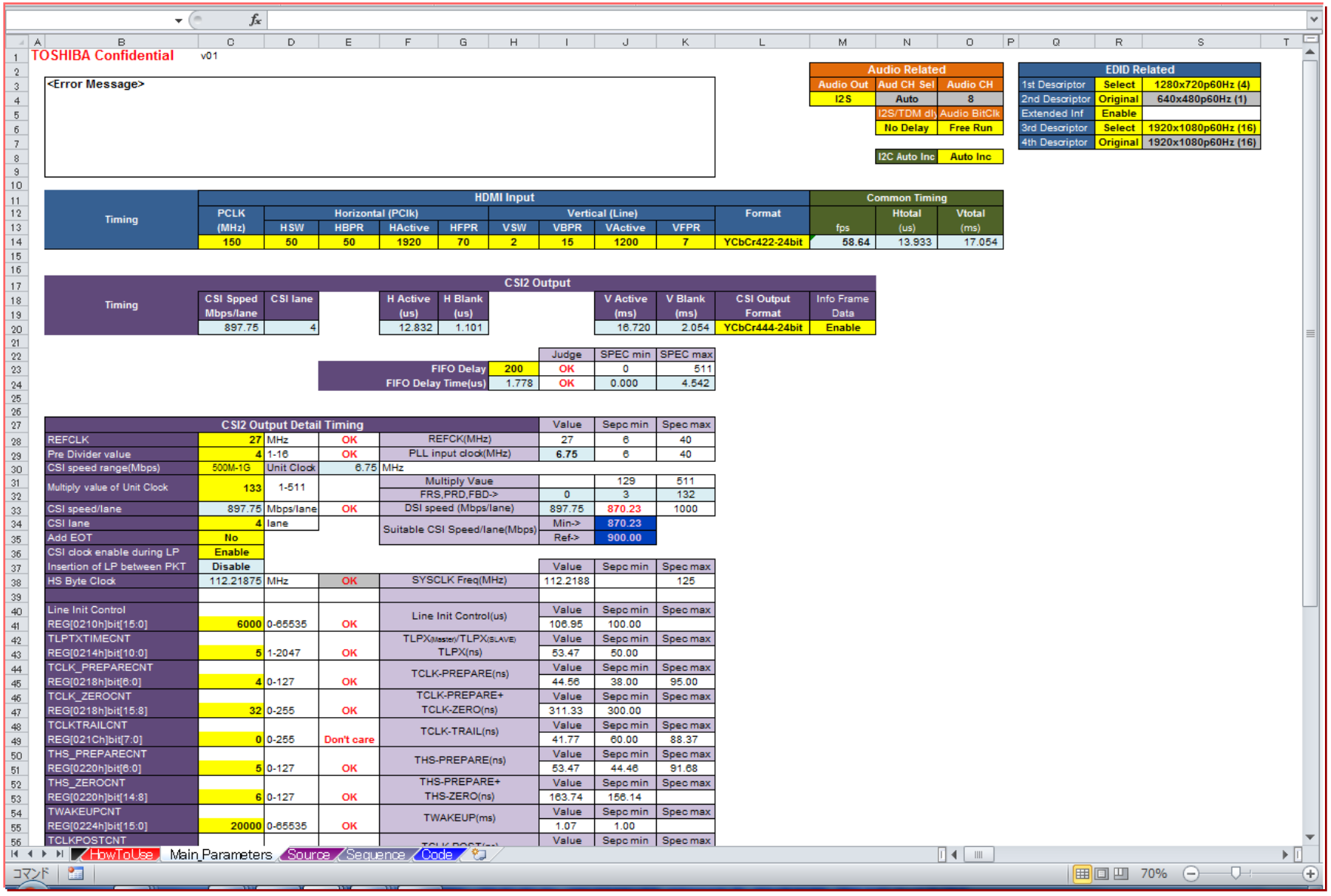
0.65mm ball pitch
64balls

TC358743XBG Ball distribution diagram

A1 REXT	**A2** VSS	**A3** VPGM	**A4** BIASDA	**A5** DAOUT	**A6** PFIL	**A7** CSID3N	**A8** CSID3P
B1 AVDD33	**B2** AVDD12	**B3** INT	**B4** IR	**B5** AVDD25	**B6** PCKIN	**B7** CSID2N	**B8** CSID2P
C1 HDMICP	**C2** HDMICN	**C3** VDDC2	**C4** VSS	**C5** VSS	**C6** VDD_MIPI	**C7** CSICN	**C8** CSICP
D1 HDMID0P	**D2** HDMID0N	**D3** AVDD12	**D4** VSS	**D5** VSS	**D6** VSS	**D7** CSID1N	**D8** CSID1P
E1 HDMID1P	**E2** HDMID1N	**E3** VSS	**E4** VSS	**E5** TEST	**E6** VSS	**E7** CSID0N	**E8** CSID0P
F1 HDMID2P	**F2** HDMID2N	**F3** AVDD33	**F4** VDDIO1	**F5** VDDC2	**F6** VDD_MIPI	**F7** A_SCK	**F8** A_SD
G1 CEC	**G2** VDDC1	**G3** DDC_SDA	**G4** I2C_SDA	**G5** RESETN	**G6** EDID_SDA	**G7** A_WFS	**G8** A_OSCK
H1 HPDO	**H2** HPDI	**H3** DDC_SCL	**H4** I2C_SCL	**H5** REFCLK	**H6** EDID_SCL	**H7** VDDIO2	**H8** VSS

Top View

TC358743XBG Setting Sequence generation tool (1)



TOSHIBA Confidential v01

<Error Message>

Audio Related		
Audio Out	Aud CH Sel	Audio CH
I2S	Auto	8
	I2S/TDM dly	Audio BitClk
	No Delay	Free Run
	I2C Auto Inc	Auto Inc

EDID Related		
1st Descriptor	Select	1280x720p60Hz (4)
2nd Descriptor	Original	640x480p60Hz (1)
Extended Inf	Enable	
3rd Descriptor	Select	1920x1080p60Hz (16)
4th Descriptor	Original	1920x1080p60Hz (16)

Timing	HDMI Input										Common Timing		
	PCLK	Horizontal (PCIk)				Vertical (Line)				Format		Htotal	Vtotal
	(MHz)	HSW	HBPR	HActive	HFPR	VSW	VBPR	VActive	VFPR		fps	(us)	(ms)
	150	50	50	1920	70	2	15	1200	7	YCbCr422-24bit	58.64	13.933	17.054

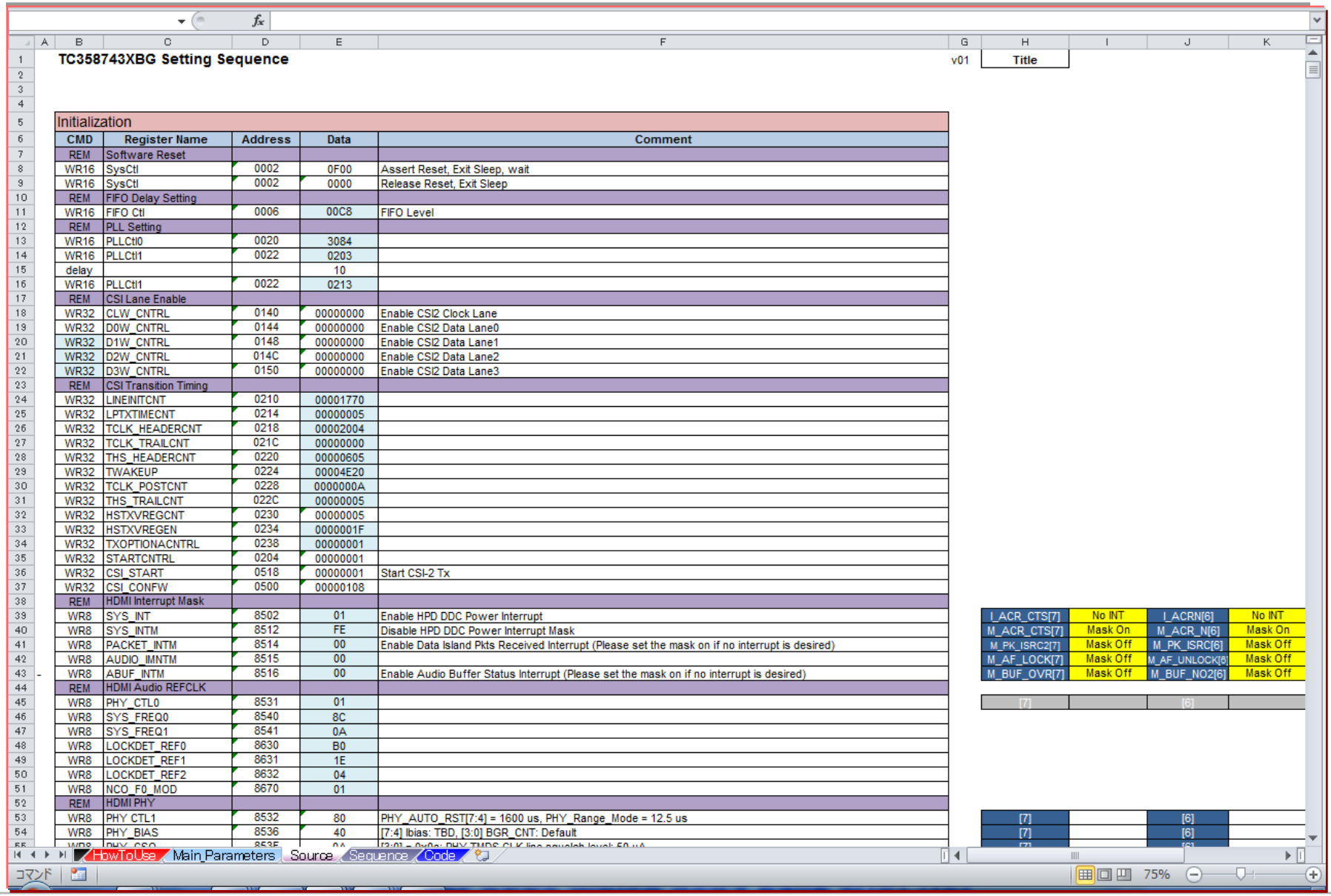
Timing	CSI2 Output							
	CSI Spped Mbps/lane	CSI lane	H Active (us)	H Blank (us)	V Active (ms)	V Blank (ms)	CSI Output Format	Info Frame Data
	897.75	4	12.832	1.101	16.720	2.054	YCbCr444-24bit	Enable

		Judge	SPEC min	SPEC max
FIFO Delay	200	OK	0	511
FIFO Delay Time(us)	1.778	OK	0.000	4.542

CSI2 Output Detail Timing					Value	Sepc min	Spec max
REFCLK	27	MHz	OK	REFCK(MHz)	27	6	40
Pre Divider value	4	1-16	OK	PLL input clock(MHz)	6.75	6	40
CSI speed range(Mbps)	500M-1G	Unit Clock	6.75	MHz			
Multiply value of Unit Clock	133	1-511		Multiply Vaue		129	511
				FRS,PRD,FBD->	0	3	132
CSI speed/lane	897.75	Mbps/lane	OK	DSI speed (Mbps/lane)	897.75	870.23	1000
CSI lane	4	lane		Suitable CSI Speed/lane(Mbps)	Min->	870.23	
Add EOT	No				Ref->	900.00	
CSI clock enable during LP	Enable						
Insertion of LP between PKT	Disable				Value	Sepc min	Spec max
HS Byte Clock	112.21875	MHz	OK	SYSCLK Freq(MHz)	112.2188		125
Line Init Control REG[0210h]bit[15:0]	6000	0-65535	OK	Line Init Control(us)	Value	Sepc min	Spec max
					106.95	100.00	
TLPTXTIMECNT REG[0214h]bit[10:0]	5	1-2047	OK	TLPX(Master)/TLPX(SLAVE) TLPX(ns)	Value	Sepc min	Spec max
					53.47	50.00	
TCLK_PREPARECNT REG[0218h]bit[6:0]	4	0-127	OK	TCLK-PREPARE(ns)	Value	Sepc min	Spec max
					44.56	38.00	95.00
TCLK_ZEROCNT REG[0218h]bit[15:8]	32	0-255	OK	TCLK-PREPARE+ TCLK-ZERO(ns)	Value	Sepc min	Spec max
					311.33	300.00	
TCLKTRAILCNT REG[021Ch]bit[7:0]	0	0-255	Don't care	TCLK-TRAIL(ns)	Value	Sepc min	Spec max
					41.77	60.00	88.37
THS_PREPARECNT REG[0220h]bit[6:0]	5	0-127	OK	THS-PREPARE(ns)	Value	Sepc min	Spec max
					53.47	44.46	91.68
THS_ZEROCNT REG[0220h]bit[14:8]	6	0-127	OK	THS-PREPARE+ THS-ZERO(ns)	Value	Sepc min	Spec max
					163.74	156.14	
TWAKEUPCNT REG[0224h]bit[15:0]	20000	0-65535	OK	TWAKEUP(ms)	Value	Sepc min	Spec max
					1.07	1.00	
TCLKPOSTCNT					Value	Sepc min	Spec max

HowToUse | Main_Parameters | Source | Sequence | Code

TC358743XBG Setting Sequence generation tool (2)



TC358743XBG Setting Sequence

v01 | Title

Initialization

CMD	Register Name	Address	Data	Comment
REM	Software Reset			
WR16	SysCtl	0002	0F00	Assert Reset, Exit Sleep, wait
WR16	SysCtl	0002	0000	Release Reset, Exit Sleep
REM	FIFO Delay Setting			
WR16	FIFO Ctl	0006	00C8	FIFO Level
REM	PLL Setting			
WR16	PLLCtl0	0020	3084	
WR16	PLLCtl1	0022	0203	
delay			10	
WR16	PLLCtl1	0022	0213	
REM	CSI Lane Enable			
WR32	CLW_CNTRL	0140	00000000	Enable CSI2 Clock Lane
WR32	D0W_CNTRL	0144	00000000	Enable CSI2 Data Lane0
WR32	D1W_CNTRL	0148	00000000	Enable CSI2 Data Lane1
WR32	D2W_CNTRL	014C	00000000	Enable CSI2 Data Lane2
WR32	D3W_CNTRL	0150	00000000	Enable CSI2 Data Lane3
REM	CSI Transition Timing			
WR32	LINEINITCNT	0210	00001770	
WR32	LPTXTIMECNT	0214	00000005	
WR32	TCLK_HEADERCNT	0218	00002004	
WR32	TCLK_TRAILCNT	021C	00000000	
WR32	THS_HEADERCNT	0220	00000605	
WR32	TWAKEUP	0224	00004E20	
WR32	TCLK_POSTCNT	0228	0000000A	
WR32	THS_TRAILCNT	022C	00000005	
WR32	HSTXVREGCNT	0230	00000005	
WR32	HSTXVREGEN	0234	0000001F	
WR32	TXOPTIONACNTRL	0238	00000001	
WR32	STARTCNTRL	0204	00000001	
WR32	CSI_START	0518	00000001	Start CSI-2 Tx
WR32	CSI_CONFW	0500	00000108	
REM	HDMI Interrupt Mask			
WR8	SYS_INT	8502	01	Enable HPD DDC Power Interrupt
WR8	SYS_INTM	8512	FE	Disable HPD DDC Power Interrupt Mask
WR8	PACKET_INTM	8514	00	Enable Data Island Pkts Received Interrupt (Please set the mask on if no interrupt is desired)
WR8	AUDIO_IMNTM	8515	00	
WR8	ABUF_INTM	8516	00	Enable Audio Buffer Status Interrupt (Please set the mask on if no interrupt is desired)
REM	HDMI Audio REFCLK			
WR8	PHY_CTL0	8531	01	
WR8	SYS_FREQ0	8540	8C	
WR8	SYS_FREQ1	8541	0A	
WR8	LOCKDET_REF0	8630	B0	
WR8	LOCKDET_REF1	8631	1E	
WR8	LOCKDET_REF2	8632	04	
WR8	NCO_F0_MOD	8670	01	
REM	HDMI PHY			
WR8	PHY CTL1	8532	80	PHY_AUTO_RST[7:4] = 1600 us, PHY_Range_Mode = 12.5 us
WR8	PHY_BIAS	8536	40	[7:4] Ibias: TBD, [3:0] BGR_CNT: Default

I_ACR_CTS[7]	No INT	I_ACRN[6]	No INT
M_ACR_CTS[7]	Mask On	M_ACR_N[6]	Mask On
M_PK_ISRC2[7]	Mask Off	M_PK_ISRC[6]	Mask Off
M_AF_LOCK[7]	Mask Off	M_AF_UNLOCK[6]	Mask Off
M_BUF_OVR[7]	Mask Off	M_BUF_NO2[6]	Mask Off

[7]		[6]	

[7]		[6]	
[7]		[6]	

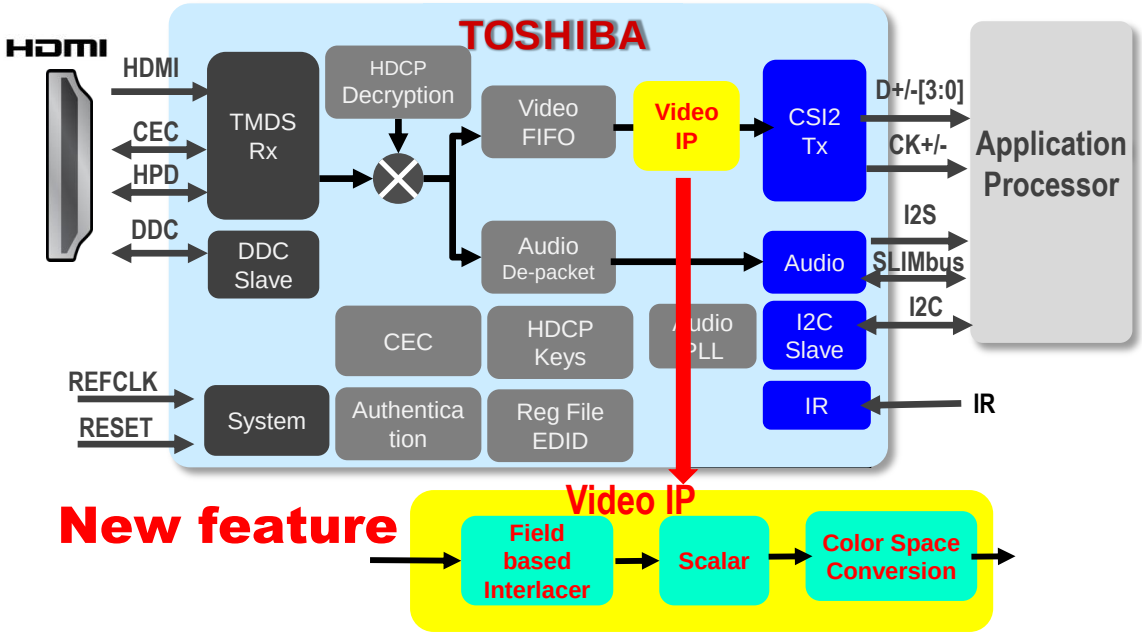
- **TC358749XBG**
  (HDMI->CSI2+Scalar/2D IP converter)
- **TC358779XBG**
  (HDMI->DSI+Scalar/2D IP converter)

Block diagram

TC358749XBG

Market

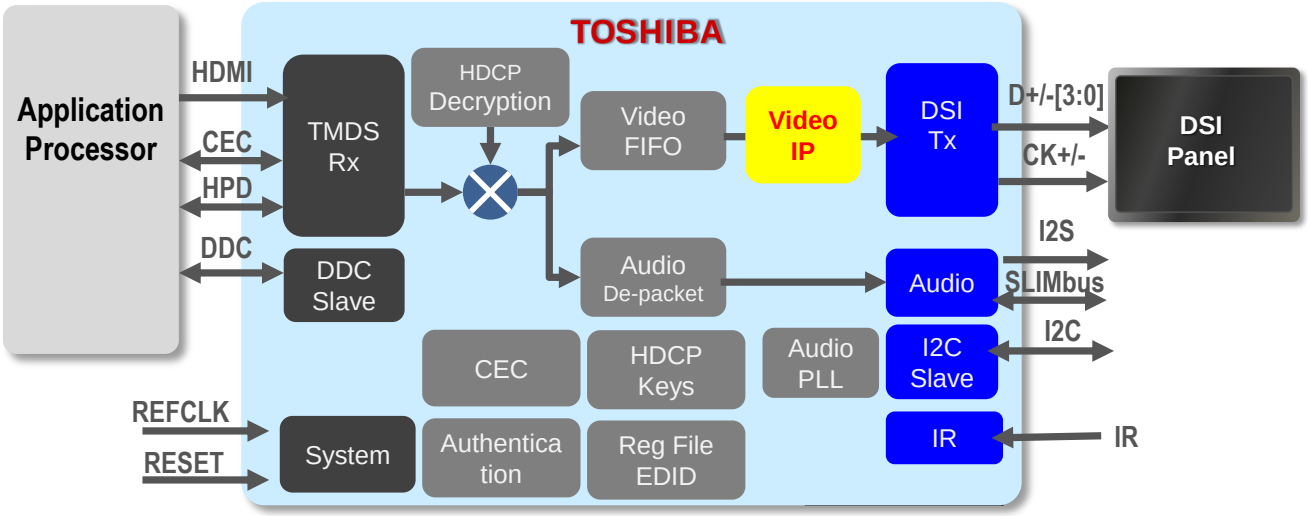
- STB
- Car entertainment
- Flight entertainment
- Game accessory
- Tablet/ Smart monitor
- etc.



TC358779XBG

Market

- Monitors
- Docking station
- DSC
- Game accessory



TC358749/TC358779 Feature

Basic feature(Same as TC358743)

- **HDMI streams converted to MIPI® CSI-2 data**
- **MIPI CSI-2 4 data line to Application Processor interface**
- **HDMI 1.4a standard protocols (Up to 165MHz TMDS CLK)**
- **Supports 3D formats (FP, Side by side, Top and bottom)**
- **RGB to YCbCr Color space conversion**

Additional feature

- **Field(2D)de-interlacing (scaling) from 480i/1080i to 1080p**
- **Scaling of 720p video to 1080p @ 60fps**
  -> see detail scaling combination next page
- **YCbCr to RGB Color space conversion**
- **Several Audio Interface**
  - I2S (up to 8ch)
  - TDM (fixed 8ch)
  - SPDIF
  - MIPI SLIMbus I/F (up to 8ch)

Scaling for 720P and 1080P Display

HDMI input	CSI output
640x480 P	1280x720 P
720x480 I/P	1280x720 P
720x576 I/P	1280x720 P
1280x720 P	1280x720 P
1920x1080 I/P	1280x720 P

HDMI input	CSI output
640x480 P	1920x1080 P
720x480 I/P	1920x1080 P
720x576 I/P	1920x1080 P
1280x720 P	1920x1080 P
1920x1080 I/P	1920x1080 P

Scalar for 3D 720P and 1080P Display

HDMI input	CSI output
1280x720P FP	1280x720 FP
1280x720P SbS (half)	1280x720 SbS (full)
1280x720P T&B (half)	1280x720 T&B (full)
1920x1080P FP	1280x720 FP
1920x1080P SbS (half)	1280x720 SbS (full)
1920x1080P T&B (half)	1280x720 T&B (full)
1920x1080I SbS (half)	1280x720 SbS (full)

HDMI input	CSI output
1280x720P FP	1920x1080 FP*
1280x720P FP	1280x720P FP
1280x720P SbS (half)	1280x720 SbS (full)
1280x720P T&B (half)	1280x720 T&B (full)
1920x1080P FP	1920x1080 FP*
1920x1080P SbS (half)	1920x1080 SbS (full)*
1920x1080P T&B (half)	1920x1080 T&B (full)*
1920x1080P FP	1280x720 FP
1920x1080P SbS (half)	1280x720 SbS (full)
1920x1080P T&B (half)	1280x720 T&B (full)

TC358860XBG

(eDP to DSI Bridge with video compression)

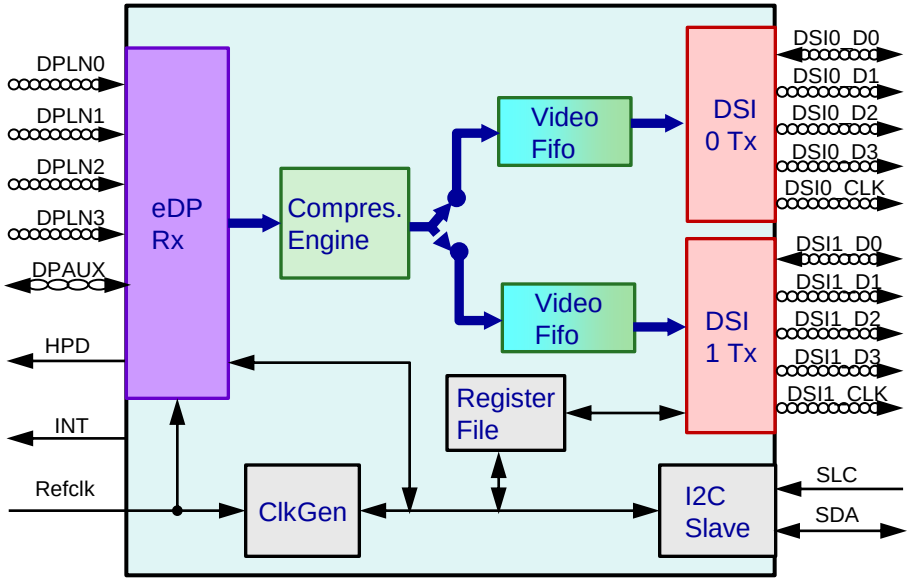
TC358860XBG

Features

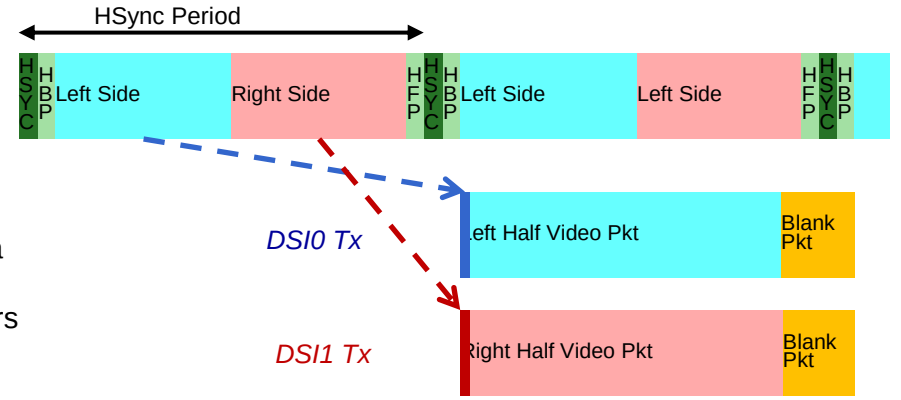
Input	eDP (1,2,4Lane) Bit Rate 1.62/2.7/4.32/5.4Gbps
Output	MIPI DSI 1,2,3 or 4Lane × 2port Max 1.5Gbps/Lane
Data Compression	Data compression engine 2-to-1/3-to-1 selectable
Resolution	~ 4k2k 4096(H) x 2160(V)
Package (TBD)	PFVGA 64Pin 5.0mm × 5.0mm,0.5mm Pitch
Power Supply	MIPI DPHY : 1.2V Core : 1.1V I/O & HPD : 1.8-3.3V
Status	Under Development ES: '14/Q2

The compression engine is provided to compress one line of video data into 1/2 or 1/3 data of its original size.
The compressed video is expected to be decompressed by LCD Drivers before displaying.
The compressed/de-compressed algorithm can produce visual lossless video stream.

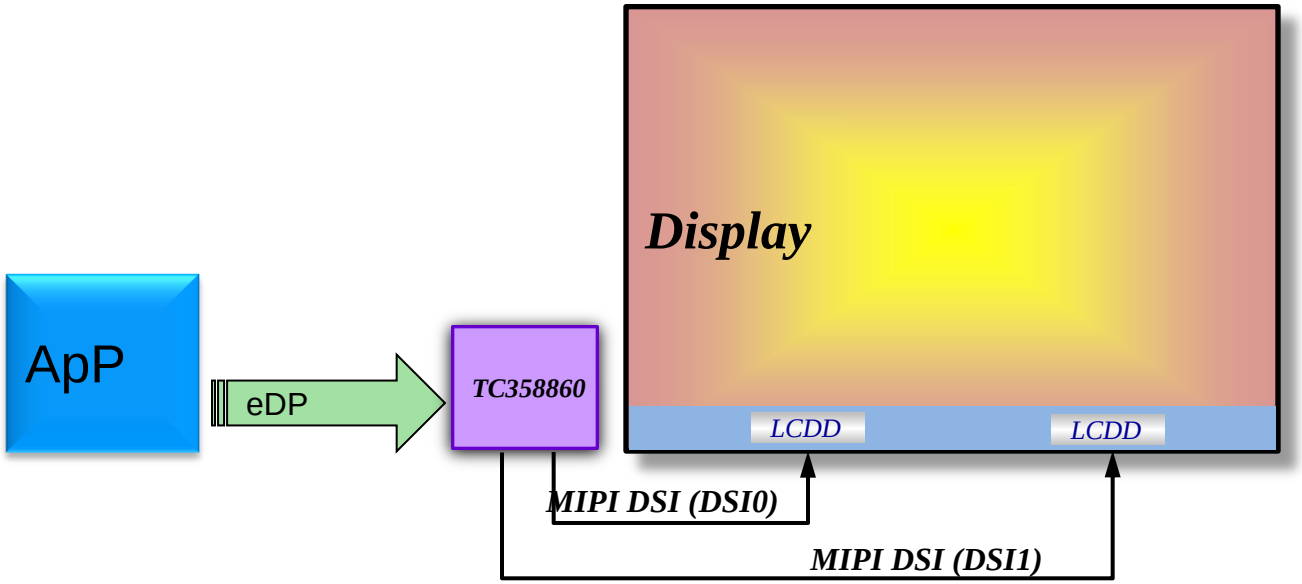
Block Diagram



Line Splitting for Dual DSI Link

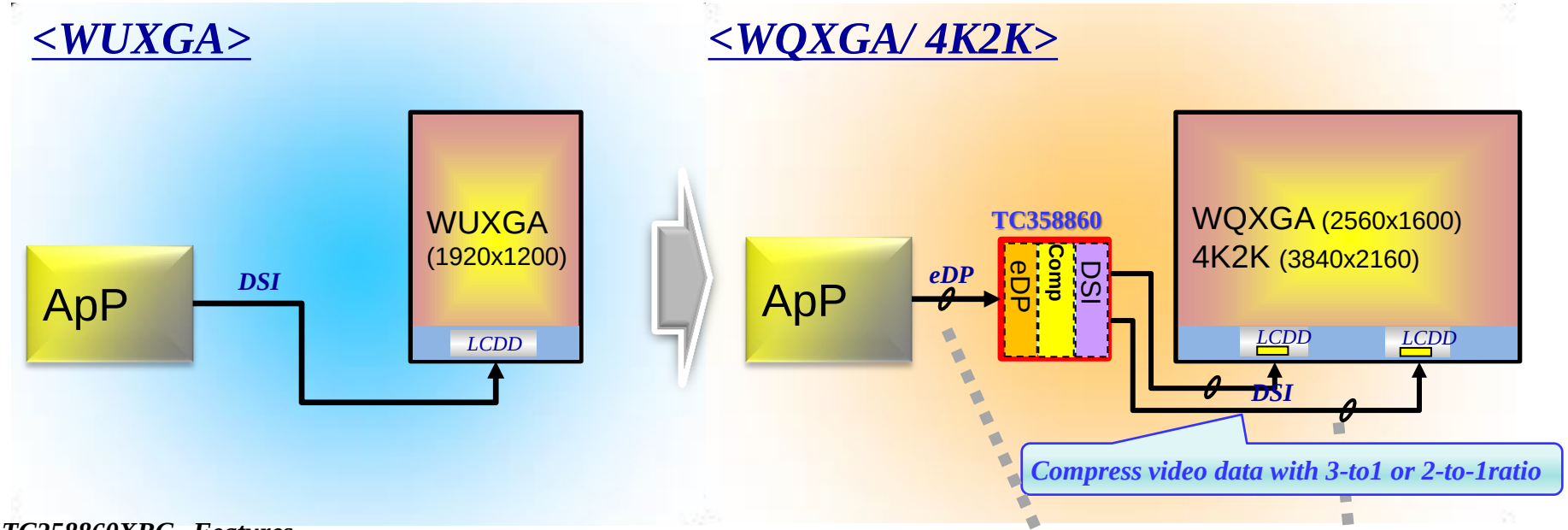


System Application



	VESA Timing	PCLK [MHz]	Stream Bit Rate [Gbps]	eDP [Lane]			MIPI DSI (LCDD x 2) [Lane]		
				2.7Gbps	4.32Gbps	5.4Gbps	Non Comp	Compression 2 to 1	Compression 3 to 1
FHD	1920 x 1080 @60Hz	148.5	3.56	4	2	1	2 0.89[Gbps]	1 0.89[Gbps]	1 0.59[Gbps]
WUXGA	1920 x 1200 @60Hz CVT (Reduced Blanking)	154	3.70	4	2	1	2 0.92[Gbps]	1 0.92[Gbps]	1 0.62[Gbps]
WQXGA	2560 x 1600 @60Hz CVT (Reduced Blanking)	268.5	6.44	4	2	2	3 1.07[Gbps]	2 0.81[Gbps]	1 1.07[Gbps]
UHD	3840 x 2160 @60Hz	645	15.5	N/A	N/A	4	–	–	2 1.29[Gbps]

High Resolution Display System



TC358860XBG Features

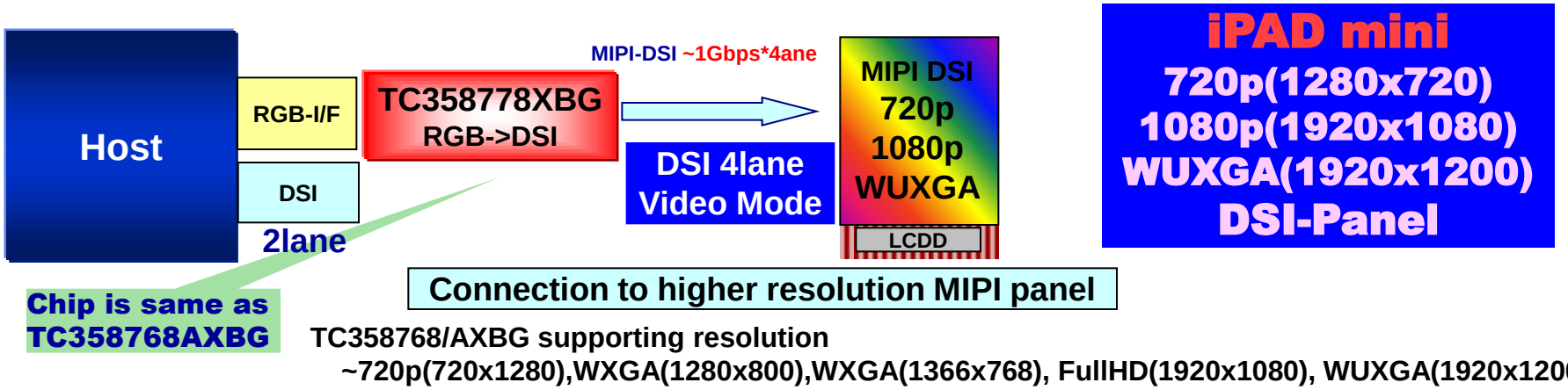
Input	eDP (1,2,4Lane) Bit Rate 1.62/2.7/4.32/5.4Gbps
Output	MIPI DSI 1,2,3 or 4Lane × 2port Max 1.5Gbps/Lane
Compression Operation	Data compression engine 2-to-1/3-to-1 selectable
Resolution	~ 4k2k 4096(H) x 2160(V)
Package (TBD)	PFVGA 64Pin 5.0mm × 5.0mm,0.5mm Pitch
Power Supply	MIPI DPHY : 1.2V Core : 1.1V I/O & HPD : 1.8-3.3V
Status	Under Development(ES: '14/5)

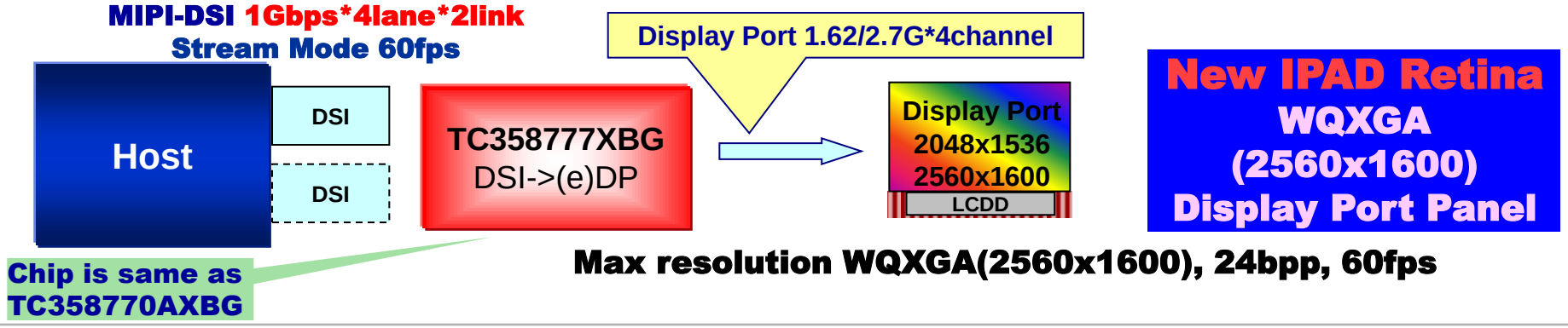
	VESA Timing	PCLK [MHz]	Stream Bit Rate [Gbps]	eDP [Lane]			MIPI DSI (LCDD x 2) [Lane]		
				2.7Gbps	4.32Gbps	5.4Gbps	Non Comp	Compression 2 to 1	Compression 3 to 1
FHD	1920 x 1080 @60Hz	148.5	3.56	4	2	1	2 0.89[Gbps]	1 0.89[Gbps]	1 0.59[Gbps]
WUXGA	1920 x 1200 @60Hz CVT (Reduced Blanking)	154	3.70	4	2	1	2 0.92[Gbps]	1 0.92[Gbps]	1 0.62[Gbps]
WQXGA	2560 x 1600 @60Hz CVT (Reduced Blanking)	268.5	6.44	4	2	2	3 1.07[Gbps]	2 0.81[Gbps]	1 1.07[Gbps]
UHD	3840 x 2160 @60Hz	645	15.5	N/A	N/A	4	–	–	2 1.29[Gbps]

Package variation for non HDI PCB
TC358778XBG(RGB->DSI)
TC358777XBG(DSI->DisplayPort(eDP))

Package for non HDI PCB

For PAD and PC application, TOSHIBA prepares 0.65mm pitch BGA for non HDI PCB. Signals and powers can be routed on one layer.
This package will be applied for TC358768AXBG(RGB->DSI) and TC358770AXBG(DSI->eDP(Display Port)).





Package information of TC358778XBG(RGB->DSI)

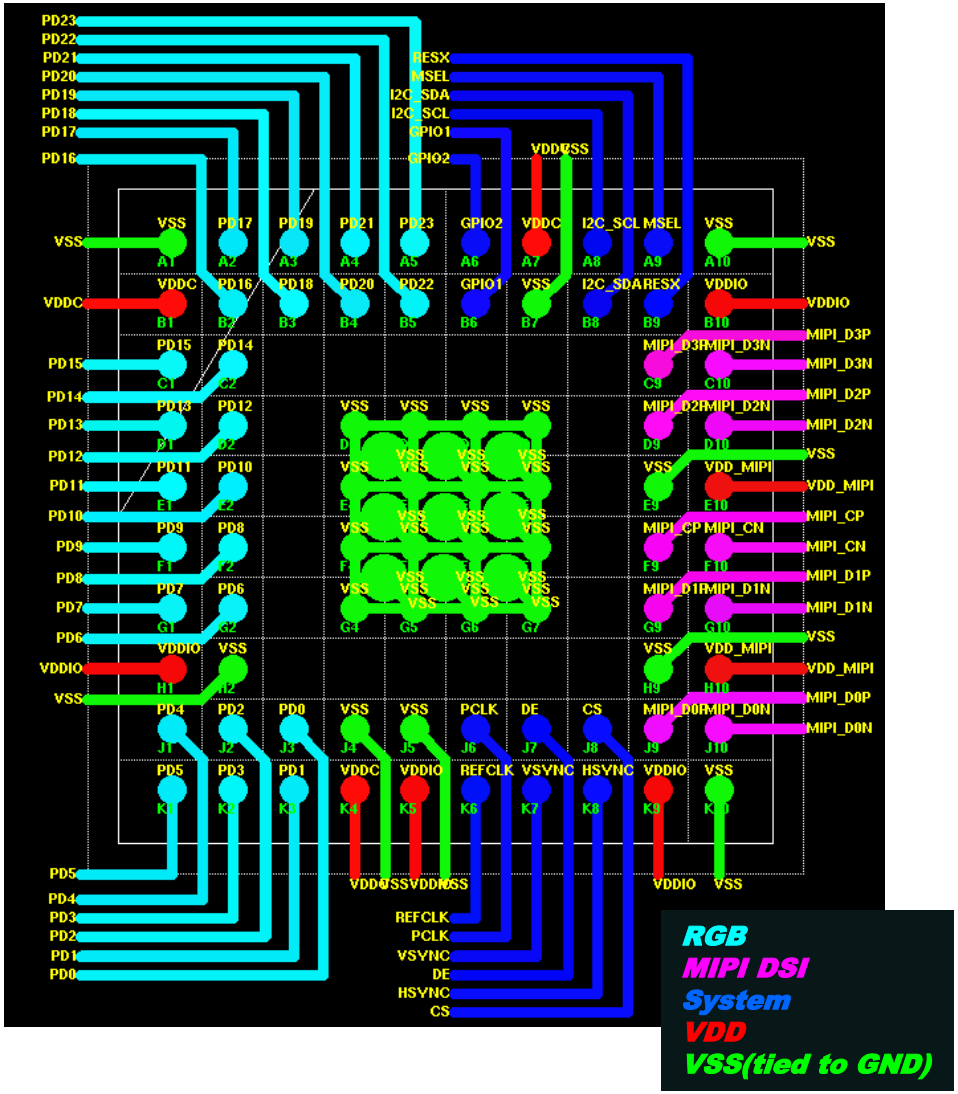
	TC358768AXBG(current Product)	TC358778XBG(for non HDI PCB)
Package Body Size	4.5mm x 4.5mm	7mm x 7mm
Ball pitch	0.4mm	0.65mm
Pin counts	72pins	80pins

A1	A2	A3	A4	A5	A6	A7	A8	A9
VSS	PD17	PD19	PD21	PD23	GPIO2	I2C_SCL	MSEL	VSS
B1	B2	B3	B4	B5	B6	B7	B8	B9
VDDC	PD16	PD18	PD20	PD22	GPIO1	I2C_SDA	RESX	VDDIO
C1	C2	C3	C4	C5	C6	C7	C8	C9
PD15	PD14	VSS	VSS	VSS	VSS	VDD_MIPI	MIPI_D3P	MIPI_D3N
D1	D2	D3				D7	D8	D9
PD13	PD12	VSS				VSS	MIPI_D2P	MIPI_D2N
E1	E2	E3				E7	E8	E9
VSS	VSS	VDDC				VDD_MIPI	MIPI_CP	MIPI_CN
F1	F2	F3				F7	F8	F9
VSS	VSS	VSS				VSS	MIPI_D1P	MIPI_D1N
G1	G2	G3	G4	G5	G6	G7	G8	G9
PD11	PD10	VDDIO	VSS	VSS	VDDIO	VDDIO	MIPI_D0P	MIPI_D0N
H1	H2	H3	H4	H5	H6	H7	H8	H9
VDDC	PD8	PD6	PD4	PD2	PD0	PCLK	HSYNC	CS
J1	J2	J3	J4	J5	J6	J7	J8	J9
VSS	PD9	PD7	PD5	PD3	PD1	REFCLK	VSYNC	GPIO0

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
VSS	PD17	PD19	PD21	PD23	GPIO2	VDDC	I2C_SCL	MSEL	VSS
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
VDDC	PD16	PD18	PD20	PD22	GPIO1	VSS	I2C_SDA	RESX	VDDIO
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
PD15	PD14							MIPI_D3P	MIPI_D3N
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
PD13	PD12		VSS	VSS	VSS	VSS		MIPI_D2P	MIPI_D2N
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
PD11	PD10		VSS	VSS	VSS	VSS		VSS	VDD_MIPI
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
PD9	PD8		VSS	VSS	VSS	VSS		MIPI_CP	MIPI_CN
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
PD7	PD6		VSS	VSS	VSS	VSS		MIPI_D1P	MIPI_D1N
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
VDDIO	VSS							VSS	VDD_MIPI
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
PD4	PD2	PD0	VSS	VSS	PCLK	HSYNC	CS	MIPI_D0P	MIPI_D0N
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
PD5	PD3	PD1	VDDC	VDDIO	REFCLK	VSYNC	GPIO0	VDDIO	VSS

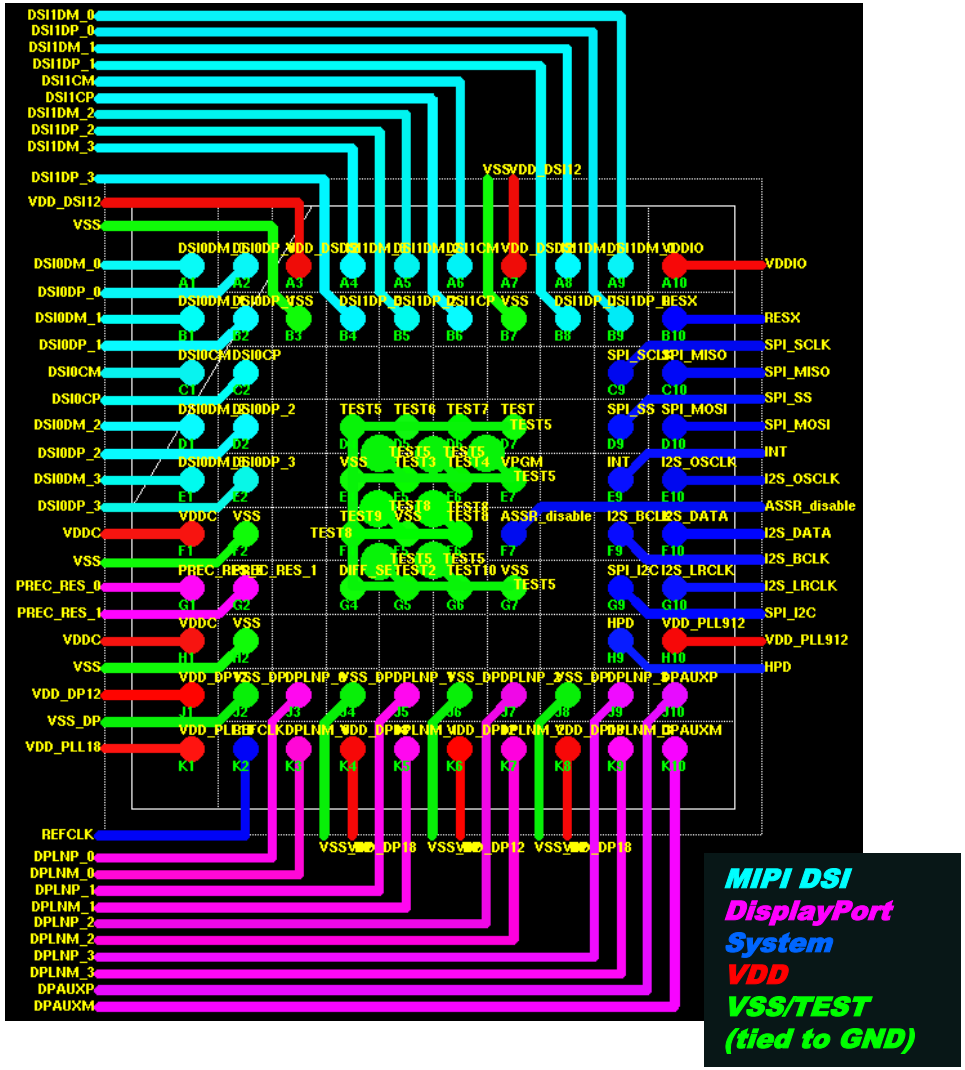
Routing information of TC358778XBG(RGB->DSI)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
VSS	PD17	PD19	PD21	PD23	GPIO2	VDDC	I2C_SCL	MSEL	VSS
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
VDDC	PD16	PD18	PD20	PD22	GPIO1	VSS	I2C_SDA	RESX	VDDIO
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
PD15	PD14							MIPI_D3P	MIPI_D3N
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
PD13	PD12		VSS	VSS	VSS	VSS		MIPI_D2P	MIPI_D2N
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
PD11	PD10		VSS	VSS	VSS	VSS		VSS	VDD_MIPI
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
PD9	PD8		VSS	VSS	VSS	VSS		MIPI_CP	MIPI_CN
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
PD7	PD6		VSS	VSS	VSS	VSS		MIPI_D1P	MIPI_D1N
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
VDDIO	VSS							VSS	VDD_MIPI
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
PD4	PD2	PD0	VSS	VSS	PCLK	HSYNC	CS	MIPI_D0P	MIPI_D0N
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
PD5	PD3	PD1	VDDC	VDDIO	REFCLK	VSYNC	GPIO0	VDDIO	VSS

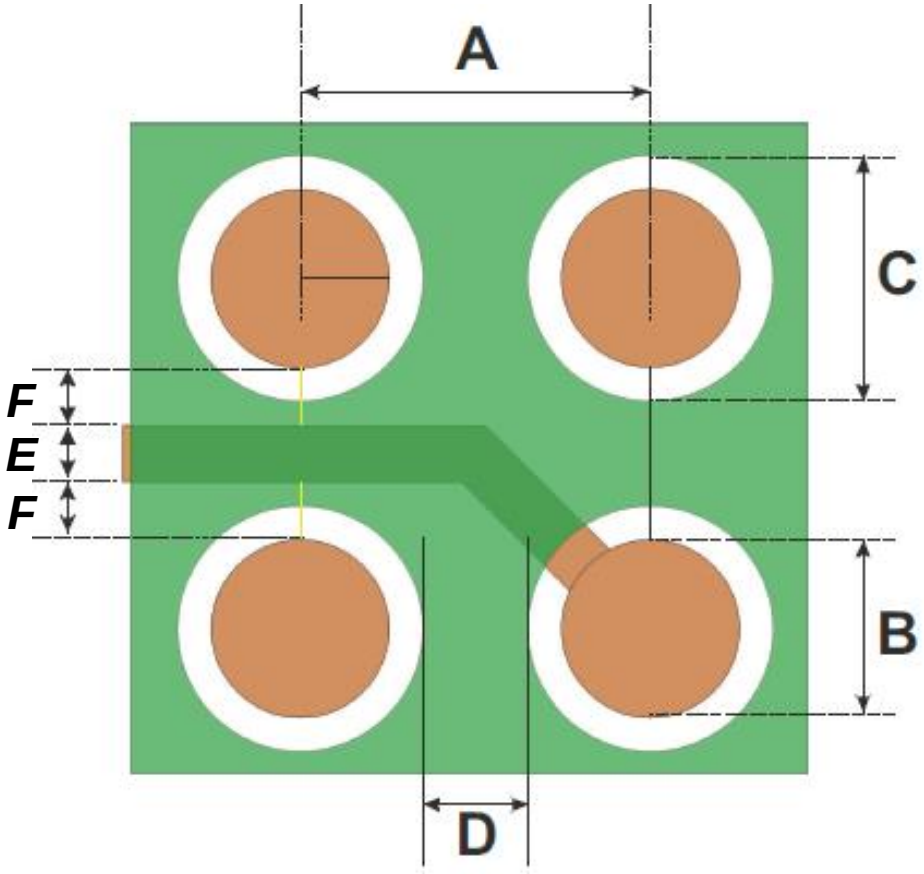


Routing information of TC358777XBG(DSI->eDP)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
DSI0DM_0	DSI0DP_0	VDD_DSI12	DSI1DM_3	DSI1DM_2	DSI1CM	VDD_DSI12	DSI1DM_1	DSI1DM_0	VDDIO
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
DSI0DM_1	DSI0DP_1	VSS	DSI1DP_3	DSI1DP_2	DSI1CP	VSS	DSI1DP_1	DSI1DP_0	RESX
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
DSI0CM	DSI0CP							SPI_SCLK	SPI_MISO
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
DSI0DM_2	DSI0DP_2		TEST5	TEST6	TEST7	TEST		SPI_SS	SPI_MOSI
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
DSI0DM_3	DSI0DP_3		VSS	TEST3	TEST4	VPGM		INT	I2S_OSCLK
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
VDDC	VSS		TEST9	VSS	TEST8	Disable_ ASSR		I2S_BCLK	I2S_DATA
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
PREC_RES_0	PREC_RES_1		DIFF_SE	TEST2	TEST10	VSS		SPI_I2C	I2S_LRCLK
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
VDDC	VSS							HPD	VDD_PLL912
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
VDD_DP12	VSS_DP	DPLNP_0	VSS_DP	DPLNP_1	VSS_DP	DPLNP_2	VSS_DP	DPLNP_3	DPAUXP
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
VDD_PLL18	REFCLK	DPLNM_0	VDD_DP18	DPLNM_1	VDD_DP12	DPLNM_2	VDD_DP18	DPLNM_3	DPAUXM

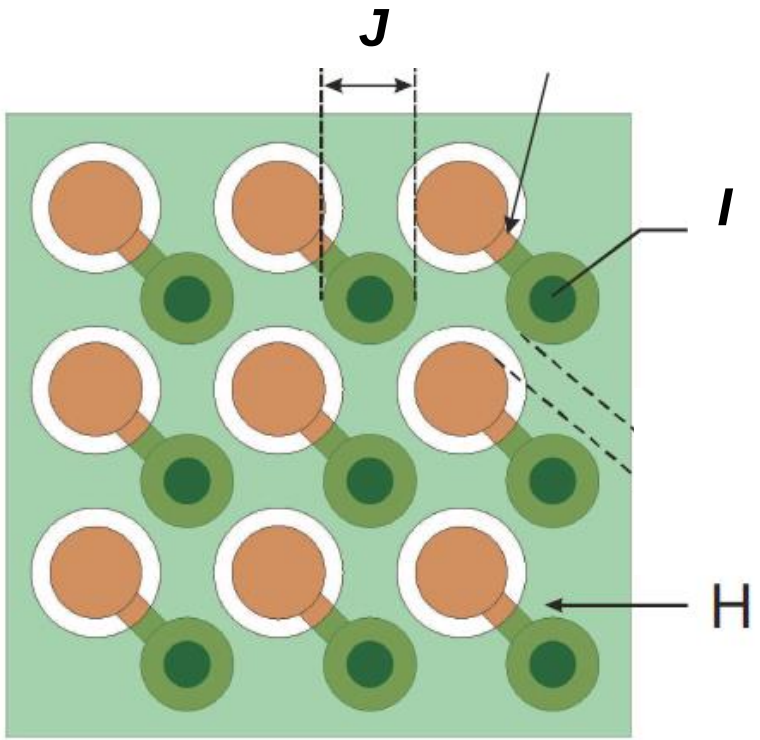


PCB Dimensions for 0.65mm Pitch with Routing Track



Layout constraints		
A	Pad pitch	0.65 mm (26 mil)
B	Pad size	0.25mm
C	Mask opening	0.35mm
D	Mask spacing	0.3mm
E	Trace width	4mil
F	Trace spacing	5.87mil

PCB Dimensions for 0.65mm Pitch with Via



Layout constraints		
H	Pad-to-via trace width	4mil
I	Via drill size	10mil
J	Via pad size	20mil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