UNIVERSITY OF TEHRAN

School of Electrical and Computer Engineering

Digital Logic Laboratory, ECE 045, Fall 1392

Experiment 1 (Sessions 1, 2)

Introduction to TTL 74 Series Basic Logic Gates, Clock Generator, FPGA Educational Board and Altera Quartus II

The purpose of this lab is to:

- Familiar with primitive tools of digital logic design such as:
    - Power supply, Function Generator, and Oscilloscope
    - TTL 74 Series Basic Logic Gates
    - LM555 timer IC
    - DE0-nano FPGA Educational Board
- Familiar with primitive concepts of digital logic design such as:
    - Static Characteristics of Digital Logic Gates Viewed as Transistor Electronic Circuits
    - Delay Times Effects and Glitch
    - Clock Frequency Generation
    - Digital Systems Design using Schematic Diagram and Verilog HDL
    - Simulation of Logic Circuits
    - FPGA Implementation

Note: After each part of the lab and before proceeding to the next part, present your work to the laboratory instructor. Record your results for later use in the report by taking good resolution photos from the waveforms on oscilloscope, capturing simulation waveform, etc.

1. Static Characteristics of Inverter

In this experiment you will need a '74LS00' which is available in red box handed to you at the start of the lab session. Pin diagram of '74LS00' is shown in Figure 1.

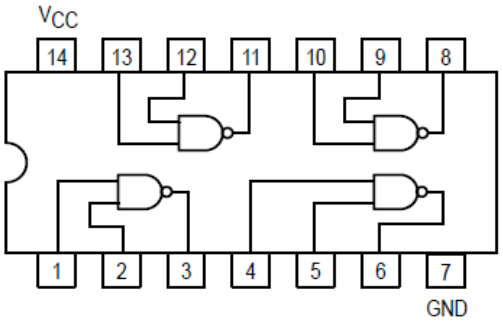

Figure 1-74LS00 IC pin diagram

Construct the circuit shown in Figure 2. Use the fixed '5v' output of the power supply to power the chip, connect the ground signals, and feed one of the inputs of one of the NAND gates to the supply power. Use the variable output of power supply to feed the other input of the NAND gate. Note that ground of power supply, oscilloscope, and your circuit should be connected together.

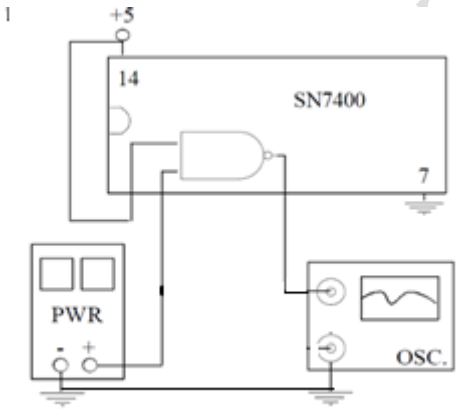

Figure 2-The SN7400 logic levels measurement circuit

Figure 3 shows definitions for static characteristics of a gate. The right bar shows input value regions, while the left bar shows output value regions. When increasing input from '0v' at a specific value, a wide band is observed in the output. The input value before start of wideband is called 'V_{IL}' and output value at that instance is called 'V_{OH}'. By further increasing the input, output stays stable. The value on the input at this point is called 'V_{IH}' and the output value is called 'V_{OL}'. Sweep input from '0v' to '5v' and report values for 'V_{OL}', 'V_{OH}', 'V_{IL}' and 'V_{IH}' in a table.

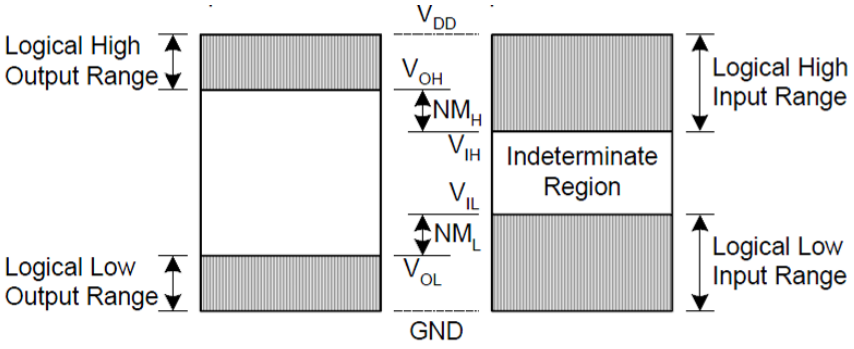

Figure 3-Logic level and DC noise margin

According to the table obtained in the experiment, answer the following questions in your report.

1. Calculate the 'NM_H' and 'NM_L' by using the results of the table.
2. Explain why 'V_{IH}' should be less than 'V_{OH}'.
3. Find the nominal value of 'V_{OL}' and 'V_{OH}' by referring to datasheet.
4. Explain the reason for observing the wide band on the monitor of the oscilloscope.
5. Why are the values of V_{OH}, V_{OL}, V_{IH}, and V_{IL} important?

Plot the output of the gate when its input is fed with a '5v' rectangular wave.

2. Glitches

Using a function generator produce a square-wave signal with amplitude of '5v' and frequency of 1 MHz. Then construct the circuit shown in Figure 4 with a 74LS00 package. Feed the CLK input with function generator's output.

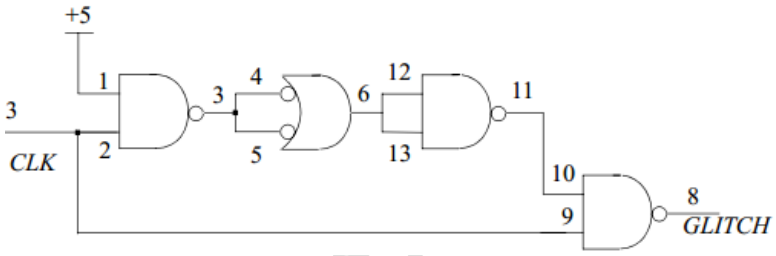

Figure 4-Glitch measurement circuit

Observe the output with oscilloscope, and explain the reason behind the phenomenon (glitches at the output). When are glitches hazardous?

3. Clock Generator

In this part, you are to design a circuit that generates a clock signal, which can be used to drive digital circuits. We will examine the use of the LM555 Timer to output a clock pulse. The LM555 timer is a device for generating oscillation or time delays. Figure 5 illustrates the pin layout of the LM555 IC.

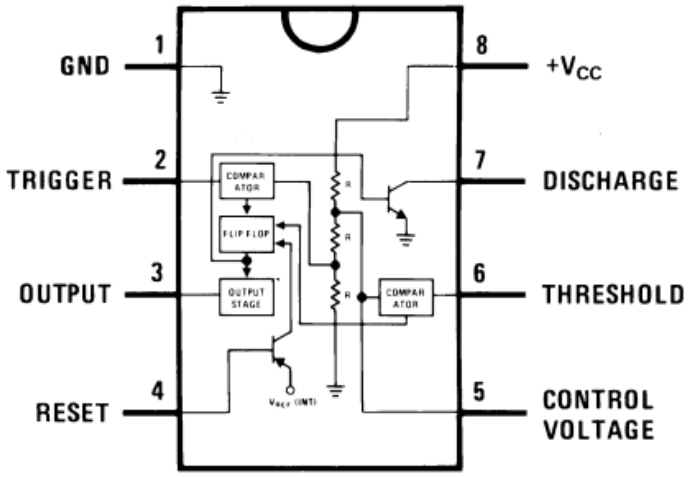

Figure 5-The LM555 pin layout

This IC operates in three modes: Monostable, Bistable and Astable. The astable mode, which we use in this experiment, allows the timer to operate as an oscillator that outputs a continuous rectangular pulse of a required frequency. For astable operation, we need two resistors and one capacitor to design a circuit that operates at the frequency required. The timing during which the output is either high or low is determined by these externally connected resistors and capacitor. Note that the durations of the low and high states may be different. Figure 6 shows the LM555 output in astable mode.

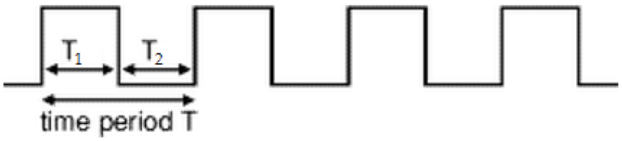

Figure 6. LM555 astable output, a square wave (Tm and Ts may be different)

Figure 7 illustrates an LM555 configuration for astable mode operation.

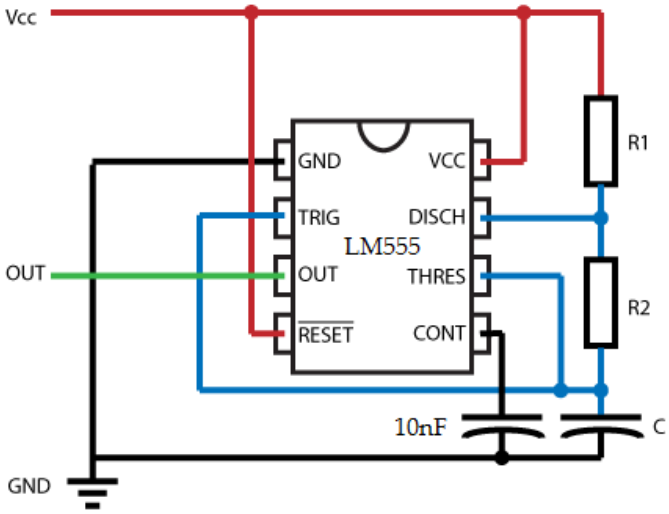

Figure 7. The LM555 in astable mode

The external capacitor (C_1) charges through $R_1 + R_2$ and discharges through R_2. Thus, the duty cycle and frequency may be precisely set by selecting the right combination of resistances and capacitance. According to Figure 6 and Figure 7, the charge time (output high) is given by $T_1 = 0.693 \times (R_1 + R_2) \times C$. The discharge time (output low) by: $T_2 = 0.693 \times R_2 \times C$. Thus, the total time period of square wave is $T = T_1 + T_2 = 0.693 \times (R_1 + 2R_2) \times C$. Consequently, the frequency of oscillation is $\frac{1.44}{(R1 + 2R2) \times C}$. The duty cycle also can be computed by $D = \frac{R_2}{R_1 + 2R_2}$.

These equations describe how we can choose these three values to decide on the frequency and the high and low durations of our signal. With the LM555 timer, the default value of R2 in this configuration is 1kΩ and this means that we cannot get a perfect 50% duty cycle. (If we make R2 >> R1 then we can get close.)

Do the following work. Your report must include the procedure you followed, as well as any observation and results.

1. Implement the LM555 in astable mode using the wiring diagram from Figure 7 and observe the output on oscilloscope.

Change the value of R1 resistors to produce different clock frequencies. To do so, R_1 should be 1kΩ, 10KΩ, and 100KΩ. Calculate the frequency and duty cycle using above equations and compare them to the clock signal you see on the oscilloscope.

4. ADDER

A half adder (HA) is a circuit that adds two bits together and outputs a sum (S), and a carry, (C). The full adder (FA) is a circuit very similar to the half adder. This circuit adds three input bits: A, B, and C_i (called Carry-In). The outputs are the same: S and Co (called a Carry-Out). A full adder can be implemented using two half adders and an OR gate.

1. Design a half adder circuit using only NAND gates, and implement it using 74LS00 ICs. Then verify its correctness by applying all possible inputs.
2. Design a half adder in Verilog.
3. Using schematics make a full adder using half adder blocks of the previous part.
4. Simulate the full adder in functional mode and verify its correctness.
5. Now simulate it in timing mode. Explain the difference between timing and functional simulation.
6. Assign input pins to switches on a DE0 board and use LEDs for the output. Then, compile and program the full adder circuit on the DE0 FPGA. Verify correctness of your design.

Report (At the start of the next lab)

Your report that is due at the start of the next lab should contain the following:

1. Course title, lab number, lab title, your name, and date of the day report is submitted.
2. Brief description of the experiment including goals and theory of the work.
3. Circuit schematics (screenshots, include your names).
4. Waveform simulations (screen shots).
5. Discussion of the results that indicate correct functionality of your circuit.
6. Conclusions
7. Answer questions that were included in this instruction in your report. Also include in your report questions that the TA asked you during the lab and your answers, and possibly, the corrections that the TA made to your answers.

Tips on writing your report:

1. You can provide a table of values based on the waveform. By referring to the time periods for each value, you can explain how the simulator provided the correct results.
2. You may find it easier to walk through the procedure.

The lab report is an important part of the laboratory. Write it carefully, be clear, and well-organized. It is the only way to convey that you did a great job in the lab. It is mandatory that you type the report. The report is due at the start of the next lab session.