MAX® 10 FPGA Device Family Pin Connection Guidelines

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Disclaimer

MAX® 10 FPGA Pin Connection Guidelines

Clock and PLL Pins

Note: Altera recommends that you create a Quartus® Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Table 1. Clock and PLL Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
CLK [0..7]p	Clock, I/O	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins. When these clock input pins are used as single-ended pins, you can disregard the p notation. The CLK[0..7]p pins can function as regular I/O pins.	Connect unused pins to the VCCIO of the bank in which the pins reside or GND. See Notes 2 and 3 of the *Notes to the MAX® 10 FPGA Pin Connection Guidelines* section.
CLK[0..7]n	Clock, I/O	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins. When these clock input pins are used as single-ended pins, you can disregard the n notation. The CLK[0..7]n pins can function as regular I/O pins.	Connect unused pins to the VCCIO of the bank in which the pins reside or GND. See Notes 2 and 3 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.
DPCLK[0..3]	I/O, Input	The DPCLK pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets, and clock enables. The DPCLK pins cannot feed a PLL input.	Connect unused pins to the VCCIO of the bank they reside in or GND. These pins can function as regular I/O pins. See Note 3 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.
PLL_[L,R,B,T]_CLKOUTp	I/O, Output	Optional positive terminal for external clock outputs from PLL[1..4]. These pins can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output. • PLL_L_CLKOUTp is referring to PLL_1. • PLL_R_CLKOUTp is referring to PLL_2. • PLL_T_CLKOUTp is referring to PLL_3. • PLL_B_CLKOUTp is referring to PLL_4.	Connect unused pins to GND. These pins can function as regular I/O pins. See Note 3 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		The availability for the PLL_[L,R,B,T]_CLKOUTp pins varies for each device density and package combination. For more details, refer to the specific device pinout file.	
PLL_[L,R,B,T]_CLKOUTn	I/O, Output	Optional negative terminal for external clock outputs from PLL[1..4]. These pins can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output. • PLL_L_CLKOUTn is referring to PLL_1. • PLL_R_CLKOUTn is referring to PLL_2. • PLL_T_CLKOUTn is referring to PLL_3. • PLL_B_CLKOUTn is referring to PLL_4. The availability for the PLL_[L,R,B,T]_CLKOUTn pins varies for each device density and package combination. For more details, refer to the specific device pinout file.	Connect unused pins to GND. These pins can function as regular I/O pins. See Note 3 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.

Related Information

- MAX 10 Device Pin-Out Files
- Notes to the MAX 10 FPGA Pin Connection Guidelines on page 22

Configuration/JTAG Pins

Note: Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Table 2. Configuration/JTAG Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
CONFIG_SEL	Input, I/O	This is a dual-purpose pin. Use this pin to choose the configuration image in the dual-configuration images mode. If the CONFIG_SEL pin is set to low, the first configuration image is configuration image 0. If the CONFIG_SEL pin is set to high, the first configuration image is configuration image 1. This pin is read before user mode and before the nSTATUS pin is asserted.	To select the configuration image in the dual-configuration images mode, connect a weak 10-KΩ pull-up or weak 10-KΩ pull-down to this pin externally during the power-up phase. By default, this pin is tristated. A weak 10-KΩ pull-up or weak 10-KΩ pull-down is not needed if you do not plan to use the dual configuration images mode. See Note 10 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.
CONF_DONE	Bidirectional (open-drain), I/O	This is a dual-purpose pin. The CONF_DONE pin drives low before and during configuration. After all configuration data is received without error and the initialization cycle starts, the CONF_DONE pin is released.	The CONF_DONE pin should be pulled high to VCCIO Bank 8 by an external 10-KΩ pull-up resistor. The MAX 10 device cannot enter the initialization and user mode if the CONF_DONE pin is pulled low. Hot socketing is disabled for the CONF_DONE pin. Due to this, a glitch maybe observed at the CONF_DONE pin. To monitor the status of the pin, Altera recommends to implement input buffer with hysteresis and digital filtering with the sampling duration larger than 5.5 ms in the external device to avoid false trip.
CRC_ERROR	Output (open-drain), I/O	This is a dual-purpose pin. Active high signal indicates that the error detection circuitry has detected errors in the configuration CRAM bits. The CRC_ERROR pin is an optional pin and is used when the cyclic redundancy check (CRC) error detection circuitry is enabled.	Altera recommends you to tie the CRC_ERROR pin to VCCIO, GND, or leave the pin unconnected when the CRC error detection circuitry is disabled or when you are not using the CRC_ERROR pin.
DEV_CLRn	Input, I/O	This is a dual-purpose pin. Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared. When this pin is driven high, all registers behave as programmed.	Altera recommends you to tie the DEV_CLRn pin to GND when the **Enable device-wide reset (DEV_CLRn)** option is disabled and not used as a user I/O pin. You can also tie the DEV_CLRn pin to VCCIO or leave the DEV_CLRn pin

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		The DEV_CLRn pin does not affect JTAG boundary-scan or programming operations. You can enable this pin by turning on the **Enable device-wide reset (DEV_CLRn)** option in the Quartus Prime software.	unconnected provided that the **Enable device-wide reset (DEV_CLRn)** option is disabled and not used as a user I/O pin. When you leave the DEV_CLRn pin unconnected, Altera recommends you to set the DEV_CLRn pin to input tristate with a weak pull-up.
DEV_OE	Input, I/O	This is a dual-purpose pin. Optional pin that allows you to override all tristates on the device. When this pin is driven low, all I/O pins are tristated. When this pin is driven high, all I/O pins behave as programmed. You can enable this pin by turning on the **Enable device-wide output enable (DEV_OE)** option in the Quartus Prime software.	Altera recommends you to tie the DEV_OE pin to GND when the **Enable device-wide output enable (DEV_OE)** option is disabled and not used as a user I/O pin. You can also tie the DEV_OE pin to VCCIO or leave the DEV_OE pin unconnected provided that the **Enable device-wide output enable (DEV_OE)** option is disabled and not used as a user I/O pin. When you leave the DEV_OE pin unconnected, Altera recommends you to set the DEV_OE pin to input tristate with a weak pull-up.
JTAGEN	I/O	This is a dual-purpose pin. This pin functions according to the setting of the JTAG pin sharing option bit. If the JTAG pin sharing is not enabled, the JTAGEN pin is a regular I/O pin and JTAG pins function as JTAG dedicated pins. If the JTAG pin sharing is enabled and the JTAGEN pin is pulled low, the JTAG pins function as dual-purpose pins. If the JTAG pin sharing is enabled and the JTAGEN pin is pulled high, the JTAG pins function as JTAG dedicated pins.	This pin has an internal 25-kΩ pull up. In user mode, to use the JTAG pins as regular I/O pins, tie the JTAGEN pin to a weak 1-kΩ pull-down. To use the JTAG pin as dedicated pin, tie the JTAGEN pin to a weak 10-kΩ pull-up.
nCONFIG	Input, I/O	This is a dual-purpose pin, as an nCONFIG pin or a single-ended input pin in user mode. Before user mode, these pins function as configuration pins. During configuration mode, the pin name is nCONFIG. During user mode, the pin name is Input_only. If you pull this pin low during user mode the device loses its configuration data, enter a reset state, and tristate all I/O pins. Pulling this pin to a logic-high level initiates reconfiguration.	Upon power up, the nCONFIG pin must be pulled high. Connect this pin directly or through a 10-kΩ resistor to VCCIO.
nSTATUS	Bidirectional (open-drain), I/O	This is a dual-purpose pin, as an nSTATUS pin or a regular user I/O pin in user mode. By default, the nSTATUS pin is a dedicated configuration pin in user mode. The device drives the nSTATUS pin low immediately after power up and releases the pin after power-on reset (POR) time.	Pull the nSTATUS pin high using an external 10-kΩ pull-up resistor. Pull the nSTATUS pin high using an external 10-kΩ pull-up resistor. Hot socketing is disabled for the nSTATUS pin. Due to this, a glitch maybe observed at the nSTATUS pin. To monitor the status of the pin, Altera recommends to implement input

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		As a status output, the nSTATUS pin is pulled low if an error occurs during configuration. As a status input, the device enters an error state when the nSTATUS pin is driven low by an external source during configuration or initialization.	buffer with hysteresis and digital filtering with the sampling duration larger than 5.5 ms in the external device to avoid false trip.
TCK	Input, I/O	JTAG test clock input pin. This is a dual-purpose pin.	This TCK pin does not support internal weak pull-down. Connect this pin to an external 1-KΩ – 10-KΩ pull-down resistor. By default, this pin is tristated. If the configuration voltage (VCCIO Bank 1B) exceed 2.5 V, Altera recommends that you add an external capacitor and diode to reduce voltage overshoot. For more information about overshoot prevention circuitry, refer to the *MAX 10 FPGA Configuration User Guide*.
TDO	Output, I/O	This is a dual-purpose pin, as a JTAG TDO pin or a regular user I/O pin in user mode.	Altera recommends you to leave this pin unconnected if not used. By default, this pin is tristated. If the configuration voltage (VCCIO Bank 1B) exceed 2.5 V, Altera recommends that you add an external capacitor and diode to reduce voltage overshoot. For more information about overshoot prevention circuitry, refer to the *MAX 10 FPGA Configuration User Guide*.
TDI	Input, I/O	This is a dual-purpose pin, as a JTAG TDI pin or a regular user I/O pin in user mode. You can disable the JTAG circuitry by connecting the TDI pin to VCCIO Bank 1B.	This pin has a weak internal pull-up. For configuration voltage of 2.5 V, 3.0 V, or 3.3 V, connect this pin through a 10-kΩ resistor to VCCIO Bank 1B. If power supplies exceed 2.5 V, Altera recommends that you add an external capacitor and diode to reduce voltage overshoot. For configuration voltage of 1.5 V and 1.8 V, connect this pin through a 10-kΩ resistor to 1.5 V or 1.8 V (VCCIO Bank 1B) supply, respectively. For more information about overshoot prevention circuitry, refer to the *MAX 10 FPGA Configuration User Guide*.
TMS	Input, I/O	This is a dual-purpose pin, as a JTAG TMS pin or a regular user I/O pin in user mode. You can disable the JTAG circuitry by connecting the TMS pin to VCCIO Bank 1B.	This pin has a weak internal pull-up. For configuration voltage of 2.5 V, 3.0 V, or 3.3 V, connect this pin through a 10-kΩ resistor to VCCIO Bank 1B. If power supplies exceed 2.5 V, Altera recommends that you add an external capacitor and diode to reduce voltage overshoot. For configuration voltage of 1.5 V and 1.8 V, connect this pin through a 10-kΩ resistor to 1.5 V or 1.8 V (VCCIO Bank 1B) supply, respectively. For more information about overshoot prevention circuitry, refer to the *MAX 10 FPGA Configuration User Guide*.

Related Information

- MAX 10 FPGA Configuration User Guide
- Notes to the MAX 10 FPGA Pin Connection Guidelines on page 22

Differential I/O Pins

Note: Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Table 3. Differential I/O Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DIFFIO_RX_L[#:#][n,p], DIFFOUT_L[#:#][n,p]	I/O, dedicated RX channel, emulated LVDS output channel	When used as differential inputs, these are true LVDS receiver channels on left I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. When used as differential outputs, these are emulated LVDS output channels on left I/O banks. External resistor network is needed for emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in the Quartus Prime software. For the number of LVDS pair count for each MAX 10 device, refer to the respective device pinout file.
DIFFIO_RX_R[#:#][n,p], DIFFOUT_R[#:#][n,p]	I/O, dedicated RX channel, emulated LVDS output channel	When used as differential inputs, these are true LVDS receiver channels on right I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. When used as differential outputs, these are emulated LVDS output channels on right I/O banks. External resistor network is needed for emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in the Quartus Prime software. For the number of LVDS pair count for each MAX 10 device, refer to the respective device pinout file.
DIFFIO_RX_T[#:#][n,p], DIFFOUT_T[#:#][n,p]	I/O, dedicated RX channel, emulated LVDS output channel	When used as differential inputs, these are true LVDS receiver channels on top I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in the Quartus Prime software. For the number of LVDS pair count for each MAX 10 device, refer to the respective device pinout file.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		When used as differential outputs, these are emulated LVDS output channels on top I/O banks. External resistor network is needed for emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	
DIFFIO_RX_B[#:#][n,p], DIFFOUT_B[#:#][n,p]	I/O, dedicated RX channel, emulated LVDS output channel	When used as differential inputs, these are true LVDS receiver channels on bottom I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. When used as differential outputs, these are emulated LVDS output channels on bottom I/O banks. External resistor network is needed for emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in the Quartus Prime software. For the number of LVDS pair count for each MAX 10 device, refer to the respective device pinout file.
DIFFIO_TX_RX_B[#:#][n,p]	I/O, dedicated TX/RX channel	These are true LVDS transmitter channels or true LVDS receiver channels on bottom I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in the Quartus Prime software. For the number of LVDS pair count for each MAX 10 device, refer to the respective device pinout file.
High_Speed	I/O	These are I/O pins. The High_Speed I/O pins have higher performance compared to the Low_Speed I/O pins. The High_Speed I/O pins reside in Banks 2, 3, 4, 5, 6, and 7.	Connect unused pins as defined in the Quartus Prime software.
Low_Speed	I/O	These are I/O pins. The Low_Speed I/O pins have lower performance compared to the High_Speed I/O pins. The Low_Speed I/O pins reside in Banks 1A, 1B, and 8.	Connect unused pins as defined in the Quartus Prime software.
RDN	I/O, Input	This pin is required for each OCT RS calibration block. OCT is only applicable for right I/O banks (banks 5 and 6) of 10M16, 10M25, and 10M50 devices.	When you use OCT, tie these pins to GND through either a 25-, 34-, 40-, 48-, or 50-Ω resistor depending on the desired I/O standard. When the device does not use this dedicated input pin for the external precision resistor or as an I/O pin, Altera recommends you to connect the RDN pin to GND.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		This pin is a dual-purpose pin, you can use the RDN pin as a regular I/O pin if the OCT calibration is not used. When you use OCT calibration, connect the RDN pin to GND through an external resistor.	
RUP	I/O, Input	This pin is required for each OCT RS calibration block. OCT is only applicable for right I/O banks (banks 5 and 6) of 10M16, 10M25, and 10M50 devices. This pin is a dual-purpose pin, you can use the RUP pin as a regular I/O pin if the OCT calibration is not used. When you use OCT calibration, connect the RUP pin to VCCN through an external resistor.	When you use OCT, tie these pins to the required VCCIO banks through either a 25-, 34-, 40-, 48-, or 50-Ω resistor depending on the desired I/O standard. When the device does not use this dedicated input pin for the external precision resistor or as an I/O pin, Altera recommends you to connect the RUP pin to VCCIO of the bank in which the RUP pin resides or GND.
VREFB<#>N0	Power, I/O	These pins are dual-purpose pins. For Banks 1A and 1B, the VREF pins are shared. Input reference voltage for each I/O bank. If a bank uses a voltage referenced I/O standard for input operation, then these pins are used as the voltage-reference pins for the bank.	If you are not using the VREF pins in banks or shared banks, connect unused pins as defined in the Quartus Prime software. When the VREF pins are used as I/O pins, they have higher capacitance than regular I/O pins which slow the edge rates and affect I/O timing.

Related Information

MAX 10 Device Pin-Out Files

External Memory Interface Pins

Note: Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Table 4. External Memory Interface Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DQ[#]R	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important. However, use with caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width.	Connect unused pins as defined in the Quartus Prime software.
DQS[#]R	I/O, DQS	Optional data strobe signal for use in external memory interfacing.	Connect unused pins as defined in the Quartus Prime software.
DQSn[#]R	I/O, DQSn	Optional complementary data strobe signal for use in external memory interfacing.	Connect unused pins as defined in the Quartus Prime software.
DM[#]R	I/O, DM	A low signal on the DM pin indicates that the write is valid. Driving the DM pin high results in the memory masking of the DQ signals.	Connect unused pins as defined in the Quartus Prime software.
CK_[6]	I/O, Output	Input clock for external memory devices.	Connect unused pins as defined in the Quartus Prime software.
CK#_[6]	I/O, Output	Input clock for external memory devices, inverted CK.	Connect unused pins as defined in the Quartus Prime software.

Reference Pins

Note: Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Table 5. Reference Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
GND	Ground	Device ground pins.	Altera recommends you to tie REFGND to the GND pin with an isolating ferrite bead for the best ADC performance. Connect all GND pins to the board GND plane.
NC	No Connect	Do not drive signals into these pins.	When designing for device migration you may connect these pins to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern, leave these pins floating.
DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, GND, or any other signal. These pins must be left floating.

Analog Input Pins

Note: Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Table 6. Analog Input Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
ADC[1..2]IN[1..16]	I/O, Input	These multi-purpose pins support single-ended analog input or, bank does not support both analog and digital signals simultaneously. When not used as analog input pins, these pins can be used as any other digital I/O pins. The ADCIN[8] and ADCIN[16] pins support the prescalar feature. For 10M08 and 10M16 devices, the ADC1IN[1..8] pins are available for the single power supply devices and the ADC1IN[1..16] pins are available for 10M08U324 devices. The ADC1IN[1..16] pins are available for the dual power supply devices. For 10M25 and 10M50 devices, the ADC1IN[1..8] and ADC2IN[1..8] pins are available for both single and dual power supply devices.	All digital I/O pins are tristated if any of these pins is configured as an analog input pin. For unused ADCIN pins, Altera recommends you to connect them to GND. No parallel routing between analog input signals and I/O traces. The crosstalk requirement for analog to digital signal is -100 dB up to 2 GHz. Route the analog input signal adjacent to the REFGND. Total RC value including package, trace, and driver parasitic values should be less than 42.4 ns. This is to ensure the input signal is fully settled during the sampling phase. Low pass filter is required for each analog input pin. The filter ground reference is REFGND. For details about the board design guidelines, refer to the *MAX 10 Analog to Digital Converter User Guide*.
ADC_VREF	Input	Analog-to-digital converter (ADC) voltage reference input.	Tie the ADC_VREF pin to an external accurate voltage reference source. If you are not using the external reference, this pin is a no connect (NC). No parallel routing between analog input signals and I/O traces. The crosstalk requirement for analog to digital signal is -100 dB up to 2 GHz. For more information, refer to the *Guidelines: Board Design for ADC Reference Voltage Pin* section of the *MAX 10 Analog to Digital Converter User Guide*.
ANAIN[1]	Input	This is a dedicated single-ended analog input pin for ADC1.	If this pin is not used, Altera recommends you to connect it to GND. No parallel routing between analog input signals and I/O traces. The crosstalk requirement for analog to digital signal is -100 dB up to 2 GHz. Route the analog input signal adjacent to the REFGND.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			Total RC value including package, trace, and driver parasitic values should be less than 42.4 ns. This is to ensure the input signal is fully settled during the sampling phase. Low pass filter is required for each analog input pin. The filter ground reference is REFGND. For details about the board design guidelines, refer to the *MAX 10 Analog to Digital Converter User Guide*.
ANAIN[2]	Input	This is a dedicated single-ended analog input pin for ADC2. This pin is not available in each device density and package combination. For details, refer to the specific device pinout file.	If this pin is not used, Altera recommends you to connect it to GND. No parallel routing between analog input signals and I/O traces. The crosstalk requirement for analog to digital signal is -100 dB up to 2 GHz. The RC filter ground reference is REFGND. Total RC value including package, trace, and driver parasitic values should be less than 42.4 ns. This is to ensure the input signal is fully settled during the sampling phase. Low pass filter is required for each analog input pin. The filter ground reference is REFGND. For more information, refer to the *MAX 10 Analog to Digital Converter User Guide*.
REFGND	Input	This pin is the ADC ground reference pin for analog pins.	Altera recommends you to tie REFGND to the GND pin with an isolating ferrite bead for the best ADC performance. If you are not using ADC, tie this pin directly to GND.

Related Information

MAX 10 Analog to Digital Converter User Guide

MAX 10 (Single Supply) FPGA

Note: Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Table 7. MAX 10 (Single Supply) FPGA

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCC_ONE	Power	Power supply pin for core and periphery through an on-die regulator. The voltage is internally regulated to 1.2 V to supply power to the core and periphery.	The VCC_ONE power supply pin supports E144, M153, U169, and U324 package-types only. Connect all VCC_ONE pins to either 3.0 V or 3.3 V power supply. Tie VCC_ONE and VCCA with filter using the same power supply on board level.
VCCIO[#]	Power	I/O supply voltage pins for banks 1 through 8. Each bank supports different voltage level. The VCCIO pin supplies power to the input and output buffers for banks 1 through 8 for all I/O standards. The VCCIO pin powers up the JTAG and configuration pins.	Connect these pins to 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V power supplies, depending on the I/O standard assigned to each I/O bank. *Note:* The 1.0 V VCCIO is not supported on I/O banks 1B and 8. For single-supply device option, the 1.0-V VCCIO is only supported on specific MAX 10 devices. For the list of supported devices, refer to the *Supported I/O Standards* section in the *MAX 10 General Purpose I/O User Guide*. If you power-up a device from the power-down state, you need to power the VCCIO for bank 1B (bank 1 for 10M02 devices), bank 8, and the core to the appropriate level for the device to exit POR. The MAX 10 device enters the configuration stage after exiting the power-up stage with a small POR delay. The VCCIO for bank 1B (bank 1 for 10M02 devices) and bank 8 must be powered up to a voltage between 1.5 V to 3.3 V during configuration. If you are migrating from other MAX 10 devices to the 10M02 device, the VCCIO1A and VCCIO1B pins are shorted to the VCCIO1 pin of the 10M02 device. If you do not enable the ADC feature, you may connect the VCCIO1A and VCCIO1B pins to different voltage levels, provided that the VREF pin is not used. If the VREF pin is used, you must connect the VCCIO1A and VCCIO1B pins to the same voltage level.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			If you enable the ADC feature, connect VCCIO1A and VCCIO1B to either 3.0 V or 3.3 V depending on the VCC_ONE pins used. The power supply sharing between the VCCIO1A and VCCIO1B pins requires filtering to isolate the noise. The filter should be located near to the VCCIO1A pins. Only 10M02 devices do not require filtering if VCCIO1A and VCCIO1B share the same power supply. When the ADC feature is enabled, filter is required. If you are migrating from the 10M08 or 10M16 device to the 10M02 device with ADC enabled, replace the filter with 0-Ω resistor in the 10M02 device. For details about the available VCCIO pins for each MAX 10 device, refer to the respective device pinout file. See Note 4 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section. Decoupling of these pins depends on the design decoupling requirements of the specific board.
VCCA[1..6]	Power	Power supply pins for PLL and ADC block.	Connect these pins to a 3.0 V or 3.3 V power supplies even if the PLL and ADC are not used. These pins must be powered up and powered down at the same time. Connect all VCCA pins together. The VCCA power supply to the FPGA should be isolated for better jitter performance. See Notes 5 and 6 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section. VCCA[1..4] is available for M153, U169, and U324 packages while VCCA[1..6] is available for the E144 package. For more information about the UFM and CFM power-down requirement, refer to the *MAX 10 User Flash Memory User Guide*.

Related Information

- MAX 10 User Flash Memory User Guide
- Supported I/O Standards in MAX 10 Devices, MAX 10 General Purpose I/O User Guide
- MAX 10 Device Pin-Out Files

MAX 10 (Dual Supply) FPGA

Note: Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Table 8. MAX 10 (Dual Supply) FPGA

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCC	Power	Power supply pin for core and periphery.	Connect all VCC pins to 1.2 V power supply. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Note 4 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.
VCCIO[#]	Power	I/O supply voltage pins for banks 1 through 8. Each bank supports different voltage level. The VCCIO pin supplies power to the input and output buffers for all I/O standards. The VCCIO pin powers up the JTAG and configuration pins.	Connect these pins to 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V power supplies, depending on the I/O standard assigned to each I/O bank. *Note:* The 1.0 V VCCIO is not supported on I/O banks 1B and 8. For dual-supply device option, the 1.0 V VCCIO is only supported on specific MAX 10 devices. For the list of supported devices, refer to the *Supported I/O Standards* section in the *MAX 10 General Purpose I/O User Guide*. If you power-up a device from the power-down state, you need to power the VCCIO for bank 1B (bank 1 for 10M02 devices), bank 8, and the core to the appropriate level for the device to exit POR. The MAX 10 device enters the configuration stage after exiting the power-up stage with a small POR delay. The VCCIO for bank 1B (bank 1 for 10M02 devices) and bank 8 must be powered up to a voltage between 1.5V – 3.3V during configuration. If you are migrating from other MAX 10 devices to the 10M02 device, the VCCIO1A and VCCIO1B pins are shorted to the VCCIO1 pin of the 10M02 device. If you do not enable the ADC feature, you may connect the VCCIO1A and VCCIO1B pins to different voltage levels, provided that the VREF pin is not used. If the VREF pin is used, you must connect the VCCIO1A and VCCIO1B pins to the same voltage level. If you enable the ADC feature, connect VCCIO1A and VCCIO1B to 2.5 V.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			The power supply sharing between the VCCIO1A and VCCIO1B pins requires filtering to isolate the noise. The filter should be located near to the VCCIO1A pins. Only 10M02 devices do not require filtering if VCCIO1A and VCCIO1B share the same power supply. When the ADC feature is enabled, filter is required. If you are migrating from the 10M08 or 10M16 device to the 10M02 device with ADC enabled, replace the filter with 0-Ω resistor in the 10M02 device. For details about the available VCCIO pins for each MAX 10 device, refer to the respective device pinout file. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Note 4 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.
VCCA[1..4]	Power	Power supply pins for PLL analog block.	Connect these pins to a 2.5 V power supply even if the PLL is not used. These pins must be powered up and powered down at the same time. Connect all VCCA pins together. The VCCA power supply to the FPGA should be isolated for better jitter performance. See Notes 5 and 6 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section. For more information about the UFM and CFM power-down requirement, refer to the *MAX 10 User Flash Memory User Guide*.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCD_PLL[1..4]	Power	Power supply pins for PLL digital block.	Connect the VCCD_PLL[1..4] pins to 1.2 V power supply even if the PLL is not used. Connect all VCCD_PLL[1..4] pins together. Altera recommends you to keep these pins isolated from other VCC pins for better jitter performance. See Notes 5 and 7 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.
VCCA_ADC	Power	Power supply pin for ADC analog block.	Connect the VCCA_ADC pin to the recommended power supply specification for the best ADC performance. Tie the VCCA_ADC pin to any 2.5 V power domain if you are not using ADC, and do not tie the VCCA_ADC pin to GND. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Note 4 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.
VCCINT	Power	Power supply pin for ADC digital block.	Connect the VCCINT pin to the recommended power supply specification for the best ADC performance. Tie the VCCINT pin to any 1.2 V power domain if you are not using ADC. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Note 4 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.

Related Information

- MAX 10 User Flash Memory User Guide
- Supported I/O Standards in MAX 10 Devices, MAX 10 General Purpose I/O User Guide
- Notes to the MAX 10 FPGA Pin Connection Guidelines on page 22

Notes to the MAX 10 FPGA Pin Connection Guidelines

Note: Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are created based on the MAX 10 FPGA device family.
2. The number of dedicated global clocks for each device density is different.
3. The unused pins must be connected as specified in the Quartus Prime software settings. The default Quartus Prime setting for unused pins is 'As inputs tri-stated with weak pull-up resistors', unless for specific pins that the Quartus Prime software connects them to GND automatically.
4. Capacitance values for the power supply decoupling capacitors should be selected after consideration of the amount of power needed to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage drop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To assist in decoupling analysis, Altera's "Power Distribution Network (PDN) Design Tool" serves as an excellent decoupling analysis tool. The PDN design tool can be obtained at Power Distribution Network Design Tool.

Table 9. Transient Current and Voltage Ripple for MAX 10 Devices

To calculate the target impedance of each MAX 10 device supply, you should use the following transient current and voltage ripple percentages. Setting Ftarget to 70 MHz or higher should result in a robust PDN.

MAX 10 Supply Rail	Transient Current (%)	Voltage Ripple (%)
VCC	50	5
VCCIO	100	5
VCCA	10	5
VCCD_PLL	10	3
VCCA_ADC	50	2
VCCINT	50	3

5. Use separate power islands for VCCA and VCCD_PLL. PLL power supply may originate from another plane on the board but must be isolated using a ferrite bead or other equivalent methods. If using a ferrite bead, choose an 0402 package with low DC resistance, higher current rating than the maximum steady state current for the supply it is connected to (VCCA or VCCD_PLL) and high impedance at 100 MHz.
6. The VCCA power island can be decoupled with a combination of decoupling capacitors. Please refer to the Power Distribution Network Design Tool to determine the decoupling capacitors value. Use 0402 package for 0.1 uF and smaller capacitors for lower mounting inductance. Place 0.1 uF and smaller capacitors as close to the device as possible. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To minimize impact on jitter, a 20 mV ripple voltage was used in the analysis for VCCA decoupling.
7. The VCCD_PLL power island can be decoupled with a combination of decoupling capacitors. Refer to the "Power Distribution Network Design Tool" at Power Distribution Network Design Tool to determine the decoupling capacitors value. Place 0.1 uF and smaller capacitors as close to the device as possible. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To minimize impact on jitter, a 20 mV ripple voltage was used in the analysis for VCCD_PLL decoupling.
8. All configuration pins used in user mode are low-speed I/Os.
9. Low Noise Switching Regulator—defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has fast transient response. The switching frequency range is not an Altera requirement. However, Altera does require the Line Regulation and Load Regulation meet the following specifications:
   - Line Regulation < 0.4%
   - Load Regulation < 1.2%
10. If you enable the **Configure device from CFM0 only** option in the Quartus Prime software when generating the POF file, the FPGA always loads the configuration image 0 without sampling the physical CONFIG_SEL pin during power up.

Power Supply Sharing Guidelines for MAX 10 FPGA Devices

Example 1—MAX 10 (Dual Supply) FPGA

Note: Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Table 10. Power Supply Sharing Guidelines for MAX 10 (Dual Supply) FPGA – The ADC Feature is Not Used

Example Requiring 3 Power Regulators

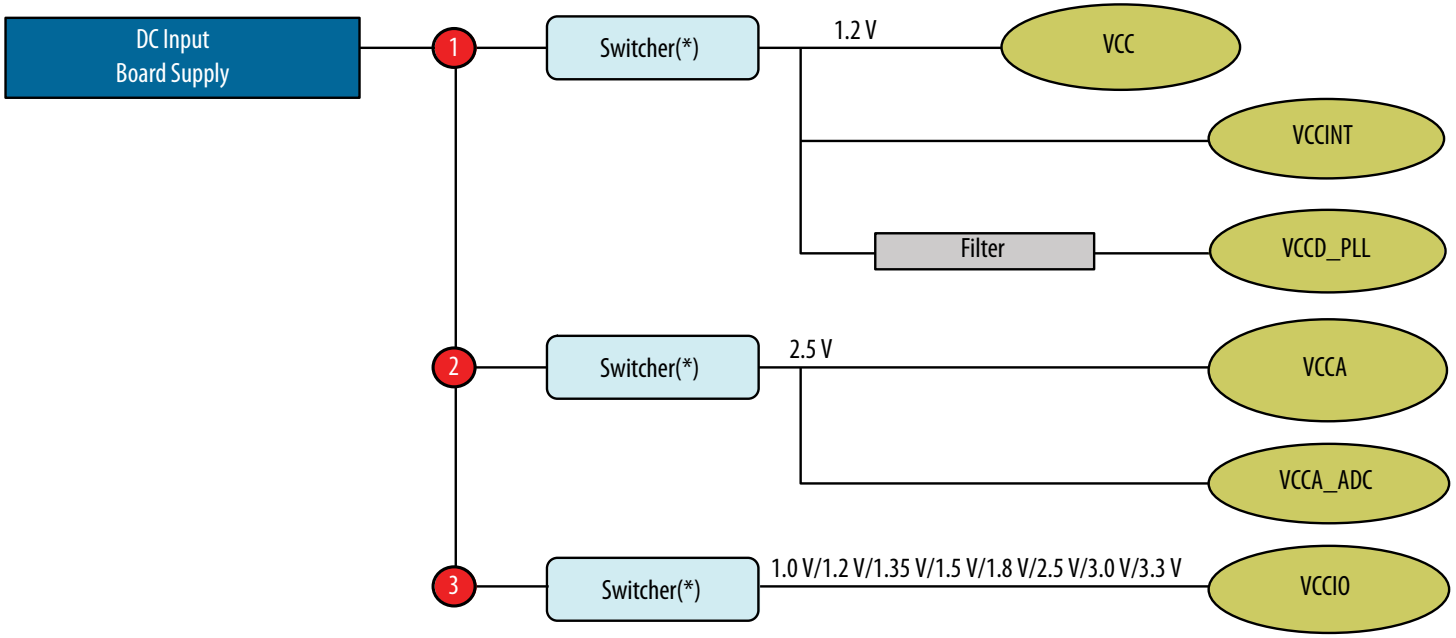
Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.2	±50 mV	Switcher(1)	Share	You have the option to share VCCINT and VCCD_PLL with VCC using proper isolation filters.
VCCINT					Isolate	
VCCD_PLL					Isolate	
VCCA	2	2.5	±5%	Switcher(1)	Share	You have the option to share VCCA_ADC with VCCA.
VCCA_ADC						
VCCIO	3	Varies	±5%	Switcher(1)	Share	Individual power rail.

Note:

1. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
2. Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the MAX 10 FPGA device is provided in the following figure.
3. For LPDDR2 interface targeting 200 MHz, you need to constraint the memory device I/O and core power supply to ±3% variation.
4. Refer to the *MAX 10 FPGA Configuration User Guide* for maximum ramp rate requirement.

(1) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in Note 9 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines*.

Figure 1. Example Power Supply Sharing Guidelines for MAX 10 (Dual Supply) FPGA – The ADC Feature is Not Used



The ADC power supply requires 0.1 uF decoupling cap near the package and ferrite bead filter at power supply.
(*) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in Note 9 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.

Related Information

Notes to the MAX 10 FPGA Pin Connection Guidelines on page 22

Example 2—MAX 10 (Dual Supply) FPGA

Note: Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Table 11. Power Supply Sharing Guidelines for MAX 10 (Dual Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up at 2.5 V

Example Requiring 3 Power Regulators

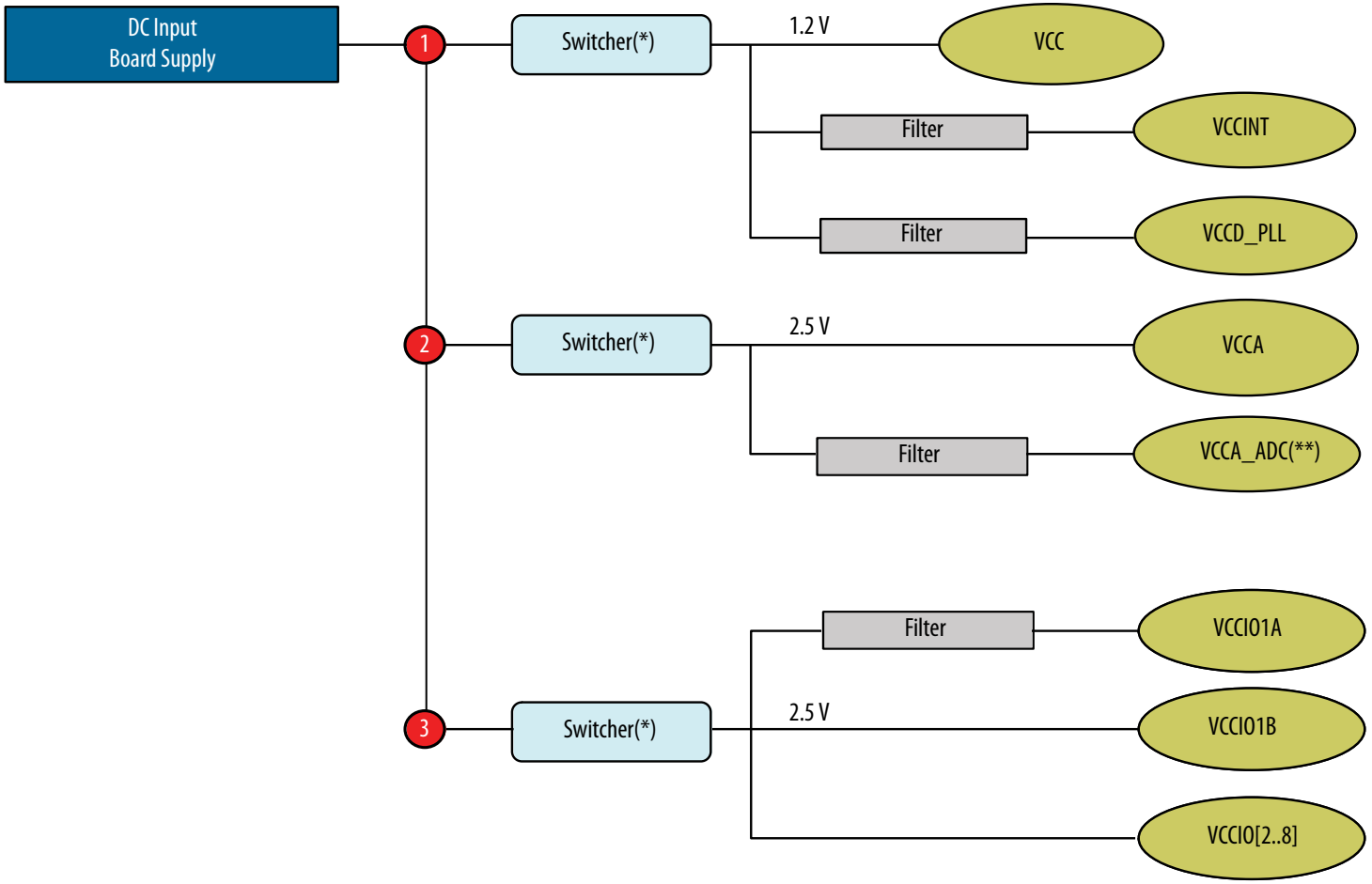
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.2	±50 mV	Switcher(2)	Share	You have the option to share VCCINT and VCCD_PLL with VCC with proper isolation filters.
VCCINT					Isolate	
VCCD_PLL					Isolate	
VCCA	2	2.5	±5%	Switcher(2)	Share	You have the option to share VCCA_ADC with VCCA with proper isolation filters.
VCCA_ADC					Isolate	
VCCIO1B	3	2.5	±5%	Switcher(2)	Share	You have the option to share VCCIO1B and VCCIO[2..8] when these pins are powered up at 2.5 V.
VCCIO[2..8]						
VCCIO1A					Isolate	You have the option to share VCCIO1A with VCCIO1B and VCCIO[2..8] using proper isolation filter.

(2) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in Note 9 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines*.

Note:

1. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
2. Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the MAX 10 FPGA device is provided in the following figure.
3. For LPDDR2 interface targeting 200 MHz, you need to constraint the memory device I/O and core power supply to ±3% variation.
4. Refer to the *MAX 10 FPGA Configuration User Guide* for maximum ramp rate requirement.

Figure 2. Example Power Supply Sharing Guidelines for MAX 10 (Dual Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up at 2.5 V



The ADC power supply requires 0.1 uF decoupling cap near the package and ferrite bead filter at power supply.
(*) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in Note 9 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.
(**) Ferrite beads should be connected in series followed by a 10 uF capacitor to ground. Place the decoupling of 0.1 uF cap closer to the pin.

Related Information

- MAX 10 FPGA Configuration User Guide
- Notes to the MAX 10 FPGA Pin Connection Guidelines on page 22

Example 3—MAX 10 (Dual Supply) FPGA

Note: Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Table 12. Power Supply Sharing Guidelines for MAX 10 (Dual Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up at 1.0 V/1.2 V/1.35 V/1.5 V/1.8 V/2.5 V/3.0 V/3.3 V

Example Requiring 4 Power Regulators

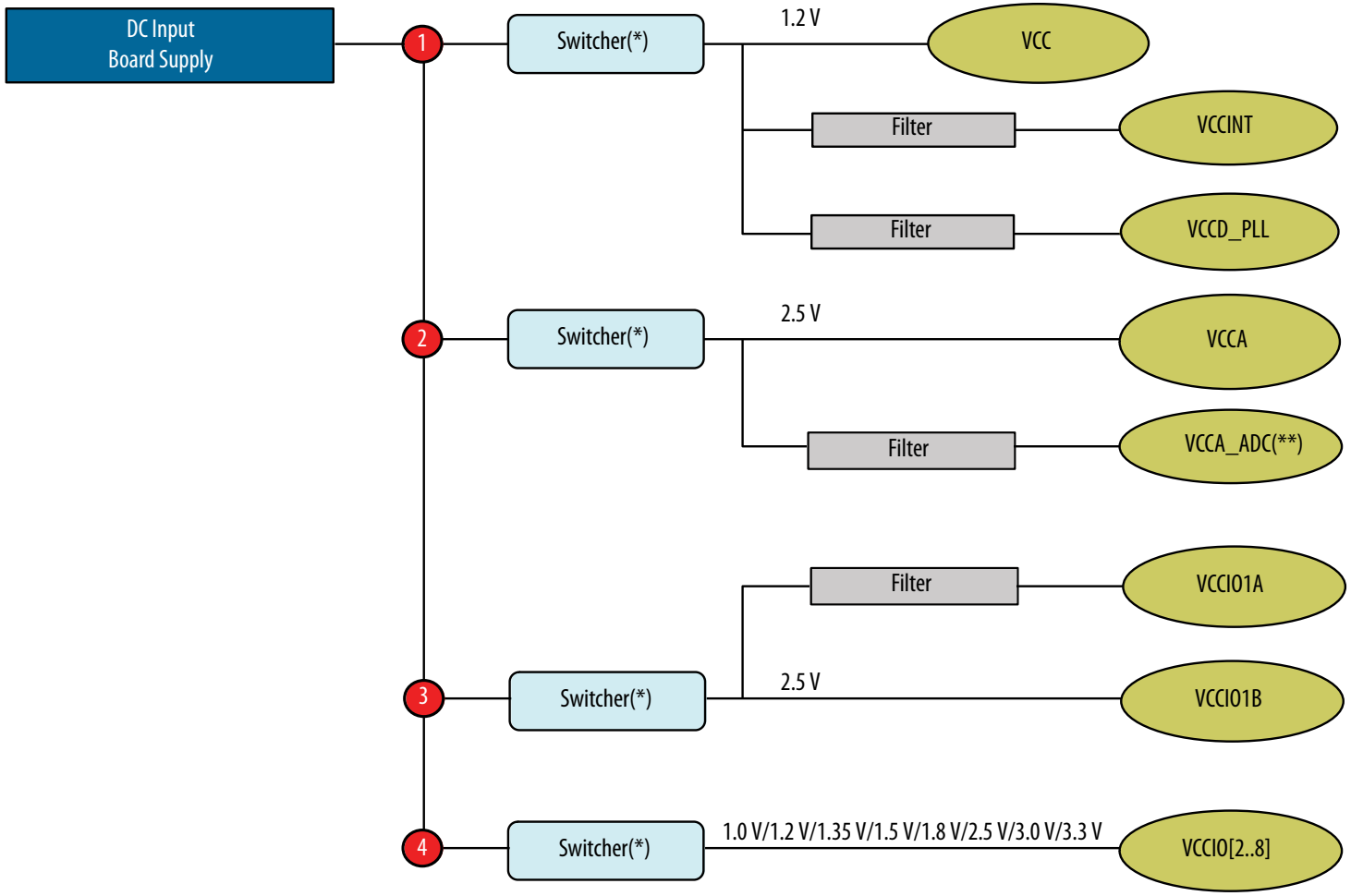
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.2	±50 mV	Switcher(3)	Share	You have the option to share VCCINT and VCCD_PLL with VCC using proper isolation filters.
VCCINT					Isolate	
VCCD_PLL					Isolate	
VCCA	2	2.5	±5%	Switcher(3)	Share	You have the option to share VCCA_ADC with VCCA using proper isolation filters.
VCCA_ADC					Isolate	
VCCIO1B	3	2.5	±5%	Switcher(3)	Share	You have the option to share VCCIO1A with VCCIO1B using proper isolation filter.
VCCIO1A					Isolate	
VCCIO[2..8]	4	Varies	±5%	Switcher(3)	Share	Individual power rail.

Note:

1. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
2. Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the MAX 10 FPGA device is provided in the following figure.
3. For LPDDR2 interface targeting 200 MHz, you need to constraint the memory device I/O and core power supply to ±3% variation.
4. Refer to the *MAX 10 FPGA Configuration User Guide* for maximum ramp rate requirement.

(3) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in Note 9 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines*.

Figure 3. Example Power Supply Sharing Guidelines for MAX 10 (Dual Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up at 1.0 V/1.2 V/1.35 V/1.5 V/1.8 V/2.5 V/3.0 V/3.3 V



The ADC power supply requires 0.1 uF decoupling cap near the package and ferrite bead filter at power supply.
(*) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in Note 9 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.
(**) Ferrite beads should be connected in series followed by a 10 uF capacitor to ground. Place the decoupling of 0.1 uF cap closer to the pin.

Related Information

Notes to the MAX 10 FPGA Pin Connection Guidelines on page 22

Example 4—MAX 10 (Single Supply) FPGA

Note: Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Table 13. Power Supply Sharing Guidelines for MAX 10 (Single Supply) FPGA (E144, M153, U169, and U324 Packages) – The ADC Feature is Not Used

Example Requiring 2 Power Regulator

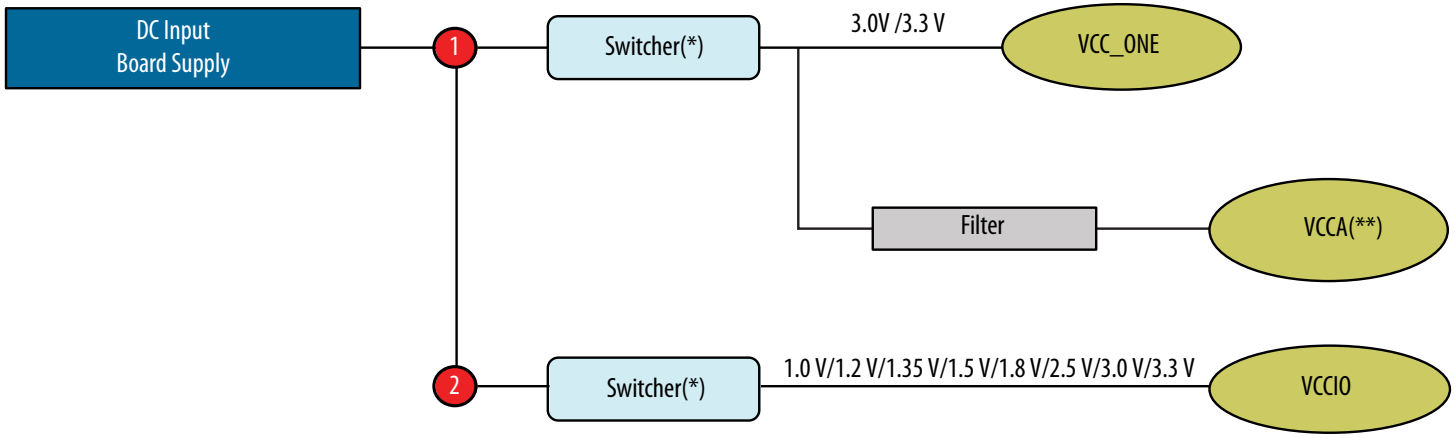
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC_ONE	1	3.0/3.3	±5%	Switcher(4)	Share	Both VCCA and VCC_ONE must share a single power source using proper isolation filter.
VCCA					Isolate	
VCCIO	2	Varies	±5%	Switcher(4)	Share	Individual power rail.

Note:

1. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
2. Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the MAX 10 FPGA device is provided in the following figure.
3. Refer to the *MAX 10 FPGA Configuration User Guide* for maximum ramp rate requirement.

(4) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in Note 9 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines*.

Figure 4. Example Power Supply Sharing Guidelines for MAX 10 (Single Supply) FPGA (E144, M153, U169, and U324 Packages) – The ADC Feature is Not Used



(*) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in Note 9 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.
(**) The VCCA power supply requires ferrite bead filter for noise isolation.

Related Information

- MAX 10 FPGA Configuration User Guide
- Notes to the MAX 10 FPGA Pin Connection Guidelines on page 22

Example 5—MAX 10 (Single Supply) FPGA

Note: Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Table 14. Power Supply Sharing Guidelines for MAX 10 (Single Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up 3.0 V/3.3 V (E144, M153, U169, and U324 Packages)

Example Requiring 2 Power Regulator

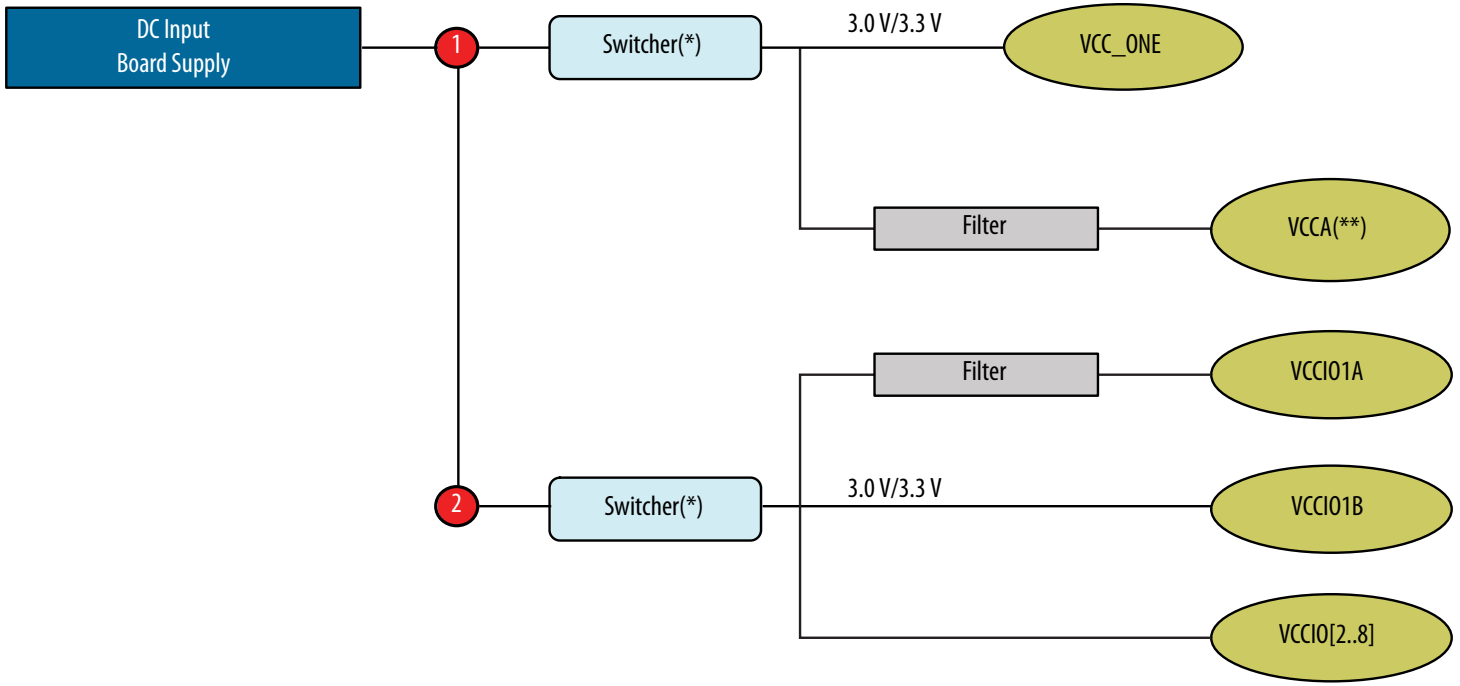
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC_ONE	1	3.0/3.3	±5%	Switcher(5)	Share	Both VCCA and VCC_ONE must share a single power source using proper isolation filter.
VCCA					Isolate	
VCCIO1B	2	3.0/3.3	±5%	Switcher(5)	Share	You have the option to share VCCIO1B and VCCIO[2..8] when these pins are powered up at 3.0V/3.3V.
VCCIO[2..8]						
VCCIO1A					Isolate	You have the option to share VCCIO1A with VCCIO1B and VCCIO[2..8] using proper isolation filter.

Note:

1. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
2. Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the MAX 10 FPGA device is provided in the following figure.
3. Refer to the *MAX 10 FPGA Configuration User Guide* for maximum ramp rate requirement.

(5) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in Note 9 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines*.

Figure 5. Example Power Supply Sharing Guidelines for MAX 10 (Single Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up 3.0 V/3.3 V (E144, M153, U169, and U324 Packages)



(*) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in Note 9 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.
(**) The VCCA power supply requires ferrite bead filter for noise isolation.

Related Information

- MAX 10 FPGA Configuration User Guide
- Notes to the MAX 10 FPGA Pin Connection Guidelines on page 22

Example 6—MAX 10 (Single Supply) FPGA

Note: Altera recommends that you create a Quartus Prime design, enter your device I/O assignments, and compile the design. The Quartus Prime software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device user guides.

Table 15. Power Supply Sharing Guidelines for MAX 10 (Single Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up 1.0 V/1.2 V/1.35 V/1.5 V/1.8 V/2.5 V (E144, M153, U169, and U324 Packages)

Example Requiring 3 Power Regulator

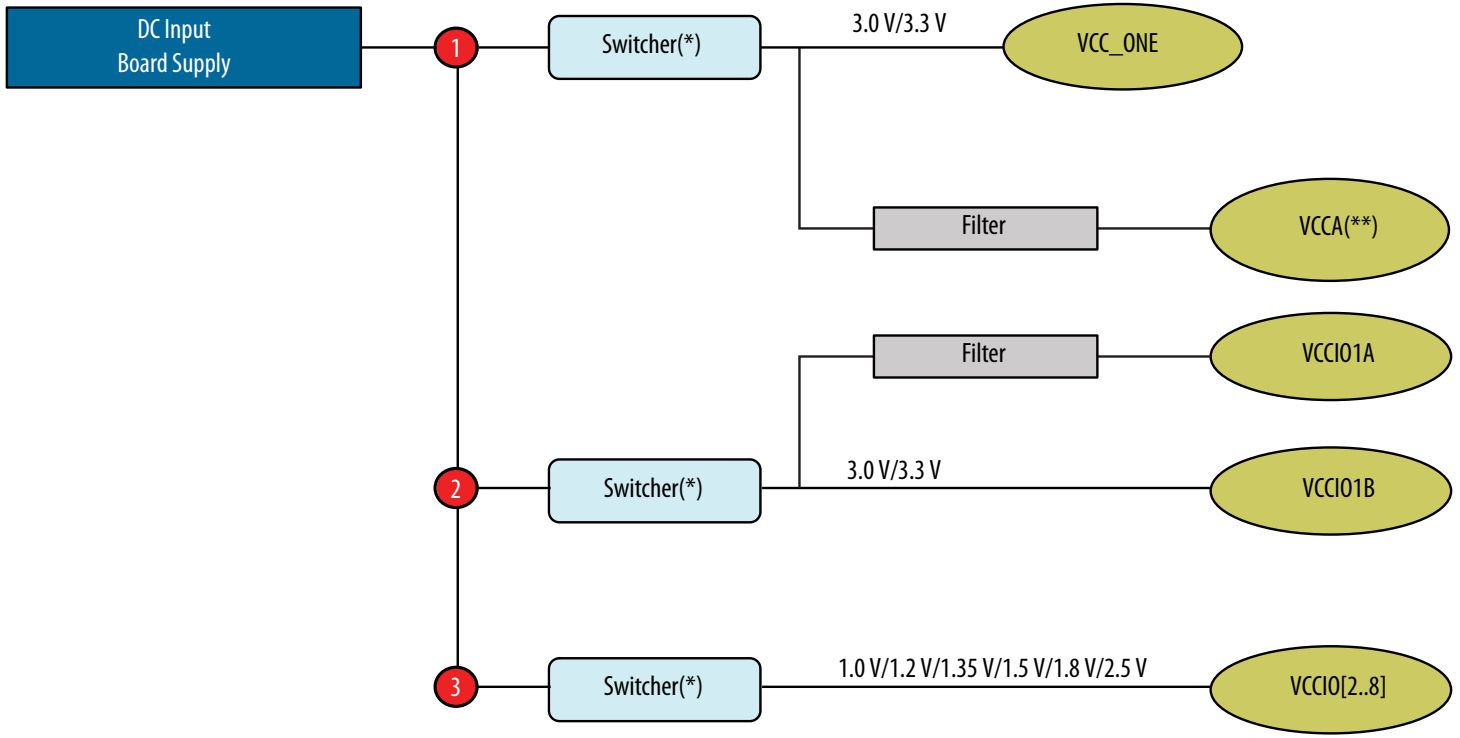
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC_ONE	1	3.0/3.3	±5%	Switcher(6)	Share	Both VCCA and VCC_ONE must share a single power source using proper isolation filter.
VCCA					Isolate	
VCCIO1B	2	3.0/3.3	±5%	Switcher(6)	Share	You have the option to share VCCIO1A with VCCIO1B using proper isolation filter.
VCCIO1A					Isolate	
VCCIO[2..8]	3	Varies	±5%	Switcher(6)	Share	Individual power rail.

Note:

1. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
2. Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the MAX 10 FPGA device is provided in the following figure.
3. Refer to the *MAX 10 FPGA Configuration User Guide* for maximum ramp rate requirement.

(6) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in Note 9 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines*.

Figure 6. Example Power Supply Sharing Guidelines for MAX 10 (Single Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up 1.0 V/1.2 V/1.35 V/1.5 V/1.8 V/2.5 V (E144, M153, U169, and U324 Packages)



(*) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in Note 9 of the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.
(**) The VCCA power supply requires ferrite bead filter for noise isolation.

Related Information

- MAX 10 FPGA Configuration User Guide

- Notes to the MAX 10 FPGA Pin Connection Guidelines on page 22

Document Revision History for the MAX 10 FPGA Device Family Pin Connection Guidelines

Document Version	Changes
2024.08.20	• Updated the connection guidelines for the following pins in *Configuration/JTAG Pins*: — TCK — TDO — TDI — TMS • Made editorial edits throughout the document.
2022.05.27	Removed all instances of Enpirion from *Example 1—Intel MAX 10 (Dual Supply) FPGA, Example 2—Intel MAX 10 (Dual Supply) FPGA, Example 3—Intel MAX 10 (Dual Supply) FPGA, Example 4—Intel MAX 10 (Single Supply) FPGA, Example 5—Intel MAX 10 (Single Supply) FPGA* and *Example 6—Intel MAX 10 (Single Supply) FPGA* sections.
2022.04.27	Updated the pin description of the ADC[1..2]IN[1..16] pins.
2021.11.26	Updated the connection guidelines of the VCCIO[#] pins for the *MAX 10 (Single Supply) FPGA* and *MAX 10 (Dual Supply) FPGA*.
2021.11.01	• Updated the 1.0-V VCCIO note in the connection guidelines of the VCCIO[#] pins in the *MAX 10 (Single Supply) FPGA* and *MAX 10 (Dual Supply) FPGA*.
2020.06.30	• Added the 1.0-V support to the VCCIO[#] pins for the *MAX 10 (Single Supply) FPGA* and *MAX 10 (Dual Supply) FPGA*. • Added 1.0-V support to the V_{CCIO} power supplies in the following power supply sharing guidelines: — Example Power Supply Guidelines for MAX 10 (Dual Supply) FPGA – The ADC Feature is Not Used — Example Power Supply Sharing Guidelines for MAX 10 (Dual Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up at 1.0V/1.2V/1.35V/1.5V/1.8V/2.5V/3.0V/3.3V — Example Power Supply Sharing Guidelines for MAX 10 (Single Supply) FPGA (E144, M153, U169, and U324 Packages) – The ADC Feature is Not Used — Example Power Supply Sharing Guidelines for MAX 10 (Single Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up 1.0V/1.2V/1.35V/1.5V/1.8V/2.5V (E144, M153, U169, and U324 Packages)
2019.07.01	• Updated the connection guidelines about how to enable the ADC feature in the VCCIO[#] pin of the *MAX 10 (Single Supply) FPGA* table. • Updated the connection guidelines of the DEV_CLRn and DEV_OE pins.
2019.02.20	Updated the connection guidelines of the DEV_CLRn and DEV_OE pins.
2019.01.29	• Updated the connection guidelines of the CONFIG_SEL pin. • Updated note 10 in the *Notes to the MAX 10 FPGA Pin Connection Guidelines* section.

Date	Version	Description of Changes
December 2017	2017.12.15	• Added the support for the U324 package. • Added a reference for the UFM and CFM power-down requirement to the VCCA[1..6] pins for the MAX 10 (Single Supply) FPGA and VCCA[1..4] pins for the MAX 10 (Dual Supply) FPGA. • Added a note to provide references for each PLL clock output of the PLL_[L,R,B,T]_CLKOUTp and PLL_[L,R,B,T]_CLKOUTn pins. • Updated the voltage overshoot connection guidelines for the TCK, TDO, TDI, and TMS pins. • Updated the Voltage Sensor Pins section to Analog Input Pins. • Removed PowerPlay text from tool name.
June 2017	2017.06.16	Updated the connection guidelines of the JTAGEN pin.
February 2017	2017.02.21	• Rebranded as Intel.
December 2016	2016.12.09	• Updated the connection guidelines of the TDI and TMS pins.
May 2016	2016.05.02	• Added note (5) to the following power sharing guidelines: — Example 1. Power Supply Sharing Guidelines for MAX 10D (Dual Supply) FPGA – The ADC Feature is Not Used — Example 2. Power Supply Sharing Guidelines for MAX 10D (Dual Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up at 2.5V — Example 3. Power Supply Sharing Guidelines for MAX 10D (Dual Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up at 1.2V/1.35V/1.5V/1.8V/3.0V/3.3V • Added note (4) to the following power sharing guidelines: — Example 4. Power Supply Sharing Guidelines for MAX 10S (Single Supply) FPGA (E144, M153, and U169 Packages) – The ADC Feature is Not Used — Example 5. Power Supply Sharing Guidelines for MAX 10S (Single Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up 3.0V/3.3V — Example 6. Power Supply Sharing Guidelines for MAX 10S (Single Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up 1.2V/1.35V/1.5V/1.8V/2.5V • Updated CONF_DONE should pulled up to VCCIO Bank 8. • Removed Note 3 “The voltage level for each power rail is preliminary.” from the following power sharing guidelines: — Example 1. Power Supply Sharing Guidelines for MAX 10D (Dual Supply) FPGA – The ADC Feature is Not Used — Example 2. Power Supply Sharing Guidelines for MAX 10D (Dual Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up at 2.5V — Example 3. Power Supply Sharing Guidelines for MAX 10D (Dual Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up at 1.2V/1.35V/1.5V/1.8V/3.0V/3.3V — Example 4. Power Supply Sharing Guidelines for MAX 10S (Single Supply) FPGA (E144, M153, and U169 Packages) – The ADC Feature is Not Used — Example 5. Power Supply Sharing Guidelines for MAX 10S (Single Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up 3.0V/3.3V (E144, M153, and U169 Packages) — Example 6. Power Supply Sharing Guidelines for MAX 10S (Single Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up 1.2V/1.35V/1.5V/1.8V/2.5V (E144, M153, and U169 Packages)

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Date	Version	Description of Changes
November 2015	2015.11.02	• Changed instances of Quartus II to Quartus Prime. • Updated the connection guidelines of the VCCIO[#] pins. • Updated the connection guidelines of the TDI and TMS pins.
June 2015	2015.06.12	Added the DNU pin.
May 2015	2015.05.06	• Added the following power sharing guidelines: — Example 2. Power Supply Sharing Guidelines for MAX 10D (Dual Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up at 2.5V — Example 3. Power Supply Sharing Guidelines for MAX 10D (Dual Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up at 1.2V/1.35V/1.5V/1.8V/3.0V/3.3V — Example 5. Power Supply Sharing Guidelines for MAX 10S (Single Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up 3.0V/3.3V (E144, M153, and U169 Packages) — Example 6. Power Supply Sharing Guidelines for MAX 10S (Single Supply) FPGA – Using the ADC Feature and VCCIO[2..8] Pins are Powered Up 1.2V/1.35V/1.5V/1.8V/2.5V (E144, M153, and U169 Packages) • Updated the following power sharing guidelines: — Example 1. Power Supply Sharing Guidelines for MAX 10D (Dual Supply) FPGA – The ADC Feature is Not Used • Updated the pin description of the DPCLK[0..3] pins. • Updated the connection guidelines of the VCCIO[#] pins. • Updated the connection guidelines of the ADC[1..2]IN[1..16] pins. • Updated the connection guidelines of the ADC_VREF pin.
January 2015	2015.01.29	• Updated the connection guidelines of the DPCLK[0..3] pins. • Updated the connection guidelines of the PLL_[L,R,B,T]_CLKOUTp and PLL_[L,R,B,T]_CLKOUTn pins. • Updated the connection guidelines of the VREFB<#>N0 pins. • Updated the pin description of the ADC[1..2]IN[1..16] pins.
December 2014	2014.12.15	• Added note 10 in the Notes to Pin Connection Guidelines. • Added note (**) to Figure 2. • Updated the pin name from BOOT_SEL to CONFIG_SEL. • Updated the pin description of the CONFIG_SEL pin. • Updated the connection guidelines of the VCC_ONE pin. • Updated the connection guidelines of the nSTATUs pin. • Updated the connection guidelines of the CONF_DONE pin. • Updated note 4 in the Notes to Pin Connection Guidelines.
September 2014	2014.09.22	Initial release.