E144	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
6	1A	VREFB1N0	IO			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed
7	1A	VREFB1N0	IO			DIFFIO_RX_L1p	DIFFOUT_L1p	Low_Speed
8	1A	VREFB1N0	IO			DIFFIO_RX_L3n	DIFFOUT_L3n	Low_Speed
10	1A	VREFB1N0	IO			DIFFIO_RX_L3p	DIFFOUT_L3p	Low_Speed
11	1A	VREFB1N0	IO			DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed
12	1A	VREFB1N0	IO			DIFFIO_RX_L5p	DIFFOUT_L5p	Low_Speed
13	1A	VREFB1N0	IO			DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed
14	1A	VREFB1N0	IO			DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed
15	1B	VREFB1N0	IO		JTAGEN			Low_Speed
16	1B	VREFB1N0	IO		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed
17	1B	VREFB1N0	IO	VREFB1N0				Low_Speed
18	1B	VREFB1N0	IO		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed
19	1B	VREFB1N0	IO		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed
20	1B	VREFB1N0	IO		TDO	DIFFIO_RX_L12p	DIFFOUT_L12p	Low_Speed
21	1B	VREFB1N0	IO			DIFFIO_RX_L14n	DIFFOUT_L14n	Low_Speed
22	1B	VREFB1N0	IO			DIFFIO_RX_L14p	DIFFOUT_L14p	Low_Speed
24	1B	VREFB1N0	IO			DIFFIO_RX_L16n	DIFFOUT_L16n	Low_Speed
25	1B	VREFB1N0	IO			DIFFIO_RX_L16p	DIFFOUT_L16p	Low_Speed
26	2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed
27	2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	High_Speed
28	2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L20n	DIFFOUT_L20n	High_Speed
29	2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L20p	DIFFOUT_L20p	High_Speed
30	2	VREFB2N0	IO	VREFB2N0				High_Speed
32	2	VREFB2N0	IO	PLL_L_CLKOUTn		DIFFIO_RX_L27n	DIFFOUT_L27n	High_Speed
33	2	VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO_RX_L27p	DIFFOUT_L27p	High_Speed
38	3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed
39	3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed
41	3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed
43	3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed
44	3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed
45	3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed
46	3	VREFB3N0	IO			DIFFIO_TX_RX_B7n	DIFFOUT_B7n	High_Speed
47	3	VREFB3N0	IO			DIFFIO_TX_RX_B7p	DIFFOUT_B7p	High_Speed
50	3	VREFB3N0	IO			DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High_Speed
48	3	VREFB3N0	IO	VREFB3N0				High_Speed
52	3	VREFB3N0	IO			DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High_Speed
54	3	VREFB3N0	IO					High_Speed
55	3	VREFB3N0	IO			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	High_Speed

E144	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
56	3	VREFB3N0	IO			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High_Speed
57	3	VREFB3N0	IO			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High_Speed
58	3	VREFB3N0	IO			DIFFIO_TX_RX_B14p	DIFFOUT_B14p	High_Speed
59	3	VREFB3N0	IO			DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High_Speed
60	3	VREFB3N0	IO			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed
61	4	VREFB4N0	IO	VREFB4N0				High_Speed
62	4	VREFB4N0	IO					High_Speed
64	4	VREFB4N0	IO			DIFFIO_TX_RX_B23n	DIFFOUT_B23n	High_Speed
65	4	VREFB4N0	IO			DIFFIO_TX_RX_B23p	DIFFOUT_B23p	High_Speed
66	4	VREFB4N0	IO					High_Speed
69	4	VREFB4N0	IO			DIFFIO_TX_RX_B27n	DIFFOUT_B27n	High_Speed
70	4	VREFB4N0	IO			DIFFIO_TX_RX_B27p	DIFFOUT_B27p	High_Speed
75	5	VREFB5N0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed
74	5	VREFB5N0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed
77	5	VREFB5N0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed
76	5	VREFB5N0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	High_Speed
79	5	VREFB5N0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	High_Speed
78	5	VREFB5N0	IO					High_Speed
81	5	VREFB5N0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed
80	5	VREFB5N0	IO	VREFB5N0				High_Speed
85	5	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed
84	5	VREFB5N0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	High_Speed
87	5	VREFB5N0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed
86	5	VREFB5N0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	High_Speed
88	6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R14p	DIFFOUT_R14p	High_Speed
89	6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R14n	DIFFOUT_R14n	High_Speed
90	6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed
91	6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R16n	DIFFOUT_R16n	High_Speed
92	6	VREFB6N0	IO			DIFFIO_RX_R18p	DIFFOUT_R18p	High_Speed
93	6	VREFB6N0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n	High_Speed
96	6	VREFB6N0	IO	DPCLK3		DIFFIO_RX_R26p	DIFFOUT_R26p	High_Speed
97	6	VREFB6N0	IO	VREFB6N0				High_Speed
98	6	VREFB6N0	IO	DPCLK2		DIFFIO_RX_R26n	DIFFOUT_R26n	High_Speed
99	6	VREFB6N0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	High_Speed
100	6	VREFB6N0	IO			DIFFIO_RX_R28p	DIFFOUT_R28p	High_Speed
101	6	VREFB6N0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	High_Speed
102	6	VREFB6N0	IO			DIFFIO_RX_R28n	DIFFOUT_R28n	High_Speed
105	6	VREFB6N0	IO			DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed

E144	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
106	6	VREFB6N0	IO			DIFFIO_RX_R33n	DIFFOUT_R33n	High_Speed
110	7	VREFB7N0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	High_Speed
111	7	VREFB7N0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	High_Speed
112	7	VREFB7N0	IO	VREFB7N0				High_Speed
113	7	VREFB7N0	IO					High_Speed
114	7	VREFB7N0	IO					High_Speed
118	7	VREFB7N0	IO			DIFFIO_RX_T10p	DIFFOUT_T10p	High_Speed
119	7	VREFB7N0	IO			DIFFIO_RX_T10n	DIFFOUT_T10n	High_Speed
120	8	VREFB8N0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	Low_Speed
121	8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed
122	8	VREFB8N0	IO		DEV_OE			Low_Speed
123	8	VREFB8N0	IO	VREFB8N0				Low_Speed
126	8	VREFB8N0	IO		CONFIG_SEL			Low_Speed
124	8	VREFB8N0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed
129	8	VREFB8N0	Input_only		nCONFIG			Low_Speed
127	8	VREFB8N0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed
130	8	VREFB8N0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	Low_Speed
131	8	VREFB8N0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed
132	8	VREFB8N0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	Low_Speed
134	8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T22n	DIFFOUT_T22n	Low_Speed
135	8	VREFB8N0	IO					Low_Speed
136	8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T24p	DIFFOUT_T24p	Low_Speed
138	8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T24n	DIFFOUT_T24n	Low_Speed
140	8	VREFB8N0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed
141	8	VREFB8N0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed
3			GND					
4			GND					
95			GND					
83			GND					
68			GND					
63			GND					
53			GND					
42			GND					
142			GND					
137			GND					
133			GND					
125			GND					
116			GND					

E144	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
104			GND					
9			VCCIO1A					
23			VCCIO1B					
31			VCCIO2					
49			VCCIO3					
40			VCCIO3					
67			VCCIO4					
82			VCCIO5					
94			VCCIO6					
103			VCCIO6					
117			VCCIO7					
139			VCCIO8					
128			VCCIO8					
35			VCCA1					
34			VCCA2					
5			VCCA3					
107			VCCA3					
143			VCCA4					
71			VCCA5					
2			VCCA6					
73			VCC_ONE					
72			VCC_ONE					
51			VCC_ONE					
37			VCC_ONE					
36			VCC_ONE					
144			VCC_ONE					
115			VCC_ONE					
109			VCC_ONE					
108			VCC_ONE					
1			VCC_ONE					

Note:
The E144-pin package has an exposed ground pad at the bottom of the package.
The exposed ground pad is used for electrical connectivity and not for thermal purposes. You must connect the exposed ground pad to the ground plane of the PCB.

M153	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
D2	1A	VREFB1N0	IO			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed
C2	1A	VREFB1N0	IO			DIFFIO_RX_L1p	DIFFOUT_L1p	Low_Speed
F5	1A	VREFB1N0	IO			DIFFIO_RX_L3n	DIFFOUT_L3n	Low_Speed
G5	1A	VREFB1N0	IO			DIFFIO_RX_L3p	DIFFOUT_L3p	Low_Speed
C1	1A	VREFB1N0	IO			DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed
B1	1A	VREFB1N0	IO			DIFFIO_RX_L5p	DIFFOUT_L5p	Low_Speed
E1	1A	VREFB1N0	IO			DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed
E2	1A	VREFB1N0	IO			DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed
G7	1B	VREFB1N0	IO		JTAGEN			Low_Speed
G1	1B	VREFB1N0	IO		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed
G2	1B	VREFB1N0	IO	VREFB1N0				Low_Speed
J1	1B	VREFB1N0	IO		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed
H5	1B	VREFB1N0	IO		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed
H4	1B	VREFB1N0	IO		TDO	DIFFIO_RX_L12p	DIFFOUT_L12p	Low_Speed
H3	1B	VREFB1N0	IO			DIFFIO_RX_L14n	DIFFOUT_L14n	Low_Speed
J2	1B	VREFB1N0	IO			DIFFIO_RX_L14p	DIFFOUT_L14p	Low_Speed
L1	1B	VREFB1N0	IO			DIFFIO_RX_L16n	DIFFOUT_L16n	Low_Speed
K2	1B	VREFB1N0	IO			DIFFIO_RX_L16p	DIFFOUT_L16p	Low_Speed
J4	2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed
J5	2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	High_Speed
K5	2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L20n	DIFFOUT_L20n	High_Speed
K4	2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L20p	DIFFOUT_L20p	High_Speed
L5	2	VREFB2N0	IO	DPCLK0		DIFFIO_RX_L22n	DIFFOUT_L22n	High_Speed
P1	2	VREFB2N0	IO	VREFB2N0				High_Speed
L4	2	VREFB2N0	IO	DPCLK1		DIFFIO_RX_L22p	DIFFOUT_L22p	High_Speed
R2	2	VREFB2N0	IO					High_Speed
N1	2	VREFB2N0	IO	PLL_L_CLKOUTn		DIFFIO_RX_L27n	DIFFOUT_L27n	High_Speed
P2	2	VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO_RX_L27p	DIFFOUT_L27p	High_Speed
M4	3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed
P3	3	VREFB3N0	IO			DIFFIO_RX_B2n	DIFFOUT_B2n	High_Speed
M5	3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed
R3	3	VREFB3N0	IO			DIFFIO_RX_B2p	DIFFOUT_B2p	High_Speed
L6	3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed
P4	3	VREFB3N0	IO			DIFFIO_RX_B4n	DIFFOUT_B4n	High_Speed
L7	3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed
R5	3	VREFB3N0	IO			DIFFIO_RX_B4p	DIFFOUT_B4p	High_Speed
P6	3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed
R7	3	VREFB3N0	IO			DIFFIO_RX_B6n	DIFFOUT_B6n	High_Speed

M153	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
P7	3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed
P8	3	VREFB3N0	IO			DIFFIO_RX_B6p	DIFFOUT_B6p	High_Speed
L8	3	VREFB3N0	IO			DIFFIO_TX_RX_B7n	DIFFOUT_B7n	High_Speed
P9	3	VREFB3N0	IO			DIFFIO_RX_B8n	DIFFOUT_B8n	High_Speed
M7	3	VREFB3N0	IO			DIFFIO_TX_RX_B7p	DIFFOUT_B7p	High_Speed
R9	3	VREFB3N0	IO			DIFFIO_RX_B8p	DIFFOUT_B8p	High_Speed
M8	3	VREFB3N0	IO			DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High_Speed
R11	3	VREFB3N0	IO	VREFB3N0				High_Speed
N8	3	VREFB3N0	IO			DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High_Speed
P12	3	VREFB3N0	IO					High_Speed
R14	3	VREFB3N0	IO			DIFFIO_TX_RX_B10n	DIFFOUT_B10n	High_Speed
P15	3	VREFB3N0	IO			DIFFIO_TX_RX_B10p	DIFFOUT_B10p	High_Speed
L9	3	VREFB3N0	IO			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	High_Speed
M9	3	VREFB3N0	IO			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High_Speed
L10	3	VREFB3N0	IO			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High_Speed
M11	3	VREFB3N0	IO			DIFFIO_TX_RX_B14p	DIFFOUT_B14p	High_Speed
P14	3	VREFB3N0	IO			DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High_Speed
R13	3	VREFB3N0	IO			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed
M12	5	VREFB5N0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed
N15	5	VREFB5N0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed
L11	5	VREFB5N0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed
N14	5	VREFB5N0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	High_Speed
K11	5	VREFB5N0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	High_Speed
M14	5	VREFB5N0	IO					High_Speed
K12	5	VREFB5N0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed
L15	5	VREFB5N0	IO	VREFB5N0				High_Speed
J9	5	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed
K14	5	VREFB5N0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	High_Speed
J11	5	VREFB5N0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed
J14	5	VREFB5N0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	High_Speed
J12	6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R14p	DIFFOUT_R14p	High_Speed
H11	6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R14n	DIFFOUT_R14n	High_Speed
H12	6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed
H13	6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R16n	DIFFOUT_R16n	High_Speed
J15	6	VREFB6N0	IO			DIFFIO_RX_R18p	DIFFOUT_R18p	High_Speed
G15	6	VREFB6N0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n	High_Speed
G11	6	VREFB6N0	IO	DPCLK3		DIFFIO_RX_R26p	DIFFOUT_R26p	High_Speed
E15	6	VREFB6N0	IO	VREFB6N0				High_Speed

M153	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
G12	6	VREFB6N0	IO	DPCLK2		DIFFIO_RX_R26n	DIFFOUT_R26n	High_Speed
E14	6	VREFB6N0	IO					High_Speed
F11	6	VREFB6N0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	High_Speed
C15	6	VREFB6N0	IO			DIFFIO_RX_R28p	DIFFOUT_R28p	High_Speed
F12	6	VREFB6N0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	High_Speed
C14	6	VREFB6N0	IO			DIFFIO_RX_R28n	DIFFOUT_R28n	High_Speed
E11	6	VREFB6N0	IO			DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed
D12	6	VREFB6N0	IO			DIFFIO_RX_R33n	DIFFOUT_R33n	High_Speed
D11	8	VREFB8N0	IO			DIFFIO_RX_T14p	DIFFOUT_T14p	Low_Speed
B15	8	VREFB8N0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	Low_Speed
D10	8	VREFB8N0	IO			DIFFIO_RX_T14n	DIFFOUT_T14n	Low_Speed
B14	8	VREFB8N0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	Low_Speed
C8	8	VREFB8N0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	Low_Speed
B13	8	VREFB8N0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	Low_Speed
B8	8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed
A14	8	VREFB8N0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	Low_Speed
E10	8	VREFB8N0	IO		DEV_OE	DIFFIO_RX_T18p	DIFFOUT_T18p	Low_Speed
E9	8	VREFB8N0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	Low_Speed
A13	8	VREFB8N0	IO	VREFB8N0				Low_Speed
D8	8	VREFB8N0	IO		CONFIG_SEL			Low_Speed
B12	8	VREFB8N0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed
E8	8	VREFB8N0	Input_only		nCONFIG			Low_Speed
B11	8	VREFB8N0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed
B7	8	VREFB8N0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	Low_Speed
A9	8	VREFB8N0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	Low_Speed
B6	8	VREFB8N0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed
A11	8	VREFB8N0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	Low_Speed
D7	8	VREFB8N0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	Low_Speed
A7	8	VREFB8N0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	Low_Speed
E7	8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T22n	DIFFOUT_T22n	Low_Speed
A5	8	VREFB8N0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	Low_Speed
D6	8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T24p	DIFFOUT_T24p	Low_Speed
B4	8	VREFB8N0	IO					Low_Speed
E6	8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T24n	DIFFOUT_T24n	Low_Speed
A2	8	VREFB8N0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed
A3	8	VREFB8N0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed
D4			GND					
E4			GND					

M153	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
R15			GND					
R1			GND					
M6			GND					
M2			GND					
M10			GND					
L12			GND					
J7			GND					
H8			GND					
H14			GND					
G9			GND					
G4			GND					
E5			GND					
E12			GND					
D9			GND					
D5			GND					
B2			GND					
A15			GND					
A1			GND					
F2			VCCIO1A					
H2			VCCIO1B					
L2			VCCIO2					
P5			VCCIO3					
P11			VCCIO3					
P10			VCCIO3					
L14			VCCIO5					
G14			VCCIO6					
F14			VCCIO6					
B9			VCCIO8					
B5			VCCIO8					
B10			VCCIO8					
N2			VCCA1					
D14			VCCA2					
F4			VCCA3					
B3			VCCA3					
P13			VCCA4					
J8			VCC_ONE					
H9			VCC_ONE					
H7			VCC_ONE					

M153	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
G8			VCC_ONE					

U169	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
D1	1A	VREFB1N0	IO			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed
C2	1A	VREFB1N0	IO			DIFFIO_RX_L1p	DIFFOUT_L1p	Low_Speed
E3	1A	VREFB1N0	IO			DIFFIO_RX_L3n	DIFFOUT_L3n	Low_Speed
E4	1A	VREFB1N0	IO			DIFFIO_RX_L3p	DIFFOUT_L3p	Low_Speed
C1	1A	VREFB1N0	IO			DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed
B1	1A	VREFB1N0	IO			DIFFIO_RX_L5p	DIFFOUT_L5p	Low_Speed
F1	1A	VREFB1N0	IO			DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed
E1	1A	VREFB1N0	IO			DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed
E5	1B	VREFB1N0	IO		JTAGEN			Low_Speed
G1	1B	VREFB1N0	IO		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed
H1	1B	VREFB1N0	IO	VREFB1N0				Low_Speed
G2	1B	VREFB1N0	IO		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed
F5	1B	VREFB1N0	IO		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed
F6	1B	VREFB1N0	IO		TDO	DIFFIO_RX_L12p	DIFFOUT_L12p	Low_Speed
F4	1B	VREFB1N0	IO			DIFFIO_RX_L14n	DIFFOUT_L14n	Low_Speed
G4	1B	VREFB1N0	IO			DIFFIO_RX_L14p	DIFFOUT_L14p	Low_Speed
H2	1B	VREFB1N0	IO			DIFFIO_RX_L16n	DIFFOUT_L16n	Low_Speed
H3	1B	VREFB1N0	IO			DIFFIO_RX_L16p	DIFFOUT_L16p	Low_Speed
G5	2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed
J1	2	VREFB2N0	IO			DIFFIO_RX_L19n	DIFFOUT_L19n	High_Speed
H6	2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	High_Speed
J2	2	VREFB2N0	IO			DIFFIO_RX_L19p	DIFFOUT_L19p	High_Speed
H5	2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L20n	DIFFOUT_L20n	High_Speed
M1	2	VREFB2N0	IO			DIFFIO_RX_L21n	DIFFOUT_L21n	High_Speed
H4	2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L20p	DIFFOUT_L20p	High_Speed
M2	2	VREFB2N0	IO			DIFFIO_RX_L21p	DIFFOUT_L21p	High_Speed
N2	2	VREFB2N0	IO	DPCLK0		DIFFIO_RX_L22n	DIFFOUT_L22n	High_Speed
L1	2	VREFB2N0	IO	VREFB2N0				High_Speed
N3	2	VREFB2N0	IO	DPCLK1		DIFFIO_RX_L22p	DIFFOUT_L22p	High_Speed
L2	2	VREFB2N0	IO					High_Speed
M3	2	VREFB2N0	IO	PLL_L_CLKOUTn		DIFFIO_RX_L27n	DIFFOUT_L27n	High_Speed
K1	2	VREFB2N0	IO			DIFFIO_RX_L28n	DIFFOUT_L28n	High_Speed
L3	2	VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO_RX_L27p	DIFFOUT_L27p	High_Speed
K2	2	VREFB2N0	IO			DIFFIO_RX_L28p	DIFFOUT_L28p	High_Speed
L5	3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed
M4	3	VREFB3N0	IO			DIFFIO_RX_B2n	DIFFOUT_B2n	High_Speed
L4	3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed
M5	3	VREFB3N0	IO			DIFFIO_RX_B2p	DIFFOUT_B2p	High_Speed

U169	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
K5	3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed
N4	3	VREFB3N0	IO			DIFFIO_RX_B4n	DIFFOUT_B4n	High_Speed
J5	3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed
N5	3	VREFB3N0	IO			DIFFIO_RX_B4p	DIFFOUT_B4p	High_Speed
N6	3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed
N7	3	VREFB3N0	IO			DIFFIO_RX_B6n	DIFFOUT_B6n	High_Speed
M7	3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed
N8	3	VREFB3N0	IO			DIFFIO_RX_B6p	DIFFOUT_B6p	High_Speed
J6	3	VREFB3N0	IO			DIFFIO_TX_RX_B7n	DIFFOUT_B7n	High_Speed
M8	3	VREFB3N0	IO			DIFFIO_RX_B8n	DIFFOUT_B8n	High_Speed
K6	3	VREFB3N0	IO			DIFFIO_TX_RX_B7p	DIFFOUT_B7p	High_Speed
M9	3	VREFB3N0	IO			DIFFIO_RX_B8p	DIFFOUT_B8p	High_Speed
J7	3	VREFB3N0	IO			DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High_Speed
N11	3	VREFB3N0	IO	VREFB3N0				High_Speed
K7	3	VREFB3N0	IO			DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High_Speed
N12	3	VREFB3N0	IO					High_Speed
M13	3	VREFB3N0	IO			DIFFIO_TX_RX_B10n	DIFFOUT_B10n	High_Speed
N10	3	VREFB3N0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	High_Speed
M12	3	VREFB3N0	IO			DIFFIO_TX_RX_B10p	DIFFOUT_B10p	High_Speed
N9	3	VREFB3N0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	High_Speed
M11	3	VREFB3N0	IO			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	High_Speed
L11	3	VREFB3N0	IO			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High_Speed
J8	3	VREFB3N0	IO			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High_Speed
K8	3	VREFB3N0	IO			DIFFIO_TX_RX_B14p	DIFFOUT_B14p	High_Speed
M10	3	VREFB3N0	IO			DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High_Speed
L10	3	VREFB3N0	IO			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed
K10	5	VREFB5N0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed
K11	5	VREFB5N0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed
J10	5	VREFB5N0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed
L12	5	VREFB5N0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	High_Speed
K12	5	VREFB5N0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	High_Speed
L13	5	VREFB5N0	IO					High_Speed
J12	5	VREFB5N0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed
K13	5	VREFB5N0	IO	VREFB5N0				High_Speed
J9	5	VREFB5N0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	High_Speed
J13	5	VREFB5N0	IO			DIFFIO_RX_R9p	DIFFOUT_R9p	High_Speed
H10	5	VREFB5N0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	High_Speed
H13	5	VREFB5N0	IO			DIFFIO_RX_R9n	DIFFOUT_R9n	High_Speed

U169	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
H9	5	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed
G13	5	VREFB5N0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	High_Speed
H8	5	VREFB5N0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed
G12	5	VREFB5N0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	High_Speed
G9	6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R14p	DIFFOUT_R14p	High_Speed
G10	6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R14n	DIFFOUT_R14n	High_Speed
F13	6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed
E13	6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R16n	DIFFOUT_R16n	High_Speed
F12	6	VREFB6N0	IO			DIFFIO_RX_R18p	DIFFOUT_R18p	High_Speed
E12	6	VREFB6N0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n	High_Speed
F9	6	VREFB6N0	IO	DPCLK3		DIFFIO_RX_R26p	DIFFOUT_R26p	High_Speed
D13	6	VREFB6N0	IO	VREFB6N0				High_Speed
F10	6	VREFB6N0	IO	DPCLK2		DIFFIO_RX_R26n	DIFFOUT_R26n	High_Speed
C13	6	VREFB6N0	IO					High_Speed
F8	6	VREFB6N0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	High_Speed
B12	6	VREFB6N0	IO			DIFFIO_RX_R28p	DIFFOUT_R28p	High_Speed
E9	6	VREFB6N0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	High_Speed
B11	6	VREFB6N0	IO			DIFFIO_RX_R28n	DIFFOUT_R28n	High_Speed
C12	6	VREFB6N0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	High_Speed
B13	6	VREFB6N0	IO			DIFFIO_RX_R30p	DIFFOUT_R30p	High_Speed
C11	6	VREFB6N0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	High_Speed
A12	6	VREFB6N0	IO			DIFFIO_RX_R30n	DIFFOUT_R30n	High_Speed
E10	6	VREFB6N0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	High_Speed
D9	6	VREFB6N0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	High_Speed
D12	6	VREFB6N0	IO			DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed
D11	6	VREFB6N0	IO			DIFFIO_RX_R33n	DIFFOUT_R33n	High_Speed
C10	8	VREFB8N0	IO			DIFFIO_RX_T14p	DIFFOUT_T14p	Low_Speed
A8	8	VREFB8N0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	Low_Speed
C9	8	VREFB8N0	IO			DIFFIO_RX_T14n	DIFFOUT_T14n	Low_Speed
A9	8	VREFB8N0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	Low_Speed
B10	8	VREFB8N0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	Low_Speed
A10	8	VREFB8N0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	Low_Speed
B9	8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed
A11	8	VREFB8N0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	Low_Speed
D8	8	VREFB8N0	IO		DEV_OE	DIFFIO_RX_T18p	DIFFOUT_T18p	Low_Speed
E8	8	VREFB8N0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	Low_Speed
B7	8	VREFB8N0	IO	VREFB8N0				Low_Speed
D7	8	VREFB8N0	IO		CONFIG_SEL			Low_Speed

U169	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
A7	8	VREFB8N0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed
E7	8	VREFB8N0	Input_only		nCONFIG			Low_Speed
A6	8	VREFB8N0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed
B6	8	VREFB8N0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	Low_Speed
A4	8	VREFB8N0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	Low_Speed
B5	8	VREFB8N0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed
A3	8	VREFB8N0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	Low_Speed
E6	8	VREFB8N0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	Low_Speed
B3	8	VREFB8N0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	Low_Speed
D6	8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T22n	DIFFOUT_T22n	Low_Speed
B4	8	VREFB8N0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	Low_Speed
C4	8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T24p	DIFFOUT_T24p	Low_Speed
A5	8	VREFB8N0	IO					Low_Speed
C5	8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T24n	DIFFOUT_T24n	Low_Speed
A2	8	VREFB8N0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed
B2	8	VREFB8N0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed
D2			GND					
E2			GND					
N13			GND					
N1			GND					
M6			GND					
L9			GND					
J4			GND					
H12			GND					
G7			GND					
F3			GND					
E11			GND					
D5			GND					
C3			GND					
B8			GND					
A13			GND					
A1			GND					
F2			VCCIO1A					
G3			VCCIO1B					
K3			VCCIO2					
J3			VCCIO2					
L8			VCCIO3					
L7			VCCIO3					

U169	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
L6			VCCIO3					
J11			VCCIO5					
H11			VCCIO5					
G11			VCCIO6					
F11			VCCIO6					
C8			VCCIO8					
C7			VCCIO8					
C6			VCCIO8					
K4			VCCA1					
D10			VCCA2					
D3			VCCA3					
D4			VCCA3					
K9			VCCA4					
H7			VCC_ONE					
G8			VCC_ONE					
G6			VCC_ONE					
F7			VCC_ONE					

U324	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
D4	1A	VREFB1N0	IO			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed
C2	1A	VREFB1N0	IO			DIFFIO_RX_L2n	DIFFOUT_L2n	Low_Speed
E4	1A	VREFB1N0	IO			DIFFIO_RX_L1p	DIFFOUT_L1p	Low_Speed
D2	1A	VREFB1N0	IO			DIFFIO_RX_L2p	DIFFOUT_L2p	Low_Speed
G6	1A	VREFB1N0	IO			DIFFIO_RX_L3n	DIFFOUT_L3n	Low_Speed
B1	1A	VREFB1N0	IO			DIFFIO_RX_L4n	DIFFOUT_L4n	Low_Speed
H6	1A	VREFB1N0	IO			DIFFIO_RX_L3p	DIFFOUT_L3p	Low_Speed
C1	1A	VREFB1N0	IO			DIFFIO_RX_L4p	DIFFOUT_L4p	Low_Speed
F5	1A	VREFB1N0	IO			DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed
D1	1A	VREFB1N0	IO			DIFFIO_RX_L6n	DIFFOUT_L6n	Low_Speed
E5	1A	VREFB1N0	IO			DIFFIO_RX_L5p	DIFFOUT_L5p	Low_Speed
E1	1A	VREFB1N0	IO			DIFFIO_RX_L6p	DIFFOUT_L6p	Low_Speed
G3	1A	VREFB1N0	IO			DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed
F1	1A	VREFB1N0	IO			DIFFIO_RX_L8n	DIFFOUT_L8n	Low_Speed
F2	1A	VREFB1N0	IO			DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed
G1	1A	VREFB1N0	IO			DIFFIO_RX_L8p	DIFFOUT_L8p	Low_Speed
G7	1B	VREFB1N0	IO			DIFFIO_RX_L9n	DIFFOUT_L9n	Low_Speed
H2	1B	VREFB1N0	IO			DIFFIO_RX_L10n	DIFFOUT_L10n	Low_Speed
H7	1B	VREFB1N0	IO		JTAGEN	DIFFIO_RX_L9p	DIFFOUT_L9p	Low_Speed
H1	1B	VREFB1N0	IO			DIFFIO_RX_L10p	DIFFOUT_L10p	Low_Speed
J7	1B	VREFB1N0	IO		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed
J3	1B	VREFB1N0	IO	VREFB1N0				Low_Speed
J8	1B	VREFB1N0	IO		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed
J4	1B	VREFB1N0	IO					Low_Speed
H3	1B	VREFB1N0	IO		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed
J2	1B	VREFB1N0	IO			DIFFIO_RX_L13n	DIFFOUT_L13n	Low_Speed
H4	1B	VREFB1N0	IO		TDO	DIFFIO_RX_L12p	DIFFOUT_L12p	Low_Speed
J1	1B	VREFB1N0	IO			DIFFIO_RX_L13p	DIFFOUT_L13p	Low_Speed
J6	1B	VREFB1N0	IO			DIFFIO_RX_L14n	DIFFOUT_L14n	Low_Speed
K2	1B	VREFB1N0	IO			DIFFIO_RX_L15n	DIFFOUT_L15n	Low_Speed
K7	1B	VREFB1N0	IO			DIFFIO_RX_L14p	DIFFOUT_L14p	Low_Speed
K1	1B	VREFB1N0	IO			DIFFIO_RX_L15p	DIFFOUT_L15p	Low_Speed
K4	1B	VREFB1N0	IO			DIFFIO_RX_L16n	DIFFOUT_L16n	Low_Speed
L1	1B	VREFB1N0	IO			DIFFIO_RX_L17n	DIFFOUT_L17n	Low_Speed
K3	1B	VREFB1N0	IO			DIFFIO_RX_L16p	DIFFOUT_L16p	Low_Speed
L2	1B	VREFB1N0	IO			DIFFIO_RX_L17p	DIFFOUT_L17p	Low_Speed
L3	2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed
M1	2	VREFB2N0	IO			DIFFIO_RX_L19n	DIFFOUT_L19n	High_Speed

U324	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
M3	2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	High_Speed
M2	2	VREFB2N0	IO			DIFFIO_RX_L19p	DIFFOUT_L19p	High_Speed
K8	2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L20n	DIFFOUT_L20n	High_Speed
N1	2	VREFB2N0	IO			DIFFIO_RX_L21n	DIFFOUT_L21n	High_Speed
L8	2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L20p	DIFFOUT_L20p	High_Speed
P1	2	VREFB2N0	IO			DIFFIO_RX_L21p	DIFFOUT_L21p	High_Speed
M4	2	VREFB2N0	IO	DPCLK0		DIFFIO_RX_L22n	DIFFOUT_L22n	High_Speed
R1	2	VREFB2N0	IO	VREFB2N0				High_Speed
N3	2	VREFB2N0	IO	DPCLK1		DIFFIO_RX_L22p	DIFFOUT_L22p	High_Speed
R2	2	VREFB2N0	IO					High_Speed
R3	2	VREFB2N0	IO			DIFFIO_RX_L23n	DIFFOUT_L23n	High_Speed
P2	2	VREFB2N0	IO			DIFFIO_RX_L24n	DIFFOUT_L24n	High_Speed
T3	2	VREFB2N0	IO			DIFFIO_RX_L23p	DIFFOUT_L23p	High_Speed
P3	2	VREFB2N0	IO			DIFFIO_RX_L24p	DIFFOUT_L24p	High_Speed
L7	2	VREFB2N0	IO			DIFFIO_RX_L25n	DIFFOUT_L25n	High_Speed
T1	2	VREFB2N0	IO			DIFFIO_RX_L26n	DIFFOUT_L26n	High_Speed
M7	2	VREFB2N0	IO			DIFFIO_RX_L25p	DIFFOUT_L25p	High_Speed
T2	2	VREFB2N0	IO			DIFFIO_RX_L26p	DIFFOUT_L26p	High_Speed
N4	2	VREFB2N0	IO	PLL_L_CLKOUTn		DIFFIO_RX_L27n	DIFFOUT_L27n	High_Speed
U1	2	VREFB2N0	IO			DIFFIO_RX_L28n	DIFFOUT_L28n	High_Speed
P4	2	VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO_RX_L27p	DIFFOUT_L27p	High_Speed
U2	2	VREFB2N0	IO			DIFFIO_RX_L28p	DIFFOUT_L28p	High_Speed
R4	3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed
U3	3	VREFB3N0	IO			DIFFIO_RX_B2n	DIFFOUT_B2n	High_Speed
T4	3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed
V2	3	VREFB3N0	IO			DIFFIO_RX_B2p	DIFFOUT_B2p	High_Speed
P6	3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed
V3	3	VREFB3N0	IO			DIFFIO_RX_B4n	DIFFOUT_B4n	High_Speed
P5	3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed
V4	3	VREFB3N0	IO			DIFFIO_RX_B4p	DIFFOUT_B4p	High_Speed
R5	3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed
U5	3	VREFB3N0	IO			DIFFIO_RX_B6n	DIFFOUT_B6n	High_Speed
R6	3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed
V5	3	VREFB3N0	IO			DIFFIO_RX_B6p	DIFFOUT_B6p	High_Speed
T5	3	VREFB3N0	IO			DIFFIO_TX_RX_B7n	DIFFOUT_B7n	High_Speed
T7	3	VREFB3N0	IO			DIFFIO_RX_B8n	DIFFOUT_B8n	High_Speed
T6	3	VREFB3N0	IO			DIFFIO_TX_RX_B7p	DIFFOUT_B7p	High_Speed
T8	3	VREFB3N0	IO			DIFFIO_RX_B8p	DIFFOUT_B8p	High_Speed

U324	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
N7	3	VREFB3N0	IO			DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High_Speed
U6	3	VREFB3N0	IO	VREFB3N0				High_Speed
N8	3	VREFB3N0	IO			DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High_Speed
V6	3	VREFB3N0	IO					High_Speed
R8	3	VREFB3N0	IO			DIFFIO_TX_RX_B10n	DIFFOUT_B10n	High_Speed
U7	3	VREFB3N0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	High_Speed
R9	3	VREFB3N0	IO			DIFFIO_TX_RX_B10p	DIFFOUT_B10p	High_Speed
V7	3	VREFB3N0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	High_Speed
V9	3	VREFB3N0	IO			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	High_Speed
U8	3	VREFB3N0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	High_Speed
U9	3	VREFB3N0	IO			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High_Speed
V8	3	VREFB3N0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	High_Speed
M8	3	VREFB3N0	IO			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High_Speed
V10	3	VREFB3N0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	High_Speed
M9	3	VREFB3N0	IO			DIFFIO_TX_RX_B14p	DIFFOUT_B14p	High_Speed
V11	3	VREFB3N0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	High_Speed
T9	3	VREFB3N0	IO			DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High_Speed
V12	3	VREFB3N0	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	High_Speed
T10	3	VREFB3N0	IO			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed
U11	3	VREFB3N0	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	High_Speed
P10	4	VREFB4N0	IO			DIFFIO_TX_RX_B18n	DIFFOUT_B18n	High_Speed
U12	4	VREFB4N0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	High_Speed
N11	4	VREFB4N0	IO			DIFFIO_TX_RX_B18p	DIFFOUT_B18p	High_Speed
U13	4	VREFB4N0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	High_Speed
M10	4	VREFB4N0	IO			DIFFIO_TX_RX_B20n	DIFFOUT_B20n	High_Speed
T11	4	VREFB4N0	IO	VREFB4N0				High_Speed
L10	4	VREFB4N0	IO			DIFFIO_TX_RX_B20p	DIFFOUT_B20p	High_Speed
T12	4	VREFB4N0	IO					High_Speed
R10	4	VREFB4N0	IO			DIFFIO_TX_RX_B21n	DIFFOUT_B21n	High_Speed
V13	4	VREFB4N0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	High_Speed
R11	4	VREFB4N0	IO			DIFFIO_TX_RX_B21p	DIFFOUT_B21p	High_Speed
V14	4	VREFB4N0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	High_Speed
R12	4	VREFB4N0	IO			DIFFIO_TX_RX_B23n	DIFFOUT_B23n	High_Speed
T13	4	VREFB4N0	IO			DIFFIO_RX_B24n	DIFFOUT_B24n	High_Speed
R13	4	VREFB4N0	IO			DIFFIO_TX_RX_B23p	DIFFOUT_B23p	High_Speed
T14	4	VREFB4N0	IO			DIFFIO_RX_B24p	DIFFOUT_B24p	High_Speed
R14	4	VREFB4N0	IO			DIFFIO_TX_RX_B25n	DIFFOUT_B25n	High_Speed
V15	4	VREFB4N0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	High_Speed

U324	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
T15	4	VREFB4N0	IO			DIFFIO_TX_RX_B25p	DIFFOUT_B25p	High_Speed
U15	4	VREFB4N0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	High_Speed
U16	4	VREFB4N0	IO			DIFFIO_TX_RX_B27n	DIFFOUT_B27n	High_Speed
V16	4	VREFB4N0	IO			DIFFIO_RX_B28n	DIFFOUT_B28n	High_Speed
U17	4	VREFB4N0	IO			DIFFIO_TX_RX_B27p	DIFFOUT_B27p	High_Speed
V17	4	VREFB4N0	IO			DIFFIO_RX_B28p	DIFFOUT_B28p	High_Speed
N14	5	VREFB5N0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed
T16	5	VREFB5N0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed
P14	5	VREFB5N0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed
R16	5	VREFB5N0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	High_Speed
M12	5	VREFB5N0	IO			DIFFIO_RX_R3p	DIFFOUT_R3p	High_Speed
U18	5	VREFB5N0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	High_Speed
M11	5	VREFB5N0	IO			DIFFIO_RX_R3n	DIFFOUT_R3n	High_Speed
T18	5	VREFB5N0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	High_Speed
N15	5	VREFB5N0	IO			DIFFIO_RX_R5p	DIFFOUT_R5p	High_Speed
N16	5	VREFB5N0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	High_Speed
M15	5	VREFB5N0	IO			DIFFIO_RX_R5n	DIFFOUT_R5n	High_Speed
M16	5	VREFB5N0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	High_Speed
R15	5	VREFB5N0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	High_Speed
P16	5	VREFB5N0	IO					High_Speed
P15	5	VREFB5N0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed
P17	5	VREFB5N0	IO	VREFB5N0				High_Speed
L12	5	VREFB5N0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	High_Speed
T17	5	VREFB5N0	IO			DIFFIO_RX_R9p	DIFFOUT_R9p	High_Speed
L11	5	VREFB5N0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	High_Speed
R17	5	VREFB5N0	IO			DIFFIO_RX_R9n	DIFFOUT_R9n	High_Speed
L15	5	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed
L16	5	VREFB5N0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	High_Speed
K15	5	VREFB5N0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed
K16	5	VREFB5N0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	High_Speed
R18	5	VREFB5N0	IO			DIFFIO_RX_R12p	DIFFOUT_R12p	High_Speed
N18	5	VREFB5N0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	High_Speed
P18	5	VREFB5N0	IO			DIFFIO_RX_R12n	DIFFOUT_R12n	High_Speed
M18	5	VREFB5N0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	High_Speed
K12	6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R14p	DIFFOUT_R14p	High_Speed
M17	6	VREFB6N0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	High_Speed
K11	6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R14n	DIFFOUT_R14n	High_Speed
L18	6	VREFB6N0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	High_Speed

U324	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
L17	6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed
K18	6	VREFB6N0	IO			DIFFIO_RX_R17p	DIFFOUT_R17p	High_Speed
K17	6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R16n	DIFFOUT_R16n	High_Speed
J18	6	VREFB6N0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	High_Speed
H18	6	VREFB6N0	IO			DIFFIO_RX_R18p	DIFFOUT_R18p	High_Speed
H17	6	VREFB6N0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	High_Speed
G18	6	VREFB6N0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n	High_Speed
G17	6	VREFB6N0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	High_Speed
J11	6	VREFB6N0	IO			DIFFIO_RX_R20p	DIFFOUT_R20p	High_Speed
J12	6	VREFB6N0	IO			DIFFIO_RX_R20n	DIFFOUT_R20n	High_Speed
J15	6	VREFB6N0	IO			DIFFIO_RX_R22p	DIFFOUT_R22p	High_Speed
J16	6	VREFB6N0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	High_Speed
H15	6	VREFB6N0	IO			DIFFIO_RX_R22n	DIFFOUT_R22n	High_Speed
H16	6	VREFB6N0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	High_Speed
H11	6	VREFB6N0	IO	DPCLK3		DIFFIO_RX_R26p	DIFFOUT_R26p	High_Speed
F18	6	VREFB6N0	IO	VREFB6N0				High_Speed
H12	6	VREFB6N0	IO	DPCLK2		DIFFIO_RX_R26n	DIFFOUT_R26n	High_Speed
E18	6	VREFB6N0	IO					High_Speed
F15	6	VREFB6N0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	High_Speed
G16	6	VREFB6N0	IO			DIFFIO_RX_R28p	DIFFOUT_R28p	High_Speed
G15	6	VREFB6N0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	High_Speed
F16	6	VREFB6N0	IO			DIFFIO_RX_R28n	DIFFOUT_R28n	High_Speed
E16	6	VREFB6N0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	High_Speed
D18	6	VREFB6N0	IO			DIFFIO_RX_R30p	DIFFOUT_R30p	High_Speed
D16	6	VREFB6N0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	High_Speed
E17	6	VREFB6N0	IO			DIFFIO_RX_R30n	DIFFOUT_R30n	High_Speed
G11	6	VREFB6N0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	High_Speed
C18	6	VREFB6N0	IO			DIFFIO_RX_R32p	DIFFOUT_R32p	High_Speed
G12	6	VREFB6N0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	High_Speed
B18	6	VREFB6N0	IO			DIFFIO_RX_R32n	DIFFOUT_R32n	High_Speed
E15	6	VREFB6N0	IO			DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed
D17	6	VREFB6N0	IO			DIFFIO_RX_R34p	DIFFOUT_R34p	High_Speed
D15	6	VREFB6N0	IO			DIFFIO_RX_R33n	DIFFOUT_R33n	High_Speed
C17	6	VREFB6N0	IO			DIFFIO_RX_R34n	DIFFOUT_R34n	High_Speed
E14	7	VREFB7N0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	High_Speed
B17	7	VREFB7N0	IO			DIFFIO_RX_T2p	DIFFOUT_T2p	High_Speed
D14	7	VREFB7N0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	High_Speed
B16	7	VREFB7N0	IO			DIFFIO_RX_T2n	DIFFOUT_T2n	High_Speed

U324	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
D12	7	VREFB7N0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	High_Speed
A17	7	VREFB7N0	IO					High_Speed
D13	7	VREFB7N0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	High_Speed
A16	7	VREFB7N0	IO	VREFB7N0				High_Speed
C16	7	VREFB7N0	IO			DIFFIO_RX_T4p	DIFFOUT_T4p	High_Speed
A15	7	VREFB7N0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	High_Speed
C15	7	VREFB7N0	IO			DIFFIO_RX_T4n	DIFFOUT_T4n	High_Speed
A14	7	VREFB7N0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	High_Speed
C14	7	VREFB7N0	IO			DIFFIO_RX_T6p	DIFFOUT_T6p	High_Speed
B14	7	VREFB7N0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	High_Speed
C13	7	VREFB7N0	IO			DIFFIO_RX_T6n	DIFFOUT_T6n	High_Speed
B13	7	VREFB7N0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	High_Speed
F11	7	VREFB7N0	IO			DIFFIO_RX_T8p	DIFFOUT_T8p	High_Speed
C12	7	VREFB7N0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	High_Speed
F12	7	VREFB7N0	IO			DIFFIO_RX_T8n	DIFFOUT_T8n	High_Speed
B12	7	VREFB7N0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	High_Speed
C11	7	VREFB7N0	IO			DIFFIO_RX_T10p	DIFFOUT_T10p	High_Speed
A13	7	VREFB7N0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	High_Speed
B11	7	VREFB7N0	IO			DIFFIO_RX_T10n	DIFFOUT_T10n	High_Speed
A12	7	VREFB7N0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	High_Speed
D10	8	VREFB8N0	IO			DIFFIO_RX_T12p	DIFFOUT_T12p	Low_Speed
A11	8	VREFB8N0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	Low_Speed
D9	8	VREFB8N0	IO			DIFFIO_RX_T12n	DIFFOUT_T12n	Low_Speed
A10	8	VREFB8N0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	Low_Speed
F10	8	VREFB8N0	IO			DIFFIO_RX_T14p	DIFFOUT_T14p	Low_Speed
A9	8	VREFB8N0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	Low_Speed
G10	8	VREFB8N0	IO			DIFFIO_RX_T14n	DIFFOUT_T14n	Low_Speed
A8	8	VREFB8N0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	Low_Speed
B9	8	VREFB8N0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	Low_Speed
C10	8	VREFB8N0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	Low_Speed
B8	8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed
C9	8	VREFB8N0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	Low_Speed
D8	8	VREFB8N0	IO		DEV_OE	DIFFIO_RX_T18p	DIFFOUT_T18p	Low_Speed
A7	8	VREFB8N0	IO					Low_Speed
D7	8	VREFB8N0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	Low_Speed
B7	8	VREFB8N0	IO	VREFB8N0				Low_Speed
G9	8	VREFB8N0	IO		CONFIG_SEL			Low_Speed
A6	8	VREFB8N0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed

U324	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
H9	8	VREFB8N0	Input_only		nCONFIG			Low_Speed
A5	8	VREFB8N0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed
C6	8	VREFB8N0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	Low_Speed
C8	8	VREFB8N0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	Low_Speed
B5	8	VREFB8N0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed
C7	8	VREFB8N0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	Low_Speed
C5	8	VREFB8N0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	Low_Speed
A4	8	VREFB8N0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	Low_Speed
C4	8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T22n	DIFFOUT_T22n	Low_Speed
B4	8	VREFB8N0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	Low_Speed
G8	8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T24p	DIFFOUT_T24p	Low_Speed
A3	8	VREFB8N0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	Low_Speed
H8	8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T24n	DIFFOUT_T24n	Low_Speed
B3	8	VREFB8N0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	Low_Speed
D6	8	VREFB8N0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed
A2	8	VREFB8N0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	Low_Speed
D5	8	VREFB8N0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed
B2	8	VREFB8N0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	Low_Speed
E2			GND					
E3			GND					
V18			GND					
V1			GND					
U4			GND					
U14			GND					
U10			GND					
R7			GND					
N5			GND					
N2			GND					
N17			GND					
N12			GND					
N10			GND					
M14			GND					
L4			GND					
K9			GND					
K6			GND					
K13			GND					
J17			GND					
J10			GND					

U324	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
H14			GND					
G4			GND					
G2			GND					
F8			GND					
F17			GND					
E6			GND					
E13			GND					
E10			GND					
D3			GND					
B6			GND					
B15			GND					
B10			GND					
A18			GND					
A1			GND					
H5			VCCIO1A					
G5			VCCIO1A					
K5			VCCIO1B					
J5			VCCIO1B					
M5			VCCIO2					
L6			VCCIO2					
L5			VCCIO2					
P9			VCCIO3					
P8			VCCIO3					
P7			VCCIO3					
N9			VCCIO3					
P12			VCCIO4					
P11			VCCIO4					
M13			VCCIO5					
L14			VCCIO5					
L13			VCCIO5					
K14			VCCIO5					
J14			VCCIO6					
J13			VCCIO6					
H13			VCCIO6					
G14			VCCIO6					
G13			VCCIO6					
E12			VCCIO7					
E11			VCCIO7					

U324	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance
D11			VCCIO7					
F9			VCCIO8					
E9			VCCIO8					
E8			VCCIO8					
E7			VCCIO8					
N13			NC					
F7			NC					
M6			VCCA1					
F14			VCCA2					
F3			VCCA3					
F6			VCCA3					
F4			VCCA3					
P13			VCCA4					
L9			VCC_ONE					
K10			VCC_ONE					
J9			VCC_ONE					
H10			VCC_ONE					
N6			VCC_ONE					
F13			VCC_ONE					
C3			VCC_ONE					

Date	Version	Revision History for E144 Package
September 2014	2014-09-22	Initial release.
December 2014	2014-12-15	-Updated the BOOT_SEL pin name to CONFIG_SEL pin name. -Removed differential pair pins for non-differential function support.
May 2015	2015-05-08	Added note (2) to pin list E144.
December 2016	2016-12-23	Removed I/O performance for single-ended pins.
February 2017	2017-02-21	Rebranded as Intel.
December 2017	2017-12-15	Added pin list U324.
February 2025	2025-02-18	Updated I/O performance information for single-ended I/O.

Date	Version	Revision History for M153 Package
September 2014	2014-09-22	Initial release.
December 2014	2014-12-15	-Updated the BOOT_SEL pin name to CONFIG_SEL pin name. -Removed differential pair pins for non-differential function support.
December 2016	2016-12-23	Removed I/O performance for single-ended pins.
February 2017	2017-02-21	Rebranded as Intel.
February 2025	2025-02-18	Updated I/O performance information for single-ended I/O.

Date	Version	Revision History for U169 Package
September 2014	2014-09-22	Initial release.
December 2014	2014-12-15	-Updated the BOOT_SEL pin name to CONFIG_SEL pin name. -Removed differential pair pins for non-differential function support.
December 2016	2016-12-23	Removed I/O performance for single-ended pins.
February 2017	2017-02-21	Rebranded as Intel.
February 2025	2025-02-18	Updated I/O performance information for single-ended I/O.

Date	Version	Revision History for U324 Package
December 2017	2017-12-15	Initial release.
February 2025	2025-02-18	Updated I/O performance information for single-ended I/O.

(1) For more information about pin definition and pin connection guidelines, refer to the MAX® 10 FPGA Device Family Pin Connection Guidelines

(2) To obtain a Comma Delimited (CSV) file using Excel - From the active tab, select "Save As" in the FILE menu and then select CSV (*.csv) format and SAVE. CSV File may be viewed in a TEXT editor or in Excel.