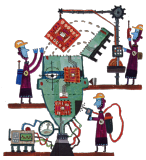

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Dr. Committee Member 2
Prof. Dr. Committee Member 3

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Abstract

Acknowledgements

Contents

Nomenclature

Symbols

Acronyms and Abbreviations

ADC Analog to Digital Converter

AdExp-I&F Adaptive-Exponential Integrate and Fire

ADM Asynchronous Delta Modulator

AER Address-Event Representation

AEX AER EXtension board

AE Address-Event

AFM Atomic Force Microscope

AGC Automatic Gain Control

AI Artificial Intelligence

AMDA AER Motherboard with D/A converters

ANN Artificial Neural Network

API Application Programming Interface

APMOM Alternate Polarity Metal On Metal

ARM Advanced RISC Machine

ASIC Application Specific Integrated Circuit

AdExp-IF Adaptive Exponential Integrate-and-Fire

BMC Bienenstock-Cooper-Munro

BD Bundled Data

BEOL Back-end of Line

BG Bias Generator

BMI Brain-Machince Interface

BTB band-to-band tunnelling

CAD Computer Aided Design

CAM Content Addressable Memory

CAVIAR Convolution AER Vision Architecture for Real-Time

CA Cortical Automaton

CCN Cooperative and Competitive Network

CDR Clock-Data Recovery

CFC Current to Frequency Converter

CHP Communicating Hardware Processes

CMIM Metal-insulator-metal Capacitor

CML Current Mode Logic

CMOL Hybrid CMOS nanoelectronic circuits

CMOS Complementary Metal-Oxide-Semiconductor

CNN Convolutional Neural Network

COTS Commercial Off-The-Shelf

CPG Central Pattern Generator

CPLD Complex Programmable Logic Device

CPU Central Processing Unit

CSM Cortical State Machine

CSP Constraint Satisfaction Problem

CTXCTL CortexControl

CV Coefficient of Variation

DAC Digital to Analog Converter

DAS Dynamic Auditory Sensor

DAVIS Dynamic and Active Pixel Vision Sensor

DBN Deep Belief Network

DFA Deterministic Finite Automaton

DIBL drain-induced-barrier-lowering

DI delay insensitive

DMA Direct Memory Access

DNF Dynamic Neural Field

DNN Deep Neural Network

DOF Degrees of Freedom

DPE Dynamic Parameter Estimation

DPI Differential Pair Integrator

DRAM Dynamic Random Access Memory

DR-RZ Dual-Rail Return-to-Zero

DR Dual Rail

DSP Digital Signal Processor

DVS Dynamic Vision Sensor

DYNAP Dynamic Neuromorphic Asynchronous Processor

EBL Electron Beam Lithography

EDVAC Electronic Discrete Variable Automatic Computer

EEG electroencephalography

EIN Excitatory-Inhibitory Network

EM Expectation Maximization

EPSC Excitatory Post-Synaptic Current

EPSP Excitatory Post-Synaptic Potential

EZ Epileptogenic Zone

FDSOI Fully-Depleted Silicon on Insulator

FET Field-Effect Transistor

FFT Fast Fourier Transform

F-I Frequency-Current

FNN Feed-forward Neural Network

FPGA Field Programmable Gate Array

FR Fast Ripple

FSA Finite State Automaton

FSM Finite State Machine

GIDL gate-induced-drain-leakage

GOPS Giga-Operations per Second

GPU Graphical Processing Unit

GT Ground Truth

GUI Graphical User Interface

HAL Hardware Abstraction Layer

HFO High Frequency Oscillation

H&H Hodgkin & Huxley

HMM Hidden Markov Model

HRS High-Resistive State

HR Human Readable

HSE Handshaking Expansion

HW Hardware

ICT Information and Communication Technology

IC Integrated Circuit

iEEG intracranial electroencephalography

IF2DWTA Integrate & Fire 2–Dimensional WTA

IFSLWTA Integrate & Fire Stop Learning WTA

I&F Integrate-and-Fire

IMU Inertial Measurement Unit

INCF International Neuroinformatics Coordinating Facility

INI Institute of Neuroinformatics

I/O Input/Output

IPSC Inhibitory Post-Synaptic Current

IPSP Inhibitory Post-Synaptic Potential

IP Intellectual Property

ISI Inter-Spike Interval

IoT Internet of Things

JFLAP Java - Formal Languages and Automata Package

LEDR Level-Encoded Dual-Rail

LFP Local Field Potential

LI&F Leak Integrate-and-Fire

LLC Low Leakage Cell

LNA Low-Noise Amplifier

LPF Low Pass Filter

LRS Low-Resistive State

LSM Liquid State Machine

LTD Long Term Depression

LTI Linear Time-Invariant

LTP Long Term Potentiation

LTU Linear Threshold Unit

LUT Look-Up Table

LVDS Low Voltage Differential Signaling

MCMC Markov-Chain Monte Carlo

MEMS Micro Electro Mechanical System

MFR Mean Firing Rate

MIM Metal Insulator Metal

ML Machine Learning

MLP Multilayer Perceptron

MOSCAP Metal Oxide Semiconductor Capacitor

MOSFET Metal Oxide Semiconductor Field-Effect Transistor

MOS Metal Oxide Semiconductor

MRI Magnetic Resonance Imaging

NCS Neuromorphic Cognitive Systems

NDFSM Non-deterministic Finite State Machine

ND Noise-Driven

NEF Neural Engineering Framework

NHML Neuromorphic Hardware Mark-up Language

NIL Nano-Imprint Lithography

NMDA N-Methyl-D-Aspartate

NE Neuromorphic Engineering

NN Neural Network

NoC Network-on-Chip

NRZ Non-Return-to-Zero

NSM Neural State Machine

OR Operating Room

OTA Operational Transconductance Amplifier

PCB Printed Circuit Board

PCHB Pre-Charge Half-Buffer

PCM Phase Change Memory

PE Phase Encoding

PFA Probabilistic Finite Automaton

PFC prefrontal cortex

PFM Pulse Frequency Modulation

PR Production Rule

PSC Post-Synaptic Current

PSP Post-Synaptic Potential

PSTH Peri-Stimulus Time Histogram

QDI Quasi Delay Insensitive

RAM Random Access Memory

RA Resected Area

RDF random dopant fluctuation

ReLu Rectified Linear Unit

RLS Recursive Least-Squares

RMSE Root Mean Squared-Error

RMS Root Mean Squared

RNN Recurrent Neural Networks

ROLLS Reconfigurable On-Line Learning Spiking

R-RAM Resistive Random Access Memory

R Ripples

SAC Selective Attention Chip

SAT Boolean Satisfiability Problem

SCX Silicon CorteX

SD Signal-Driven

SEM Spike-based Expectation Maximization

SLAM Simultaneous Localization and Mapping

SNN Spiking Neural Network

SNR Signal to Noise Ratio

SOC System-On-Chip

SOI Silicon on Insulator

SOZ Seizure Onset Zone

SP Separation Property

SRAM Static Random Access Memory

STDP Spike-Timing Dependent Plasticity

STD Short-Term Depression

STP Short-Term Plasticity

STT-MRAM Spin-Transfer Torque Magnetic Random Access Memory

STT Spin-Transfer Torque

SW Software

TCAM Ternary Content-Addressable Memory

TFT Thin Film Transistor

TLE Temporal Lobe Epilepsy

USB Universal Serial Bus

VHDL VHSIC Hardware Description Language

VLSI Very Large Scale Integration

VOR Vestibulo-Ocular Reflex

WCST Wisconsin Card Sorting Test

WTA Winner-Take-All

XML eXtensible Mark-up Language

DIVMOD3 divisibility of a number by three

hWTA hard Winner-Take-All

sWTA soft Winner-Take-All

1. Introduction

1.1. Section

subSection

1.2. Thesis Outline

Add a sentence with a random citation [1].

A. Appendix Title

B. Supplementary Material

Bibliography

[1] The address-event representation communication protocol AER 0.02. Caltech internal memo, February 1993.

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