Computer Architecture Lab 1
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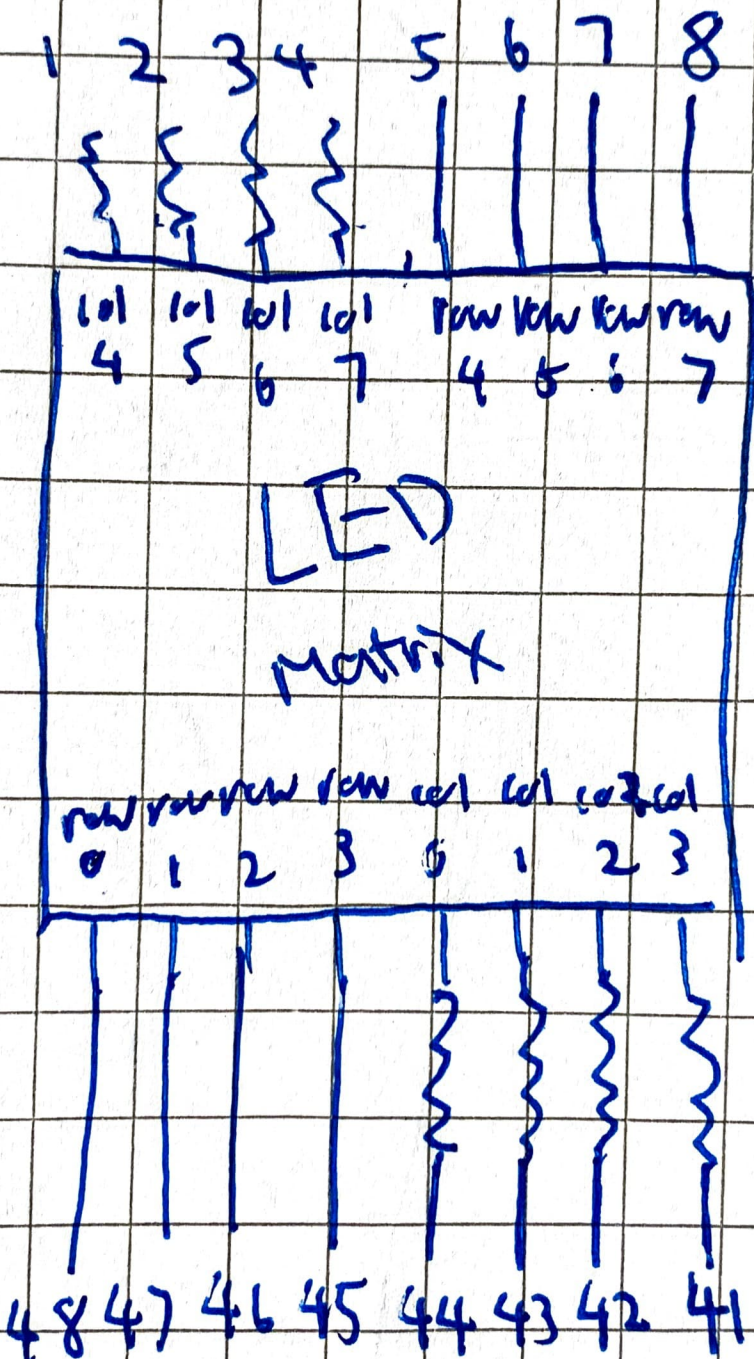
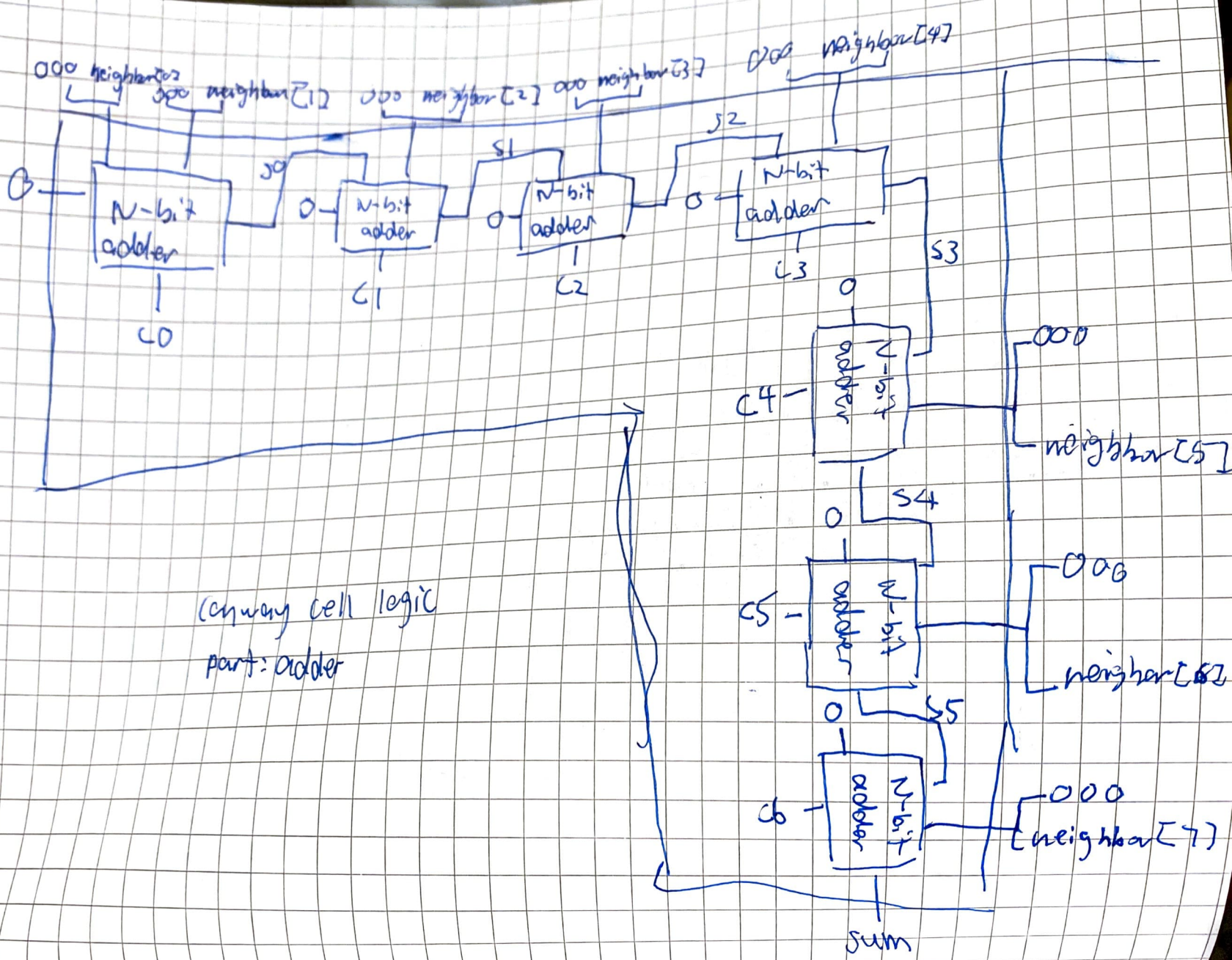
In this lab, we implemented Conway's Game of Life on an 8 x 8 LED array using an FPGA. To start off, we drew out circuit schematics for the hardware we planned to implement: a 3:8 decoder, a 1 bit adder, an n bit adder, logic for a conway cell, and wiring for the LED matrix. We then implemented this logic in SystemVerilog and flashed it to the FPGA to implement the Game of Life. The lab was initially very challenging, as none of us were experienced with SystemVerilog. However, once we became more acquainted with the software the lab became a lot less overwhelming.



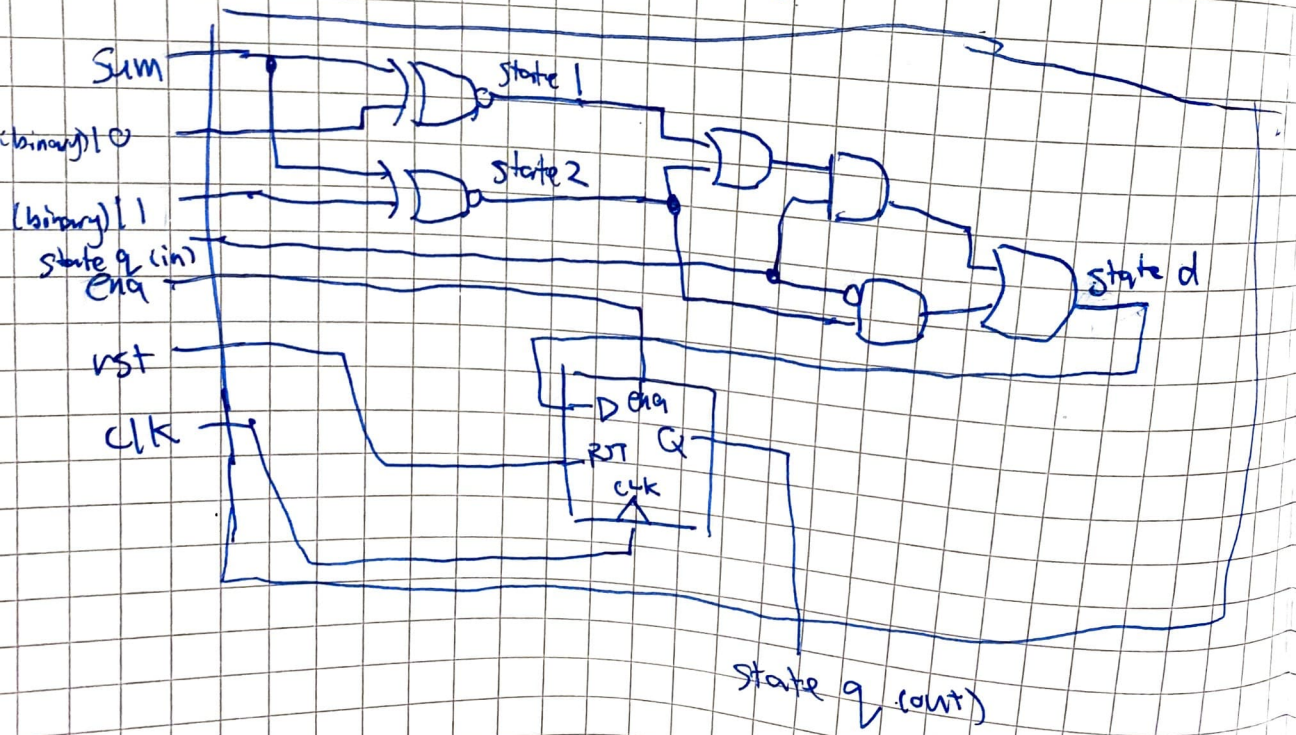
Ω = 220Ω resistors.

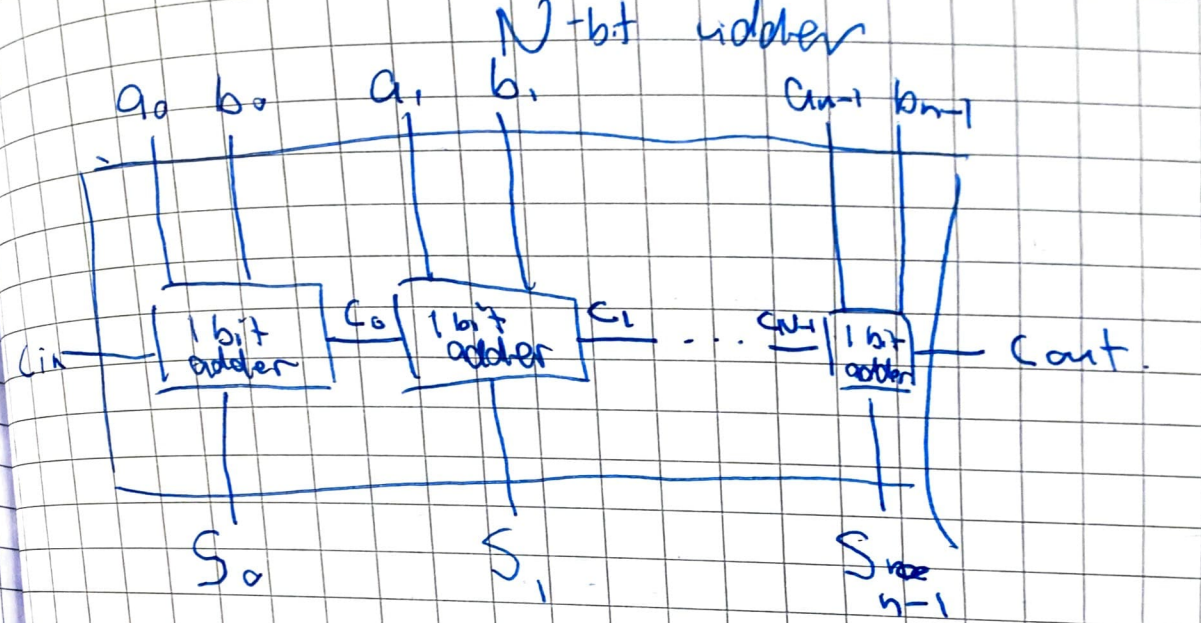


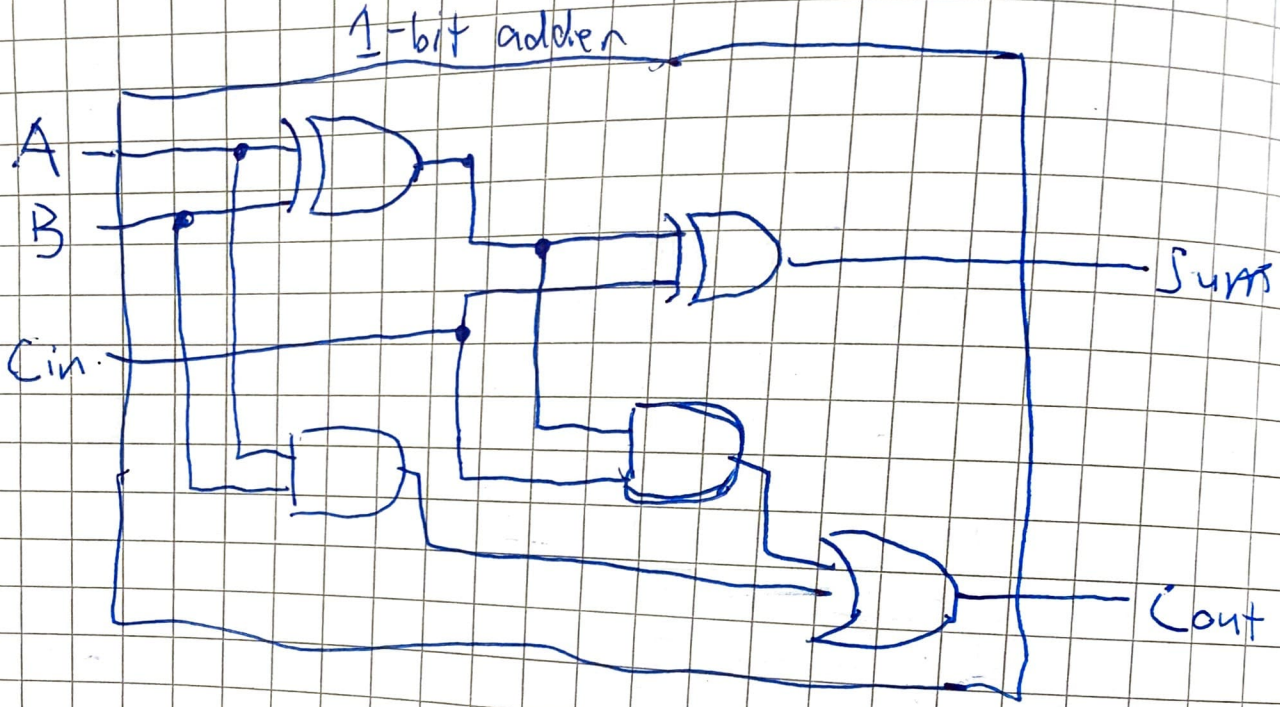
conway cell logic

part: adder

Conway Cell Logic




N-bit adder
a_0 b_0
a_1 b_1
a_{n-1} b_{n-1}
1 bit adder
1 bit adder
1 bit adder
C_{in}
C_0
C_1
C_{n-1}
C_{out}
S_0
S_1
S_{n-1}


1-bit adder
A
B
Cin
Sum
Cout

3 to 8 decoder.