PROBLEMS

1.1   What would happen to the transfer function analysis results for the circuit in Fig. 1.11 if a capacitor were added in series with R1? Why? What about adding a capacitor in series with R2?

1.2   Resimulate the op-amp circuit in Fig. 1.15 if the open-loop gain is increased to 100 million while, at the same time, the resistor used in the ideal op-amp is increased to 100 Ω. Does the output voltage move closer to the ideal value?

1.3   Simulate the op-amp circuit in Fig. 1.15 if Vin is varied from −1 to +1V. Verify, with hand calculations, that the simulation output is correct.

1.4   Regenerate IV curves, as seen in Fig. 1.18, for a PNP transistor.

1.5   Resimulate the circuit in Fig. 1.20 if the sinewave doesn't start to oscillate until 1 μs after the simulation starts.

1.6   At what frequency does the output voltage, in Fig. 1.21, become half of the input voltage? Verify your answer with SPICE

1.7   Determine the output of the circuit seen in Fig. 1.22 if a 1k resistor is added from the output of the circuit to ground. Verify your hand calculations using SPICE.

1.8   Using an AC analysis verify the time domain results seen in Fig. 1.22.

1.9   If the capacitor in Fig. 1.24 is increased to 1 μF simulate, similar to Fig. 1.26 but with a longer time scale, the step response of the circuit. Compare the simulation results to the hand-calculated values using Eqs. (1.10) and (1.11).

1.10   Using a PWL source (instead of a pulse source), regenerate the simulation data seen in Fig. 1.26.

1.11   Using the values seen in Fig. 1.32, for the inductor and capacitor determine the Q of a series resonant LC tank with a resistor value of 10 ohms. Note that the resistor is in series with the LC and that an input voltage source should be used (the voltage across the LC tank goes to zero at resonance.)

1.12   Suppose the input voltage of the integrator in Fig. 1.34 is zero and that the op-amp has a 10 mV input-referred offset voltage. If the input-referred offset voltage is modeled using a 10 mV voltage source in series with the non-inverting (+) op-amp input then estimate the output voltage of the op-amp in the time-domain. Assume that at $t = 0$ $V_{out} = 0$. Verify your answer with SPICE.

ADDITIONAL READING

[1]   Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Second Edition, Cambridge University Press, 2010. ISBN 978-0521832946

[2]   S. A. Campbell, *Fabrication Engineering at the Micro- and Nanoscale*, 3rd ed, Oxford University Press, 2008. ISBN 978-0195320176

[3]   M. J. Madou, *Fundamentals of Microfabrication: The Science of Miniaturization*, 2nd ed., CRC Publisher, 2002. ISBN 978-0849308260

[4]   R. C. Jaeger, *Introduction to Microelectronic Fabrication*, 2nd ed, volume 5 of the Modular Series on Solid State Devices, Prentice-Hall Publishers, 2002. ISBN 0-20-144494-1

[5]   J. D. Plummer, M. D. Deal, and P. B. Griffin, *Silicon VLSI Technology*, *Fundamentals, Practice, and Modeling*, Prentice-Hall Publishers, 2000. ISBN 978-0130850379

PROBLEMS

2.1   For the layout seen in Fig. 2.27, sketch the cross-sectional views at the places indicated. Is there a parasitic pn junction in the layout? If so, where? Is there a parasitic bipolar transistor? If so, where?
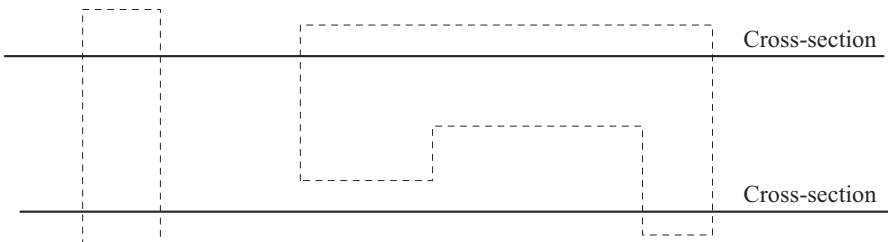

Figure 2.27   Layout used in problem 2.1.

2.2   Sketch (or use a layout tool) the layout of an n-well box that measures 100 by 10. If the scale factor is 50 nm, what is the actual size of the box after fabrication? What is the area before and after scaling? Neglect lateral diffusion or any other fabrication imperfections.

2.3   Lay out a nominally 250 kΩ resistor using the n-well in a serpentine pattern similar to what's seen in Fig. 2.28. Assume that the maximum length of a segment is 100 and the sheet resistance is 2 kΩ/square. Design rule check the finished resistor. If the scale factor in the layout is 50 nm, estimate the fabricated size of the resistor.

2.4   If the fabricated n-well depth, t, is 1 μm, then what are the minimum, typical, and maximum values of the n-well resistivity, ρ? Assume that the measured sheet resistances (minimum, typical, and maximum) are 1.6, 2.0, and 2.2 kΩ/square?

Figure 2.28 Layout of an n-well resistor using a serpentine pattern.

2.5 Normally, the scale current of a pn junction is specified in terms of a scale current density, J_s (A/m²), and the width and length of a junction (i.e., $I_s = J_s \cdot L \cdot W \cdot scale^2$ neglecting the sidewall component). Estimate the scale current for the diode of Ex. 2.3 if $J_s = 10^{-8}$ A/m².

2.6 Repeat problem 2.5, including the sidewall component ($I_s = J_s \cdot L \cdot W \cdot scale^2 + J_s \cdot (2L+2W) \cdot scale \cdot depth$).

2.7 Using the diode of Ex. 2.3 in the circuit of Fig. 2.29, estimate the frequency of the input signal when the AC component of v_{out} is 707 µV (i.e., estimate the 3 dB frequency of the $|v_{out}/v_{in}|$).

Figure 2.29 Treating the diode as a capacitor. See Problem 2.7.

2.8 Verify the answer given in problem 2.7 with SPICE.

2.9   Using SPICE, show that a diode can conduct significant current from its cathode to its anode when the diode is forward biased.

2.10   Estimate the delay through a 1 MΩ resistor (10 by 2,000) using the values given in Ex. 2.5. Verify the estimate with SPICE.

2.11   If one end of the resistor in problem 2.10 is tied to +1 V and the other end is tied to the substrate that is tied to ground, estimate the depletion capacitance (F/m^2) between the n-well and the substrate at the beginning, the middle, and the end of the resistor. Assume that the resistance does not vary with position along the resistor and that the scale factor is 50 nm, $C_{j0} = 25$ aF for a 10 by 10 square, m = 0.5, and $V_{bi} = 1$.

2.12   The diode reverse breakdown current, that is, the current that flows when $|V_D| <$ BV (breakdown voltage), is modeled in SPICE by

$$I_D = IBV \cdot e^{-(V_D + BV)/V_T}$$

Assuming that 10 μA of current flows when the junction starts to break down at 10 V, simulate, using a SPICE DC sweep, the reverse breakdown characteristics of the diode. (The breakdown voltage, BV, is a positive number. When the diode starts to break down $-BV = V_D$. For this diode, breakdown occurs when $V_D = -10$ V.)

2.13   Repeat Ex. 2.3 if the n-well/p-substrate diode is 50 square and the acceptor doping concentration is changed to 10^{15} atoms/cm^3.

2.14   Estimate the storage time, that is, the time it takes to remove the stored charge in a diode, when $\tau_T = 5$ ns, $V_F = 5$ V, $V_R = -5$ V, $C_{j0} = 0.5$ pF, and $R = 1$k. Verify the estimate using SPICE.

2.15   Repeat problem 2.14 if the resistor is increased to 10k. Comment on the difference in storage time between using a 1k and a 10k resistor. What dominates the increase the diode's reverse recovery time when using a 10k resistor instead of a 1k resistor?

ADDITIONAL READING

[1]   R. S. Muller, T. I. Kamins, and M. Chan, *Device Electronics for Integrated Circuits*, John Wiley and Sons Publishers, 2002. ISBN 0-471-59398-2

[2]   J. D. Plummer, M. D. Deal, and P. B. Griffin, *Silicon VLSI Technology*, *Fundamentals, Practice, and Modeling*, Prentice-Hall Publishers, 2000. ISBN 0-13-085037-3

PROBLEMS

Unless otherwise indicated, use the data from Table 3.1, a metal sheet resistance of 0.1 Ω/square, and a metal contact resistance of 10 Ω.

3.1   Redraw the layout and cross-sectional views of a pad, similar to Fig. 3.2, if the final pad size is 50 μm by 75 μm with a scale factor of 100 nm.

3.2   Estimate the capacitance to ground of the pad in Fig. 3.20 made with both metal1 and metal2.

3.3   Suppose a parallel plate capacitor was made by placing a 100 μm square piece of metal1 directly below the metal2 in Fig. 3.2. Estimate the capacitance between the two plates of the capacitor (metal1 and metal2). Estimate the capacitance from metal1 to substrate. The unwanted parasitic capacitance from metal1 to substrate is often called the **bottom plate** parasitic.

3.4   Sketch the cross-sectional view for the layout seen in Fig. 3.26.
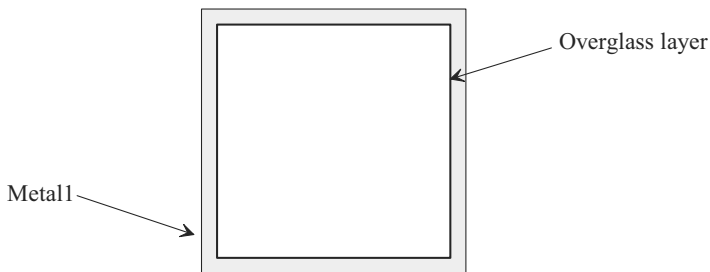
Figure 3.26   Layout used in Problem 3.4.

3.5   Sketch the cross-sectional view, at the dashed line, for the layout seen in Fig. 3.27. What is the contact resistance between metal3 and metal2?
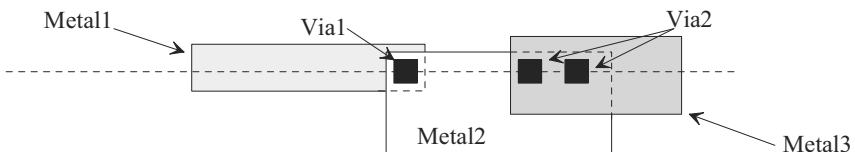

Figure 3.27   Layout for Problem 3.5.

3.6   The insulator used between the metal layers (the interlayer dielectric, ILD) can have a relative dielectric constant well under the relative dielectric constant of SiO_2 (= 4). Estimate the intrinsic propagation delay through a metal line encapsulated in an ILD with a relative dielectric constant of 1.5. What value of metal sheet resistance, using the values from Ex. 3.3, would be required if the RC delay through the metal line is equal to the intrinsic delay?

3.7   Using $CV = Q$, rederive the results in Ex. 3.5.

3.8   For the layout seen in Fig. 3.28, sketch the cross-sectional view (along the dotted line) and estimate the resistance between points A and B. Remember that a via is sized 1.5 by 1.5.
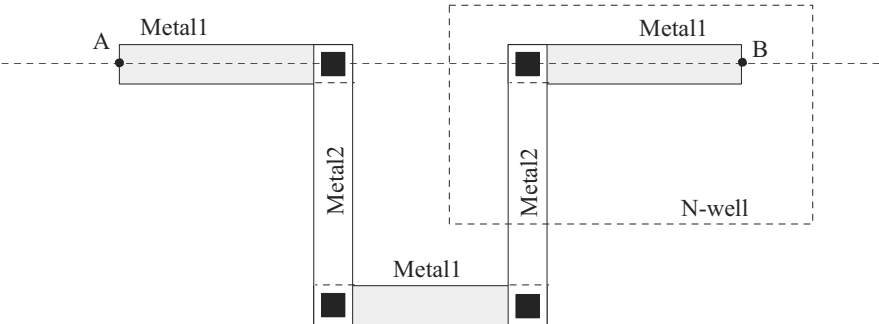
Figure 3.28 Layout for Problem 3.8.

3.9   Laying out two metal wires directly next to each other, and with minimum spacing, for a long distance increases the capacitance between the two conductors, C_m. If the two conductors are *VDD* and ground, is this a good idea? Why or why not?

3.10   Consider the schematic seen in Fig. 3.29. This circuit can be used to model ground bounce and *VDD* droop. Show, using SPICE, that a decoupling capacitor can be used to reduce these effects for various amplitude and duration current pulses.
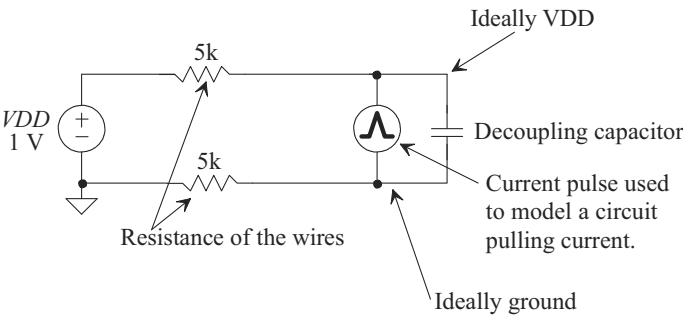

Figure 3.29 Circuit used to show the benefits of a decoupling capacitor.

3.11   Lay out the padframe specified by the information in Table 3.2. Assume a 3 metal CMOS process is used. Comment on how the scale factor affects the (drawn) layout size.

3.12   Propose, and lay out, a test structure to measure the sheet resistance of metal3. Comment on the trade-offs between accuracy and layout size. Using your test structure provide a numerical example of calculating sheet resistance for metal3.

ADDITIONAL READING

[1]   Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Second Edition, Cambridge University Press, 2010. ISBN 978-0521832946

[2]   A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, John Wiley and Sons Publishers, 2002. ISBN 0-471-49871-8

[3]   D. Clein, *CMOS IC Layout: Concepts, Methodologies, and Tools*, Newnes Publishers, 2000. ISBN 0-750-67194-7

[4]   S. Dabral and T. J. Maloney, *Basic ESD and I/O Design*, John Wiley and Sons Publishers, 1999. ISBN 0-471-25359-6

PROBLEMS

4.1   Lay out a nominally 200 kΩ resistor with metal1 wire connections. DRC your layout. What would happen if the layout did not include n+ under the contacts? Use the sheet resistances from Table 4.1.

4.2   Sketch the cross-sectional view along the line indicated in Fig. 4.21.
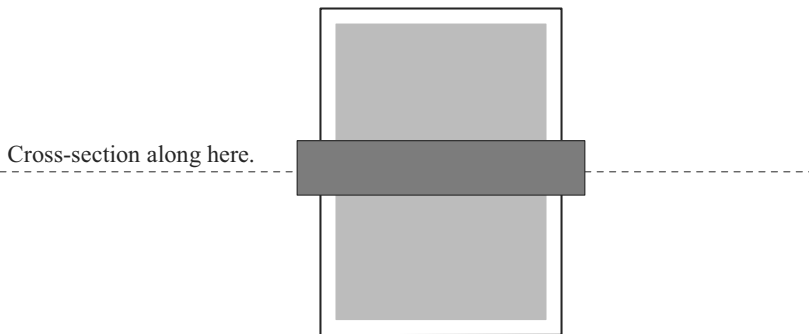
Figure 4.21 Layout used in Problem 4.2.

4.3   Sketch the cross-sectional views across the *VDD* and ground power buses in the standard cell frame of Fig. 4.15.

4.4   Suppose the "bad" layout seen in Fig. Ex4.1 is used to fabricate an NMOS device. Will the poly be doped? Why or why not?

4.5   Why is polysilicon's parasitic capacitance larger than metal1's?

4.6   Lay out an NMOS device with an length of 1 and width of 10. Label all four of the MOSFET terminals.

4.7   Lay out an PMOS device with a length of 1 and width of 20. Label all four of the MOSFET terminals.

4.8   Using the standard cell frame, lay out 10 (length) by 10 (width) NMOS and PMOS transistors. Sketch several cross-sectional views of the resulting layouts showing all four terminals of the MOSFETs.

4.9   Repeat Ex. 4.2 for a poly wire that is 5 wide.

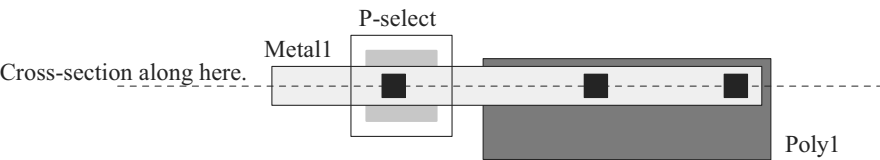**4.10**   Sketch the cross-sectional view at the line indicated in Fig. 4.22.

Figure 4.22   Layout used in Problem 4.10.

4.11   Sketch the cross-sectional views across the lines shown in Fig. 4.23.
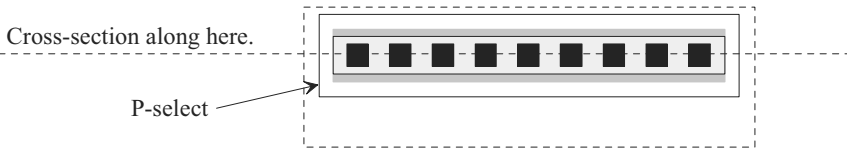
Figure 4.23   Layout used in Problem 4.11.

4.12   The layout of a PMOS device is seen in Fig. 4.24 is incorrect. What is the (fatal) problem?
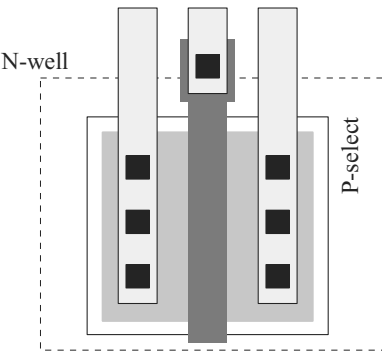
Figure 4.24   Flawed layout of a PMOS device. What is the error?

the top string of Fig. 5.29 (on the left) has a value of 14 (6 + 8). The MSB $2R$ in the bottom string (on the right) has a value of 24. Adding the values of the two resistors, by connecting them in series, results in a resistor value of 38 ($2R = 38$ while $R = 19$). The middle resistor value in the top string has a value of 12, while the bottom resistor has a value of 7. Again, adding the two resistors results in a value of 19. Fundamentally, the limiting factor in matching then becomes the voltage and temperature (because of the different current densities through the resistors) coefficients of the resistors.

ADDITIONAL READING

[1]   R. A. Pease, J. D. Bruce, H. W. Li, and R. J. Baker, "Comments on Analog Layout Using ALAS!" *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, September 1996, pp. 1364–1365.

[2]   D. J. Allstot and W. C. Black, "Technology Design Considerations for Monolithic MOS Switched-Capacitor Filtering Systems," *Proceedings of the IEEE*, vol. 71, no. 8, August 1983, pp. 967–986.

PROBLEMS

5.1   Suppose a current in a circuit is given by

$$I = \frac{V_{REF}}{R}$$

If the voltage, V_{REF}, comes from a precision voltage reference and doesn't change with temperature, determine the temperature coefficient of the current in terms of the resistor's temperature coefficient. If the resistor is fabricated using the n-well plot, similar to Fig. 5.1, the current's change with temperature. Use the TCR1 given in Table 4.1.

5.2   Suppose a silicided n+ resistor with a value of 100 Ω is used. Using the data from Table 4.1, sketch the layout and cross-sectional views of the resistor. The current in the resistor flows mainly in the silicide. Suppose the mobility of free carriers in the silicide is constant with increasing temperature. Would the temperature coefficient of the resistor be positive or negative? Why?

5.3   Using a layout program, make a schematic and layout for the 1/5 voltage divider seen in Fig. 5.4 if the resistor's value is 5k. Use n-well resistors and DRC/LVS the final layout and schematic.

5.4   Using a layout program, make a schematic and layout for an RC lowpass circuit where the resistor's value is 10k and the poly-poly capacitor's value is 100 fF. Use the 50 nm process (see Table 5.1). DRC/LVS the final layout and schematic. Simulate the operation of the circuit with a pulse input (see Fig. 1.27).

5.5   Estimate the areas and perimeters of the source/drain in the layout seen in Fig. 5.18 if the length of the device, L, is 2 and the width of a finger, W, is 20.

5.6   Provide a qualitative discussion for the capacitances of the PMOS device similar to the discussion associated with Fig. 5.21 for the NMOS device. Make sure the descriptions of operation in the strong inversion and depletion regions are clear. Draw the equivalent (to Fig. 5.21) figure for the PMOS devices.

[10]   D. K. Schroder, *Modular Series on Solid State Devices-Advanced MOS Devices,* Addison-Wesley, 1987.

[11]   S. M. Sze, *Physics of Semiconductor Devices,* 2nd ed., John-Wiley and Sons, 1981. ISBN 0-471-05661-8.

PROBLEMS

6.1   Plot the magnitude and phase of v_{out} (AC) in the following circuit, Fig. 6.20. Assume that the MOSFET was fabricated using the 50 nm process (see Table 5.1) and is operating in strong inversion. Verify your answer with SPICE.
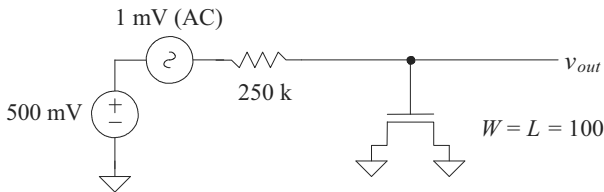

Figure 6.20   Circuit used in Problem 6.1.

6.2   If a MOSFET is used as a capacitor in the strong inversion region where the gate is one electrode and the source/drain is the other electrode, does the gate overlap of the source/drain change the capacitance? Why or not? What is the capacitance?

6.3   Repeat Problem 6.2 when the MOSFET is operating in the accumulation region. Keep in mind that the question is not asking for the capacitance from gate to substrate.

6.4   If the oxide thickness of a MOSFET is 40 Å, what is C'_{ox}?

6.5   Repeat Ex. 6.2 when $V_{SB} = 1$ V.

6.6   Repeat Ex. 6.3 for a p-channel device with a well doping concentration of 10^{16} atoms/cm^3.

6.7   What is the electrostatic potential of the oxide-semiconductor interface when $V_{GS} = V_{THN0}$?

6.8   Repeat Ex. 6.5 to get a threshold voltage of 0.8 V.

6.9   What happens to the threshold voltage in Problem 6.8 if sodium contamination of 100×10^9 sodium ions/cm^2 is present at the oxide-semiconductor interface?

6.10   How much charge (enhanced electrons) is available under the gate for conducting a drain current at the drain-channel interface when $V_{DS} = V_{GS} - V_{THN}$? Why? Assume that the MOSFET is operating in strong inversion, $V_{GS} > V_{THN}$.

6.11   Show the details of the derivation for Eq. (6.33) for the PMOS device.

6.12   Using Eq. (6.35), estimate the small-signal channel resistance (the change in the drain current with changes in the drain-source voltage) of a MOSFET operating in the triode region (the resistance between the drain and source).

6.13   Show, using Eqs. (6.33) and (6.37), that the parallel connection of MOSFETs shown in Fig. 5.18 behave as a single MOSFET with a width equal to the sum of each individual MOSFET width.

6.14   Show that the bottom MOSFET, Fig. 6.21, in a series connection of two MOSFETs cannot operate in the saturation region. Neglect the body effect. *Hint*: Show that M1 is always either in cutoff ($V_{GS1} < V_{THN}$) or triode ($V_{DS1} < V_{GS1} - V_{THN}$).
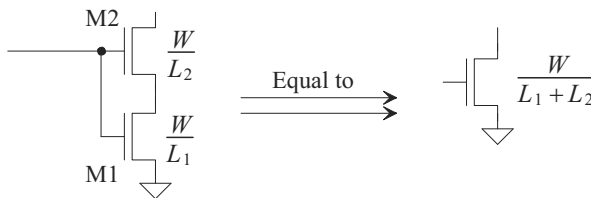
Figure 6.21   MOSFETs operating in series.

6.15   Show that the series connection of MOSFETs shown in Fig. 6.21 behaves as a single MOSFET with twice the length of the individual MOSFETs. Again, neglect the body effect.

$V_{1/f}^2(f)$ - PSD of flicker noise voltage, units of V^2/Hz.

V_{RMS} - Root mean-squared value of a voltage waveform, units of V, also written in this chapter as $\sqrt{\overline{v^2}}$.

V_{RMS}^2 - Mean-squared value of a voltage waveform, units of V^2, also written in this chapter as $\overline{v^2}$.

V_s - Source input voltage.

V_T - Thermal voltage, kT/q or 26 mV at room temperature.

ω - $2\pi f$.

Z_{in} - A complex input impedance.

PROBLEMS

8.1   Suppose that the power company is charging $ 0.25 for a kilowatthour (1,000 W of power supplied for one hour) of energy. How much are you paying for a Joule of energy? How much energy, in Joules, is supplied to a 100 W lightbulb in one hour? Is it potential energy or kinetic energy the power company sells?

8.2   The power company attempts to hold, in the United States, the RMS value of the voltage supplied to households to 120 V RMS with $\pm 3V$ at a frequency of 60 Hz. What is the peak-to-peak value of this voltage? If we were to look at the PSD of this signal in a 10 Hz bandwidth, what amplitude would we see?

8.3   Suppose a SA measures a noise voltage spectral density of $1 \ \mu V/\sqrt{Hz}$. What is the RMS value of this noisy signal over a bandwidth of DC to 1 MHz?

8.4   Suppose the noise signal in problem 3 shows a 3-dB frequency of 5 MHz. What is its RMS value over an infinite bandwidth?

8.5   Estimate the RMS output noise in the following circuit over a bandwidth of 1 to 1kHz. Verify your answer with SPICE. (Hint: simplify the circuit by combining resistors.)
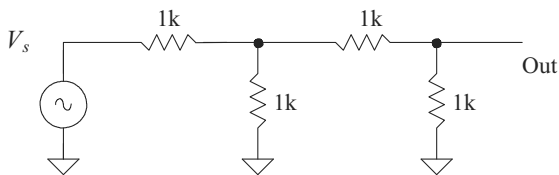

Figure 8.48   Circuit for Problem 8.5.

8.6   Estimate the RMS output noise over an infinite bandwidth for the circuit in Fig. 8.48 if the output is shunted with a 1 pF capacitor.

8.7   Show, Fig. 8.49, that the calculation of SNR_{in} results in the same value independent of treating the input as a voltage or a current.
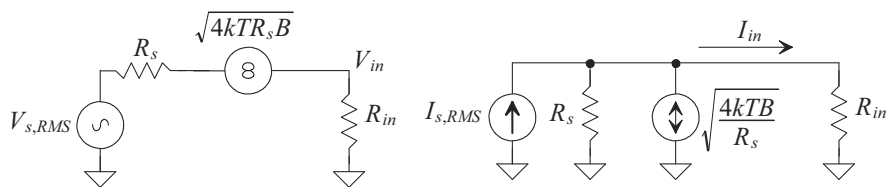
Figure 8.49 Calculating input SNR in Problem 8.7.

8.8 Using the input-referred noise model seen in Fig. 8.20b, verify that if the input resistance becomes infinite, the output noise is adequately modeled using a single input-referred noise voltage.

8.9 If an amplifier has a 0 dB NF, does that indicate the amplifier's output is free of noise? Why or why not?

8.10 Verify, as seen in Eq. (8.45), that the input-referred noise power of an amplifier is $(V_{inoise,RMS} \cdot I_{inoise,RMS})/2$.

8.11 Verify that the units for the shot noise PSD seen in Eq. (8.49) are indeed A^2/Hz.

8.12 Repeat Ex. 8.12 if the input voltage is reduced from 1.7 V to 1 V.

8.13 Verify the comment made in Sec. 8.2.5 that the RMS value of integrated flicker noise signal increases linearly with measurement time.

8.14 If the maximum allowable RMS output noise of a transimpedance amplifier built using the TLC220x is 100 µV in a bandwidth of 1 MHz is needed, what are the maximum values of C_F and R_F? What is the peak-to-peak value of the noise in the time domain?

8.15 Estimate the RMS output noise for the circuit seen in Fig. 8.50. Compare the hand-calculated result to SPICE simulation results using an ideal op-amp (as used in Ex. 8.18).
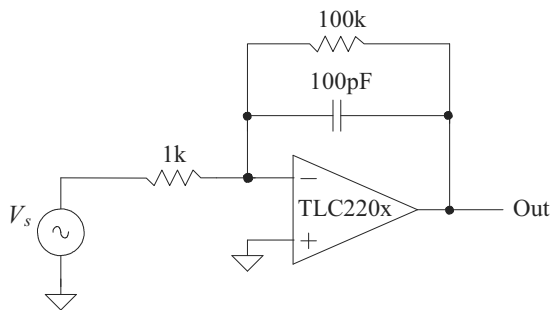

Figure 8.50 Circuit for Problem 8.15.

8.16   Suppose a 4.7 V Zener diode is used in a noise generator, as seen in Fig. 8.40. Estimate the output noise voltage PSD in terms of the diode's noise current and the biasing resistor (use 1k) if the power supply is 9 V. (Note: the noise mechanism is shot noise not avalanche noise.)

8.17   Rewrite Eq. (8.72) if $Z_{in} = R_{in} + 1/j\omega C_{in}$.

8.18   Estimate the RMS output noise for the amplifier seen in Fig. 8.51. What would placing a capacitor across the feedback resistor do to the RMS output noise and to the speed (bandwidth) of the amplifier? Name two ways to lower the RMS output noise for this amplifier. What is the cost for the lower output noise?
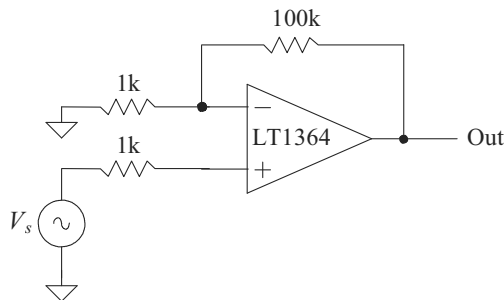
Figure 8.51 Circuit for Problem 8.18.

PROBLEMS

For the following problems use the long-channel process information given in Table 9.1 for KP, V_{TH}, and C'_{ox}, unless otherwise indicated.

9.1   Calculate and simulate the values of I_D and V_{GS} in the following circuit.
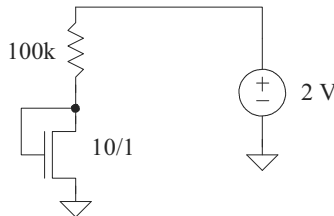
Figure 9.38   Circuit used in Problem 9.1

9.2   Repeat Problem 9.1 if the MOSFET size is changed to 10/10.

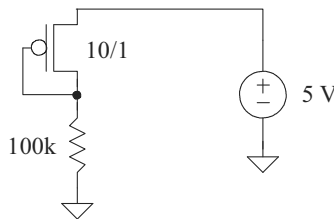**9.3**   Calculate and simulate the values of I_D and V_{SG} in the following circuit.

Figure 9.39   Circuit used in Problem 9.3

9.4   Repeat Problem 9.3 if the MOSFET size is changed to 10/10.

9.5   Calculate I_D, V_{DS}, and estimate the small-signal resistance looking into the drain of the MOSFET in the following circuit.
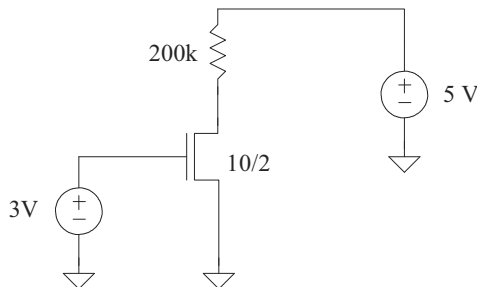
Figure 9.40   Circuit used in Problem 9.5

9.6   To determine the value of a small-signal resistance in a simulation, the circuit seen in Fig. 9.41 is used. The ratio of the test voltage, v_T, to the current that flows in the source, i_T, that is, v_T/i_T, is the small signal resistance. Using this circuit determine, with SPICE, the value of the resistance looking into the drain of the circuit in Fig. 9.40. How does the 200k resistor affect i_T in the simulation?
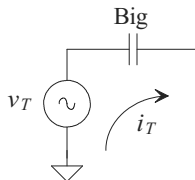

Figure 9.41   Using a test voltage to determine a resistance in a simulation.

9.7   Explain qualitatively what happens to V_{GS4} and V_{DS4} in Fig. 9.42 as the bias current is increased.
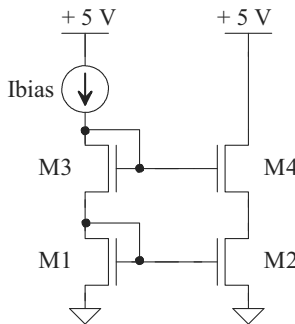

Figure 9.42 Schematic for Problem 9.7.

9.8   Describe qualitatively what happens if we steal or inject a current at the point indicated in Fig. 9.43. How does this affect the operation of M1 and M2? Verify your answer with SPICE.
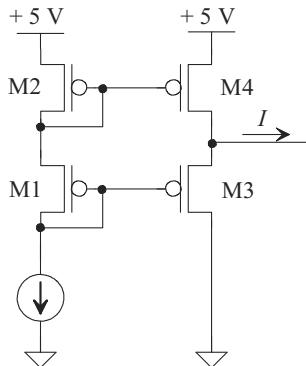

Figure 9.43   Schematic for Problem 9.8.

9.9   Using simulations, generate the plot seen in Fig. 9.12 for both NMOS and PMOS devices.

9.10 Design a circuit that will linearly convert an input voltage that ranges from 0 to 4V into a current that ranges from roughly 50 µA to 0. Simulate the operation of the design showing the linearity of the voltage-to-current conversion. How does the MOSFET's length affect the linearity?

9.11 Using a PMOS device, discuss and show with simulations how it can be used to implement a 10k resistor. Are there any limitations to the voltage across the PMOS resistor? Explain.

9.12 Using SPICE (and ensuring the MOSFET is operating in the saturation region with sufficient V_{DS}), generate the i_D versus v_{GS} curve seen in Fig. 9.15. Using SPICE take the derivative of i_D (e.g., "plot deriv(ID)") to get the device's g_m (versus V_{GS}). How does the result compare to Eq. (9.22)? Does the level 3 model used in the simulation show a continuous change from subthreshold to strong inversion?

9.13 Estimate the AC, i_d , drain current that flows in the circuit seen in Fig. 9.44. Verify your answer with SPICE in using both transient and AC simulations.
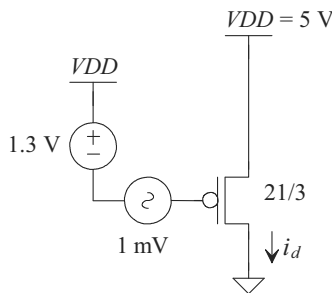

Figure 9.44   Schematic for Problem 9.13.

9.14 Calculate the DC and AC voltages and currents for the circuit seen in Fig. 9.45. Verify your answers with a SPICE AC analysis simulation.

9.15 Repeat Problem 9.14 if the bias current is reduced to 20 µA.

9.16 Using SPICE (and zero volt sources), verify the drain currents calculated in Ex. 9.5. Show both your AC analysis and transient analysis simulation results.

9.17 Using SPICE, generate the i_D versus v_{SB} curve seen in Fig. 9.21.

9.18 Repeat Ex. 9.6 if the widths and lengths of the PMOS and NMOS devices are multiplied by 10 (that is the NMOS is now 100/20 and the PMOS is now 300/20). How does the drain current change?

9.19 Compare the f_T of a 10/2 NMOS to a 100/20 NMOS. Verify your hand calculations using simulations.
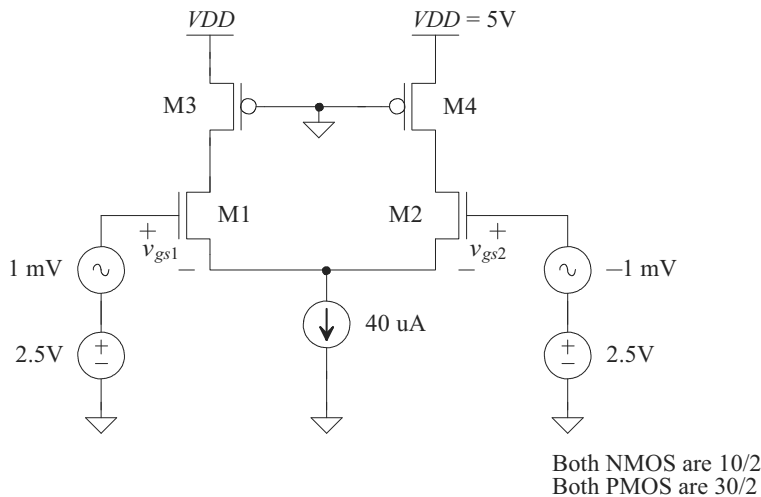
Figure 9.45 Circuit used in Problem 9.14.

9.20 Equation (9.39) is used to calculate the forward transconductance of a MOSFET operating in the subthreshold region. Is it possible to have subthreshold operation when I_D is 100 μA? If so, how?

9.21 Using the simulations that generated Fig. 9.27, estimate the threshold voltage for 50/5 PMOS and NMOS devices (both in the short-channel CMOS process).

9.22 Show the details leading to Eq. (9.43). Show, as an example, that the approximation is valid if $Q'_{b0}/C'_{ox} = 30 \, mV$. (Remember: temperature is in Kelvin.)

9.23 For the circuits seen in Fig. 9.46, estimate both the output voltage at room temperature and how it will change with temperature. Verify your answer with SPICE. Use the short-channel CMOS process.

Figure 9.46 Circuits for Problem 9.23.
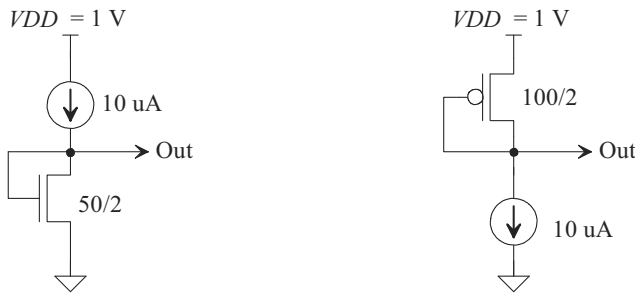
9.24   Verify, using simulations, the result given in Eq. (9.59), that is, that the GFT of a long-channel process is independent of biasing conditions. Make sure that the MOSFET is biased away from the subthreshold and triode regions.

9.25   When Eq. (9.36) was derived it was assumed that $C_{gs} \gg C_{gd}$. Looking at the data in Table 9.2, is this a good assumption? Compare the hand-calculated value of f_T to the simulation results in Table 9.2.

9.26   Using the short-channel parameters in Table 9.2, calculate the drain voltage of M1 and its drain current (both AC and DC components) for the circuit seen in Fig. 9.47.
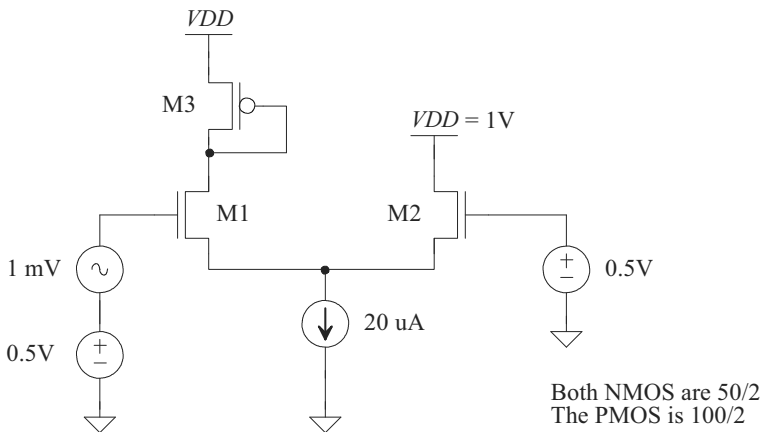

Figure 9.47   Circuit used in Problem 9.26.

9.27   What is the PSD of a MOSFET's thermal noise when it is operating in the triode region?

9.28   Looking at Eq. (9.66), we see that decreasing the MOSFET's g_m reduces the MOSFET's drain current noise PSD. If the MOSFET is to be used as an amplifier where the input signal is on the MOSFET's gate, is reducing g_m a good idea? Why or why not?

9.29   Show how the thermal noise resistance of the channel seen in Eq. (9.63) is derived for the MOSFET operating in the saturation region.

ADDITIONAL READING

[1]   J. P. Uyemura, *Introduction to VLSI Circuits and Systems*, John Wiley and Sons Publishers, 2002. ISBN 0-471-12704-3.

[2]   R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI-Design Techniques for Analog and Digital Circuits,* McGraw-Hill Publishing Company, 1990. ISBN 0-07-023253-9.

PROBLEMS

10.1   Using the parameters in Table 6.2, compare the hand-calculated effective digital switching resistance from Eq. (10.6) to the empircially derived values given in Table 10.1.

10.2   Regenerate Fig. 10.14 for the PMOS device.

10.3   Using SPICE verify the results of Ex. 10.3.

10.4   Replacing the NMOS PGs in Fig. 10.16 with PMOS PGs and changing the *VDD*-connected nodes to ground-connected nodes, show, and verify with simulations, the outputs of the two modified circuits.

10.5   For the following circuits estimate the delay between the input and the output. Use the 50 nm (short-channel CMOS) process. Verify the estimates with SPICE.
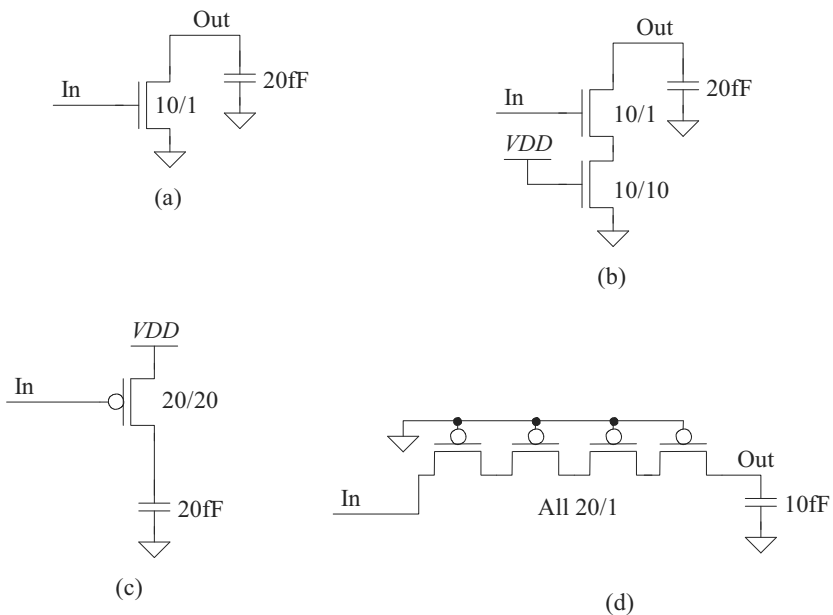

Figure 10.25   Circuits used in Problem 10.5.

[3]   M. I. Elmasry, *Digital MOS Integrated Circuits II,* IEEE Press, 1992. ISBN 0-87942-275-0, IEEE order number: PC0269-1.

[4]   R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI-Design Techniques for Analog and Digital Circuits,* McGraw-Hill Publishing Co., 1990. ISBN 0-07-023253-9.

PROBLEMS

Use the 50 nm CMOS process for the following problems unless otherwise stated.

11.1   Estimate the noise margins for the inverters used to generate Fig. 11.4.

11.2   Design and simulate the DC characteristics of an inverter with V_{SP} approximately equal to V_{THN}. Estimate the resulting noise margins for the design.

11.3   Show that the switching point of three inverters in series is dominated by the V_{SP} of the first inverter.

11.4   Repeat Ex. 11.6 using a PMOS device with a width of 10.

11.5   Repeat Ex. 11.6 using the long-channel process with a 30/10 inverter.

11.6   Estimate the oscillation frequency of a 11-stage ring oscillator using inverters 30/10 inverters in the long-channel CMOS process. Compare your hand calculations to simulation results.

11.7   Using the long-channel process, design a buffer with minimum delay ($A = 2.718$) to insert between a 30/10 inverter and a 50 pF load capacitance. Simulate the operation of the design.

11.8   Repeat Problem 11.7 using an area factor, A, of 8.

11.9   Derive an equation for the switching point voltage, similar to the derivation of Eq. (11.4), for the NMOS inverter seen in Fig. 11.24a.

11.10 Repeat Problem 11.9 for the inverter in Fig. 11.24c. Note that the PMOS transistor is operating in the triode region when the input/output are at V_{SP}.
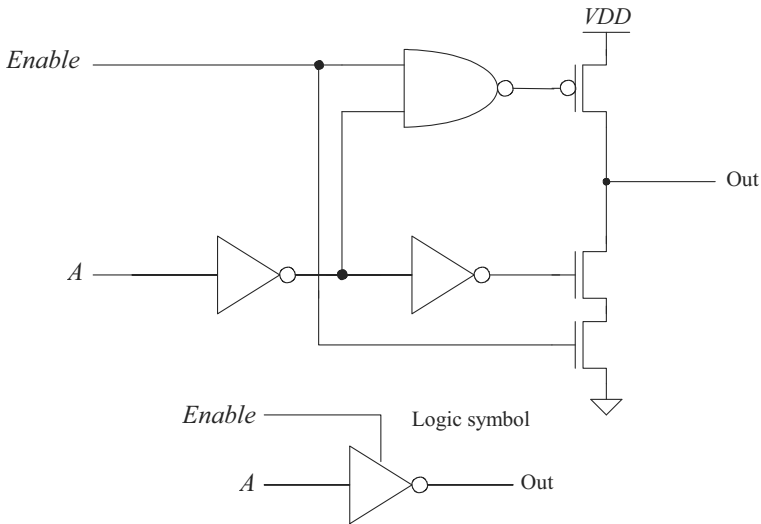
Figure 12.26 Tri-state inverting buffer.

ADDITIONAL READING

[1]   I. Sutherland, R. F. Sproull, and D. Harris, *Logical Effort: Designing Fast CMOS Circuits*, Morgan Kaufmann, 1999. ISBN 978-1558605572

[2]   M. I. Elmasry, *Digital MOS Integrated Circuits II,* IEEE Press, 1992. ISBN 0-87942-275-0, IEEE order number: PC0269-1.

[3]   J. P. Uyemura, *Circuit Design for Digital CMOS VLSI,* Kluwer Academic Publishers, 1992.

[4]   M. Shoji, *CMOS Digital Circuit Technology,* Prentice-Hall, 1988. ISBN 0-13-138850-9.

PROBLEMS

Use the 50 nm, short-channel process unless otherwise indicated.

12.1   Design, lay out, and simulate the operation of a CMOS AND gate with a V_{SP} of approximately 500 mV. Use the standard-cell frame discussed in Ch. 4 for the layout.

12.2   Design and simulate the operation of a CMOS AOI half adder circuit using static logic gates.

12.3   Repeat Ex. 12.3 for a three-input NOR gate. (Use the effective resistances to estimate the V_{SP}.)

12.4   Repeat Ex. 12.4 for a three-input NOR gate. (Use the effective resistances to estimate the V_{SP}.)

12.5   Sketch the schematic of an OR gate with 20 inputs. Comment on your design.

12.6   Sketch the schematic of a static logic gate that implements $\left(A + B \cdot \overline{C}\right) \cdot D$. Estimate the worst-case delay through the gate when driving a 50 fF load capacitance.

12.7   Design and simulate the operation of a CSVL OR gate made with minimum-size devices.

12.8   Design and simulate the operation of a tri-state buffer that has propagation delays under 5 ns when driving a 1 pF load. Assume that the maximum input capacitance of the buffer is 100 fF.

12.9   Sketch the schematic of a three-input XOR gate implemented in AOI logic.

12.10   The circuit shown in Fig. 12.27 is an edge detector. Discuss, and simulate, the operation of the circuit.
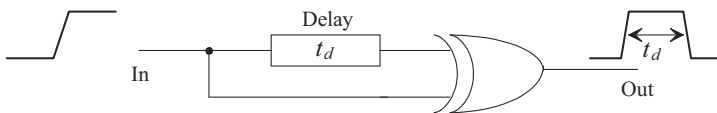

Figure 12.27   An edge detector circuit.

$$t_{PLH} = t_{PHL} = 15.75 \ ps$$

The simulation results are seen in Fig. 13.34. The delay to point A is approximately 30 ps, while the delay to point B is about 90 ps. It's important to reiterate the importance of simulations when determining delays. Hand calculations, as this example shows, have limitations. Hand calculations are still important, however, because they reveal the location of the dominant delays in a digital circuit. ■
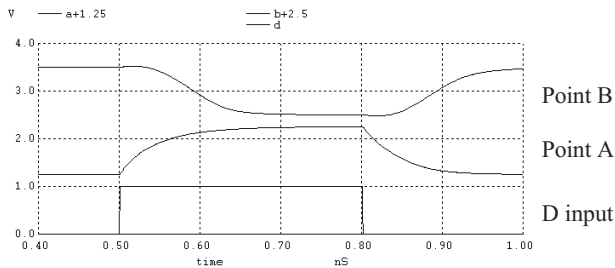

Figure 13.34 Simulating the delays through the latch seen in Fig. 13.33.

ADDITIONAL READING

[1]   M. I. Elmasry, *Digital MOS Integrated Circuits II,* IEEE Press, 1992. ISBN 0-87942-275-0, IEEE order number: PC0269-1.

[2]   J. P. Uyemura, *Circuit Design for Digital CMOS VLSI,* Kluwer Academic Publishers, 1992.

[3]   M. Shoji, *CMOS Digital Circuit Technology,* Prentice-Hall, 1988. ISBN 0-13-138850-9.

PROBLEMS

Unless otherwise stated, use the 50 nm, short-channel CMOS process with the parameters seen in Table 10.2.

13.1   Estimate and simulate the delay through 10 TGs connected a 50 fF load capacitance.

13.2   Design and simulate the operation of a half adder circuit using TGs.

13.3   Sketch the schematic of an 8-to-1 DEMUX using NMOS PGs. Estimate the delay through the DEMUX when the output is connected to a 50 fF load capacitance.

13.4   Verify, using SPICE, that the circuit seen in Fig. 13.12 operates as an XOR gate.

13.5   Simulate the operation of an SR latch made with NAND gates. Show all four possible input logic combinations.

13.6   Simulate the operation of the arbiter seen in Fig. 13.15. Show how two inputs arriving at nearly the same time results in only one output going high.

13.7   Show, using simulations, how making the feedback inverter, I2, in Fig. 13.18 stronger (decrease the lengths) can result in the output having either a long delay or not fully switching.

13.8   Redesign the FF in Fig. 13.22 without T2 and T4 present. Simulate the operation of your design. Show, by using a limited amplitude on the D input, how point B can have a metastability problems.

13.9   In your own words describe setup and hold times. Use the D-FF in Fig. 13.22 and simulations to help support your clear descriptions.
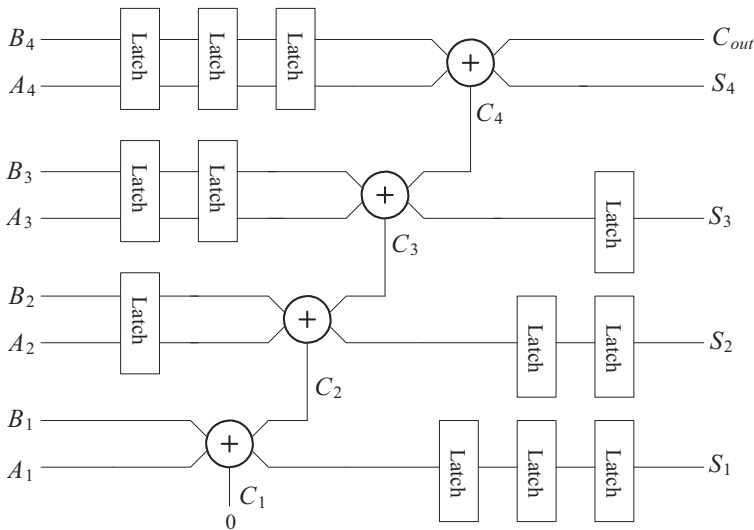
Figure 14.18 A pipelined adder. The latches (clocked) behave as delay elements.

to finish the addition of the two words. If this circuit were dedicated to continually performing the addition of two words, we could input the words at a very fast rate. However, since performing a single addition requires four clock cycles, applications of pipelining where two numbers are not added continuously can result in longer delay-times.

ADDITIONAL READING

[1]   K. Bernstein, K. M. Carrig, C. M. Durham, P. R. Hansen, D. Hogenmiller, E. J. Nowak, and N. J. Rohrer, *High Speed CMOS Design Styles*, Springer, 1999. ISBN 978-0792382201.

[2]   J. Yuen and C. Svensson, "New Single-Clock CMOS Latches and Flipflops with Improved Speed and Power Savings," *IEEE Journal of Solid-State Circuits,* vol. 32, no. 1, pp. 62–69, 1997.

[3]   M. I. Elmasry, *Digital MOS Integrated Circuits II,* IEEE Press, 1992. ISBN 0-87942-275-0, IEEE order number: PC0269-1.

[4]   J. P. Uyemura, *Circuit Design for Digital CMOS VLSI,* Kluwer Academic Publishers, 1992.

[5]   R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI-Design Techniques for Analog and Digital Circuits,* McGraw-Hill Publishing Co., 1990. ISBN 0-07-023253-9.

PROBLEMS

Unless otherwise stated, use the 50 nm, short-channel process.

14.1   Regenerate Fig. 14.2 for the PMOS device. From the results, determine the PMOS's I_{off}.

14.2   Repeat Ex. 14.2 if the storage node is a logic 0 (ground). Explain why the charge storage node charges up. What would happen if the PG's input were held at *VDD* instead of *VDD*/2.

14.3   Comment on the usefulness of dynamic logic in our 50 nm CMOS process-based on the results given in Ex. 14.3 with a clock frequency of 10 MHz.

14.4   Using the circuit in Fig. 14.6 and the SPICE simulation, show how the current drawn from *VDD*, by the inverters, changes with time. Do you see any concerns? If so, what?

14.5   Simulate the operation of the nonoverlapping clock generator circuit in Fig. 14.9. Assume that the input clock signal is running at 100 MHz. Show how both ϕ_1 and ϕ_2 are nonoverlapping.

14.6   Simulate the operation of the clocked CMOS latch shown in Fig. 14.11.

14.7   Design and simulate the operation of a PE gate that will implement the logical function $F = \overline{ABCD + E}$.

14.8   If the PE gate shown in Fig. 14.13 drives a 50 fF capacitor, estimate the worst-case t_{PHL}. Use a 20/1 PMOS and a 10/1 NMOS.

14.9   Implement an XOR gate using Domino logic. Simulate the operation of the resulting implementation.

14.10 The circuit shown in Fig. 14.19 results from the implementation of a high-speed adder cell (1-bit). What type of logic was used to implement this circuit? Using timing diagrams, describe the operation of the circuit.

14.11 Discuss the design of a 2-bit adder using the adder cell of Fig. 14.19 If a clock, running at 200 MHz, is used with the 2-bit adder, how long will it take to add two words? How long will it take if the word size is increased to 32 bits?

14.12 Sketch the implementation of an NP logic half adder cell.

14.13 Design (sketch the schematic of) a full adder circuit using PE logic.

14.14 Simulate the operation of the circuit designed in Problem 14.10.

14.15 Show that the dynamic circuit shown in Fig. 14.20 is an edge-triggered flip-flop [2]. Note that a single-phase clock signal is used.
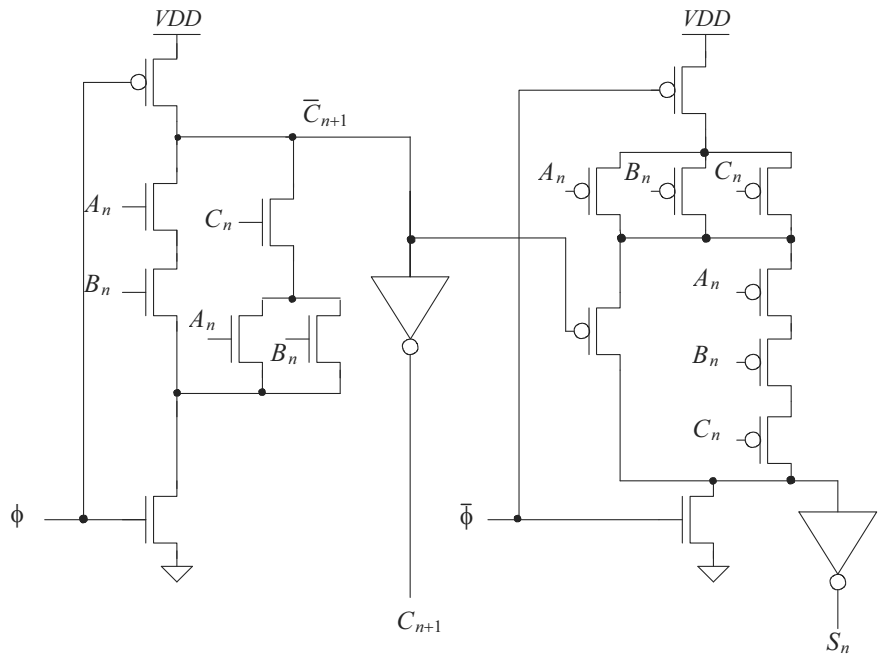
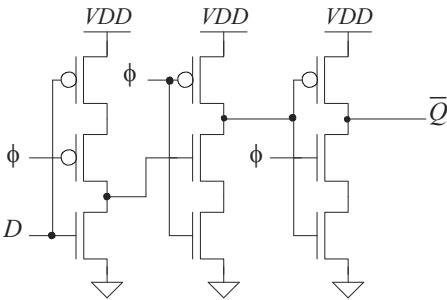**Figure 14.19**   A high speed adder cell. See Problem 14.10.

Figure 14.20   A true-single phase clocked FF, see Problem 14.15.

PROBLEMS

Unless otherwise indicated use the short-channel CMOS BSIM4 models for all simulations.

16.1   Estimate the bit line capacitance if there are 256 word lines and we include the gate-drain overlap capacitance from each MOSFET, as seen in Fig. 16.68.
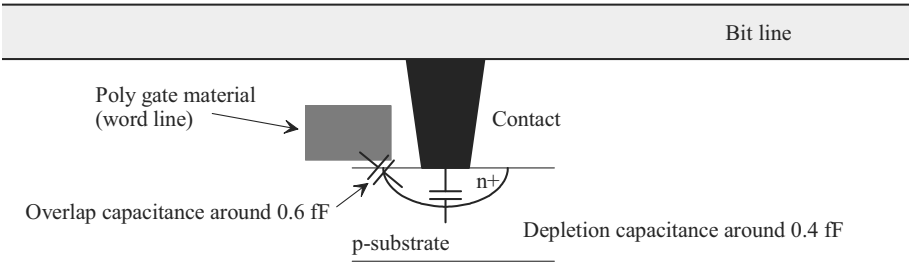

Figure 16.68 How the gate-drain overlap capacitance loads the bit line. Note that this cross-sectional view is rotated 90 degrees from the one seen in Fig. 16.3.

16.2   Consider the NSA seen in Fig. 16.69. Suppose that the load capacitance is mismatched by 20%, as seen in the figure. Assuming that both caps are equilibrated to 0.5 V prior to sensing, which capacitor will fully discharge to ground (which MOSFET will fully turn on)? What voltage difference on the capacitors is needed to cause metastability? Verify your answers with SPICE.
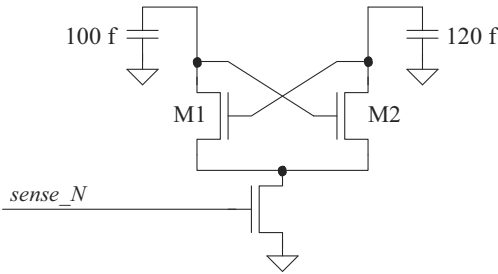

Figure 16.69 Problem 16.2 showing how a mismatch in the load capacitance of an NSA can result in in sensing errors.

16.3   Repeat Problem 16.2 with the circuit in Fig. 16.70. In this figure M1 and M2 experience a threshold voltage mismatch (modeled by the DC voltage source seen in the figure).

16.4   Examining Fig. 16.17 we see that there will be a voltage drop along the metal line labeled *NLAT* when the sense amplifiers fire. Re-sketch this metal line as resistors between each NSA. If the voltage drop along the line is significant (the length of
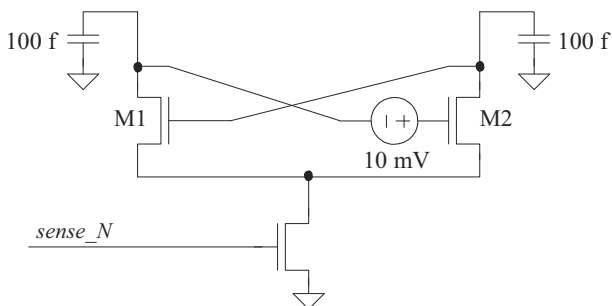
Figure 16.70 Circuit for Problem 16.3.

the line is very long), errors can result. Would we make things better by using individual MOSFETs on the bottom of each NSA connected to *sense_N*? Why or why not?

16.5 Suppose a memory array has 1024 columns. If the word line resistance of one cell is 2 Ω and the capacitance per cell (to ground) is 500 aF, estimate the delay to open a row line. Sketch the equivalent RC circuit of the word line.

16.6 In Fig. 16.71, if the top plate of capacitor C_1 is initially charged to V_1 and the top plate of capacitor C_2 is initially charged to V_2, estimate the final voltage, V_{final}, on the top plates of the capacitors after the switch closes.
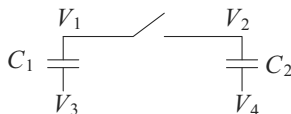

Figure 16.71 Circuit for Problem 16.6.

16.7 Figure 16.72 shows a clocked comparator topology based on the topology seen in Fig. 16.32. The location of the imbalance MOSFETs has been moved in this figure. Comment on the merits and disadvantages of this topology compared to the one in Fig. 16.32. Simulate the operation of this circuit.

16.8 Figure 16.73 shows the addition of I/O (input/output) transistors to the memory array and NSA seen in Fig. 16.17. Sketch a column decoder design using static logic. Show how the 3-bit input address is connected to each stage.

16.9 The I/O lines in the previous problem won't swing to full logic levels. To restore a full *VDD* level on these lines and to speed up the signals, a *helper flip-flop* is used. Sketch a possible implementation of the helper flip-flop. Why can it be used to speed up the signals?
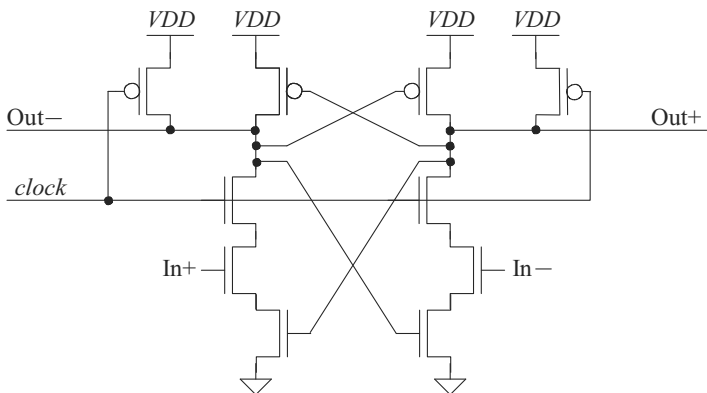
Figure 16.72   An alternative clocked sense amplifier.

16.10   Suppose a 2Mbit memory is to be designed as a x2 part (2-bit input/output words). Further suppose that 10 address pins are available to access the memory. Sketch a block diagram of how the row and column addresses are multiplexed together and stored in separate registers. Use $\overline{RAS}$ and $\overline{CAS}$, as discussed in the chapter to clock in the addresses. Comment on the validity of using 20-bits to access 2Mbits of data.

16.11   Suppose that the memory in Problem 16.10 is made up of 8-256k memory arrays (assume 1024 row lines, a folded array, and 512 column lines). How many I/O lines are needed for each array? If three bits of the address are used to select one of the memory arrays (so that only a single row is open in a single memory array
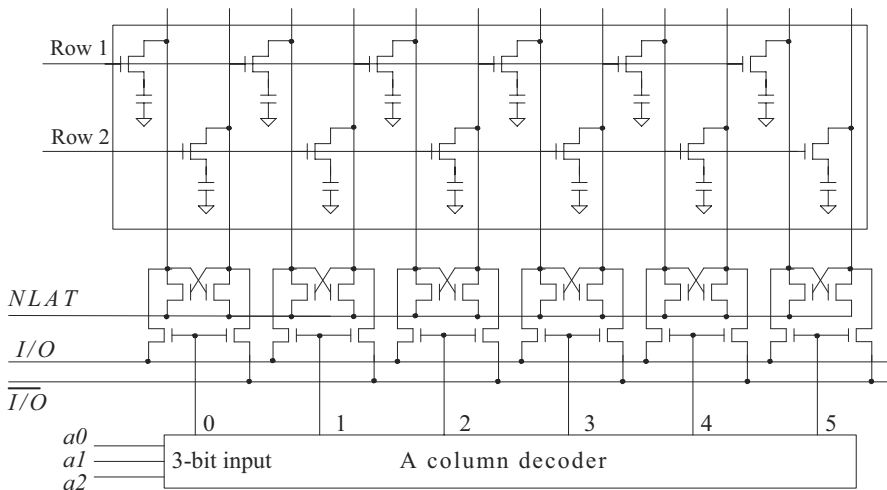

Figure 16.73   Design of a column decoder for problem 16.8.

at a time), how big is a page of data? Sketch a block diagram of a possible decoding scheme for the chip. Assume that only the three bits of the address are globally decoded and that the remaining 17 bits are locally decoded. How many of these bits must be routed to each array assuming an enable (one for each of the eight memory arrays) signal from the global decoder is routed to each memory array.

16.12 Suppose that it is suggested that the word line driver in Fig. 16.46 be modified to simplify it as seen in Fig. 16.74. What is the problem with this design? Use SPICE to illustrate the driver not functioning properly.
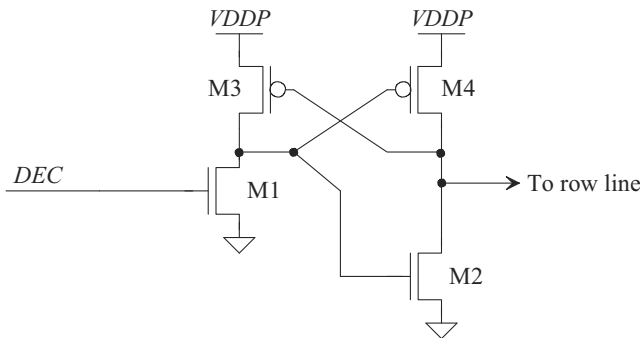

Figure 16.74 A (bad) CMOS word line driver, Problem 16.12.

16.13 Simulate the operation of the SRAM cell seen in Fig. 16.48. Use the 50 nm process with NMOS of 10/1 and PMOS of 20/1. Is it wise for the access MOSFETs to be the same size as the latch MOSFETs? Why or why not? Use simulations to verify your answers.

16.14 Suppose an array of EPROM cells, see Fig. 16.57, consisting of two row lines and four bit lines is designed. Further assume $V_{THN,Erased} = 1\ V$ and $V_{THN,Prog} = 4\ V$. Will there be any problems reading the memory out of the array if an unused row line is grounded while the accessed row line is driven to 5 V ? Explain why or why not.

16.15 Suppose that it is suggested that the n-well in a NAND Flash memory cell should be grounded at all times except when the array is being erased. Is this OK? What would be a potential benefit?

16.16 Explain in your own words and with the help of pictures why a top select MOSFET is needed in a NAND Flash memory cell.

16.17 Suppose that the transistor connected to RA3 in Fig. 16.61 is to be programmed. Further suppose that the n+ source implant seen in the layout is to remain grounded as indicated in Table 16.1. How do we float the source of the transistor connected to RA3 so that it can be programmed as seen in Fig. 16.58?

16.18 Reviewing Fig. 16.62, is it necessary that the gates of the floating gate MOSFETs connected to RA1 – RA3 be driven to 5 V? Can the gates of these MOSFETs remain grounded? Why or why not? If the RA1 MOSFET is to be programmed, in this figure, must the gate of RA0 be driven to 5 V?

16.19 If the I_{erased} of a NAND Flash memory cell is 20 µA and the I_{prog} is 2 µA, explain what the bit line voltage will do when reading out the cell in the following configuration, Fig. 16.75. Will the bit line go all the way to *VDD*? All the way to ground? Explain. If the bit line capacitance is 200 fF, estimate the length of time it will take the data on the bit line to settle before it can be read out. Assume that the *VDD* is 5 V and the bit line is equilibrated to 2.5 V prior to sensing.
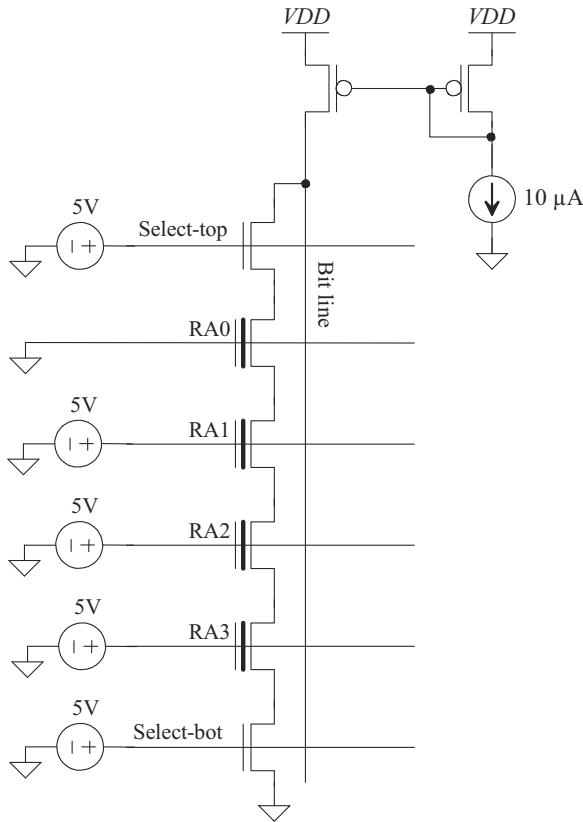

Figure 16.75   Reading the contents of RA0 in a NAND Flash cell.

16.20 Show, using a configuration similar to the one seen in Fig. 16.66, if it is possible to get negative gate tunnel gate current (used for erasing) by grounding the gate and raising the potential on the drain of the MOSFET. Explain why it works or why it doesn't work.

Finally note that whenever starting or switching the inputs during a sense operation there will be a start-up transient (see Fig. 17.34 for example). What this means is that the counter should be disabled at the beginning of the sense or in the middle (if the inputs to the DSM are swapped, as seen in Fig. 17.40, halfway through the sense operation). Not disabling the counter during these times can result in sensing errors.

ADDITIONAL READING

[1]   R. J. Baker, *CMOS: Mixed-Signal Circuit Design, Second Edition*, Wiley-IEEE Press, 2009.

[2]   R. J. Baker, "Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors," US Patent 7,515,188, April 7, 2009.

[3]   J. Taylor and R. J. Baker, "Method and apparatus for sensing flash memory using delta-sigma modulation," US Patent 7,366,021, April 29, 2008.

[4]   R. J. Baker, "Per column one-bit ADC for image sensors," US Patent 7,456,885, November 25, 2008.

[5]   R. J. Baker, "Resistive memory element sensing using averaging," US Patent 6,504,750, January 7, 2003.

PROBLEMS

17.1   Regenerate Table 17.1 in which the water level where a cup of water is removed is 4.7 instead of 5. How are the results affected? If the sensing time is increased, how are the final results affected (compare a water level of 5 against 4.7)?

17.2   Generate a table, similar to Table 17.1, for the situation seen in Fig. 17.4 if the amount of water leaving the bucket is 0.3 cups per 10 seconds.

17.3   Rederive Eqs. (17.3) − (17.8) if I_{cup} in Fig. 17.6 is replaced with a resistor. Assume that the clock frequency is large (why?) to simplify the equations. What is the requirement for the current through the resistor when it is connected to the bit line in terms of the maximum bit current, I_{bit}.

17.4   Using SPICE simulations demonstrate that the error because of parasitics, as seen in Fig. 17.7, is reduced by connecting the switch to a 1 V source instead of ground. Illustrate, with drawings, what is happening.

17.5   Show, using simulations, that if the output of the comparator swings from VDD to $VDD/2$ we can eliminate M4 in Fig. 17.9 and still have $Q_{cup} = C_{cup} \cdot (VDD - V_{REF} - V_{THP})$. Why? Does the amount of current supplied by $VDD/2$ increase? Could this be a problem?

17.6   Show how the incomplete settling seen in Fig. 17.13 can be made more complete by reducing the clock frequency or increasing the width of M4.

17.7   Demonstrate, using SPICE and discussions, that the circuit in Fig. 17.42 may be used in place of the comparator and M3 in Fig. 17.18. How do output glitches affect the sensing circuit's operation?
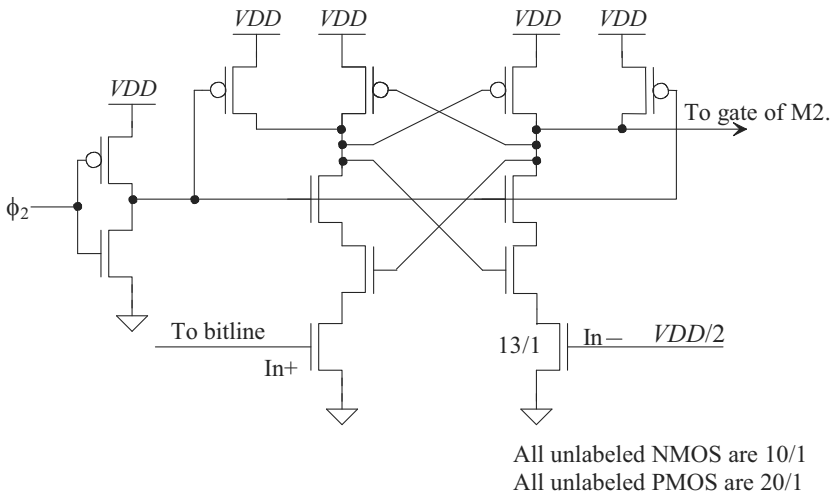
All unlabeled NMOS are 10/1
All unlabeled PMOS are 20/1

Figure 17.42   Simplifying the comparator in Figs. 17.16 and 17.18.

17.8   Design a DSM sensing circuit that will determine the value of a resistor that may range from 100k to 10 MΩ. Simulate your design with SPICE and comment on the design trade-offs concerning operating frequency and resistor (both the sensed and, if used in the DSM, the feedback resistance) changes with process variations or temperature.

17.9   Suppose that it is desired to have a noise floor of 100 μV RMS in a CMOS imager. Further suppose that the sensing circuit doesn't contribute any noise to the sense (the transformation from the analog column voltage to a digital word). Estimate the size of the hold capacitors used to sample both the reference and the intensity signals.

17.10   Using simulations, determine if the linearity of the voltage-to-current converter can be made better by adjusting the length and width of the PMOS device seen in Fig. 17.28. Why does, or doesn't, the performance get better?

17.11   Using the short-channel CMOS devices determine the average current that flows in the circuit seen in Fig. 17.43. The clocks are nonoverlapping (never low at the same time) as used throughout the chapter and have a frequency of 100 MHz. Verify your answer using SPICE.

17.12   What happens, to the simulation results seen in Fig. 17.34, if the time step used in the transient simulation is increased to 1 ns? How do the nonoverlapping clocks look with this time step?

17.13   Simulate the operation of the circuit seen in Fig. 17.44. Do the comparator outputs make full logic transitions? Are glitches a concern? Why? How do the simulation results compare to the results seen in Fig. 17.37? Note that the outputs of the comparator go low each time ϕ_2 goes high so that $\overline{Out}$ can be used to clock a counter directly.
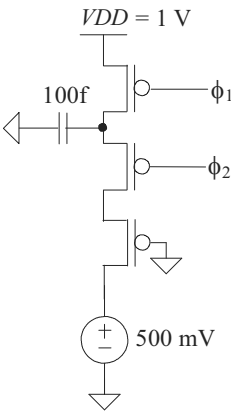
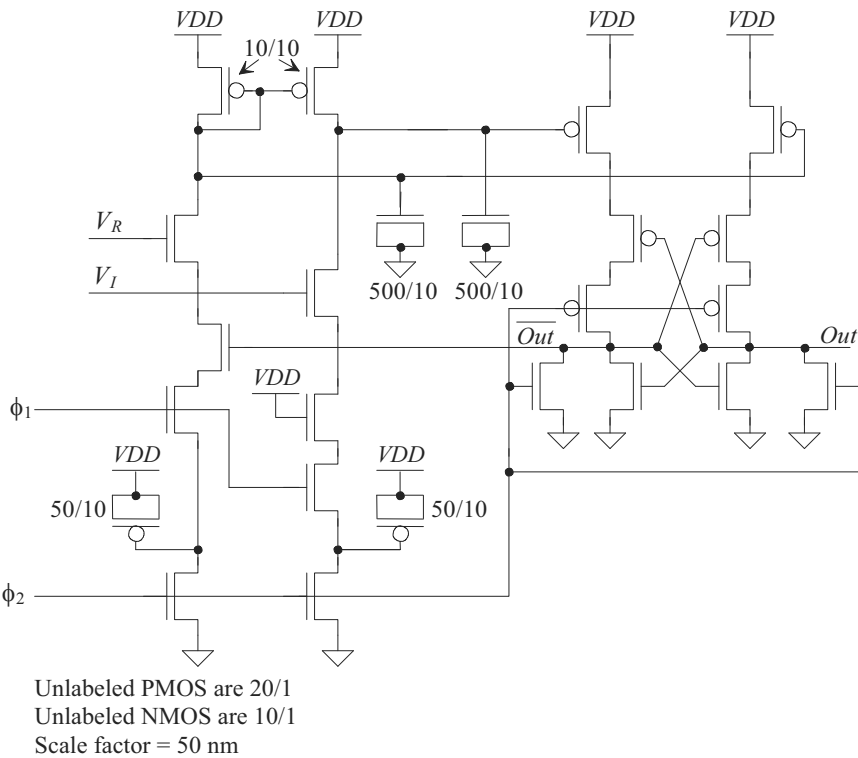**Figure 17.43** Determining the average current that flows in a switched-capacitor resistor. See Problem 17.11.

Unlabeled PMOS are 20/1
Unlabeled NMOS are 10/1
Scale factor = 50 nm

Figure 17.44 Simplifying the DSM sensing circuit, see Problem 17.13.

PROBLEMS

For the following problems use the short-channel CMOS process with a scale factor of 50 nm and a *VDD* of 1 V.

18.1   Design a Schmitt trigger with V_{SPL} = 0.35 and V_{SPH} = 0.55 V. Use SPICE to verify your design.

18.2   Estimate t_{PHL} and t_{PLH} for the Schmitt trigger of Ex. 18.1, driving a 100 fF load capacitance. Compare your hand calculations to simulation results.

18.3   Design and simulate the operation of a Schmitt trigger-based oscillator with an output frequency of 10 MHz. Simulate the design using SPICE.

18.4   Estimate the total input capacitance on the control voltage input for the VCO shown in Fig. 18.8.

18.5   Design an astable multivibrator with an output oscillation frequency of 20 MHz.

18.6   Design and simulate the operation of a one-shot that has an output pulse width of 100 ns. Comment on the maximum rate of retrigger and how ESD diodes connected to bonding pads will affect the circuit operation if the resistor and capacitor are bonded out.

18.7   Design and simulate a 100 MHz oscillator using the astable multivibrator in Fig. 18.11. Comment how process shifts in the resistor and capacitor affects the oscillation frequency. If the resistor and capacitor are bonded out, will the ESD diodes affect the circuit's operation?

18.8   Using the buffer seen in Fig. 18.23 to drive a load capacitance of 100 *fF*, plot the propagation delays against the *Vinp* input signal amplitude when *Vinm* is 250, 500, and 700 mV. (*Vinp* is centered around *Vinm.*)

18.9   The DC restore circuit seen in Fig. 18.28 has limitations, such as it stops working if a long string of 1s or 0s is applied to the input buffer or the input data moves too quickly and the long RC time constants keep the DC restore output from following the center of the data. Comment, with the help of SPICE simulation results, on these limitations. Show how changing the values of the resistors and capacitors can compensate for these limitations. (For example, using longer time constants allows for longer strings of ones are zeroes before the DC restore signal is invalid.)

18.10 Using the model for the transmission channel seen in Figs. 18.26 and 18.30, show that the circuit in Fig. 18.32 will work as an input buffer. Using SPICE show the limitations of the buffer (signal amplitude and speed). Also, comment on the power pulled by the buffer.

18.11 Design a nominally 2 V voltage generator that can supply at most 1 μA of DC current (2 MEG resistor). Simulate the operation of your design with SPICE.

18.12 Design and simulate the operation of a nominally –1 V substrate pump. Comment on the design trade-offs.

pp. 1218–1223, October, 1988. Classic paper presenting the concept of a delay-locked loop.

[8]   C. R. Hogge, Jr., "A Self Correcting Clock Recovery Circuit," *IEEE Journal of Lightwave Technology*, vol. LT-3, pp. 1312–1314, December 1985. Paper presenting the "Hogge" phase detector.

[9]   F. M. Gardner, "Charge-Pump Phase-Lock Loops," *IEEE Transactions on Communications,* COM-28, no. 11, pp. 1849–1858, November 1980. The paper first discussing charge pump PLLs.

PROBLEMS

19.1   The XOR gate PD seen in Fig. 19.4 can exhibit input-dependent skew. In other words, the delay from one of the inputs changing to the output of the PD will not be precisely the same as the delay from the other input to the output. Design an XOR PD that doesn't exhibit input-dependent skew. Hint: see Fig. 18.16.

19.2   Verify, using simulations, that a locked PLL using an XOR PD will exhibit, after RC filtering, an average value of $VDD/2$. Show, using simulations and hand calculations, the filter's average output if the XOR PD sees a phase difference in its inputs of $-\pi/4$.

19.3   Why, in your own words, is it so important for the VCO's center frequency to match the input NRZ data rate when a passive loop filter is used. Use simulations to show the problems. Why does using the active loop filter eliminate this requirement?

19.4   Suppose, for a robust high-speed PLL using an XOR PD, that it desirable to adjust the PD's gain. Show a charge pump can be used towards this goal. Should the loop filter have two outputs? Discuss the PD's gain and how it would be adjusted. What topology would be used for a passive loop filter? for an active loop filter?

19.5   Demonstrate, using simulations, how the outputs of the XOR PD can be equivalent when the loop is true or false locking (locking on a harmonic).

19.6   Describe, in your own words and using simulations, what the dotted line in Fig. 19.8 indicates.

19.7   We know that a PFD isn't generally used in clock recovery applications because both edges (*data* and *dclock*) must present when doing a phase comparison. Suggest a scheme where the edge of the input *data* enables a phase comparison. When an edge of data is not present your circuit will "swallow" the pulse from *dclock* resulting in no edges being applied to the PFD (no phase- frequency comparison).

19.8   Demonstrate, using simulations, charge sharing between the charge pump and loop filter using the topology seen in Fig. 19.12b (and Fig. 19.13b). Show how the topology in Fig. 19.37 helps with charge sharing (simulate with and without the x1 amplifier). For the x1 amplifier, use the n-type diff-amp from Fig. 18.17 without the inverter on its output. Connect the loop filter to the gate of M1 (in the diff-amp). To make the gain "1," tie the output (which is connected to drains of M1L/M2L in Fig. 19.37) of the diff-amp (the drains of M2/M4) to the gate of M2.

19.9 Using the VCO that generated the simulation data in Fig. 19.18, plot the VCO's center frequency against changes in *VDD*. Is this VCO insensitive to changes in *VDD*? Where does the sensitivity come from?

19.10 Discuss, and demonstrate with simulations, how to reduce the gain of the VCO used to generate the data in Fig. 19.18 (see Fig. 19.25 and the associated discussion). Your discussion should include some insight into the manufacturability of low-gain VCOs.

19.11 Design and simulate the operation of a 100 MHz VCO using the topology seen in Fig. 19.19a. The output of your VCO should be full logic levels. Your design should show a linearly frequency against V_{inVCO} curve. What is the gain of your design?

19.12 Using the step response of an RLC circuit, Fig. 19.76, demonstrate how selection of the resistor, inductor, and capacitor affect the output voltage's damping factor and natural frequency. From this plot show how natural frequency and lock time are related.
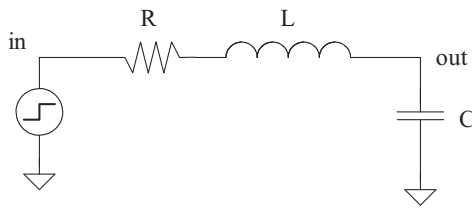

Figure 19.76 Using a second-order circuit to demonstrate how lock time and natural frequency are related.

19.13 Replace, in the DPLL that generated the waveforms in Figs. 19.27 and 19.28, the simple RC loop filter with the passive lag loop filter in Fig. 19.29. Show how the filter's component values are selected. Comment on, using simulations to support your conclusions, how the performance of the DPLL is affected.

19.14 Using the PFD in Fig. 19.33 and the charge pump in Fig. 19.36, demonstrate, with simulations, how the gain of PFD/charge-pump configuration can have a dead zone (the gain, K_{PDI}, decreases) as seen in Fig. 19.77.
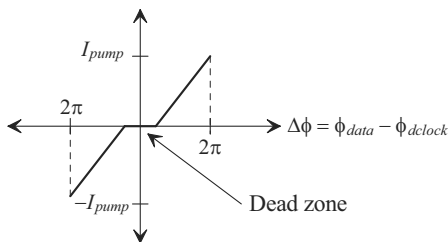

Figure 19.77 Showing the dead zone in a PFD/charge-pump.

19.15 Suppose that the pump currents used in the DPLL in Ex. 19.5 are mismatched by 50%. Will this cause a static phase error? Why or why not? Use simulations to support your answer.

19.16 Redesign the DPLL in Ex. 19.5 so that the output remains a 100 MHz square wave signal when the input signal is changed to 25 MHz.

19.17 We used pF values for the capacitors in the loop filters in this chapter. Why not reduce the filter's layout area by using fF size capacitors? Demonstrate the problems with using such small loop filter capacitors.

19.18 What are we sacrificing by using an equalizer? What does the minus sign indicate in the slope of the phase in Fig. 19.41?

19.19 Using the DPLL from Ex. 19.2, demonstrate the false locking as seen in Fig. 19.46.

19.20 Design an edge detector, like the one seen in Fig. 19.47, for use in the DPLL in Ex. 19.2. Regenerate the simulation data seen in Figs. 19.27 and 19.28. Remember to eliminate the divide by two in the feedback path.

19.21 Derive Eq. (19.71).

19.22 Design a nominal delay line of 1 ns (when $V_{indel} = 500$ mV) using the current starved delay element seen in Fig. 19.55. Determine the delay's sensitivity to variations in VDD.

19.23 Repeat Problem 19.22 for the inverter delay cell in Fig. 19.55.

19.24 Suppose, as seen in Fig. 19.78, that instead of using a half-replica of the delay cell in Fig. 19.58, the full delay cell is used to generate V_{rbias}. Electrically is there any difference in V_{rbias} when comparing the full- and half-replica circuits? What may be the benefit of using a full-replica of the delay cell?
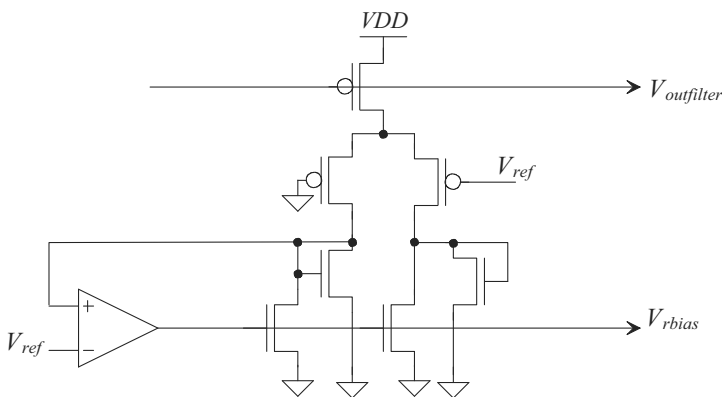

Figure 19.78 Using a full-replica of the delay element for generating Vrbias.

19.25 For the delay line that generated the simulation results in Fig. 19.62 determine, using simulations, the delay's sensitivity to changes VDD. Plot the VCDL's delay as a function of VDD with V_{indel} held at 500 mV.

19.26 The delay element seen in Fig. 19.79 doesn't use a reference voltage. Show how this element can be used in the VCDL of Fig. 19.61. Note that the input capacitance of this delay stage is twice as large as the input capacitance of the element in Fig. 19.61 (and so you may have to use fewer stages to attain the same overall delay). How does the NMOS gate potential change with the inputs/outputs switching? Why? Is the output amplitude a function of VDD?
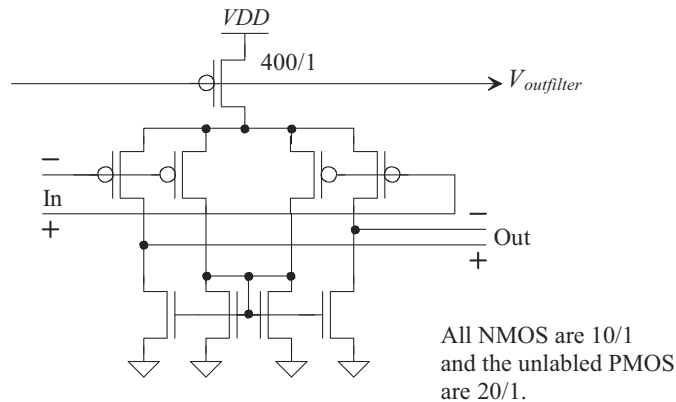

Figure 19.79   A delay element that doesn't use a reference voltage.

19.27 Use the delay element in Fig. 19.67 to implement a VCDL. Use the VCDL in the DLL seen Fig. 19.65 to generate the waveforms in Fig. 19.66. Show the 90, 180, 270, and 360 degree outputs of the VCDL swinging to full-logic levels.

19.28 The VCO output seen in Fig. 19.68 doesn't have an exactly 50% duty cycle. Will this affect a clock-recovery circuit's operation? Why or why not? Use simulations to support you answer.

19.29 Suggest another method, other than the one seen in Fig. 19.72, to equalize the widths of the *Increase* and *Decrease* outputs of the Hogge PD. Verify your design with simulations.

19.30 Must the currents in the charge pump in Fig. 19.73 be equal for proper DPLL clock-recovery operation? Why or why not? What happens if the currents aren't equal? What happens if the NMOS switches turn on at different speeds than the PMOS switches? Use SPICE to support your answers.

19.31 Modify the simulation inputs in Fig. 19.74 to show false locking. Comment on what can be done in a practical clock-recovery circuit to eliminate false locking.

19.32 Replace the charge pump used in the DPLL in Fig. 19.73 with the active-PI loop filter seen in Fig. 19.50. Calculate the loop filter component values. Using the new loop filter, regenerate Figs. 19.74 and 19.75.

PROBLEMS

20.1   Using the CMOS long-channel process (1 μm), determine the current flowing in
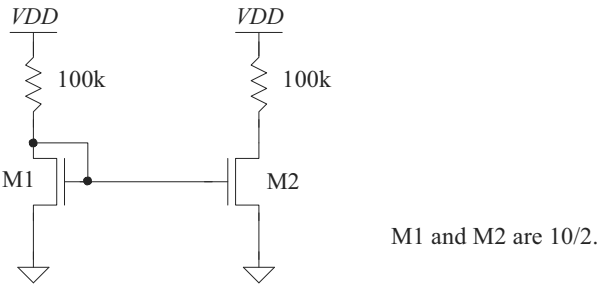the circuit seen in Fig. 20.51. Verify your answer with SPICE.

Figure 20.51   Current mirror used in Problem 20.1.

20.2   Repeat problem 20.1 for the circuit in Fig. 20.52. Can M1 and M2 be replaced
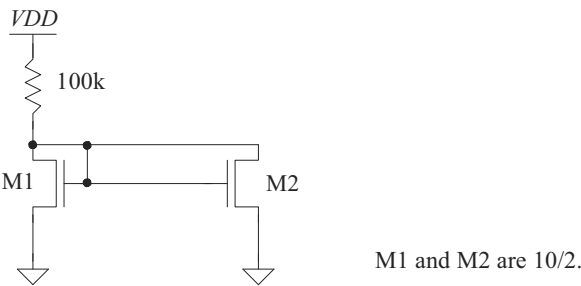with a single MOSFET? If so how and what size? If not why?

Figure 20.52   Circuit used in Problem 20.2.

20.3   Show the SPICE simulations for the PMOS devices in Ex. 20.1.

20.4   A threshold voltage mismatch in SPICE can be modeled by adding a small voltage
source in series with the gate of one of the MOSFETs, as seen in Fig. 20.53.
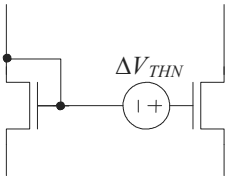Show, using SPICE, that Eq. (20.8) is valid.

Figure 20.53   Modeling an offset voltage in SPICE (or for hand calculations).

20.5 Show, using simulations and hand-calculations, that by using a larger value of $V_{DS,sat}$ when designing bias circuits, the MOSFETs enter the triode region earlier.

20.6 In Ex. 20.2, how does the gate voltage of M1/M2 change as *VDD* is decreased? How does the V_{SG} change? Use SPICE to verify your answers.

20.7 For the same bias current used in Table 9.1 (nominally 20 μA), regenerate Fig. 20.13 if minimum-length MOSFETs are used in the current mirror. Show the hand calculations leading to the selection of the MOSFET sizes.

20.8 Suppose that the bias circuit used to generate Fig. 20.16 shows a reference current change with *VDD,* as seen in Fig. 20.54. Knowing that the reference current should be constant with changes in *VDD,* what is wrong with the reference? (What important portion of the reference is causing the problem?)
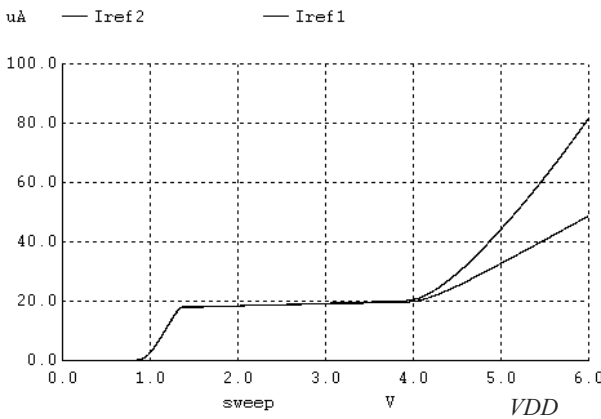

Figure 20.54   Problems with reference current increasing with VDD.

20.9 Using hand calculations, estimate the value of the voltage across *R* for the current reference in Fig. 20.15.

20.10 Using SPICE, determine if the reference circuit seen in Fig. 20.22 can become unstable with changes in *VDD*. Show that reducing the size of MCP and MCN affects the stability of the circuit.

20.11 Estimate the temperature behavior of the gate voltage of M1 in Fig. 20.10.

20.12 Design a voltage reference using the Beta-multiplier in the short-channel process and the data from Table 9.2. Generate a figure similar to Fig. 20.27 to show the temperature performance of your design.

20.13 *K* can be used to minimize *R* in Eq. (20.46) for a fixed-reference current. If M1/M2 experience a threshold voltage mismatch (see problem 20.4), discuss and show with simulations how much ΔV_{THN} can be tolerated and the error in the reference current that results.

20.14 Using an AC test voltage, determine the output resistance of the MOSFET current mirror seen in Fig. 20.28.

20.15 Based on the data in Table 9.1, what are the voltages on the drain, gate, and source terminals of M1–M4 in Fig. 20.29, assuming that the devices are operating in the saturation region? Compare your hand calculations to simulations.

20.16 If the MOSFET in Fig. 20.55 is operating in the saturation region, determine the small-signal resistance looking into its drain.

Figure 20.55   Resistance looking into the drain of a MOSFET with a source resistance. See Problem 20.16.

20.17 Suppose that the wide-swing current mirror seen in Fig. 20.38 is implemented in the long-channel CMOS process (Table 9.1). Estimate the size of MWS when M3 triodes. Verify your answer with simulations.

20.18 Label the voltages, based on the values in Table 9.1, in the schematic of the general biasing circuits seen in Fig. 20.43. Compare the tabulated values of V_{GS}, V_{DS}, etc., to the simulated values.

20.19 How would the current in Fig. 20.44 change if the width of the device connected to V_{bias2} were doubled? Were halved? Why? Explain what is going on in the circuit.

20.20 Should the voltage labeled "Out" in Fig. 20.49 be at a specific value? Why or why not?

PROBLEMS

21.1 Using simulations, show that the small-signal resistance of a gate-drain-connected PMOS device, Fig. 21.57, behaves like a resistor with a value of $1/g_m$.
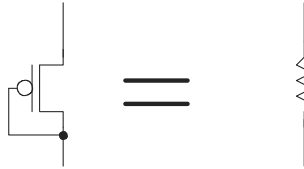

Figure 21.57 The small-signal behavior of a diode-connected MOSFET.

21.2 Estimate the frequency response of the circuit seen in Fig. 21.58. Verify your hand calculations using SPICE.
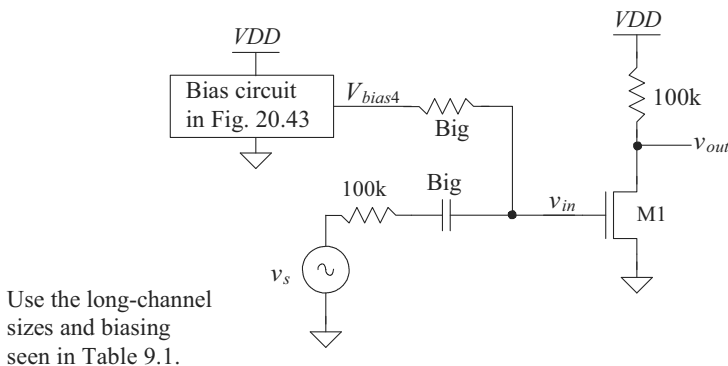

Figure 21.58 Amplifier used in Problem 21.2.

21.3 Repeat problem 21.2 if the amplifier drives a 100 fF load capacitance.

21.4 For the circuit in Fig. 21.12, estimate the effective transconductance of the circuit, g_{meff}, that relates the MOSFET drain current to the AC input voltage, v_{in}. Verify your solution with SPICE.

21.5 Simulate the operation of the common-gate amplifier in Fig. 21.16 using the bias circuit in Fig. 20.43 and the device sizes seen in Table 9.1. Compare the simulation results to hand calculations.

21.6 Estimate the transfer function of the amplifier in Ex. 21.6 if it drives a 100 fF load. Verify your hand calculations using simulations.

21.7 Determine the frequency response of the amplifier seen in Fig. 21.59. Verify your hand calculations using simulations.
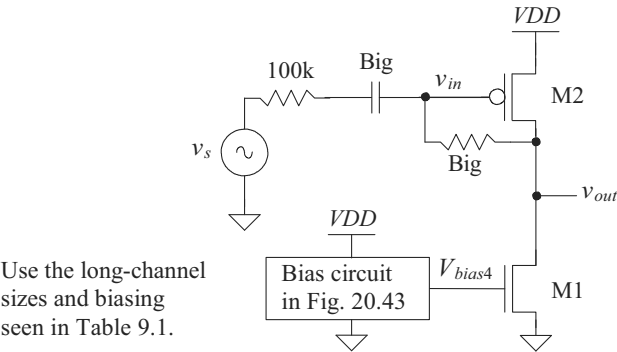
Figure 21.59 Amplifier for Problem 21.7.

21.8   Repeat Ex. 21.9 using the biasing circuit from Fig. 20.47 and the sizes in Table 9.2.

21.9   Repeat Ex. 21.10 using the biasing circuit from Fig. 20.47 and the sizes in Table 9.2.

21.10 Repeat Ex. 21.12 using the biasing circuit from Fig. 20.43 and the sizes in Table 9.1.

21.11 Show, using SPICE simulations and an ideal current source of 10 µA (device size from Table 9.2), the difference in the voltage gains with and without body effect for the circuit seen in Fig. 21.60.
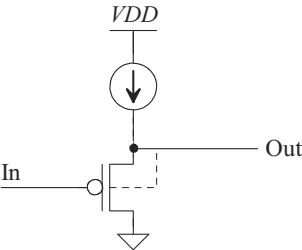

Figure 21.60   Gain of an SF with and without body effect for Problem 21.11.

21.12 Does the SF in Fig. 21.46 exhibit slew-rate limitations if it needs to discharge the 1-pF load capacitance quickly? Why or why not? Verify your answer using simulations.

21.13 Simulate the operation of the class AB output buffer in Fig. 21.48 using the bias circuit from Fig. 20.47 and the sizes in Table 9.2. If the buffer is driving a load resistor of 10k, plot v_{in} against v_{out}. What is the linear output range?

21.14 In the class AB output buffer in Fig. 21.50 or 21.51, a load resistor connected to ground causes the PMOS device to conduct more current then the NMOS. Why? Resimulate the buffer in Fig. 21.51 if it drives a 1k resistor and MON is reduced in size to 50/2. Is this a better design? Why or why not?

21.15 Using simulations, show the problem of using an inverter output buffer without a floating current source as seen in Fig. 21.53. (The quiescent current that flows in the MOSFETs is huge and not accurately controlled as it is in Fig. 21.50.)

21.16 Is the distortion the output buffer in Fig. 21.56 introduces into a signal a function of the load resistance? Verify your answer with simulations and show some time-domain waveforms with and without distortion.

PROBLEMS

22.1   Determine the drain current of M1 as a function of the input voltage, $v_{I1} - v_{I2}$, for the diff-amp shown in Fig. 22.36. Neglect body effect. What does your derivation give for i_{D1} when v_{I1} is much larger than v_{I2}?
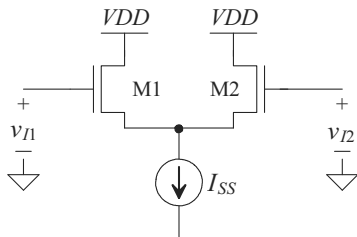

Figure 22.36 Diff-amp used in Problem 22.1

22.2   Repeat Ex. 22.1 if the widths of M1 and M2 are increased from 10 to 100. Determine the transconductance of the diff-amp. Write i_{d2} as a product of g_m ($= g_{m1} = g_{m2}$) and v_{I1} (with v_{I2} = AC ground), v_{I2} (with v_{I1} = AC ground), and $v_{I1} - v_{I2}$.

22.3   Determine the maximum and minimum common mode voltages for the PMOS version of the diff-amp seen in Fig. 22.4.

22.4   Determine the AC currents flowing in the circuit of Fig. 22.5 if the gate of M1 is grounded and the gate of M2 is an AC signal of 1 mV. Verify your answers with an AC SPICE simulation.

22.5   Determine the small-signal gain and the input common-mode-range (CMR) for the diff-amps shown in Fig. 22.37. Verify your answers with SPICE.
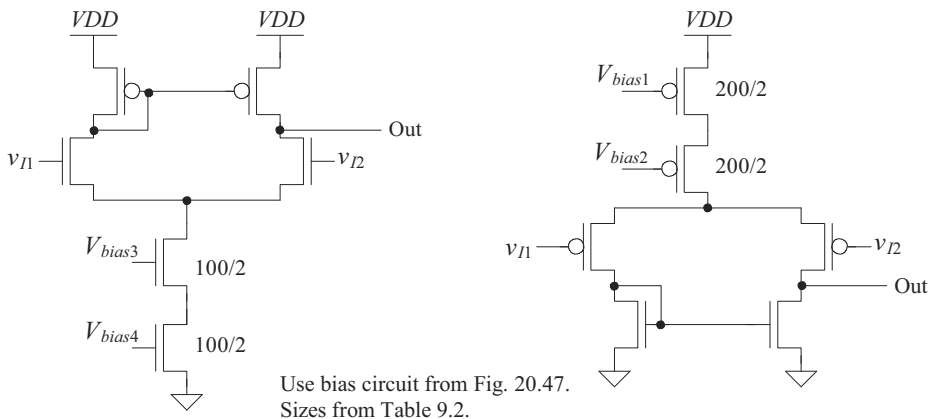

Use bias circuit from Fig. 20.47.
Sizes from Table 9.2.

Figure 22.37 Diff-amps for Problem 22.5.

22.6   Show that the capacitance on the sources of M1/M2 in Ex. 22.6 causes the *CMRR* to roll off quicker with increasing frequency. (Add a capacitance to the sources of M1/M2 in a simulation and show that *CMRR* decreases at a lower frequency.)

22.7   Estimate the slew-rate limitations in charging and discharging a 1 pF capacitor tied to the outputs of the diff-amps shown in Fig. 22.37. Verify with SPICE.

22.8   For the n-channel diff-pair shown in Fig. 22.38, show that the following relationships are valid if the body effect is included in the analysis of the transconductance.

$$i_{d1} = \frac{g_m}{2}\left[v_{i1}\left(2 - \frac{g_m}{g_m + g_{mb}} \right) - v_{i2} \cdot \frac{g_m}{g_m + g_{mb}} \right] - \frac{g_m \cdot g_{mb}}{g_m + g_{mb}} \cdot \frac{[v_{i1} + v_{i2}]}{2}$$

and

$$i_{d2} = \frac{g_m}{2}\left[v_{i2}\left(2 - \frac{g_m}{g_m + g_{mb}} \right) - v_{i1} \cdot \frac{g_m}{g_m + g_{mb}} \right] - \frac{g_m \cdot g_{mb}}{g_m + g_{mb}} \cdot \frac{[v_{i1} + v_{i2}]}{2}$$
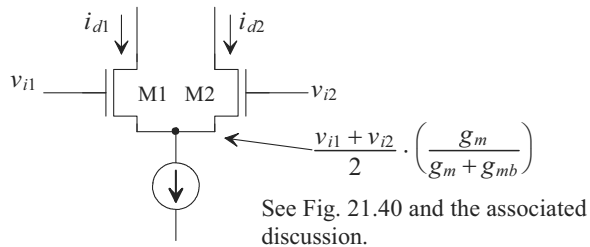

Figure 22.38   How body effect changes the AC behavior of the diff-amp.

22.9   The diff-amp configuration shown in Fig. 22.39 is useful in situations where a truly differential output signal is needed. Determine the following: (a) the transconductance of the diff-amp, (b) the AC small-signal drain currents of all MOSFETs in terms of the input voltages and g_{mn} (the transconductance of an n-channel MOSFET), and (c) the small-signal voltage gain, $(v_{O+} - v_{O-})/(v_{I+} - v_{I-})$. Verify your answers with SPICE.

22.10   Using the diff-amp topology in Fig. 22.24 and a current mirror load, show how quickly (or slowly) the diff-amp can drive a 1 pF load. Does this diff-amp exhibit slew-rate limitations? Verify your answers with SPICE.

22.11   Using the topology seen in Fig. 22.26 with the long-channel process (Table 9.1) without body effect (all MOSFET's bodies tied to their respective sources), show that the currents in M1–M4 match the biasing currents used in the source followers. Show how the currents become mismatched when the bodies of the NMOS are tied to ground and the bodies of PMOS are tied to *VDD*.
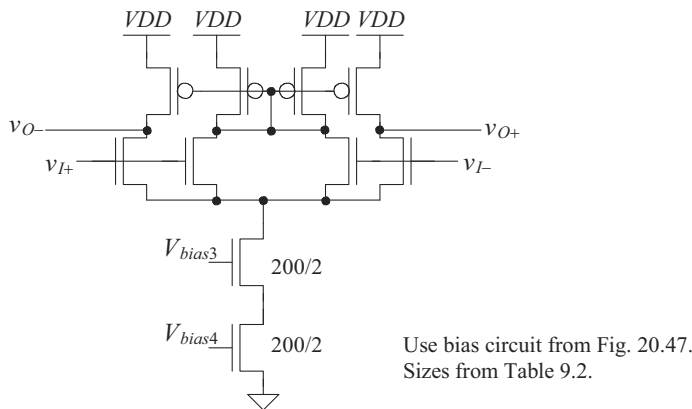
Figure 22.39   Fully differential diff-amp used in Problem 22.9.

22.12   Simulate the operation of the diff-amp seen in Fig. 22.31. Use a common-mode voltage of 2.5 V and an AC input voltage of 100 μV at 1 kHz. Compare the simulation results to your hand calculations.

22.13   Using SPICE with current sources for inputs, show the operation of the diff-amp in Fig. 22.33.

22.14   The circuit seen in Fig. 22.40 is an another example of a circuit that sums the currents from NMOS and PMOS diff-amps (so the input common-mode range can extend from beyond the power supply rails). Describe and simulate the operation of this circuit using the short-channel parameters in Table 9.2 and the bias circuit from Fig. 20.47.
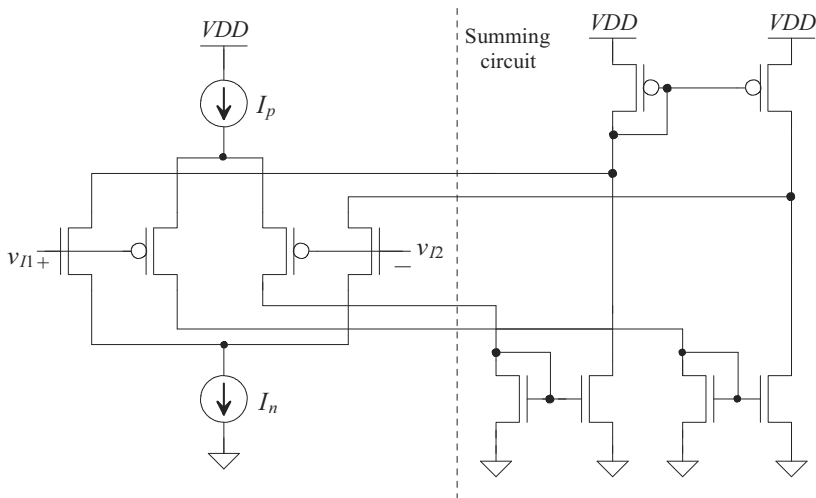

Figure 22.40   Summing circuit for Problem 22.14.

22.15 Using symbolic analysis, determine the small-signal gain of the self-biased diff-amp seen in Fig. 22.41 (see also Fig. 18.17).
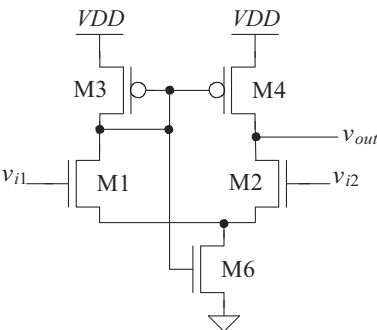

Figure 22.41   A self-biased NMOS diff-amp.

ADDITIONAL READING

[1]   K. N. Leung and P. K. T. Mok, "A Sub-1-V 15-ppm/C CMOS Bandgap Voltage Reference Without Requiring Low Threshold Voltage Device," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 4, April 2002, pp. 526–530. Develops the scheme seen in Fig. 23.33 for lowering the input common-mode range of the added amplifier.

[2]   H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS Bandgap Reference Circuit with Sub-1-V Operation," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, May 1999, pp. 670–674. Presents the design of the lower voltage BGR seen in Fig. 23.30.

[3]   G. Tzanateas, C. A. T. Salama, and Y. P. Tsividis, "A CMOS Bandgap Voltage Reference," *IEEE Journal of Solid-State Circuits*, vol. SC-13, no. 3, June 1979, pp. 655–657. Good paper discussing BGR reference design.

[4]   E. Vittoz and J. Fellrath, "CMOS Analog Integrated Circuits Based on Weak Inversion Operation," *IEEE Journal of Solid-State Circuits*, vol. SC-12, no. 3, June 1977, pp. 224–231. Covers the BMR design operating in the weak inversion region.

[5]   K. E. Kuijk, "A Precision Reference Voltage Source," *IEEE Journal of Solid-State Circuits*, vol. SC-8, no. 3, June 1973, pp. 222–226. Development of the BGR seen in Fig. 23.29b.

PROBLEMS

23.1   Using the MOSFET-only reference seen in Fig. 23.2, design a nominally 500 mV reference in the short-channel CMOS process. Using simulations, characterize the sensitivity of the reference voltage to changes in *VDD* and temperature.

23.2   Use the long-channel CMOS process and the topology seen in Fig. 23.6 to design a voltage reference of $3V_{THN}$. Simulate your design and show the *VDD* sensitivity and temperature behavior of the reference. Do TCs of R_1 and R_2 affect the performance of the reference? Why or why not?

23.3   Suppose it was desired, in Fig. 23.7 (see also Fig. 20.22), to make M1 and M2 the same size. However, to increase the gate source voltage of M1, relative to M2, the width of M3 is increased by K. How do the equations governing the operation of the BMR change? How does the current flowing in the BMR change?

23.4   Verify that if the PMOS devices in Fig. 23.11 are not cascoded (that is, they have only NMOS cascodes), the currents in each branch will not be equal and there will be significant sensitivity to *VDD* (a sensitivity similar to what is seen in Fig. 23.10).

23.5   In a CMOS process, several of the layers including poly, n+, p+, and n-well can be used for resistor formation. Each of these layers has a different temperature coefficient (TC). For the BMR that generated Fig. 23.14, use simulations to determine the optimum resistor TC.

23.6   Derive the equations that govern the operation of the reference in Fig. 23.16b.

23.7   Show why n+ directly in the p-substrate cannot be used as a diode in a CMOS process.

23.8   Generate a diode model that produces a forward voltage drop of 700 mV when driven with 1 μA and has a change with temperature, dV_D/dT, near room temperature, of −2 mV/C. Use simulations to verify your model meets the requirements.

23.9   Generate a SPICE model for the Schottky diode seen in Fig. 23.21. Assume that the series resistance of the diode is 1 kΩ.

23.10 Estimate, using hand calculations, the minimum allowable *VDD* for the reference of Ex. 23.4. What are the PMOS and NMOS gate-source and drain-source voltages when the reference current is 1 μA? Note that the parameters in Table 9.1 have nothing to do with the operating conditions in this question. Verify your answers using SPICE.

23.11 Show that *K* forward-biased diodes in parallel behave like a single diode with a scale current of $K{\cdot}I_S$, as assumed in Eq. (23.30).

23.12 Suggest a reference design that would output a voltage of $n \cdot V_T$.

23.13 Determine whether the performance of the BGR of Fig. 23.32 can be enhanced by using the topology of Fig. 23.33. Use simulations to verify your answer.

PROBLEMS

24.1   Suggest, and verify with simulations, a method for reducing the minimum input common-mode voltage of the op-amp in Fig. 24.2.

24.2   Redesign the bias circuit for the op-amp in Fig. 24.2 for minimum power. Compare the power dissipation of your new op-amp design (actually the bias circuit) to the design in Fig. 24.2. Using your redesign, generate the plots seen in Fig. 24.3.

24.3   Show, using simulations, how a 1% mismatch in the widths of M1 and M2 in the op-amp of Fig. 24.2 affect the op-amp's input-referred offset voltage. Compare this offset to the offset caused by a 1% mismatch in the widths of M3 and M4. Quantitatively explain why one is worse than the other.

24.4   Simulate the use of the "zero-nulling" circuit in Fig. 24.15 in the op-amp of Fig. 24.8. Show AC, operating-point, and transient (step) operation of the resulting op-amp. Verify with the .op analysis that the gate of MP1 is at the same potential as the gate of M7 in quiescent conditions.

24.5   When we derived Eq. (24.24), we lumped C_c into C_2 and neglected the effects of MCG. A more accurate model for the indirect compensation, assuming $C_L \gg$ the output capacitance of the amplifier, is seen in Fig. 24.64. Using this model, estimate the location of the output pole.
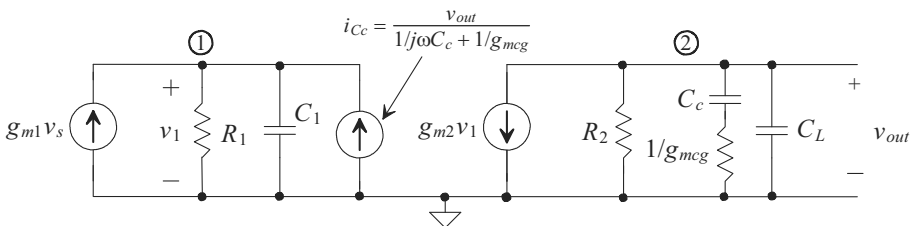

Figure 24.64   Model used to estimate bandwidth when indirect feedback current. See Problem 24.5.

24.6   Regenerate Fig. 24.19 using a 2.4 pF compensation capacitor. On the resulting simulation output, label the location f_1, f_2, f_z, and f_{un}. How do the simulated results compare to the hand calculated values?

24.7   For the op-amp in Fig. 24.21, determine the *CMRR* using hand calculations. Verify your hand calculations using simulations. How does the *CMRR* change based on the DC common-mode voltage?

24.8   Simulate the *PSRR*s for the op-amp in Fig. 24.8 (with an R_z of 6.5k and a C_c of 2.4 pF) and compare the results to the op-amp in Fig. 24.21 when C_c is set to (also) 2.4 pF (so each op-amp has the same gain-bandwidth).

24.9   Simulate the operation of the op-amp in Fig. 24.28. Show the open-loop frequency response of the op-amp. What is the op-amp's PM? Show the op-amp's step response when it is put into a follower configuration driving a 100 fF load with an input step in voltage from 100 mV to 900 mV.

24.10 The op-amp seen in Fig. 24.29 has a gain-bandwidth product (f_{un}) of about 100 MHz. Suppose that this op-amp is used in the amplifier seen in Fig. 24.65 (gain of −5). Estimate the amplifier's closed loop bandwidth (where the output of the amplifier is −3 dB down from its low-frequency value) using Eq. (24.34). Verify your results using simulations (transient analysis). What are the maximum and minimum voltages allowable for an input sinewave if the output voltage of the amplifier must lie between 100 and 900 mV?
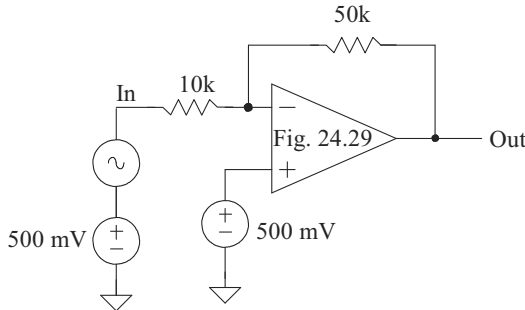

Figure 24.65 Amplifier used for Problem 24.10.

24.11 Suppose it is decided to eliminate the 500 mV common-mode voltage in the amplifier seen in Fig. 24.65 and use ground, as seen in Fig. 24.66. Knowing that the input voltage can only fall between ground and *VDD,* what is the problem one will encounter?
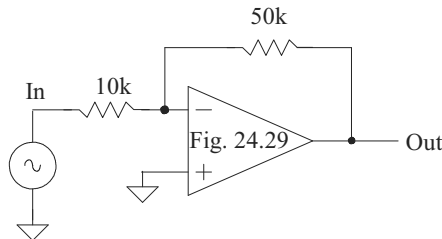

Figure 24.66 Amplifier used for Problem 24.11. What's wrong with this topology?

24.12 To limit the current flowing in MOP or MON in the op-amp of Fig. 24.29 (to protect the op-amp from destruction if its output is shorted to ground, for example), we may add 100 Ω resistors, as seen in Fig. 24.67. What is the maximum amount of current this modified op-amp can source/sink? How is the closed-loop output resistance of the op-amp affected. (Hint: see Eq. (24.70).) Simulate the operation of the op-amp using the topology seen in Fig. 24.31. Is there any noticeable difference between the simulation output in Fig. 24.31 and the output with the 100 Ω resistors present?
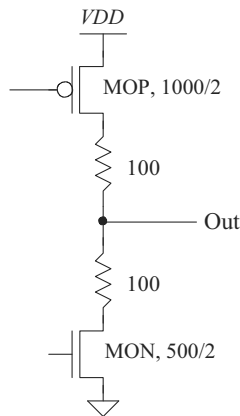
Figure 24.67 Adding resistors to the output of the op-amp in Fig. 24.29
for short circuit protection. See Problem 24.12.

24.13 Resimulate the OTA in Fig. 24.33 driving a 1 pF load (to determine f_{un}) if K = 10. How do the simulation results compare to the hand calculations using Eq. (24.41)? Estimate the parasitic poles associated with the gates of M4 and M5 (for example, the pole associated with the gate of M4 is $\approx 1/g_{m41} \cdot C_{sg4}$). Are these poles comparable to f_{un}?

24.14 Using the OTA in Fig. 24.35, design a lowpass filter with a 3 dB frequency of 1 MHz.

24.15 Suppose M8T in the op-amp of Fig. 24.37 is removed and replaced with a short from the output to the drain of M8B. How will the gain be affected? Verify your answer with SPICE.

24.16 Suppose, to simulate the open-loop gain of an OTA, the big resistor and capacitor used in Fig. 24.43 are removed and the inverting input is connected to 500 mV. Will this work? Why or why not? What happens if the OTA doesn't have an offset voltage? Will it work then?

24.17 Why is the noninverting topology (Fig. 24.49) inherently faster than the inverting topology (Fig. 24.39). What are the feedback factors, β, for each topology. Use the op-amp in Fig. 24.48 to compare the settling times for a +1 and a −1 amplifier driving 10 pF.

24.18 Suppose, to reduce power, the lengths of the current sources used in the amplifiers seen in Fig. 24.50 are increased from 2 to 10. Will the AC performance of the op-amp used to generate Fig. 24.53 change with this modification? Why or why not? Verify your answer using a SPICE simulation. Compare the currents used in the modified op-amp (with the lower power GE diff-amps) to the current seen in Fig. 24.53.

24.19 To increase the gain of the op-amp in Fig. 24.51, we may replace the GE diff-amps with folded-cascode OTAs. Will we need source-follower level-shifters

in the new design? Regenerate the simulation data seen in Fig. 24.53 using the folded-cascode OTAs.

24.20 Suppose an op-amp is to be used to amplify 250 mV to 500 mV with an error less than 1 mV. Estimate the minimum required op-amp open loop gain.

24.21 Design a voltage regulator to supply at least 50 mA of current at 500 mV with a *VDD* as low as 600 mV. Assume that a 500 mV voltage reference is available and that the load capacitance is, minimum, 1,000 pF. How does the design respond to a load current pulse from 0 to 50 mA? Use SPICE to verify your design.

24.22 Using the nominal sizes from Table 9.2 and the bias circuit in Fig. 20.47, simulate, using an .op analysis, the operation of the op-amp in Fig. 24.58 in the configuration seen in Fig. 24.9. What is the current flowing in M7 and M8 when *VDD* is 1 V? is 1.2 V?

24.23 Repeat Problem 24.22 for the op-amp in Fig. 24.59.

24.24 Using the information from Table 9.2 and the bias circuit in Fig. 20.47, demonstrate the operation (AC and transient) of the op-amp in Fig. 24.60 driving a 100 fF load. Show that the bias current pulled from *VDD* is relatively constant for a *VDD* of 1 or 1.2 V (put the op-amp in the configuration seen in Fig. 24.9).

24.25 Replace the common-source output stage in the op-amp of Fig. 24.61 with a class AB output stage like the one seen in Fig. 24.60. Simulate the operation of the amplifier (AC and transient).

[16]   K. Martin, "Improved Circuits for the Realization of Switched-Capacitor Filters,"
        IEEE Transactions on Circuits and Systems, vol. CAS-25, no. 4, pp. 237–244,
        April 1980.

[17]   R. W. Broderson, P. R. Gray, and D. A. Hodges, "MOS Switched-Capacitor
        Filters," *Proceedings of the IEEE,* vol. 67, no. 1, January 1979.

[18]   D. J. Allstot, R. W. Broderson, and P. R. Gray, "MOS Switched-Capacitor Ladder
        Filters," *IEEE Journal of Solid-State Circuits,* vol. SC-13, no. 6, pp. 806–814,
        December 1978.

[19]   J. McCreary and P. R. Gray, "All MOS Charge Redistribution Analog-to-Digital
        Conversion Techniques - Part 1," *IEEE Journal of Solid State Circuits*, vol. 10,
        pp. 371–379, December 1975.

PROBLEMS

In the following problems, where appropriate, use the short-channel CMOS process with
a scale factor of 50 nm and a *VDD* of 1 V.

25.1   Using SPICE simulations, show the effects of clock feedthrough on the voltage
        across the load capacitor for the switch circuits shown in Fig. 25.40. How does
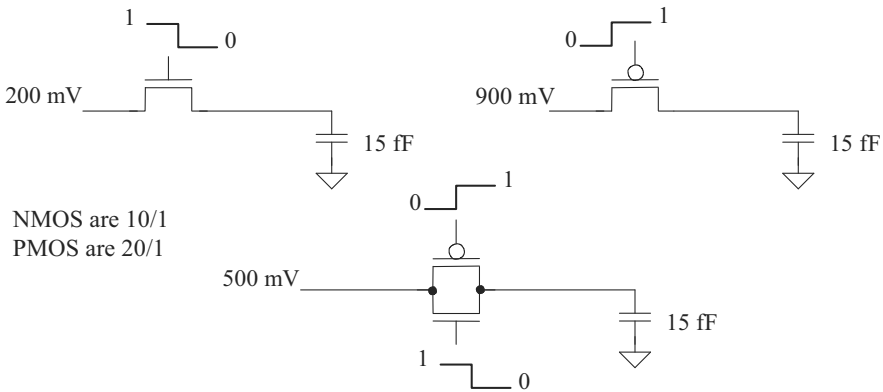   this voltage change if the capacitor value is increased to 100fF?

Figure 25.40 Circuits used in Problem 25.1 to show clock feedthrough.

25.2   Repeat problem 25.1 if dummy switches are used. Show schematics of how the
        dummy switches are added to the schematics.

25.3   Using a voltage-controlled voltage source for the op-amp (see Fig. 20.19 for
        example) with an open-loop gain of 10^6, use SPICE to show how the track-and-
        hold seen Fig. 25.8 operates with a sinewave input. What happens if the input
        sinewave's amplitude is above $VDD-V_{THN}$? Use a 100 MHz clock (strobe) pulse
        with a 50% duty cycle and an input sinewave frequency of 5 MHz. Note that the
        input sinewave should be centered around V_{CM} (= 500 mV).

25.4 Using the topology seen in Fig. 25.13a and the SPICE op-amp model in Fig. 25.18, show how both V_{in} and V_{CM} can be varied while the op-amp's inputs are equal, that is, $v_p \approx v_m$. Is the output common-mode voltage always at V_{CM} using the simple SPICE model for the fully-differential output op-amp in Fig. 25.18? Why or why not? Give an example supporting your answer.

25.5 Suppose, in Fig. 25.19, that instead of the two input sine waves being connected to ground they are tied (together) to a common mode signal (say a noise voltage). Show that a common mode signal (like a sine wave) won't change the circuits' output signals. The amplitude of the common-mode signal shouldn't be so large that the NMOS switches shut off.

25.6 Show that the switched-capacitor circuits shown in Fig. 25.41 behave like resistors, for $f \ll f_{clk}$, with the resistor values shown.
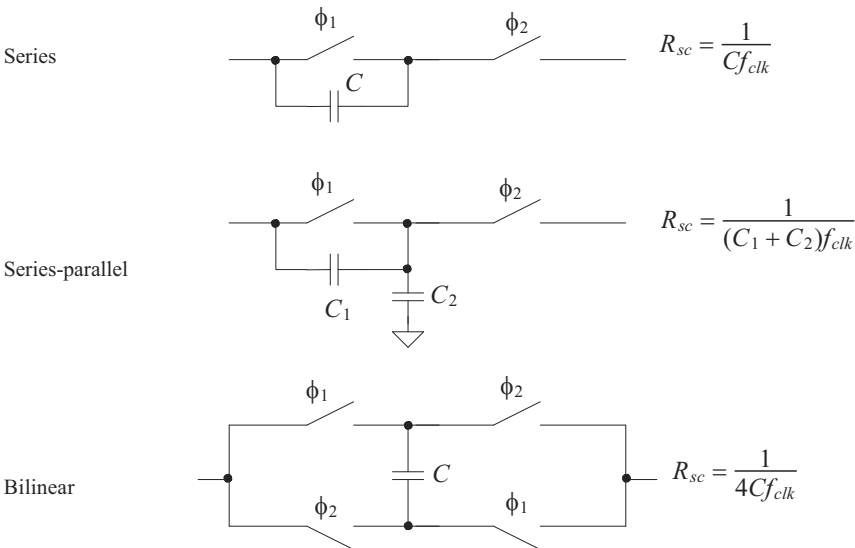

Figure 25.41 Alternative forms of switched-capacitor resistors.

25.7 Simulate the operation of the switched-capacitor resistor seen in Fig. 25.21. Plot the mean of the current flowing in the voltage sources v_1 or v_2 to show that the circuit actually behaves like a resistor. Comment on the selection of the bottom plate of the capacitor shown in Fig. 25.21a.

25.8 Comment on the selection of the bottom plate of C_F shown in Fig. 25.23.

25.9 Sketch the schematic, similar in form to Fig. 25.23, of the fully-differential switched-capacitor integrator made using a differential input/output op-amp. What is the transfer function of this topology?

25.10 Repeat Ex. 25.2 if the low-frequency gain is 40 dB and the zero is located at 50 kHz.

25.11 Using the results given in Eq. (25.29), plot the magnitude of v_{out}/v_{in} against f/f_{clk}. Comment on the resulting plot.

25.12 An important consideration in SC circuits is the slew-rate requirements of the op-amps used. In the derivation in Fig. 25.28, we assumed that a voltage source was connected to the input of the circuit. In reality, the input of the circuit is provided by an op-amp. When ϕ_1 goes high, in this figure, the capacitor C_I is charged to the input voltage v_{in} ($= v_A$). If C_I is 5 pF and f_{clk} is 100 kHz, estimate the minimum slew-rate requirements for the op-amp providing v_{in}.

25.13 Suppose that the op-amp in problem 25.12 is used with a feedback factor of 0.5. Estimate the minimum unity gain frequency, f_{un}, that the op-amp must possess.

25.14 Simulate the operation of the dynamic comparator shown in Fig. 25.35.

[13] T. C. Choi, R. T. Kaneshiro, R. Broderson, and P. R. Gray, "High-Frequency CMOS Switched Capacitor Filters for Communication Applications," *IEEE Journal of Solid State Circuits,* vol. SC-18, pp. 652–664, December 1983.

[14] D. Senderowicz, S. F. Dreyer, J. H. Huggins, C. F. Rahim, and C. A. Laber, "A family of differential NMOS analog circuits for a PCM codec filter chip," *IEEE Journal of Solid-State Circuits,* vol. 17, pp. 1014–1023, December 1982.

PROBLEMS

Unless otherwise indicated, use the 50 nm CMOS process from the examples in this chapter, the biasing circuit in Fig. 26.3, and 10/1 NMOS and 20/1 PMOS.

26.1 Using simulations, determine the transition frequencies, f_T, for the NMOS and PMOS devices seen in Fig. 26.1 at the nominal operating conditions indicated in the figure. Show that by increasing the MOSFET's overdrive voltage, the f_Ts of the MOSFETs increases.

26.2 Simulate the operation of the two-stage op-amp in Fig. 26.2. Show that the quiescent current in the output buffers is considerably below the desired 20 µA. (Note that the inputs of the op-amp should be held at V_{CM} in the simulation to keep the diff-amp conducting current.) Does this affect the speed of the output buffer? Why or why not?

26.3 Plot reference current against resistor value for the BMR seen in Fig. 26.3. Use simulations to determine the I_{REF} for each value of resistance.

26.4 Comment on the benefits and/or concerns with the CMFB input connections seen in Fig. 26.61. Use simulations to support your answers. Note the similarity to the way CMFB was implemented in Fig. 26.17.
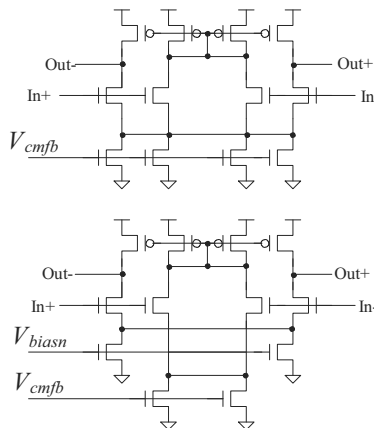

Figure 26.61 Circuits for Problem 26.4.

26.5 Verify, using simulations, that the circuit in Fig. 26.9 does indeed amplify the difference between V_{biasp} and the average on the + inputs of the amplifier.

Comment on the operation of the circuit, making sure it is clear that the limitations, uses, and operation of the amplifier are understood.

26.6   Simulate the operation of the CMFB circuit in Fig. 26.16.

26.7   Is *VDD* divided evenly amongst the drain-source voltages of the MOSFETs in Fig. 26.19? Suggest a method to better divide *VDD* amongst the MOSFETs used in the diff-amp.

26.8   Suggest a simple method to speed up the step response of the op-amp in Fig. 26.22 in the circuit of Fig. 26.24. Verify the validity of your suggestion using SPICE simulations.

26.9   Suggest an alternative method to the one seen in Fig. 26.32 for controlling the output buffer's current. Using the modification, regenerate the results seen in Fig. 26.36.

26.10   Is the CMFB loop stable in the op-amp of Fig. 26.40? Use the large-signal test circuit seen in Fig. 26.24 (at a slower frequency) and simulations to look at the stability of this loop. Suggest, and verify with simulations, methods to improve the stability of the CMFB loop.

26.11   Repeat Problem 26.10 for the op-amp in Fig. 26.43.

26.12   As discussed at the end of the chapter and in Fig. 26.59 and the associated discussion, the input common-mode voltage which drops below V_{CM}, can shut off the op-amp's input diff-amp and cause problems. The diff-amp's NMOS devices have a nominal V_{GS} of 400 mV, leaving only 100 mV across the diff-amp's tail current. Show, using the op-amp in Fig. 26.39 in the configuration seen in Fig. 26.24 with an input common-mode voltage less than 500 mV (the input pulse waveforms average to a voltage less than V_{CM}), the resulting problems. Show that increasing the widths of the NMOS diff-pair (and the mirrored NMOS in the bias circuit with gates tied to V_{CM}) from 10 to 30 helps to increase the operating range (four MOSFET widths are increased from 10 to 30). What happens if only the diff-pair widths (two MOSFETs) are increased?

26.13   Repeat Problem 26.12 for the op-amp in Fig. 26.40. What happens if the input common-mode voltage becomes greater than 500 mV?

26.14   Repeat Problem 26.12 for the op-amp in Fig. 26.43. What happens if the input common-mode voltage becomes greater than 500 mV? Why does the op-amp in Fig. 26.40 perform better with variations in the input common-mode voltage than the op-amp in Fig. 26.43?

26.15   Design and simulate the operation of an op-amp using gain-enhancement (Fig. 26.42) and with an open-loop DC gain greater than 2,000, based on the topologies seen in Figs. 26.40 or 26.43. Simulate the operation of your design and generate outputs like those seen in Fig. 26.44.

26.16   Figure 26.62 shows an op-amp based on the topology seen in Fig. 26.40 but biased for lower *VDD* operation. Select the size of the added gate-drain connected MOSFET to allow for proper operation. Simulate the operation of the design showing the DC gain and large signal step responses (as in Fig. 26.34 and 26.35).

26.17 Repeat Problem 26.16 for the op-amp in Fig. 26.43.

26.18 Using the diff-amp in Fig. 26.63 in the configuration seen in Fig. 26.54 (with SC CMFB) and the output buffer in Fig. 26.56 (again with SC CMFB), regenerate the waveforms seen in Fig. 26.60.

26.19 A switched-capacitor integrator is an example of a circuit that uses an op-amp that can't have the outputs of its diff-amp or output buffer shorted when ϕ_1 goes high. Using the diff-amp in Fig. 26.63 (with SC CMFB) and the output buffer in Fig. 26.56 without the switches (again with SC CMFB), demonstrate the operation of a SC integrator.
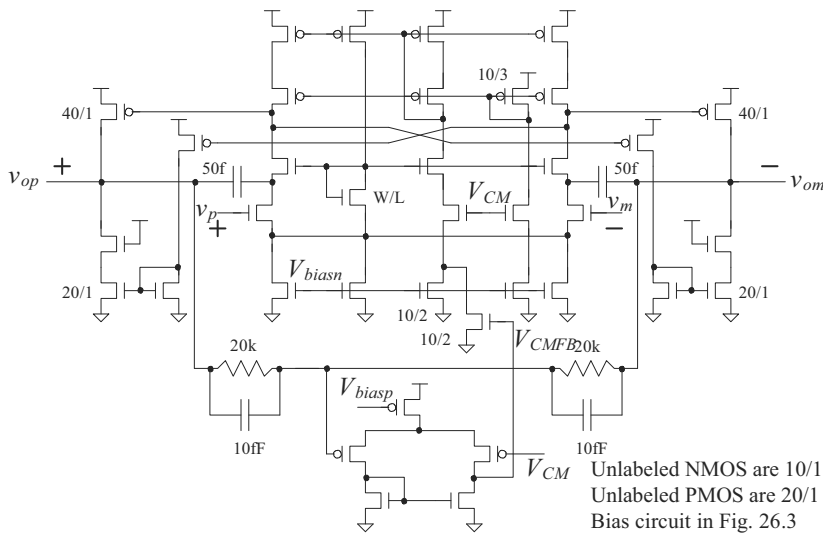
Figure 26.62 An op-amp with better biasing (but more power) for lower VDD operation.
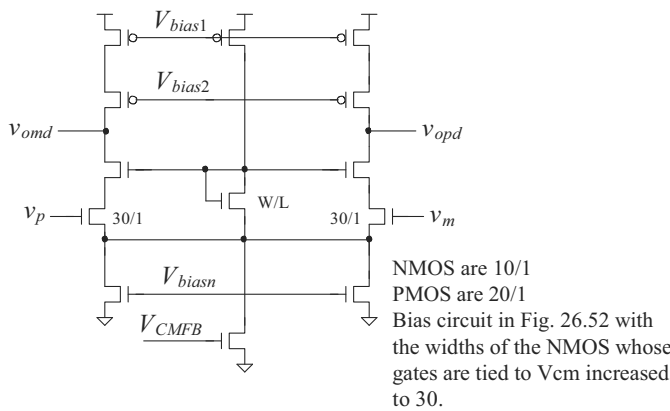

Figure 26.63 Modifying the diff-amp seen in Fig. 26.53 for wider swing operation.

[2]   E. A. Vittoz, "Micropower Techniques," Chapter 3 in J. E. Franca and Y. Tsividis (eds.) *Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing,* 2nd ed., Prentice Hall, 1994. ISBN 0-13-203639-8.

[3]   M. Ismail, S-C. Huang, and S. Sakurai, "Continuous-Time Signal Processing," Chapter 3 in M. Ismail and T. Fiez (eds.), *Analog VLSI: Signal and Information Processing*, McGraw Hill, 1994. ISBN 0-07-032386-0.

[4]   H-J. Song and C-K. Kim, "A MOS Four-Quadrant Analog Multiplier Using Simple Two-Input Squaring Circuits with Source Followers," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 3, pp. 841–848, June 1990.

[5]   B-S. Song, "CMOS RF Circuits for Data Communications Applications," *IEEE Journal of Solid-State Circuits*, vol. SC-21, no. 2, pp. 310–317, April 1986.

[6]   S. Soclof, *Applications of Analog Integrated Circuits*, Prentice Hall, 1985. ISBN 0-13-039173-5.

[7]   M. G. Degrauwe, J. Rijmenants, E. A. Vittoz, and H. J. DeMan, "Adaptive Biasing CMOS Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. SC-17, no. 3, pp. 522–528, June 1982.

[8]   D. J. Allstot, "A Precision Variable-Supply CMOS Comparator," *IEEE Journal of Solid-State Circuits,* vol. SC-17, no. 6, pp. 1080–1087, December 1982.

PROBLEMS

27.1   Using the long-channel CMOS process, compare the performance (using simulations) of the comparator in Fig. 27.8 with the comparator in Fig. 27.9. Your comparison should include DC gain, systematic offset, delay, sensitivity, and power consumption.

27.2   Show, using simulations, how the addition of a balancing resistor in Fig. 27.14 can be used to improve the response seen in Fig. 27.13.

27.3   Simulate the operation of the comparator in Fig. 27.15 in the short-channel CMOS process. Determine the comparators sensitivity and the kickback noise.

27.4   Repeat problem 27.3 for the comparator in Fig. 27.16. Show that the input common-mode range of the comparator in Fig. 27.16 extends beyond the power supply rails.

27.5   Simulate the operation of the input buffer in Fig. 27.17 in the short-channel CMOS process. How sensitive is the buffer to input slew-rate? How symmetrical are the output rise and fall times? Suggest, and verify with simulations, a method to reduce the power consumed by the input buffer.

27.6   Design a low power clocked comparator for use with a Flash ADC (discussed in Ch. 29). Use the short-channel CMOS process and a clocking frequency of 250 MHz estimate the power dissipated by 256 of these comparators.

PROBLEMS

28.1   Determine the number of quantization levels needed if one wanted to make a digital thermometer that was capable of measuring temperatures to within 0.1 °C accuracy over a range from –50 °C to 150 °C. What resolution of ADC would be required?

28.2   Using the same thermometer as above, what sampling rate, in samples per second, would be required if the temperature displayed a frequency of $15°·sin(0.01·2\pi t)$?

28.3   Determine the maximum droop allowed in an S/H used in a 16-bit ADC assuming that all other aspects of both the S/H and ADC are ideal. Assume $V_{ref} = 5$ V.

28.4   An S/H circuit settles to within 1 percent of its final value at 5 μs. What is the maximum resolution and speed with which an ADC can use this data assuming that the ADC is ideal?

28.5   A digitally programmable signal generator uses a 14-bit DAC with a 10-volt reference to generate a DC output voltage. What is the smallest incremental change at the output that can occur? What is the DAC's full-scale value? What is its accuracy?

28.6   Determine the maximum DNL (in LSBs) for a 3-bit DAC, which has the following characteristics. Does the DAC have 3-bit accuracy? If not, what is the resolution of the DAC having this characteristic?

Digital Input	Voltage Output
000	0 V
001	0.625 V
010	1.5625 V
011	2.0 V
100	2.5 V
101	3.125 V
110	3.4375 V
111	4.375 V

28.7   Repeat Problem 28.6 calculating the INL (in LSBs).

28.8   A DAC has a reference voltage of 1,000 V, and its maximum INL measures 2.5 mV. What is the maximum resolution of the converter assuming that all the other characteristics of the converter are ideal?

28.9   Determine the INL and DNL for a DAC that has a transfer curve shown in Fig. 28.33.

28.10 A DAC has a full-scale voltage of 4.97 V using a 5 V reference, and its minimum output voltage is limited by the value of one LSB. Determine the resolution and dynamic range of the converter.
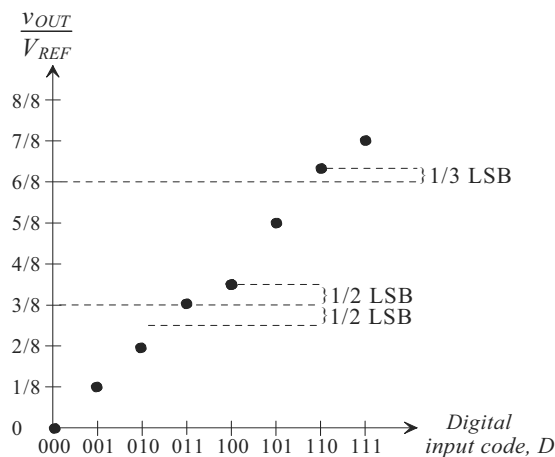
Figure 28.33 Transfer curves for Problem 28.9.

28.11 Prove that the RMS value of the quantization noise shown in Fig. 28.20b is as stated in Eq. (28.25).

28.12 An ADC has a stated *SNR* of 94 dB. Determine the effective number of bits of resolution of the converter.

28.13 Discuss the methods used to prevent aliasing and the advantages and disadvantages of each.

PROBLEMS

29.1 A 3-bit, resistor-string DAC similar to the one shown in Fig. 29.2a was designed with a desired resistor of 500 Ω. After fabrication, mismatch caused the actual value of the resistors to be

$R_1 = 500$, $R_2 = 480$, $R_3 = 470$, $R_4 = 520$, $R_5 = 510$, $R_6 = 490$, $R_7 = 530$, $R_8 = 500$

Determine the maximum INL and DNL for the DAC assuming $V_{REF} = 5$ V.

29.2 An 8-bit resistor string DAC similar to the one shown in Fig. 29.2b was fabricated with a nominal resistor value of 1 kΩ. If the process was able to provide matching of resistors to within 1%, find the effective resolution of the converter. What is the maximum INL and DNL of the converter? Assume that $V_{REF} = 5$ V.

29.3 Compare the digital input codes necessary to generate all eight output values for a 3-bit resistor string DAC similar to those shown in Fig. 29.2a and b. Design a digital circuit that will allow a 3-bit binary digital input code to be used for the DAC in Fig. 29.2a. Discuss the advantages and disadvantages of both architectures.

29.4 Plot the transfer curve of a 3-bit R-2R DAC if all Rs = 1.1 kΩ and 2Rs = 2 kΩ. What is the maximum INL and DNL for the converter? Assume all of the switches to be ideal and $V_{REF} = 5$ V.

29.5 Suppose that a 3-bit R-2R DAC contained resistors that were perfectly matched and that $R = 1$ kΩ and $V_{REF} = 5$ V. Determine the maximum switch resistance that can be tolerated for which the converter will still have 3-bit resolution. What are the values of INL and DNL?

29.6 The circuit illustrated in Fig. 29.5 is known as a current-mode R-2R DAC, since the output voltage is defined by the current through R_F. Shown in Fig. 29.52 is an N-bit voltage-mode R-2R DAC. Design a 3-bit voltage mode DAC and determine the output voltage for each of the eight input codes. Label each node voltage for each input. Assume that $R = 1$ kΩ and that $R_2 = R_1 = 10$ kΩ and $V_{REF} = 5$ V.
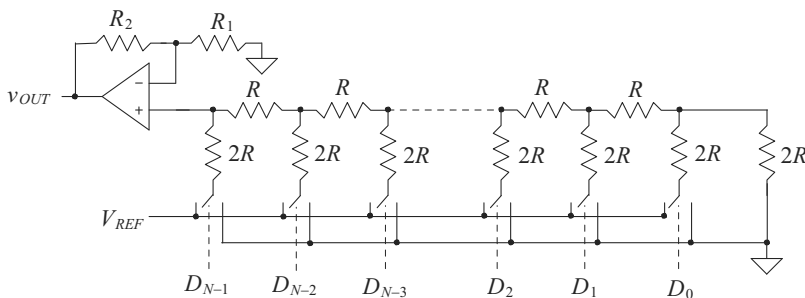

Figure 29.52   DAC used in Problem 29.6.

29.7 Design a 3-bit, current-steering DAC using the generic current-steering DAC shown in Fig. 29.9. Assume that each current source, I, is 5 μA, and find the total output current for each input code.

29.8 A certain process is able to fabricate matched current sources to within 0.05%. Determine the maximum resolution that a current-steering (nonbinary-weighted) DAC can attain using this process.

29.9 Design an 8-bit current-steering DAC using binary-weighted current sources. Assume that the smallest current source will have a value of 1 μA. What is the range of values that the current source corresponding to the MSB can have while maintaining an INL of ½ LSB? Repeat for a DNL less than or equal to ½ LSB.

29.10 Prove that the 3-bit charge-scaling DAC used in Ex. 29.6 has the same output voltage increments as the R-$2R$ DAC in Ex. 29.3 for $V_{REF} = 5$ V and $C = 0.5$ pF.

29.11 Determine the output of the 6-bit, charge-scaling DAC used in Ex. 29.7 for each of the following inputs: $D = 000010, 000100, 001000$, and 010000.

29.12 Design a 4-bit, charge-scaling DAC using a split array. Assume that $V_{REF} = 5$ V and that $C = 0.5$ pF. Draw the equivalent circuit for each of the following input words and determine the value of the output voltage: $D = 0001, 0010, 0100, 1000$. Assuming the capacitor associated with the MSB had a mismatch of 4 percent, calculate the INL and DNL.

29.13 For the cyclic converter shown in Fig. 29.17, determine the gain error for a 3-bit conversion if the feedback amplifier had a gain of 0.45 V/V. Assume that $V_{REF} = 5$ V.

29.14 Repeat Problem 29.13 assuming that the output of the summer was always 0.2 V greater than the ideal and that the amplifier in the feedback path had a perfect gain of 0.5 V/V.

29.15 Repeat Problem 29.13 assuming that the output of the summer was always 0.2 V greater than ideal and that the amplifier in the feedback path had a gain of 0.45 V/V.

29.16 Design a 3-bit pipeline DAC using $V_{REF} = 5$ V. (a) Determine the maximum and minimum gain values for the first-stage amplifier for the DAC to have less than ±½ LSBs of DNL assuming that the rest of the circuit is ideal. (b) Repeat for the second-stage amplifier. (c) Repeat for the last-stage amplifier.

29.17 Using the same DAC designed in Problem 29.16, (a) determine the overall error (offset, DNL, and INL) for the DAC if the S/H amplifier in the first stage produces an offset at its output of 0.25 V. Assume that all of the remaining components are ideal. (b) Repeat for the second-stage S/H. (c) Repeat for the last-stage S/H.

29.18 Design a 3-bit Flash ADC with its quantization error centered about zero LSBs. Determine the worst-case DNL and INL if resistor matching is known to be 5%. Assume that $V_{REF} = 5$ V.

29.19 Using the ADC designed in Problem 29.18, determine the maximum offset that can be tolerated if all of the comparators have the same magnitude of offset, but with different polarities, to attain a DNL of less than or equal to $\pm\frac{1}{2}$ LSB.

29.20 A 4-bit Flash ADC converter has a resistor string with mismatch as shown in Table 29.1. Determine the DNL and INL of the converter. How many bits of resolution does this converter possess? $V_{REF} = 5$ V.

Resistor	Mismatch (%)
1	2
2	1.5
3	0
4	−1
5	−0.5
6	1
7	1.5
8	2
9	2.5
10	1
11	−0.5
12	−1.5
13	−2
14	0
15	1
16	1

Table 29.1 Mismatch in resistors used in Problem 29.20

29.21 Determine the open-loop gain required for the residue amplifier of a two-step ADC necessary to keep the converter to within $\frac{1}{2}$ LSB of accuracy with resolutions of (a) 4 bits, (b) 8 bits, and (c) 10 bits.

29.22 Assume that a 4-bit, two-step Flash ADC uses two separate Flash converters for the MSB and LSB ADCs. Assuming that all other components are ideal, show that the first Flash converter needs to be more accurate than the second converter. Assume that $V_{REF} = 5$ V.

29.23 Repeat Ex. 29.12 for $V_{IN} = 3, 5, 7.5, 14.75$ V.

29.24 Repeat Ex. 29.13 for $V_{IN} = 1, 4, 6, 7$ V and $V_{REF} = 8$ V.

29.25 Assume that an 8-bit pipeline ADC was fabricated and that all the amplifiers had a gain of 2.1 V/V instead of 2 V/V. If $V_{IN} = 3$ V and $V_{REF} = 5$ V, what would be the resulting digital output if the remaining components were considered to be ideal? What are the DNL and INL for this converter?

29.26 Show that the first-stage accuracy is the most critical for a 3-bit, 1-bit per stage pipeline ADC by generating a transfer curve and determining DNL and INL for the ADC for two cases: (1) The gain of the first-stage residue amplifier set equal to 2.2 V/V and (2) the second-stage residue amplifier set equal to 2.2 V/V. For each case, assume that the remaining components are ideal. Assume that the V_{REF} = 5 V.

29.27 An 8-bit single-slope ADC with a 5 V reference is used to convert a slow-moving analog signal. What is the maximum conversion time assuming that the clock frequency is 1 MHz? What is the maximum frequency of the analog signal? What is the maximum value of the analog signal which can be converted?

29.28 An 8-bit single slope ADC with a 5 V reference uses a clock frequency of 1 MHz. Assuming that all of the other components are ideal, what is the limitation on the value of RC? What is the tolerance of the clock frequency which will ensure less than 0.5 LSB of INL?

29.29 An 8-bit dual slope ADC with a 5 V reference is used to convert the same analog signal in Problem 29.27. What is the maximum conversion time assuming that the clock frequency is 1 MHz? What is the minimum conversion time that can be attained? If the analog signal is 2.5 V, what will be the total conversion time?

29.30 Discuss the advantages and disadvantages of using a dual-slope versus a single slope ADC architecture.

29.31 Repeat Ex. 29.15 for a 4-bit successive approximation ADC using V_{REF} = 5 V for v_{IN} = 1, 3, and full-scale.

29.32 Assume that v_{IN} = 2.49 V for the ADC used in Problem 29.31 and that the comparator, because of its offset, makes the wrong decision for the MSB conversion. What will be the final digital output? Repeat for v_{IN} = 0.3025, assuming that the comparator makes the wrong decision on the LSB.

29.33 Design a 3-bit, charge-redistribution ADC similar to that shown in Fig. 29.39 and determine the voltage on the top plate of the capacitor array throughout the conversion process for v_{IN} = 2, 3, and 4 V, assuming that V_{REF} = 5 V. Assume that all components are ideal. Draw the equivalent circuit for each bit decision.

29.34 Determine the maximum INL and maximum DNL of the ADC designed in Problem 29.33 assuming that the capacitor array matching is 1%. Assume that the remaining components are ideal and that the unit capacitance, C, is 1 pF.

29.35 Show that the charge redistribution ADC used in Problems 29.32 and 29.33 is immune to comparator offset by assuming an initial offset voltage of 0.3 and determining the conversion for v_{IN} = 2 V.

29.36 Discuss the differences between Nyquist rate ADCs and oversampling ADCs.

29.37 Write a simple computer program or use a math program to perform the analysis shown in Ex. 29.16. Run the program for k = 200 clock cycles and show that the average value of $v_q(kT)$ converges to the correct answer. How many clock cycles will it take to obtain an average value if $v_q(kT)$ stays within 8-bit accuracy of the ideal value of 0.4 V? 12-bit accuracy? 16-bit accuracy?

29.38 Prove that the output of the second-order $\Sigma\Delta$ modulator shown in Fig. 29.49 is,

$$y(kT) = x(kT - T) + Q_e(kT) - 2Q_e(kT - T) + Q_e(kT - 2T)$$

29.39 Assume that a first order $\Sigma\Delta$ ADC used on a satellite in a low earth orbit experiences radiation in which an energetic particle causes a noise spike resulting in the comparator making the wrong decision on the 10th clock period. Using the program written in Problem 29.37, determine the number of clock cycles required before the average value of $v_q(kT)$ is within 12-bit accuracy of the ideal value of 0.4 V. How many extra clock cycles were required for this case versus the ideal conversion used in Prob. 37?

Problems

30.1   Assuming the DAC shown in Fig. 30.1 is 8 bits and $V_{REF+} = 1$ V and $V_{REF-} = 0$, what are the voltages on each of the R-$2R$ taps?

30.2   Give an example of how the traditional current-mode DAC will have limited output swing.

30.3   Repeat problem 30.1 for the DAC shown in Fig. 30.2.

30.4   For the wide-swing current mode DAC shown in Fig. 30.3, what are the voltages at the taps along the R-$2R$ string assuming 8 bits, $V_{REF+} = 1$ V, $V_{REF-} = 0$, and a digital input code of 0000 0000?

30.5   Can the op-amp shown in Fig. 30.37 be used in fully-differential implementations of the DACs shown in Figs. 30.1 - 30.3? Why or why not?

30.6   Show the detailed derivation of Eqs. (30.12)-(30.14).

30.7   Why would we want to use both current segments and binary-weighted currents to implement a current-mode DAC? (Why use segmentation?)

30.8   Why do we subtract ΔA in Eq. (30.36)? Why not add the gain variation?

30.9   Does the matching of the capacitors matter in the S/H of Fig. 30.31? Why or why not?

30.10 Derive the transfer function of the S/H in Fig. 30.30 if V_{CM} on the left side of the schematic is replaced with ground so that the bottom plates of the C_I capacitors are grounded when ϕ_3 goes high.

30.11 Determine the transfer function of the S/H in Fig. 30.34 if the top left ϕ_2-controlled switch is connected to the input instead of V_{CM}. Include the effects of offsets and simulate the operation of the circuit to verify your calculations.

30.12 Repeat Ex. 30.10 if the cyclic ADC's input is 0.41 V.

30.13 Is kick-back noise from the comparator a concern for the circuit of Fig. 30.39?

30.14 Derive the transfer function for the circuit shown in Fig. 30.80.

30.15 Repeat Ex. 30.16 if the input voltage is 0.41 V.

30.16 Repeat Ex. 30.17 if the input voltage is 0.41 V.

30.17 Resketch the clock waveforms for Fig. 30.54 if bottom plate sampling is used.

30.18 Show the derivation leading up to Eq. (30.83). Show, using practical values for mismatch, how the squared mismatch terms are negligible.

30.19 What happens to the error adjustment term in Eq. (30.92) if the capacitors in the S/H are perfectly matched?

30.20 Repeat Ex. 30.18 if all capacitors are 1 pF (the ideal situation) and verify that the error out of the stage is zero.

30.21 Sketch a circuit to provide the inputs for the four-phase, nonoverlapping clock generator shown in Fig. 30.81.
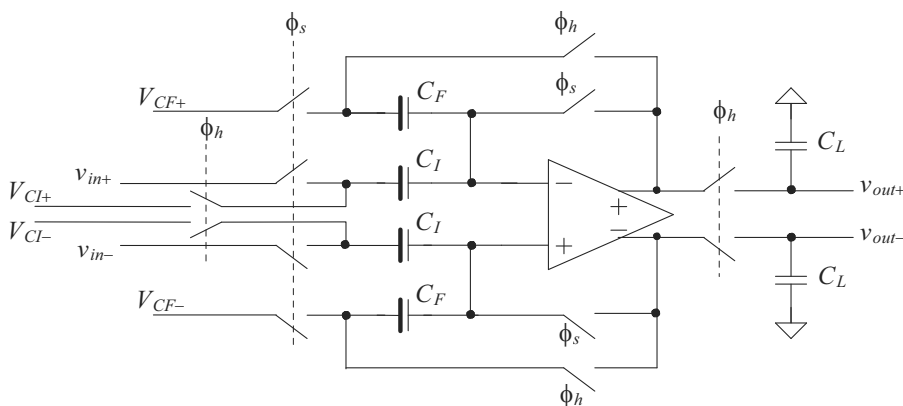
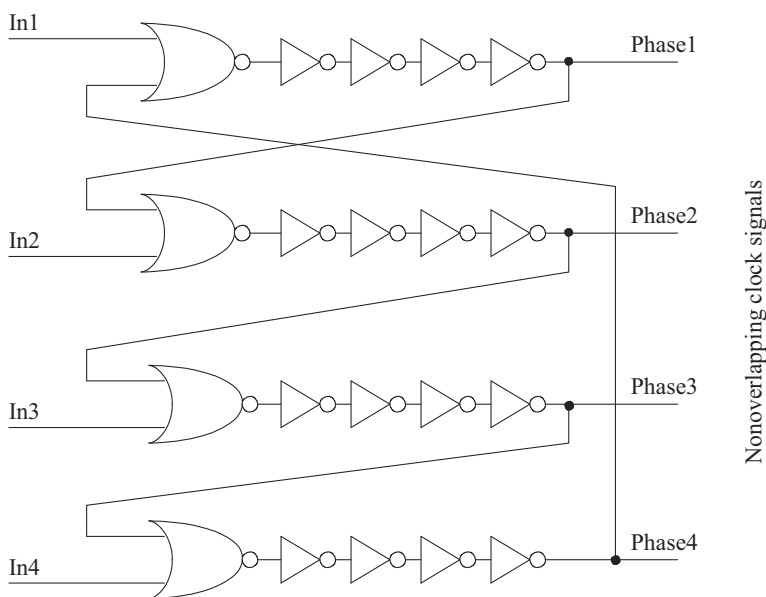**Figure 30.80** Circuit used in problem 30.14.

Figure 30.81 Four-phase, nonoverlapping clock generator.

30.22 What is the main advantage of using dynamic CMFB over other CMFB circuits? What is the main disadvantage?

30.23 Can MOSFETs be used to implement the on-chip decoupling capacitors in Fig. 30.77?

30.24 Sketch the cross-sectional view of the layout in Fig. 30.78.

30.25 Figure 30.82 shows the implementation of a pipeline DAC. How would we implement this DAC using a topology similar to Fig. 30.42? Sketch the DAC's implementation and the timing signals (clock phases) used.
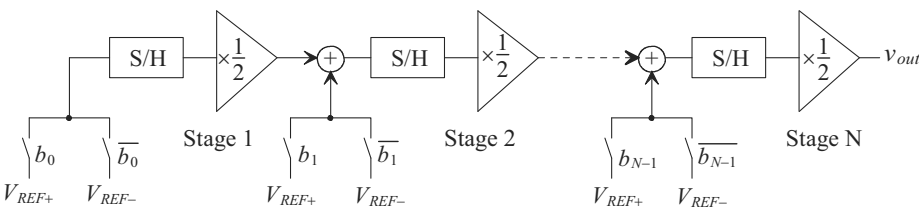
Figure 30.82 A pipeline digital-to-analog converter.
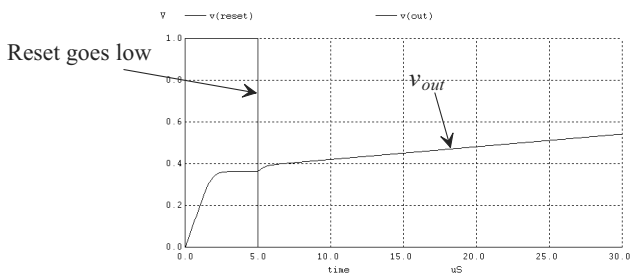
Figure 31.53 Reducing the widths of the MOSFETs in the TIA to
lower the integrated gate current from M1.

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University Press, 2010. ISBN 978-0-19-532303-0.

[2]   W. M. C. Sansen, *Analog Design Essentials,* Springer, 2006. ISBN 978-0-387-
25746-4.

[3]   P. J. Hurst, "Exact Simulation of Feedback Circuit Parameters," *IEEE
Transactions on Circuits and Systems*, Vol. 38, No. 11, pp. 1382-1389, November
1991.

PROBLEMS

31.1   An op-amp is designed so that the open-loop gain is guaranteed to be $150,000 \pm$
10 percent V/V. If the amplifier is to be used in a closed-loop configuration with β
= 0.1 V/V, determine the tolerance of the closed-loop gain.

31.2   What is the maximum possible value of β using resistors in the feedback loop of a
noninverting op-amp circuit? Sketch this op-amp circuit when $\beta = 1/2$.

31.3   Examine the feedback loop in Fig. 31.54. A noise source, v_n, is injected in the
system between two amplifier stages. (a) Determine an expression for v_o which
includes both the noise and the input signal, v_s. (b) Repeat (a) for the case where
there is no feedback ($\beta = 0$). (c) If $A_1 = A_2 = 200$, and feedback is again applied
around the circuit, what value of β will be required to reduce the noise by one-half
as compared to the case stated in (b)?

31.4   An amplifier can be characterized as follows:

$$A(s) = 10,000 \cdot \frac{100}{s + 100} \text{ V/V}$$

A series of these amplifiers are connected in cascade, and feedback is used around
each amplifier. Determine the number of stages needed to produce an overall gain
of 1,000 with a high-frequency rolloff (at -20 dB/decade) occurring at 100,000
rad/sec. Assume that the first stage produces the desired high-frequency pole and
that the remaining stages are designed so that their high-frequency poles are at
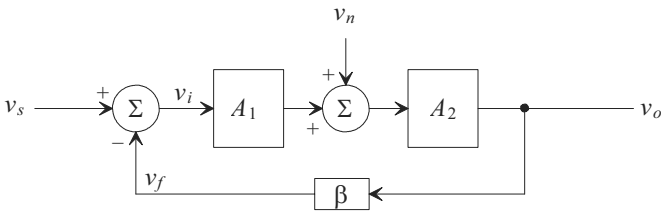least a factor of four greater.

Figure 31.54 Problem 31.3, noise injected into a feedback system.

31.5 An amplifier can be characterized as follows:

$$A(s) = 1,000 \cdot \frac{s}{s + 100} \text{ V/V}$$

and is connected in a feedback loop with a variable β. Determine the value of β for which the low-frequency rolloff is 50 rad/sec. What is the value of the closed-loop gain at that point?

31.6 Make a table summarizing the four feedback topologies according to the following categories: input variable, output variable, units of A_{OL}, units of β, method to calculate $R_{\beta i}$ and $R_{\beta o}$, and expressions for A_{CL}, R_{if}, and R_{of}.

31.7 Using the two n-channel common source amplifiers shown in Fig. 31.55a and the addition of a single resistor, draw (a) a series-shunt feedback amplifier, (b) a series-series feedback amplifier, (c) a shunt-shunt feedback amplifier, and (d) a shunt-series amplifier. For each case, identify the forward and feedback paths, ensure that the feedback is negative by counting the inversions around the loop, and label the input variable, the feedback variable, and the output variable. Assume that the input voltage has a DC component that biases M1.

31.8 Repeat problem 31.7 using the two-transistor circuit shown in Fig. 31.55b.

31.9 Repeat problem 31.7 using Fig. 31.55c.

31.10 Repeat problem 31.7 using Fig. 31.55d.
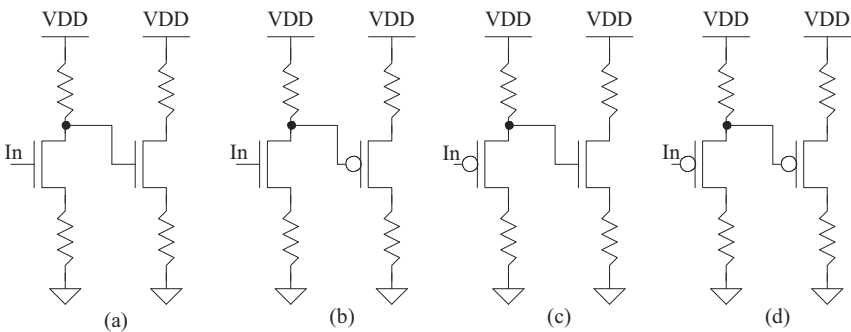
Figure 31.55 Two-transistor feedback topologies.

For each of the following feedback analysis problems, assume that the circuit has been properly DC biased and that MOSFETs have been characterized. The n-channel devices have $g_m = 0.06$ A/V and $r_o = 70$ kΩ. The p-channel devices have $g_m = 0.04$ A/V and $r_o = 50$ kΩ.

31.11 Using the series-shunt amplifier shown in Fig. 31.56, (a) identify the feedback topology by labeling the mixing variables and output variable, (b) verify that negative feedback is employed, (c) draw the closed-loop small-signal model, and (d) find the expression for the resistors $R_{\beta i}$ and $R_{\beta o}$.
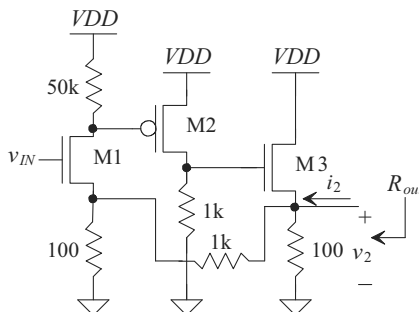
Figure 31.56 A series-shunt feedback amplifier with source-follower output buffer.

31.12 Using Fig. 31.56 and the results from problem 31.11, (a) draw the small-signal open-loop model for the circuit and (b) find the expressions for the open-loop parameters, A_{OL}, β, R_i, and R_o and (c) the closed-loop parameters, A_{CL} and R_{out}. Note that finding R_{in} is a trivial matter since the signal is input into the gate of M1.

31.13 Using the series-shunt amplifier shown in Fig. 31.57, (a) verify the feedback topology by labeling the mixing variables and the output variable closed-loop small-signal model and (b) find the values of $R_{\beta i}$ and $R_{\beta o}$.
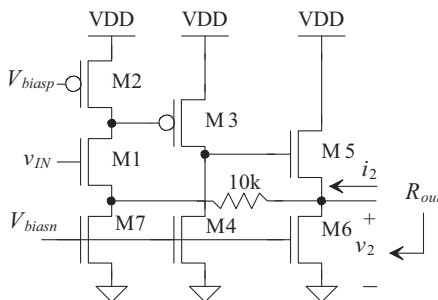

Figure 31.57 A series-shunt amplifier with source-follower output buffer.

31.14 Using the series-shunt amplifier shown in Fig. 31.57 and the results from problem 31.13, (a) draw the small-signal open-loop model for the circuit and (b) calculate the open-loop parameters, A_{OL}, β, R_i, and R_o and (c) the closed-loop parameters, A_{CL}, and R_{out}. Note that Fig. 31.57 is identical to Fig. 31.56 except that the resistors have been replaced with active loads.

31.15 Using the principles of feedback analysis, find the value of the voltage gain, $\dfrac{v_2}{v_{in}}$ and $\dfrac{v_2}{i_2}$ for the series-shunt circuit shown in Fig. 31.58.
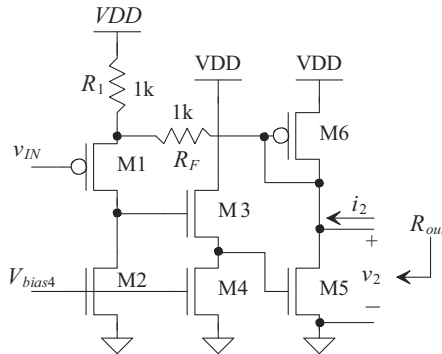
Figure 31.58 Feedback amplifier used in problem 31.15.

31.16 A shunt-shunt feedback amplifier is shown in Fig. 31.59. (a) Identify the feedback topology by labeling the input mixing variables and the output variables, (b) verify that negative feedback is employed, (c) draw the closed-loop small-signal model, and (d) find the values of $R_{\beta i}$ and $R_{\beta o}$.
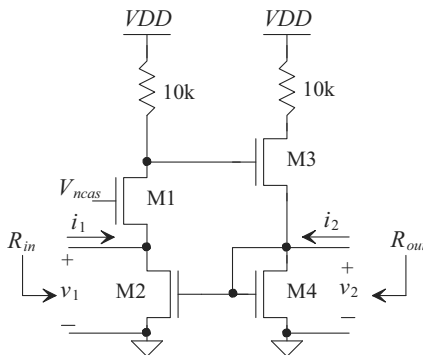
Figure 31.59 A shunt-shunt feedback amplifier.

31.17 Using the shunt-shunt amplifier shown in Fig. 31.59 and the results from problem 31.16, (a) draw the small-signal open-loop model for the circuit and (b) calculate expressions for the open-loop parameters, A_{OL}, β, R_i, and R_o and (c) the closed-loop parameters, A_{CL}, R_{in}, and R_{out}.

31.18 Using the principles of feedback analysis, find the value of the voltage gain, $\frac{v_2}{v_1}$, $\frac{v_1}{i_1}$, and $\frac{v_2}{i_2}$ for the shunt-shunt circuit shown in Fig. 31.60.
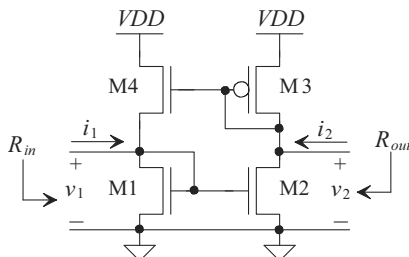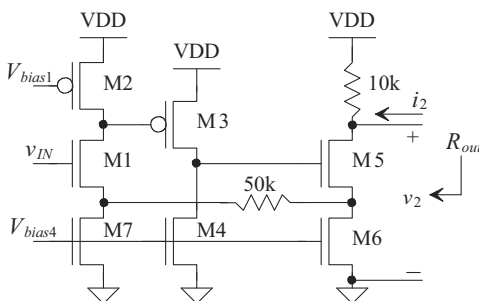

Figure 31.60 A shunt-shunt feedback amplifier, see problem 31.18.

31.19 Using the series-series feedback amplifier shown in Fig. 31.61, (a) identify the feedback topology, (b) verify that negative feedback is employed, (c) draw the closed-loop small-signal model, and (d) find the values of $R_{\beta i}$ and $R_{\beta o}$.

Figure 31.61 Series-series feedback amplifier with source-follower output buffer.

31.20 Using the series-series amplifier shown in Fig. 31.61 and the results from problem 31.19, (a) draw the small-signal open-loop model for the circuit and (b) calculate the open-loop parameters, A_{OL}, β, R_i, and R_o and (c) the closed-loop parameters, A_{CL}, R_{in}, and R_{out}.

31.21 Using the shunt-series amplifier in Fig. 31.35, derive the expressions for A_{OL}, R_{if}, and R_{of}.

31.22 Convert the shunt-shunt amplifier shown in Fig. 31.59 into a shunt-series feedback amplifier without adding any components. (a) Identify the feedback topology, (b) verify that negative feedback is employed, (c) draw the closed-loop small-signal model, and (d) find the values of $R_{\beta i}$ and $R_{\beta o}$.

31.23 Using the shunt-series amplifier from problem 31.22, (a) draw the small-signal open-loop model for the circuit and (b) calculate the open-loop parameters, A_{OL}, β, R_i, and R_o and (c) the closed-loop parameters, A_{CL}, R_{in}, and R_{out}.

31.24 A feedback amplifier is shown in Fig. 31.62. Identify the feedback topology and determine the value of the voltage gain, $\frac{v_2}{v_1}$, R_{in}, and R_{out}.
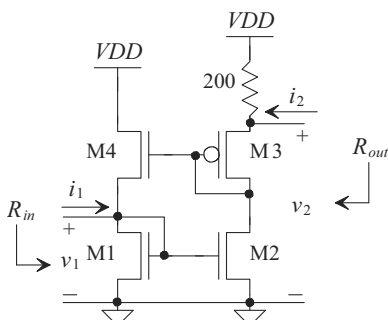

Figure 31.62 Feedback amplifier used in problem 31.24.

31.25 Notice that the amplifier shown in Fig. 31.63 is a simple common source amplifier with source resistance. Explain how this is actually a very simple feedback amplifier and determine the type of feedback used. Determine A_{OL} and β.
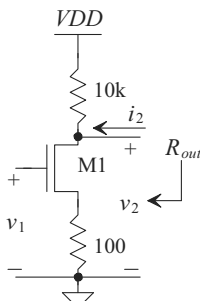

Figure 31.63 Common-source amplifier with source degeneration.

31.26 A feedback amplifier is shown in Fig. 31.64. Identify the feedback topology and determine the value of the voltage gain, $\frac{v_2}{v_1}$, R_{in}, and R_{out} .

31.27 A feedback amplifier is shown in Fig. 31.65. Identify the feedback topology and determine the value of the voltage gain, $\frac{v_2}{v_1}$ and R_{out} .

31.28 Prove that the expression for the open-loop gain derived in Ex. 31.3 is correct.

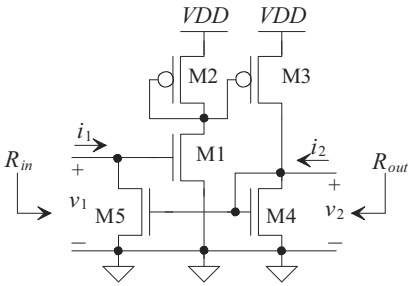**31.29** Determine if the amplifier seen in Fig. 31.44 is stable.

Figure 31.64 Feedback amplifier used in problem 31.26.
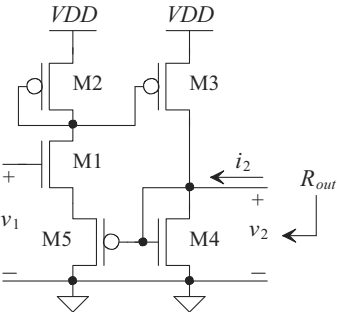

Figure 31.65 Feedback amplifier used in problem 31.27.

31.30 The op-amp shown in Fig. 31.66a can be modeled with the circuit of Fig. 31.66b. With a feedback factor, $\beta = 1$, determine if the op-amp is stable (and the corresponding phase and gain margins) for the following transfer function and ω_2 = 10^5, 10^6, 10^7, and 5×10^6 rad/sec.

$$A_{OL}(j\omega) = \frac{10,000}{\left(1 + j\frac{\omega}{100}\right)\left(1 + j\frac{\omega}{\omega_2}\right)}$$
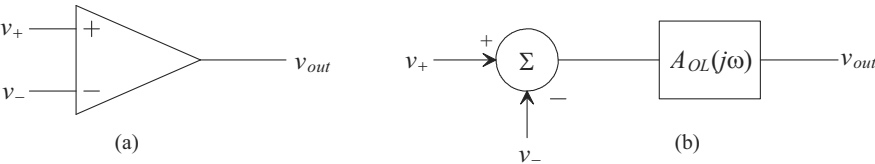

Figure 31.66 Modeling the op-amp.

31.31 The phase plot of an amplifier is shown in Fig. 31.67. The amplifier has a midband gain of −1,000 and 3 zeros at $\omega = \infty$ and three other unspecified poles. If the amplifier is configured in a feedback configuration and β is frequency independent, what is the exact value of β that would be necessary to cause the amplifier to oscillate?
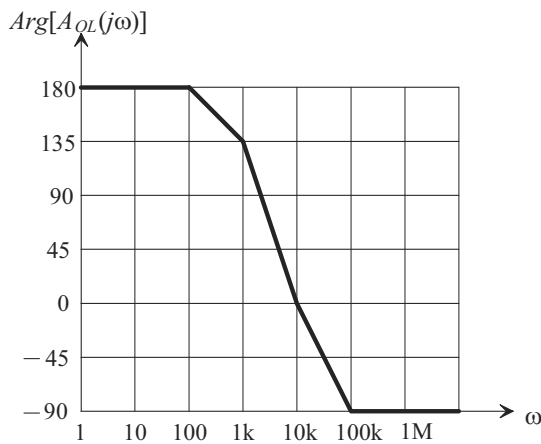
Figure 31.67 Phase response used in problem 31.31.

31.32 You have just measured the gain of the op-amp circuit shown in Fig. 31.68. You know from basic op-amp theory that the gain of the circuit should be $-R_2/R_1$ V/V. However, your measurements with $R_2 = 10$ kΩ and $R_1 = 1$ kΩ revealed that the gain was only -5 V/V. What is the open-loop gain of the op-amp?
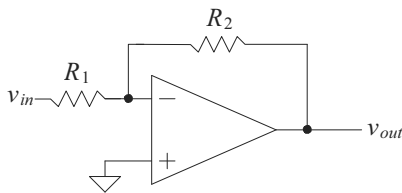

Figure 31.68 How finite open-loop gain effects closed-loop gain, problem 31.32.

31.33 Using the circuit shown in Fig. 31.69 and the *RR* method, find a value of R_1 and A_o which will cause the phase margin to equal 45° at $\omega = 8,000$ rad/sec. The amplifier can be modeled as having an infinite input impedance and zero output resistance and has a frequency response of

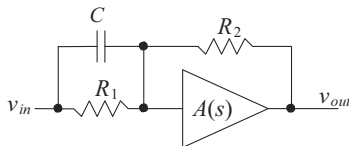$$A(s) = \frac{-A_o}{(s/200 + 1)(s/10,000 + 1)}$$

Figure 31.69 Amplifier used in problem 31.33.

31.34 Determine if the system with a return ratio as described by Eq. (31.102) is stable.

31.35 Redesign the transimpedance amplifier seen in Fig. 31.51 using the long-channel CMOS process discussed in this book.

31.36 How would the input-referred noise for the TIA design presented in Sec. 31.9.2 be reduced?