Jason Durand

Problem 2.1 – Qualitatively, using figures, show how impulse sampling a sinewave can result in an alias of the sampled sinewave at a different frequency.

The fourier transform of a sinusoid with frequency f_0 looks like

magnitude

frequency

$-f_o$ f_o
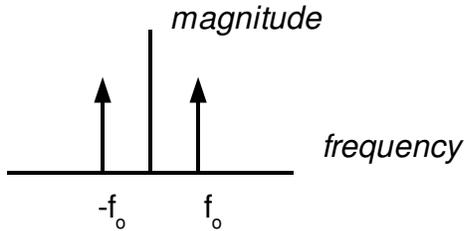
in the frequency domain. An impulse sampling scheme, with impulses in the time domain separated by T $(1/f_s)$ is, in the frequency domain, also an impulse train, with the impulses separated by the sampling frequency f_s. Multiplying these two signals in the time domain (sampling the sinusoid) results in the figure below, in the frequency domain.

magnitude

...   ...

frequency

$-f_s-f_o$ $-f_s+f_o$ $-f_o$ f_o f_s-f_o f_s+f_o
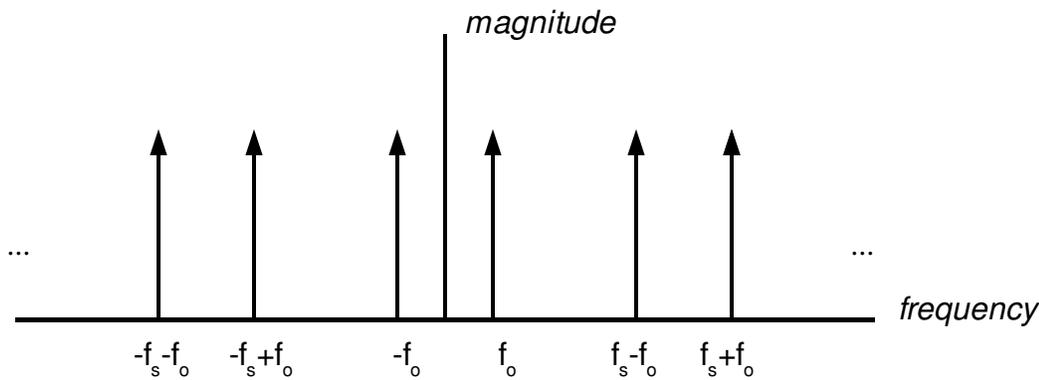
If the frequency of the sampled signal is close to the sampling frequency, the resulting frequency domain representation is closer to the figure below.

magnitude

... $-f_s$ $-f_n$ f_n f_s ...

frequency

$-2f_s+f_o$ $-f_o$ $-f_s-f_o$ f_s-f_o f_o $2f_s-f_o$
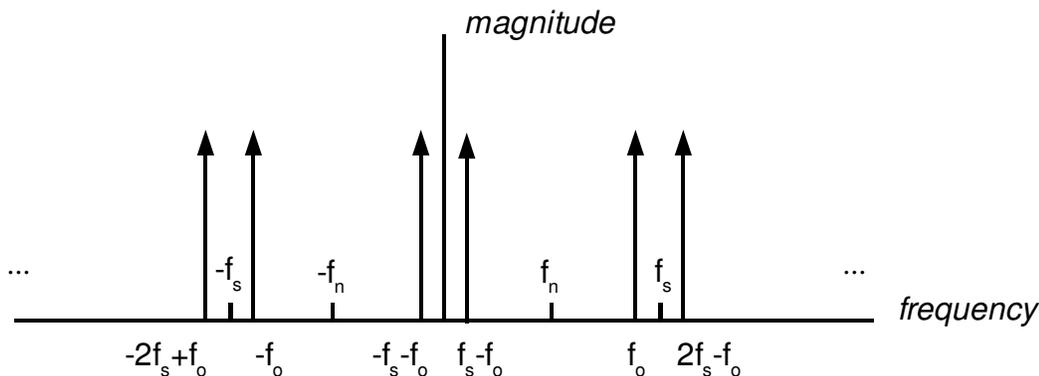
Notice slightly below the sampling frequency the signal that is wanted (f_0). Since it is higher than the nyquist frequency ($f_s/2 = f_n$), the higher frequency image from sampling folds over and appears at a lower frequency than the input to the sampler (on the graph, appears as f_s-f_0). In the time domain, it can be easier to see how the high frequency folds over to a lower frequency signal, as shows below.

Time domain graph of sine wave and the impulse samples.
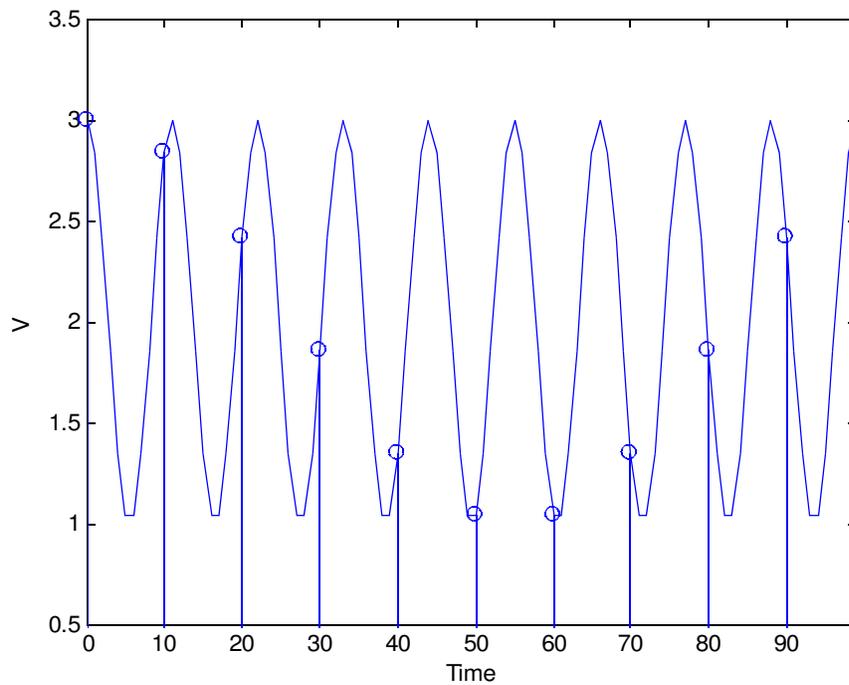
The sampled points, though they are sampled from the high frequency sine wave, also form a lower frequency sine wave alias, which is the dotted red line.
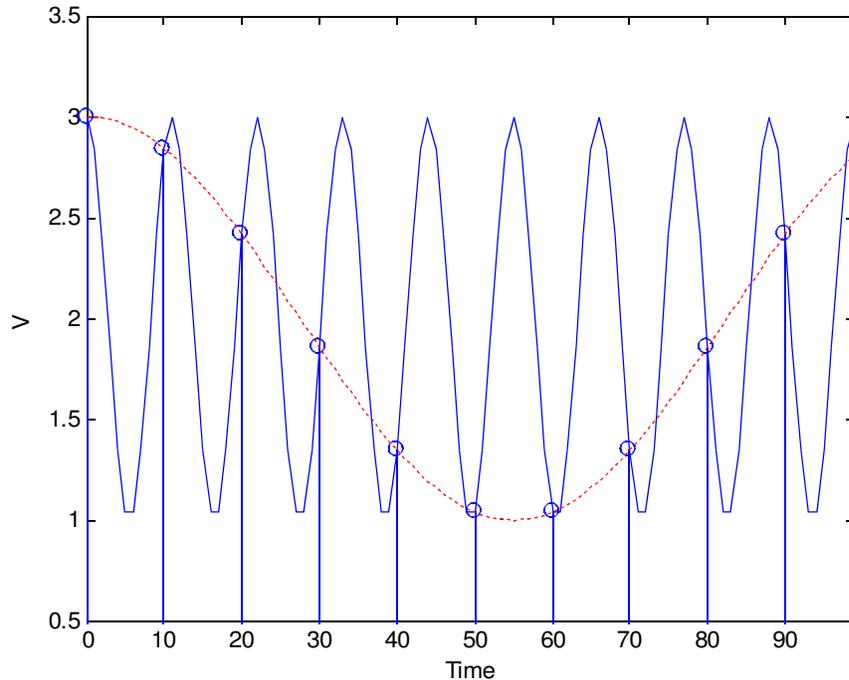
Aliasing can be seen in many places unexpectedly as well. Driving down a highway at night, and watching the rims of an adjacent car slow to a stop, then spin the other direction (though the car is still driving down the highway!) is a readily observable form of aliasing. It has to be at night, because the 60Hz flicker from fluorescent street lamps will optically 'sample' the rim's spoke position, and highway speeds are high enough that the frequency (rate of wheel spin) of the wheel is higher than or near the

60Hz sampling frequency of the fluorescent light.

Additional:
The matlab code used to generate graphs

```
%the t vector is time, and represents analog time
%the n vector represents the sampling impulse train
% and is the same dimension as t
%input = cos(2pi*fs/10), fs=sampling frequency
t = 0:99;
n_1 = [1,zeros(1,9)];
n = [n_1, n_1, n_1, n_1, n_1, n_1, n_1, n_1, n_1, n_1];
input = cos(t.*2*pi*1/11)+2;
input2 = cos(t.*2*pi*1./(10*(1/(1-1/1.1))))+2;
sampled_input = input.*n;
figure(1)
plot(t, input)
hold on
stem(t, sampled_input)
axis([0,99,0.5,3.5])
xlabel('Time'):ylabel('V')
hold off
figure(2)
stem(t, sampled_input)
axis([0,99,0.5,3.5])
xlabel('Time'):ylabel('V')
hold on
plot(t, input)
plot(t, input2, 'r:')
```

2.2. Re sketch Figs 2.12 and 2.13 when decimating by 5. Hint: use a counter and some logic to implement the divide by 5 clock divider.

Sol: First let us consider the operation of a decimation block with decimation factor *k* as shown in figure 1. Input signal is filtered by the Anti Aliasing Filter (AAF) which is band limited to *fs/2k*, and has a sample rate *fs*. This means that the desired signal spectra using decimation can not extend beyond *fs/2k*. A clock divider is used to obtain the decimation frequency *fs/k* from input clock *fs*. This decimation frequency is used as sampling frequency to process the signal obtained after Anti Aliasing Filter stage. As k=5 in this case the decimation frequency is *fs/5* and the bandwidth of the desired signal spectra lies below *fs/10*. A divide by 5 ripple counter is realized using 3 divide by 2 counters and additional logic to reset the counter to zero, once the count reaches the value of 5. An and gate (i.e. *Q2.Q1i.Q0)* with it's output connected to the active high asynchronous clear of the counter as shown in the clock divider in figure 1. As the count value reaches 5 i.e. *Q2=1,Q1=0,Q0=1* (MSB to LSB), the counter is reset (see Table 1).

Q2	Q1	Q0	Count
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
0	0	0	0

The counter value is reset once the value of "Q2Q1Q0" becomes "101"

Table 1. Divide by 5 Counter
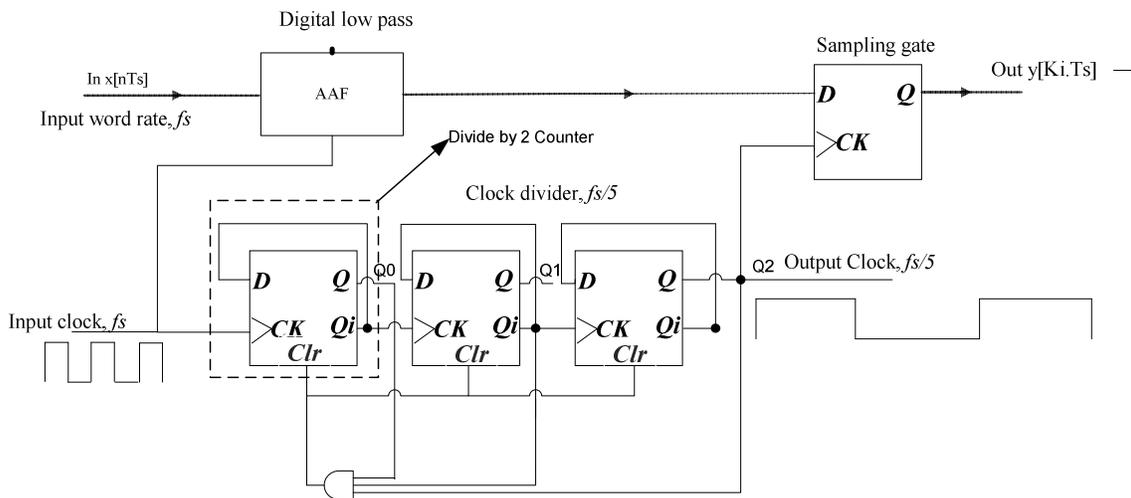
Figure 1. Components of Decimation block with k=5

The spectrum when decimation with k=5 is employed is shown in figure 2. In (a) the original input signal spectrum before processing by AAF is shown. After processing by the Anti Aliasing Filter which is band limited by *fs/10,* the desired input signal spectrum repeats at every *fs.* Since the output at AAF is sampled with the output clock from the divider i.e. *fs/5,* the output spectrum of the sampling gate repeats at *fs/5,* and the original signal spectrum lies below *fs/10.*
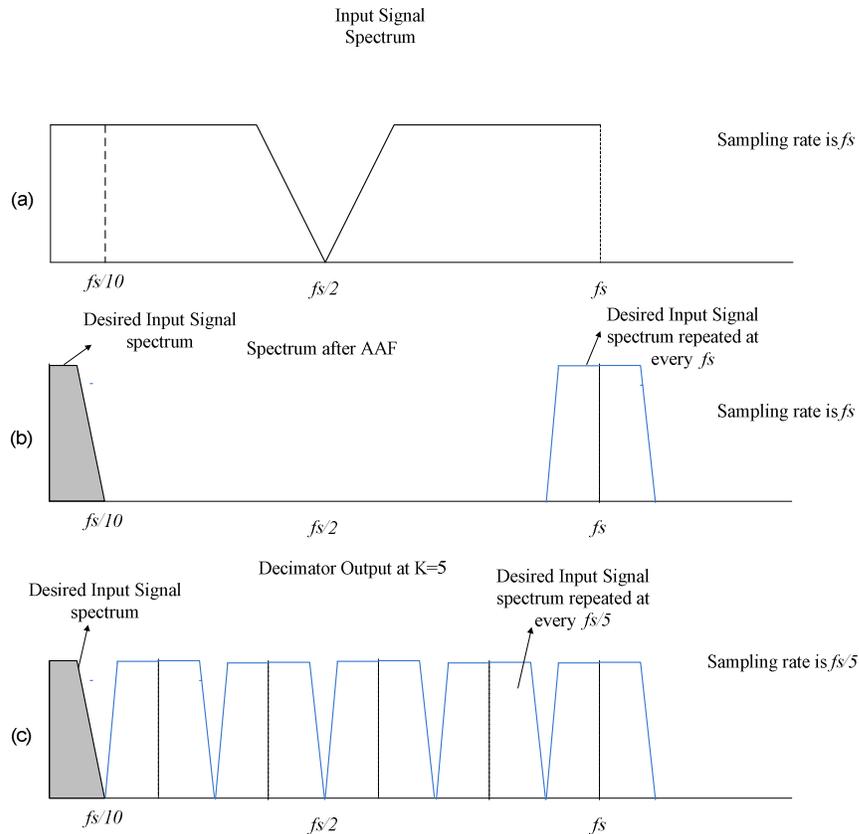

Figure 2. Spectrum when decimation with k=5 is employed

Solution by Jake Baker

2.3   Explain why returning the output of the S/H to zero reduces the distortion introduced into a signal. What is the cost for the reduced distortion in a practical circuit?

Solution: Figure 2.15 from the book, and seen below, shows how the output of the S/H can be returned to zero. The big problem with returning the output to zero is the reduction in the output signal's power. As $T \rightarrow 0$ the power in the output signal goes to zero. The effect is to reduce the signal-to-noise ratio, *SNR*. Generally, killing *SNR* to improve distortion is not a good idea.
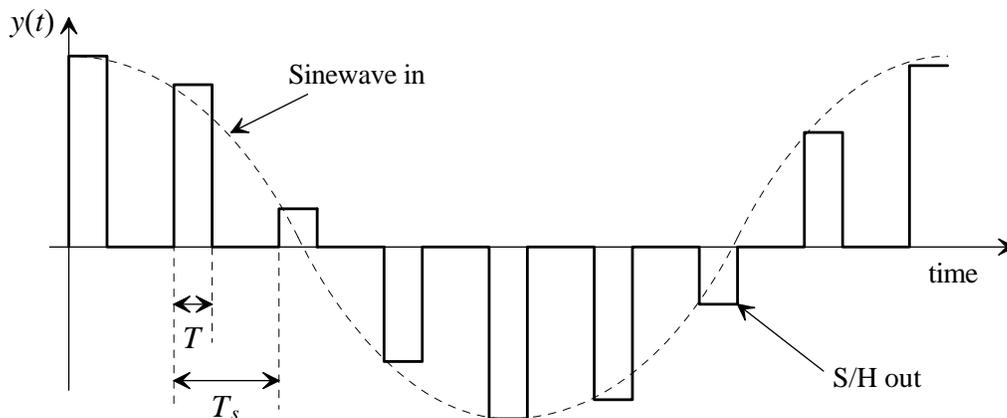

Figure 2.15 Sample-and-hold output with return-to-zero format.

Next, let's answer why returning the output of the S/H to zero reduces the distortion introduced into a signal. Reviewing the derivation for Eq. (2.16) we see that the ideal impulse sampler is weighted with a response by the S/H given by

$$|Y(f)| = \overbrace{T \cdot |Sinc(\pi \cdot T \cdot f)|}^{\text{Weighting from S/H, } |H(f)|}$$

The constant value of *T* multiplying the *Sinc* function accounts for the reduction in signal power as $T < T_s$. This term doesn't effect distortion just power. The *Sinc* term, however, effectively filters the input signal and thus causes distortion when $T > 0$. As *T* moves away from (becomes less than) T_s the *Sinc* term moves closer to 1 resulting in a reduction in distortion.

Simulation examples are seen on the next two pages.
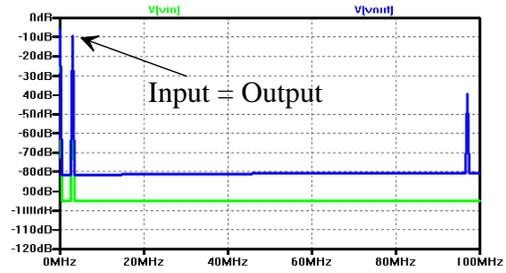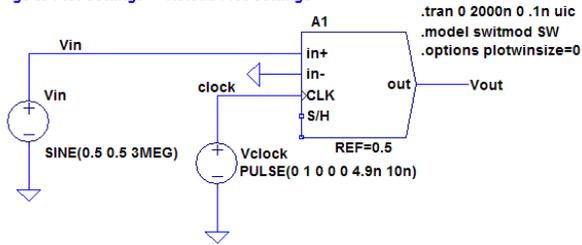
Figure showing S/H operation when $T = T_s$
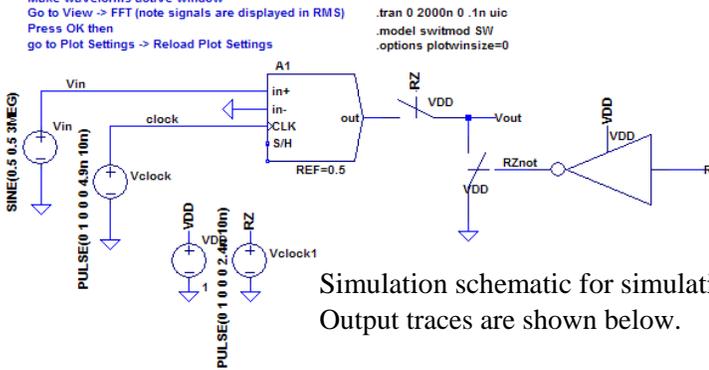
Simulation schematic for simulating a S/H with RZ output. Output traces are shown below.
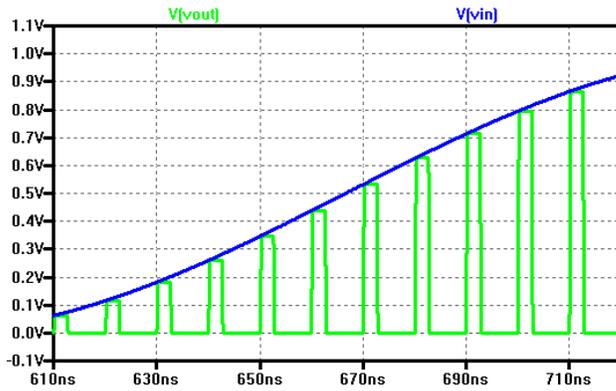
Showing return to zero with T = Ts/4
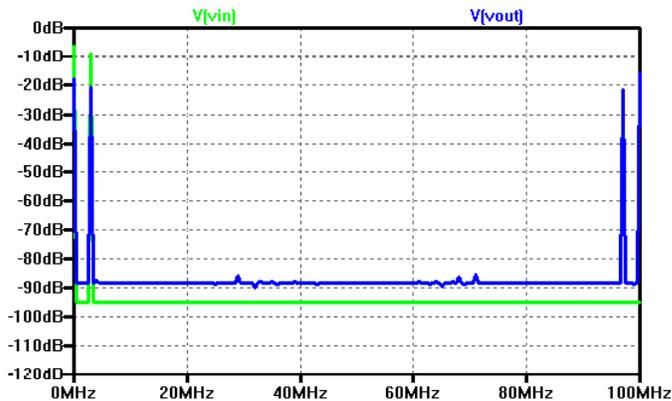
Showing the output spectrum when T = Ts/4. Note the reduction in the output power.

Final simulation comparing input sinewave at 43 MHz, S/H output with $T = T_s$, and S/H output with RZ where $T = T_s/4$.
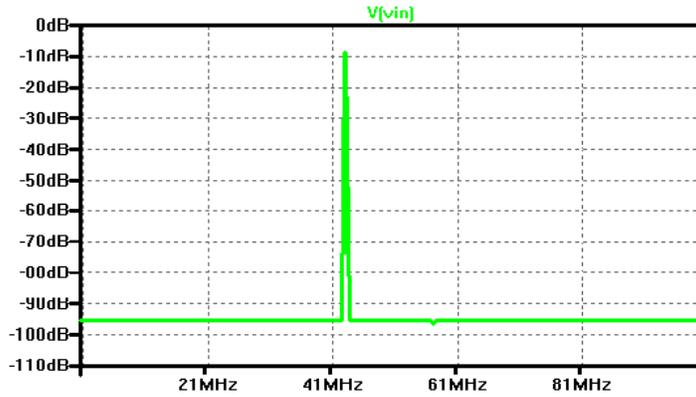
Input signal at 43 MHz
Clock frequency is 100 MHz
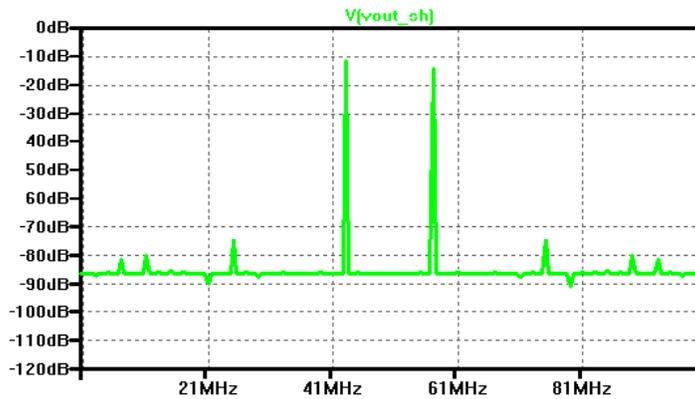
Output of the S/H with
T = Ts
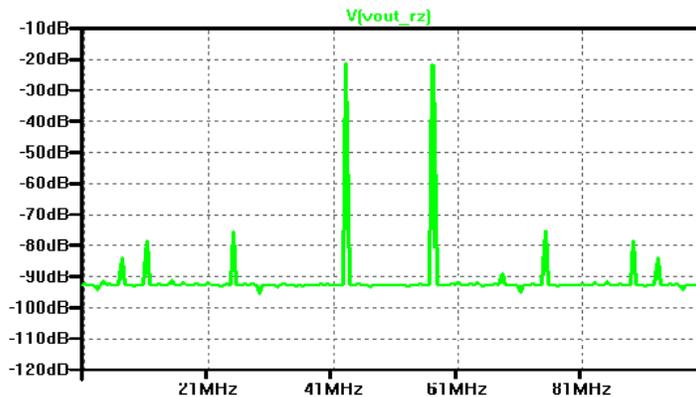
Output of the S/H with RZ
and T = Ts/4

2.4 Sketch the input and output spectrum for the following block diagram. Assume the DC component of the input is 0.5 V while the AC component is a sinewave at 4 MHz with a peak amplitude of 100 mV. Assume the clock frequency is 100 MHz.
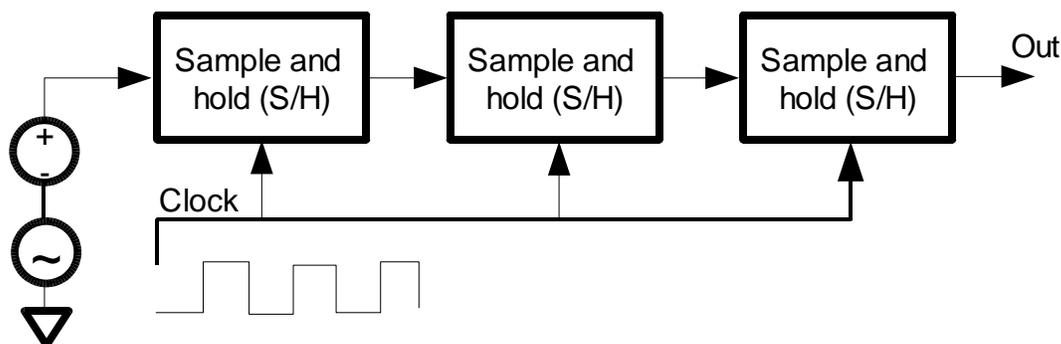

Solution:

For a sinewave input, the output spectrum, $Y(f)$, of a Sample-and-hold is described by

$$Y(f)=\frac{V_p}{2\,jT_s}\cdot\sum_{k=-\infty}^{\infty}\left[\delta(f-f_{in}-k\,f_s)-\delta(f+f_{in}-k\,f_s)\right]\cdot T\cdot Sinc(\pi\cdot f\cdot T)\cdot e^{-j\cdot 2\pi\cdot f\cdot\frac{T}{2}} \tag{1}$$

or

$$|Y(f)|=T\cdot|Sinc(\pi\cdot f\cdot T)|\frac{V_p}{2T_s}\cdot\sum_{k=-\infty}^{\infty}\left[\delta(f-f_{in}-k\,f_s)-\delta(f+f_{in}-k\,f_s)\right] \tag{2}$$

which were derived in Section 2.1.3 of [1]. As we can see in Eq. 2, the output spectrum is the ideal impulse sampler response weighted by a Sinc function. That is, there is a droop in the S/H's response. This attenuation in the S/H's output is given by

$$Attenuation=Sinc(\pi\cdot T\cdot f) \tag{3}$$

For most circuit designs $T=T_s$. And for this problem, $f_s=1/T_s=100\,MHz$. Using Eq. 3 we can calculate the attenuation of the S/H for a 4 MHz sinewave input signal as

$$Attenuation_{@\,4MHz}=Sinc(\pi\cdot T_s\cdot f_{in})=Sinc\left(\pi\cdot\frac{f_{in}}{f_s}\right)$$
$$=Sinc\left(\pi\cdot\frac{4\,M}{100\,M}\right)=0.997\ \rightarrow\ -0.02\,dB \tag{4}$$

which is a very small value. However, for the image at 96 MHz the attenuation is

$$Attenuation_{@\,96MHz}=Sinc\left(\pi\cdot\frac{96\,M}{100\,M}\right)=0.042\ \rightarrow\ -27.6\,dB \tag{5}$$

Fig. 1 shows the output spectrum of a S/H.
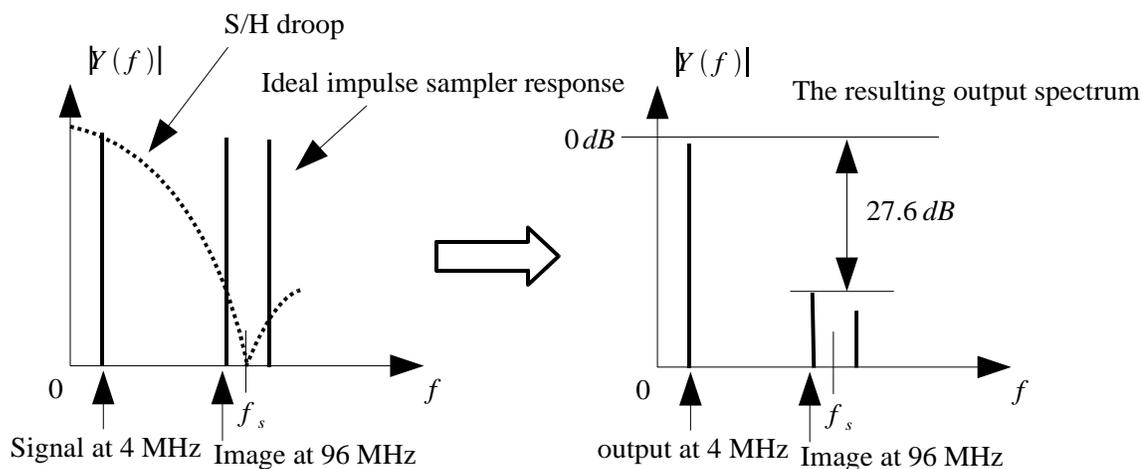
Figure 1 Output spectrum of a S/H

Repetitively sampling and holding a signal does not result in additional attenuation. If we sample the output of the a S/H circuit using another identical S/H and same clock signal, the output from the second S/H will be the same as the one from the previous S/H. So the second S/H can be seen as just a delay element. Passing the input through three identical S/H circuits in series results in the same output spectrum as passing it through one S/H. Thus the output spectrum of the 3-stage S/H is the same as shown in Fig. 1.

Now let us using SPICE simulation to verify our result. In Fig. 2 the spectrum for a 1-stage S/H is shown. Shown in Fig. 3 is the spectrum of a 3-stage S/H. The attenuation for both cases is -27.7 dB. The S/H circuit in the simulation is from the Electric jelib file for Fig. 2.18 in [1].
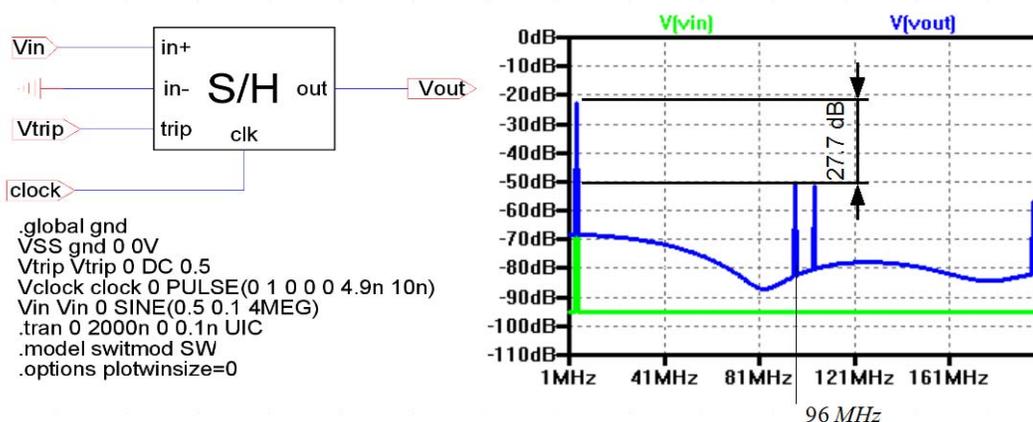
Figure 2 The spectrum of a S/H circuit.

.global gnd
VSS gnd 0 0V
Vtrip Vtrip 0 DC 0.5
Vclock clock 0 PULSE(0 1 0 0 0 4.9n 10n)
Vin Vin 0 SINE(0.5 0.5 3MEG)
.tran 0 2000n 0 0.1n UIC
.model switmod SW
.options plotwinsize=0
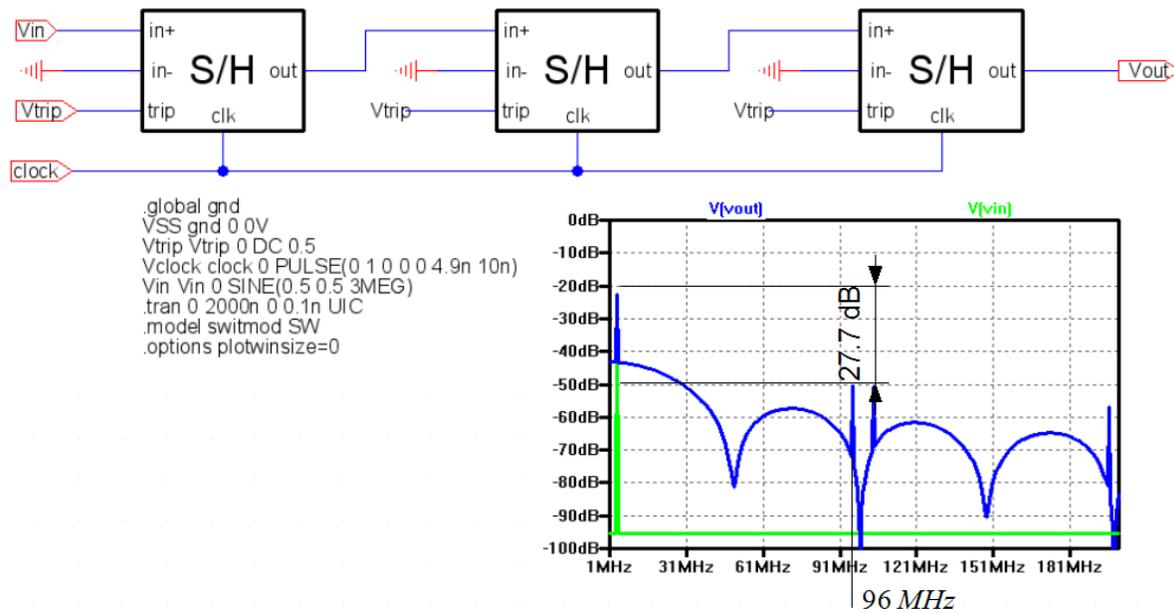
Figure 3   The spectrum of the 3-stage S/H circuit.

Reference:

[1]   R. J. Baker, *CMOS Mixed-signal Circuit Design, Second Edition*, Wiley-IEEE, 2009.

2.5) *Repeat Ex. 2.2 with an input sine wave of 30MHz.*

Example 2.2
Using an ideal SPICE model for the S/H show, and discuss, the spectrum resulting from sampling a 3MHz sine wave at 100 Msamples/s.

The example used a $0.5V_p$ magnitude sine wave (used here as well). This can be interpreted on the dB scale as $20\log\dfrac{\left(0.5/\sqrt{2}\right)V_{rms}}{1.0V_{rms}} = -9dB$. This implies that all spectral contents are 9dB below any value that is calculated using the formulae provided in chapter 2. Increasing the input signal tenfold from 3MHz to 30MHz reduces the number of samples per input signal period, and approaches the Nyquist rate but does not quite reach it. The Nyquist frequency is $f_n = f_s/2 = 100MHz/2 = 50MHz$. This indicates that one should be able to reconstruct the signal, post processing and post digital to analog conversion, alias free. It does not, however, mean that the signal will be a good representation of the input signal. Figure 2.5.1 shows sampled and held values (the blue curve, Vout) and one can see that to get a good representation of the sine wave, faster sampling should be used.

The spectral response is shown in Fig. 2.5.2. We see the primary output frequency (30MHz) is, as discussed, 9dB below the attenuated value of, using Eq. 2.16, $Sinc\left(\dfrac{\pi \cdot 30}{100}\right) = 0.858 = -1.32dB$, or -9dB – 1.32dB = -10.3dB. We see the output spectral bands for the S/H repeat at $n \cdot f_s \pm 30MHz$ (70MHz, 130MHz, 170MHz, …).
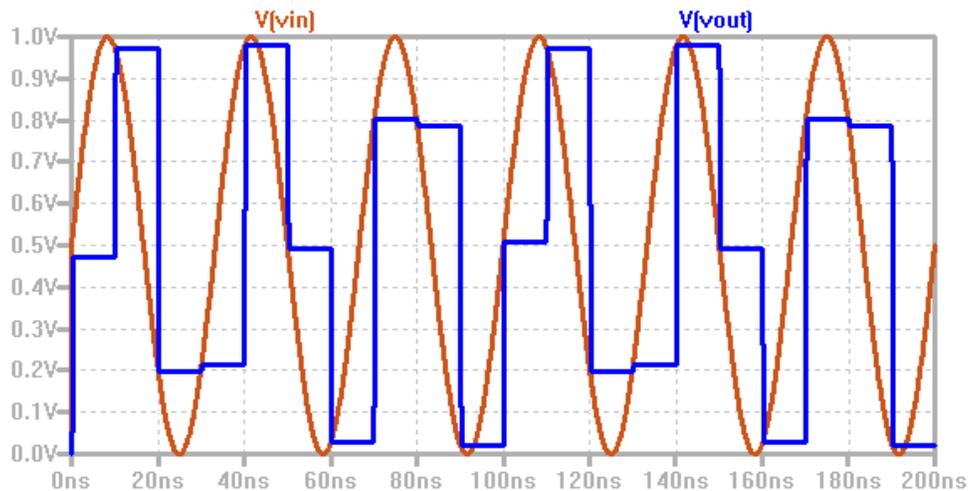
**Figure 2.5. 1. Transient response of sample and hold. Input signal = 30MHz. Output sampled at 100MSamples/s.**
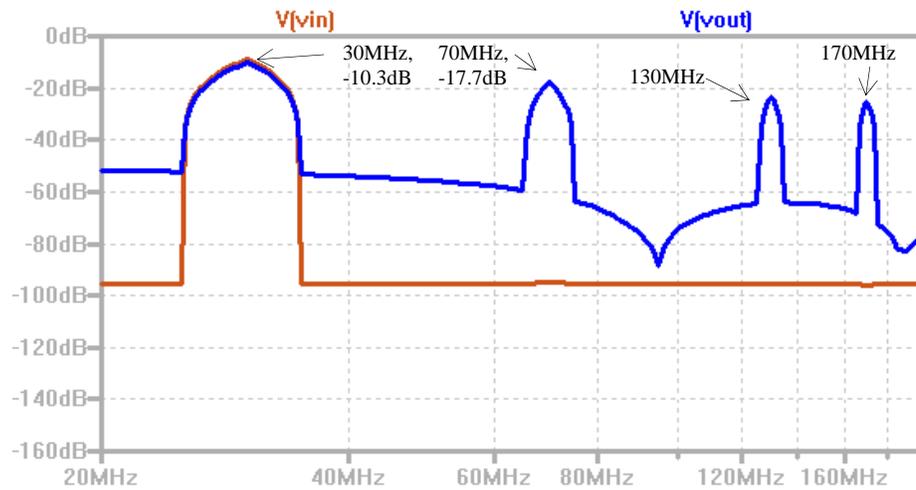
Figure 2.5. 2 Spectral response of output of S/H after sampling a 30MHz sine wave at 100MSamples/s.

The attenuation through the S/H at 70MHz is $Sinc\left(\dfrac{\pi \cdot 70}{100}\right) = 0.368$. This is -8.7dB.

When reduced by the input attenuation of -9dB we see an overall attenuation of -17.7dB.

Jason Durand

Problem 2.6 - Re-sketch figure 2.22 if the input signal is a sinewave at 10Mhz, with no other spectral content.

Frequency domain representation of a 10MHz sinusoid

magnitude

frequency

$-f_o$ f_o
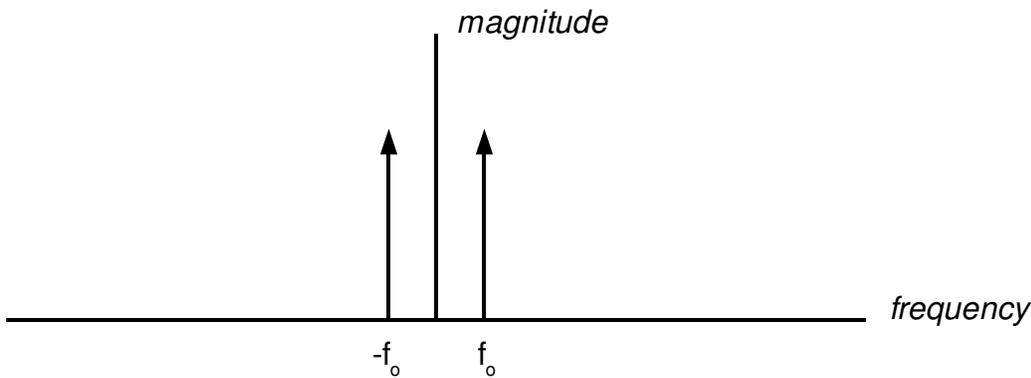
10MHz

After applying an anti-aliasing filter with cutoff of 25MHz, the spectra of the input signal is cropped to:

magnitude

frequency

$-f_o$ f_o
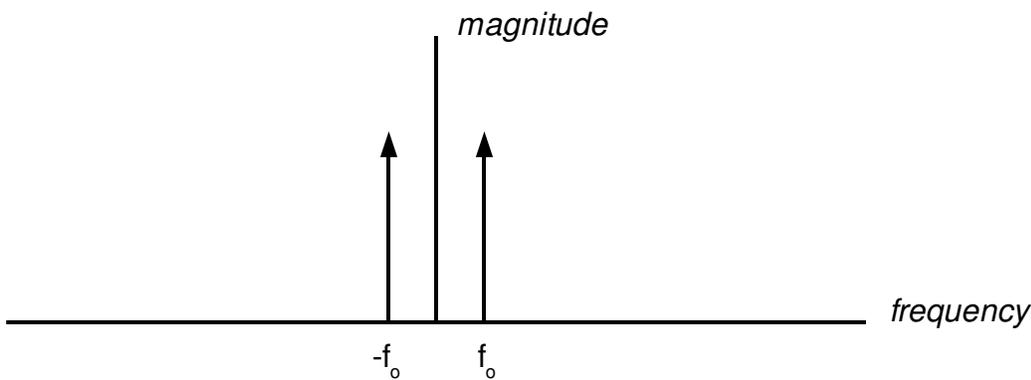
10MHz

Since the 10MHz sinusoid has no spectral content above the $f_s/2$ Nyquist limit, the anti-aliasing filter has no actual effect on this theoretical, perfect signal. A real world signal might likely have frequencies higher than half the sampling frequency.

With a sampling frequency of 50MHz, the attenuation due to an ideal sample and hold at 10MHz is

equal to $\quad Attenuation = \mathrm{sinc}(\dfrac{\pi \cdot f_o}{f_s}) = \mathrm{sinc}(\dfrac{\pi \cdot 10\mathrm{MHz}}{50\mathrm{MHZ}}) = .935 = -0.6\,dB$.

magnitude

Sample and hold without
sampling effects

.935   .935 or -0.6dB

frequency

$-f_o$ f_o
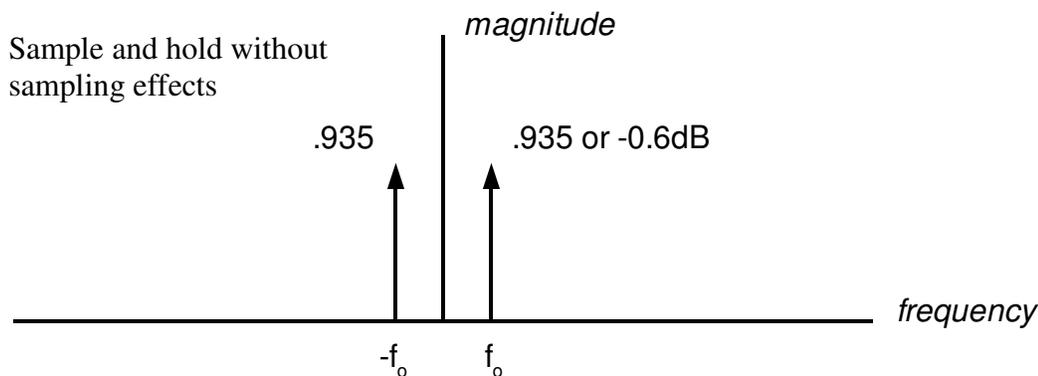
Output of ideal sample and hold, including sampling effects:

f_s=50MHz

magnitude

.935

.935 or -0.6dB

frequency

$-f_s-f_o$ $-f_s+f_o$ $-f_o$ f_o f_s-f_o f_s+f_o

10MHz   40MHz
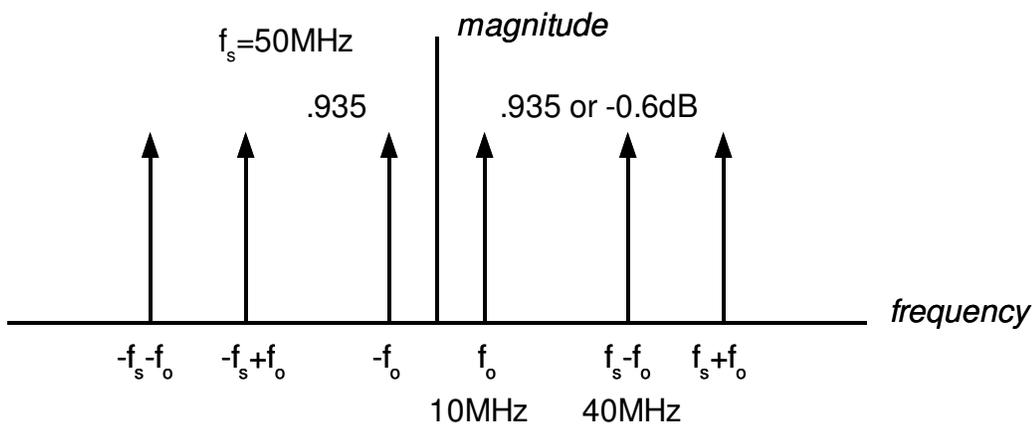
The reconstruction filter is designed to have gain equal to the attenuation of the sample and hold stage, reconstructing the exact signal that was initially sampled.

Output after ideal reconstruction:

magnitude

1   1

frequency

$-f_o$ f_o

10MHz
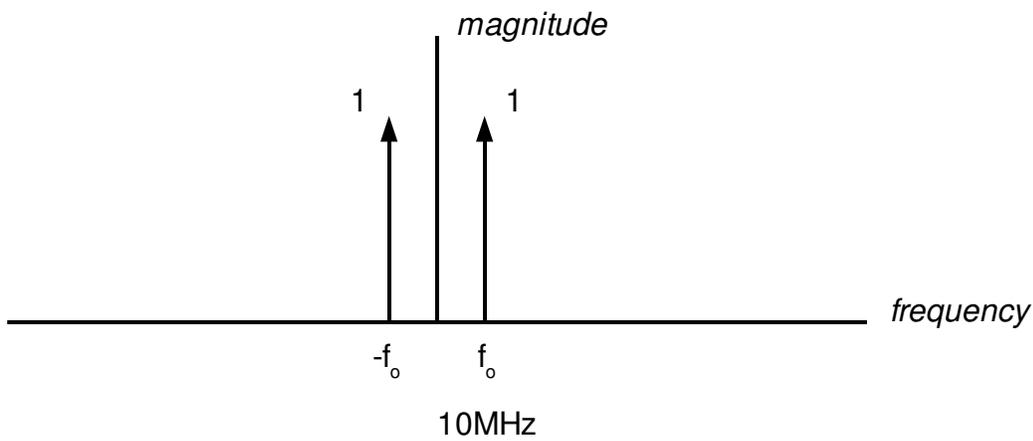
Q 2.7   Suppose we are interpolating, with $K=8$, digital data with $f_s=$ 100MHz. Prior to interpolation what is the frequency range of the desired spectrum? After interpolation what is the frequency range of desired spectrum? What is the interpolator's output clock rate?

Solution: The block diagram of interpolation scheme is as shown below:

Interpolate (increase sample rate)

$x[nT_s]$ $y\left[i.\dfrac{T_s}{K}\right]$

In   Out   K

Input word rate, f_s Output word rate, Kf_s
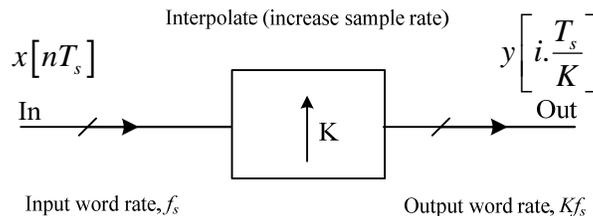
Figure 1

Interpolation is a technique which is applied to overcome the difficulties involved in designing the brickwall shaped RCFs (reconstruction filters) with a cutoff frequency of $f_s/2$ (the Nyquist frequency). In this scheme the incoming signal with sampling frequency of f_s is upsampled by a factor of K (value of K is in power of 2 usually, but not necessarily) while keeping the desired spectrum limited in bandwidth. Thus by *oversampling* the signal by K. f_s the effective Nyquist frequency becomes larger than the maximum wanted frequency of interest. Then the signal is applied to RCF for the desired data.

From the question the interpolation is carried on digital data with $f_s=$ 100MHz. Based on the discussion above the desired frequency range of the spectrum should be $\leq f_s/2$ or f_n (Nyquist frequency) i.e. $f_{desired} \leq 50\text{MHz}$.

After interpolation the new Nyquist frequency $f_{n,new}$ of the system becomes

$K \cdot f_s/2 = 8 \times 50\text{MHz}$

$f_{n,new} = 400\text{MHz}$

As mentioned earlier this new $f_{n,new}$ relaxes the criterion for the design of RCF, though the original information still resides in frequency spectrum of $\leq f_s/2$ i.e. 50 MHz now the RCF can start roll off at $f_s/2$ and extended up to $K \cdot f_s - f_s/2$.

Thus after interpolation, the frequency range of desired spectrum is still $\leq f_s/2$ i.e. 50 MHz.

From figure 1 it is clear that the interpolator output clock rate is $K \cdot f_s = 800\text{MHz}$. Figure 2 below shows an example spectrum, adapted from Figure 2.27 on page 45 of course book to explain the concept better.

$$K = 8$$
$$f_s = 100MHz$$

(a)

Desired Signal Spectrum

Interpolator Input

f_n f_s

New Nyquist Frequency

(b)

After zero padding

f

RCF response

(c)

After (ideal) image removal filter

$K \cdot f_s - f_s/2$

f

(d)

After (non-ideal) image removal filter

$K \cdot f_s/2$

$K \cdot f_s$

f
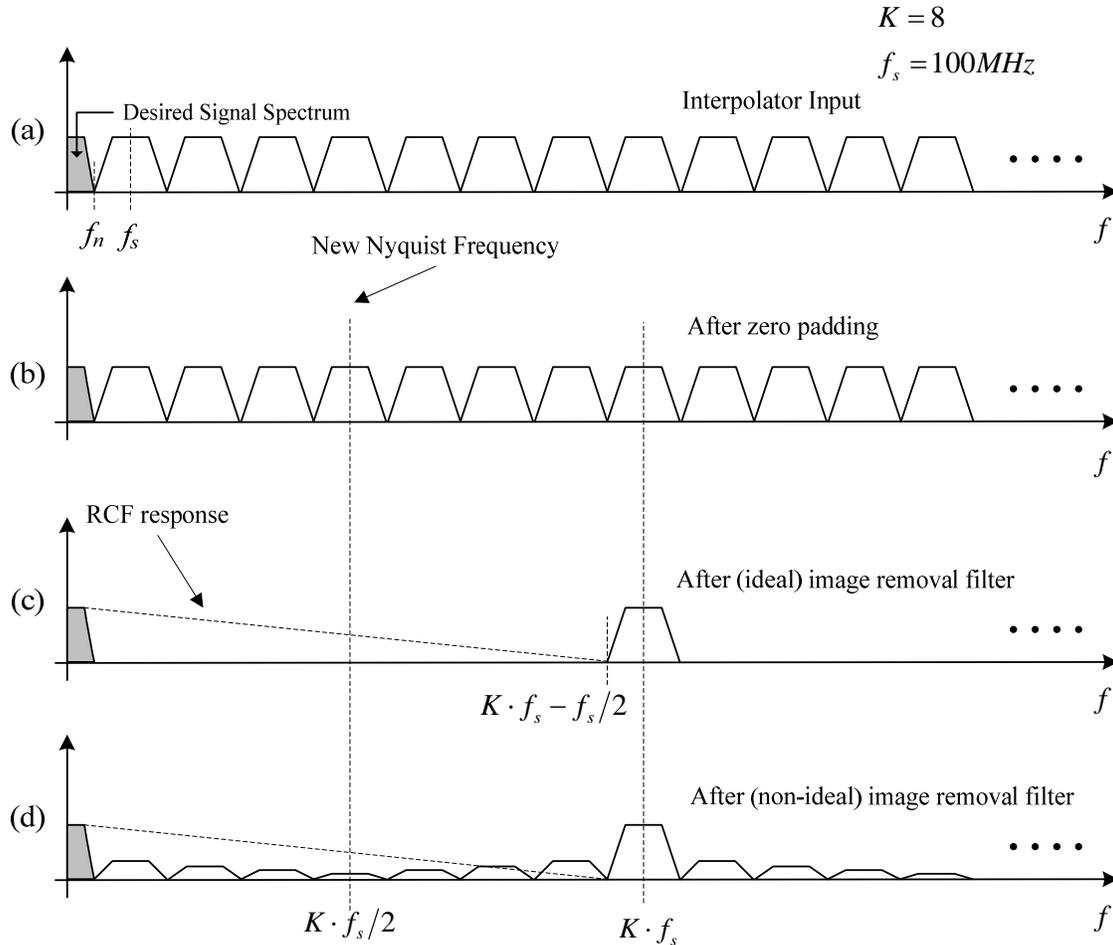
Figure 2

Figure 2 demonstrates one of the scheme for interpolation i.e. zero padding when $K = 8$. Part (a) of figure shows the desired signal spectrum and interpolator input. After zero padding part (b) shows the image frequencies along with desired signal. In part (c) after interpolation an ideal image removal filter removes the image frequencies and signal is applied to RCF. The frequency response of RCF is shown in part (c) as well, where it starts to roll of at $f_s/2$. Part (d) shows the non-ideal image removal with some minor spectral content. After passing it to RCF the major signal power lies in the spectrum of $f \leq f_s/2$.

2.8: *Verify, with simulations, that the topologies seen in Fig. 2.34 are equivalent.*

First, I will make my life easier by borrowing the LTSpice schematic and setup of an analog S/H (Sample and Hold) circuit from the one used in the book to create Figure 2.18. This is seen below in Figure 1:
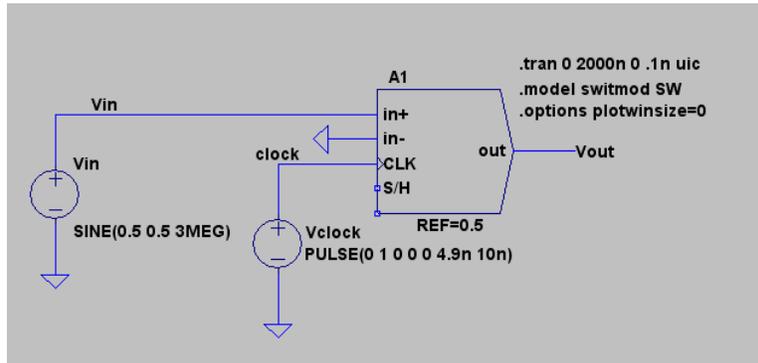
Figure 1: Analog S/H setup borrowed from the book LTSpice set used to create figure 2.18. For clarity, in this solution this configuration will be referred to as configuration A.

I will use this setup to generate the single S/H interpolation path. From Figure 1, we can see that T_s is 10ns. Since the single path S/H should have twice the frequency of the dual path S/H, the T_s of our dual path setup will be 20ns, or half of the sample frequency.

It is a simple matter to copy the previously existing schematic and apply an inverted clock pulse (**at half the frequency, or double the period of the single S/H config.**) to the second S/H path. The Input signal is plumbed to both S/H blocks, and the outputs are summed using two 5K resistors (as can be seen in the book Figure 1.11). Note that it is a time saver to modify and use previously existing schematics and simulations instead of starting from scratch. The K=2 (dual path) S/H schematic can be seen in Figure 2 below:
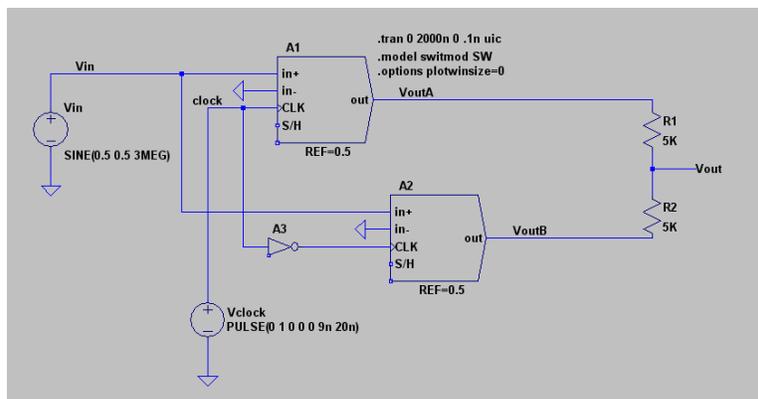
Figure 2: K=2 Dual Path S/H at 1/2 the clock frequency of the single S/H schematic. For clarity, in this solution this configuration will be referred to as configuration B, or the K=2 dual path configuration.

Now let's take a look at the simulation results for each configuration. For clarity, in this solution the configuration in Figure 1 and in Figure 2 will be referred to as configuration A and B, respectively. Figure 3 shows the simulation results of config. A.
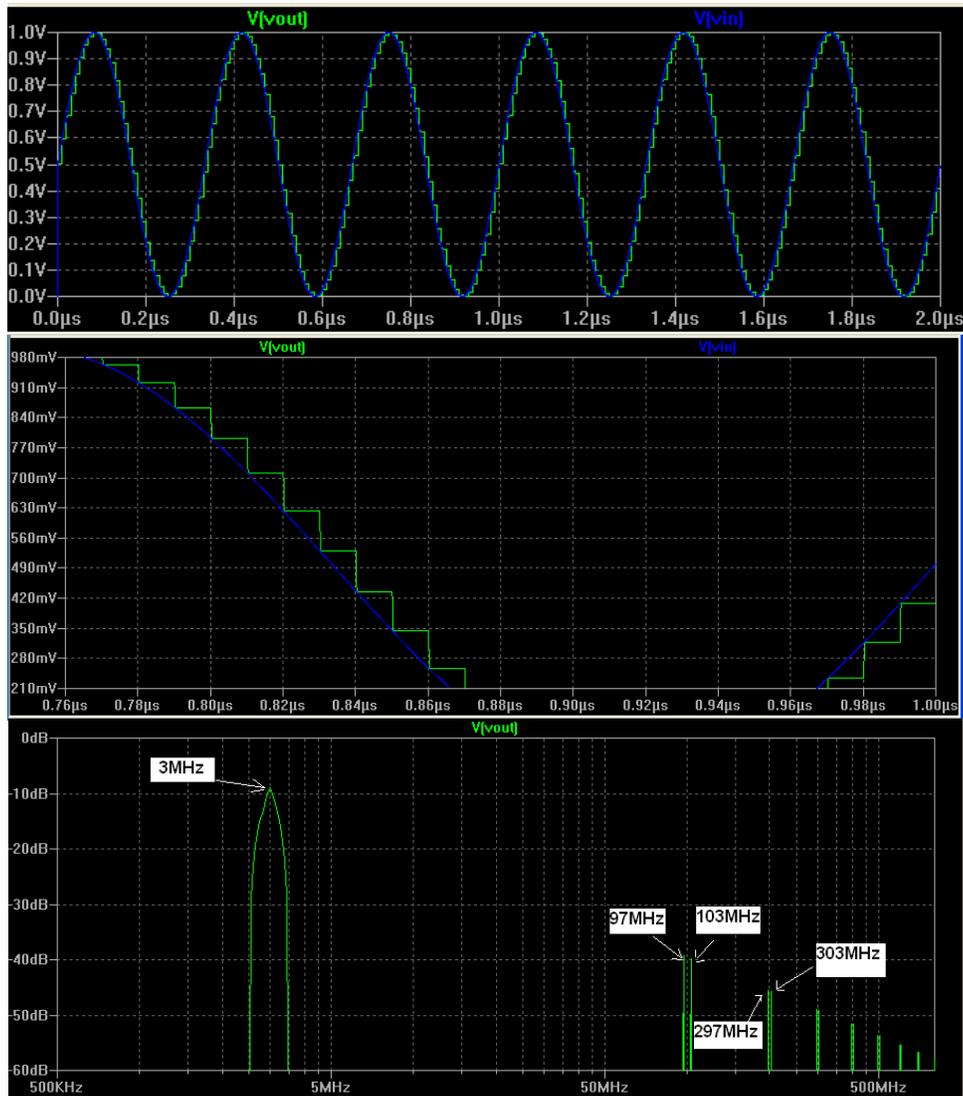
Figure 3: Input and output results of configuration A simulation, along with the fft from 0 to 800MHz of the output signal.

This is what we expect in simulation results of a simple sample and hold circuit. The S/H samples the input every 10ns and holds that value until another period passes, at which point it samples again. The fft shows our 3MHz signal at a solid ~-9dB (on account of fft's using rms values instead of peak values), and the repeating spectrum at f_s +/- our signal frequency. Also, the magnitudes of the higher frequency spectra are attenuated according to the expected sinc response of the S/H.

Now let's take a look at the results for the configuration B simulation.
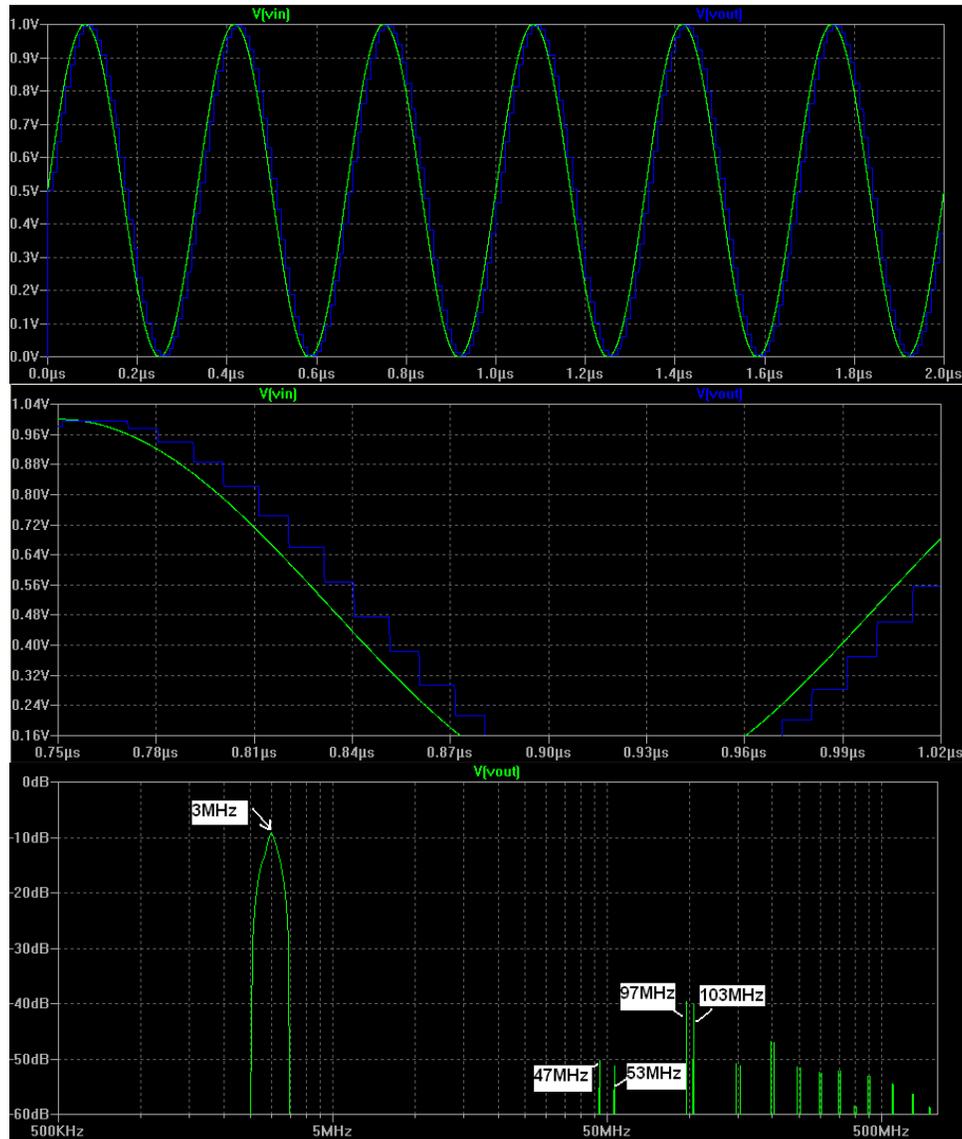
Figure 4: Input and output results of configuration B simulation, along with the fft from DC to 800MHz of the output signal.

The configuration B simulation results are also, more or less, what we expect. There are some minor differences…

In comparing the simulation results for configuration A and B a few differences are apparent. While it appears that the sample and hold occurs for both configuration at a 10ns period, there appears to be more of a delay in the K=2 dual path configuration (config B). Also, there appears to be additional frequencies, albeit they are quite attenuated, on the fft response for configuration B. Let's look at these differences, starting with the increased delay.

Increased Delay for Configuration B:
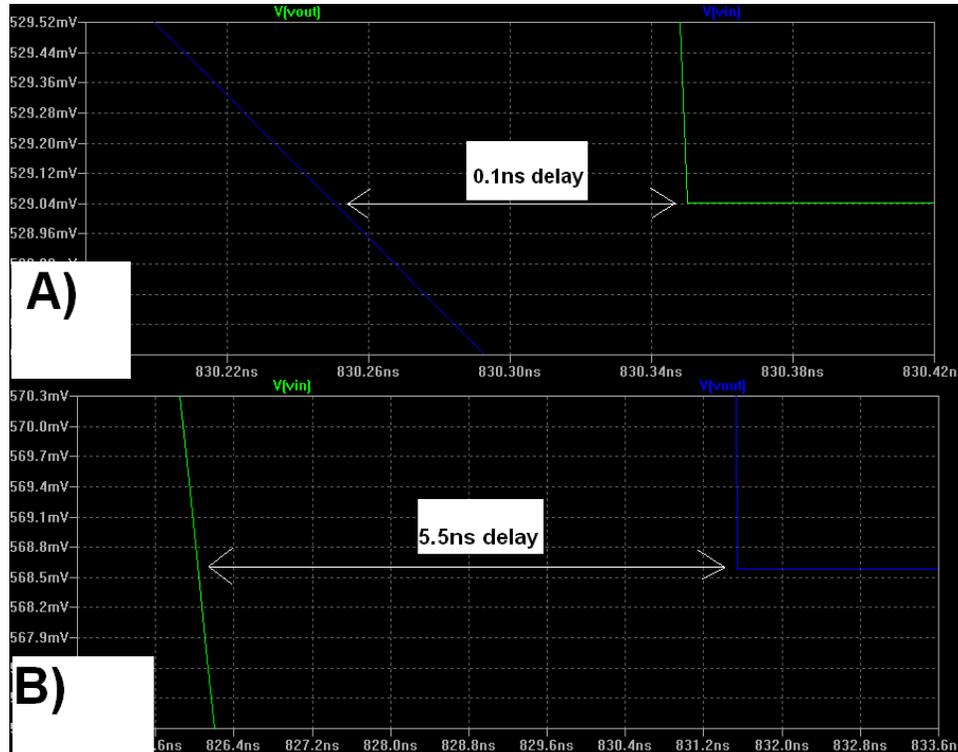
Figure 5: Comparison of the S/H delay characteristics between configuration A and B, respectively.

This difference is explained in the book on page 50. To summarize, when using a two-path topology to interpolate, a delay of T_s/K is expected on the output. T_s for configuration B is 10ns, so a delay of ~5ns is expected.

Additional fft frequencies in configuration B:

A significant benefit of a 2-path interpolation scheme such as the one we have in configuration B is to lower the requirements of the RCF by effectively increasing f_s. Using the two-path topology, we don't need to increase the clock frequency in order to increase the output signal frequency. We do this by sampling the signal twice inside of a single clock period instead of once. Then we add the two together. Each S/H operates at 20ns, a sampling frequency of 50MHz before the signals are added. However, the output sum reflects a period of 10ns, or 100MHz. Therefore, when looking at the fft, we see the large frequency spectra contributed by the output signal at repeating 100MHz intervals… but we also see some "ghosting" frequency spectra at the *actual* sample frequency of the two constituent S/H circuits at repeating 50MHz intervals. In other words, this fft effect is the result of the summing that occurs between two 50MHz signals to produce the 100MHz output.

2.9   Determine the transfer function, and verify with simulations, the behavior of 4 paths of the switched-capacitor topology seen in Fig. 2.36.

To understand how to solve this problem the reader must read sections 2.1.5 – 2.1.6. The reconstruction filter (RCF) will not be able to fully attenuate (set to 0) the spectral content above the Nyquist Frequency ($f_N = f_S/2$). F-1 shows the difference between an ideal and a typical RCF
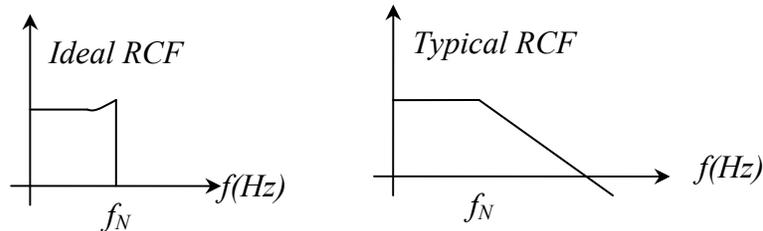
F-1 Representing an ideal and typical RCF

We can increase the sampling frequency (f_s) so that the f_N moves to a higher frequency and we keep the same restrictions on the input spectrum. Linear interpolation can be accomplished by a K path switched capacitor circuit. To determine the transfer function of a K path switched capacitor circuit let us begin with the 1 path switched capacitor circuit seen in F-2. We will go through the derivation shown on pages 51 and 52, because they are essential to understanding a 4 path switched-capacitor circuit.
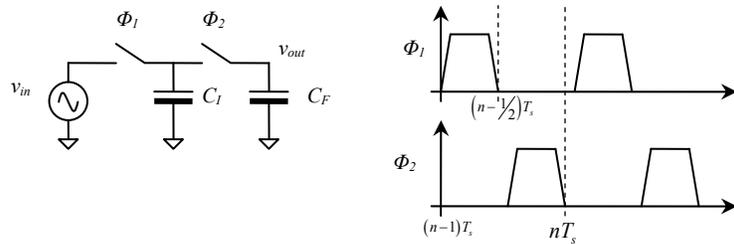
F-2 Switched-capacitor sampling circuit

To determine the transfer function of the switched-capacitor circuit seen in F-2 we will use the equations on page 51:

$$Q_{vout} = v_{out}[nT_s] \cdot (C_I + C_F) = v_{in}\left[\left(n - \frac{1}{2}\right)T_s\right] \cdot C_I + v_{out}[(n-1)T_s] \cdot C_F$$

To understand this equation let's take a closer look at how this circuit works. At $t = (n - 1) \cdot T_s$, both switches are open and we must find the charge on the capacitors:

$$Q_{C_F} = v_{out}\left[(n-1)T_s\right] \cdot C_F$$

$$Q_{C_I} = v_{in}\left[(n-1) \cdot T_s\right] \cdot C_I$$

When Φ_1 closes the charge on C_I is updated with charge from the input and at $t = (n - 1/2) \cdot T_s$ that charge is left on C_I:

$$Q_{C_I} = v\left[\left(n - \tfrac{1}{2}\right) \cdot T_s\right] \cdot C_I$$

Then Φ_2 opens at t = (n − 1/2) and because charge must be conserved we can now say that the charge left on the output is equal to the charge that was previously on the capacitors, or:

$$v_{out}\left[nT_s\right] \cdot (C_I + C_F) = v_{in}\left[\left(n - \tfrac{1}{2}\right)T_s\right] \cdot C_I + v_{out}\left[(n-1)T_s\right] \cdot C_F$$

Writing this in the z – domain and solving for the gain:

$$v\left[(n-1) \cdot T_s\right] \rightarrow V \cdot z^{-1}$$

$$\frac{v_{out}(z)}{v_{in}(z)} = \frac{C_I \cdot z^{-1/2}}{C_I + C_F - C_F \cdot z^{-1}} \tag{1}$$

For input frequencies $\ll$ f_s this circuit behaves like a low-pass RC filter. For f $\ll$ f_s we can write:

$$e^{j2\pi\frac{f}{f_s}} \approx 1 + j2\pi\frac{f}{f_s}$$

The $z^{-1/2}$ in the numerator only affects the delay of the output by half of T_s and is negligible for $f \ll f_s$. The transfer function this becomes:

$$\left|\frac{v_{out}}{v_{in}}\right| = \left|\frac{C_I}{C_I + C_F - C_F \cdot \left(1 - j2\pi\frac{f}{f_s}\right)}\right|$$

$$\left|\frac{v_{out}}{v_{in}}\right| = \left|\frac{\dfrac{C_I}{C_F}}{\dfrac{C_I}{C_F}+1-\left(1-j2\pi\dfrac{f}{f_s}\right)}\right| = \left|\frac{1}{1+j2\pi C_F\dfrac{f}{C_I f_s}}\right|$$

The transfer function now looks like a RC low-pass filter with:

$$R_{sc} = \frac{1}{C_I f_s}$$

To determine the transfer function and behavior of a 4-path switched-capacitor consider F-3.
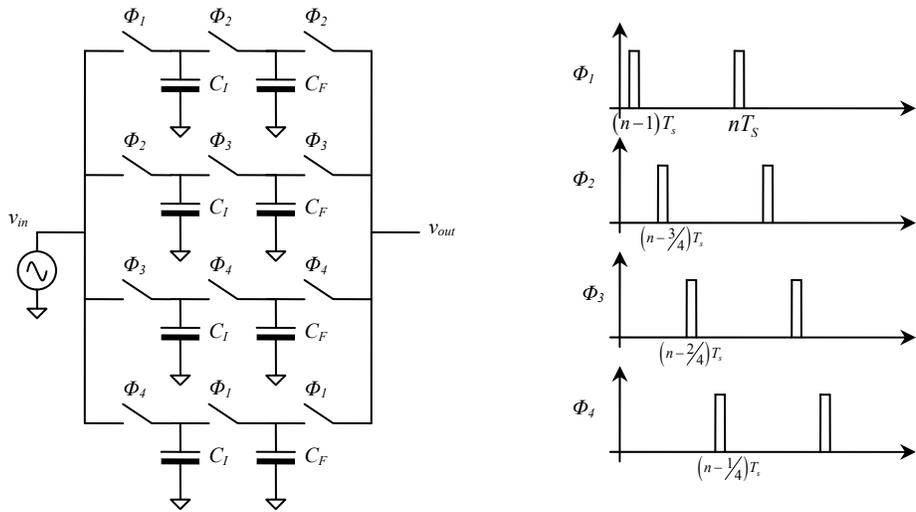
F-3 Schematic and clock pulse of a K=4 switched-capacitor interpolator

For the single path, the output is updated at every T_s so, using Eq. (2.56), where z (1-path) in Eq. (1) is at the sampling frequency $f_{snew}/K = f_s$ (or $KT_s = 1/f_{snew}$), we can write:

$$z_{1-path} = e^{j2\pi f\,4T_s} = z^4$$

$$\frac{v_{out}(z)}{v_{in}(z)} = \frac{C_I \cdot z^{-2}}{C_I + C_F - C_F z^{-4}} \quad @ \text{ a sampling rate of } 4f_s$$

It is important to note that the R_{sc} of a single path is still:

$$R_{sc} = \frac{1}{C_I f_s}$$

Because the input is sampled (on a single path every $T_s = 1/f_s$). If we let $C_I = 1$ pF, $C_F = 10$ pF, $T_s = 10$ ns:

$$R_{sc} = \frac{1}{1pF \cdot 100MHz} = 10k\Omega$$

Which (for $f \ll f_s$) leads to a low pass filter with:

$$f_{3dB} = \frac{1}{2\pi C_F R_{sc}} = \frac{1}{2\pi \cdot 10pF \cdot 10k\Omega} = 1.6MHz$$

So we would expect the output to be 3dB below the input, or if $v_{in} = 1$ V then $v_{out} = 0.708$ V. Let's prove this with a simulations using LTspice and modifying the Figure 2.36 simulation provided at the book's website:
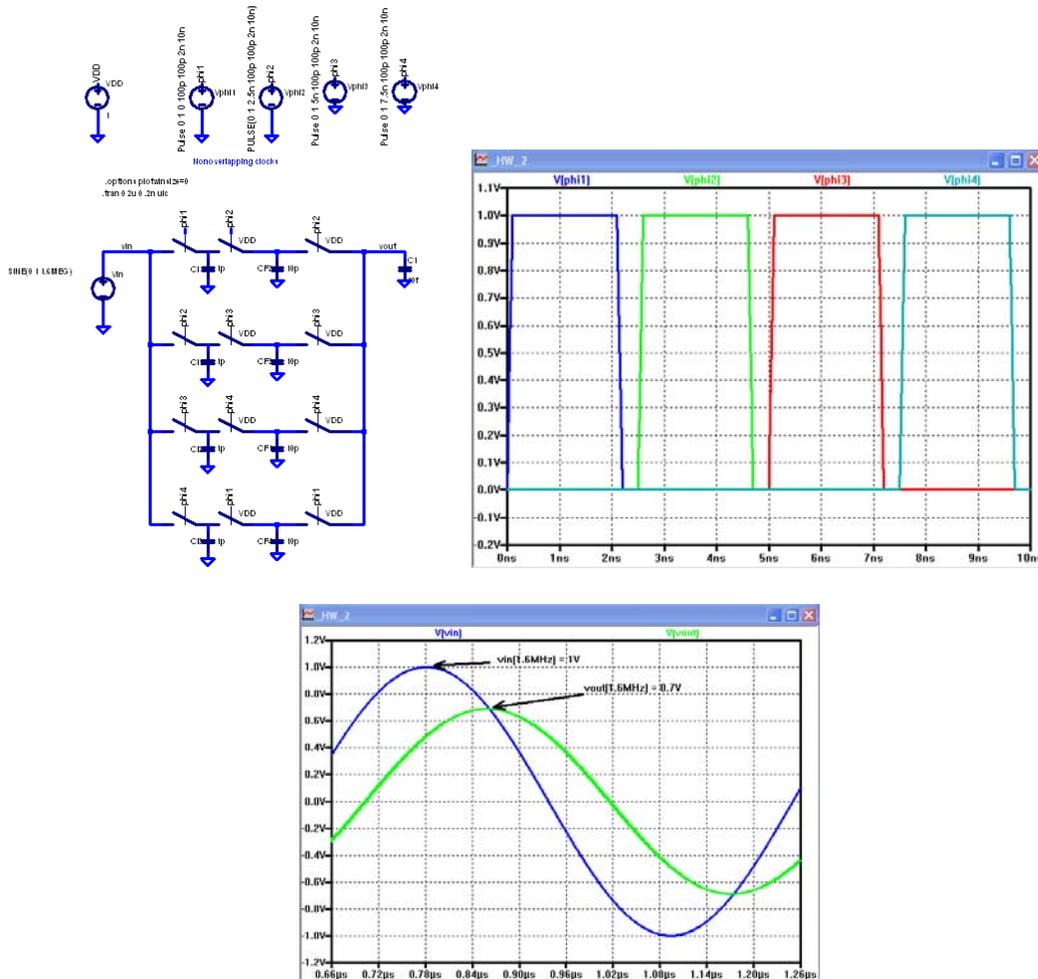
This far we have assumed $f \ll f_s$ but what happens if that stipulation isn't true for a K path switched-capacitor interpolator? We can go back to the z-domain transfer function and determine the frequency response of the transfer function:

$$\frac{v_{out}(z)}{v_{in}(z)} = \frac{\dfrac{C_I}{C_F} \cdot z^{-2}}{\dfrac{C_I}{C_F} + 1 - z^{-4}}$$

Let's look at the magnitude of this transfer function:

$$\left| \frac{v_{out}}{v_{in}} \right| = \frac{\dfrac{C_I}{C_F}}{\sqrt{\left(\dfrac{C_I}{C_F} + 1 - \cos\left(2\pi \dfrac{4f}{f_s} \right) \right)^2 + \sin^2\left(2\pi \dfrac{4f}{f_s} \right)}}$$

Let $x = 2\pi f(4T_s)$:

$$\left| \frac{v_{out}}{v_{in}} \right| = \frac{\dfrac{C_I}{C_F}}{\sqrt{\left(\dfrac{C_I}{C_F} + 1 - \cos x \right)^2 + \sin^2 x}}$$

Let's set up a table for this transfer function and determine the magnitude for crucial frequencies:

f	$x = 2\pi \dfrac{4f}{f_s}$	$\cos x$	$\dfrac{C_I}{C_F} + 1 - \cos x$	$\sin^2 x$	$\left\| \dfrac{v_{out}}{v_{in}} \right\|$	$\left\| \dfrac{v_{out}}{v_{in}} \right\| C_I = C_F$	$\left\| \dfrac{v_{out}}{v_{in}} \right\| C_I < C_F$
0	0	1	$\dfrac{C_I}{C_F}$	0	1	1	1
$\dfrac{f_s}{16}$	$\dfrac{\pi}{2}$	0	$\dfrac{C_I}{C_F} + 1$	1	$\dfrac{\frac{C_I}{C_F}}{\sqrt{\left(\frac{C_I}{C_F}+1\right)^2+1}}$	$\dfrac{1}{\sqrt{5}}$	$\left\|\dfrac{v_{out}}{v_{in}}\right\| < \dfrac{1}{\sqrt{5}}$
$\dfrac{f_s}{8}$	π	-1	$\dfrac{C_I}{C_F} + 2$	0	$\dfrac{\frac{C_I}{C_F}}{\left(\frac{C_I}{C_F}+2\right)}$	$\dfrac{1}{3}$	$\left\|\dfrac{v_{out}}{v_{in}}\right\| < \dfrac{1}{3}$
$\dfrac{3f_s}{16}$	$\dfrac{3\pi}{2}$	0	$\dfrac{C_I}{C_F} + 1$	1	$\dfrac{\frac{C_I}{C_F}}{\sqrt{\left(\frac{C_I}{C_F}+1\right)^2+1}}$	$\dfrac{1}{\sqrt{5}}$	$\left\|\dfrac{v_{out}}{v_{in}}\right\| < \dfrac{1}{\sqrt{5}}$
$\dfrac{f_s}{4}$	2π	1	$\dfrac{C_I}{C_F}$	0	1	1	1
$\dfrac{5f_s}{16}$	$\dfrac{5\pi}{2}$	0	$\dfrac{C_I}{C_F} + 1$	1	$\dfrac{\frac{C_I}{C_F}}{\sqrt{\left(\frac{C_I}{C_F}+1\right)^2+1}}$	$\dfrac{1}{\sqrt{5}}$	$\left\|\dfrac{v_{out}}{v_{in}}\right\| < \dfrac{1}{\sqrt{5}}$

We can use this to plot the frequency domain of the $K = 4$ switched-capacitor interpolator and use SPICE to verify it:
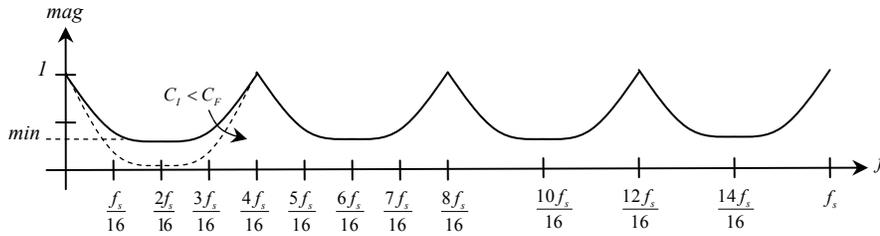
F-4 Frequency response of a K=4 path switched-capacitor interpolator

The simulation results below sets $C_I = C_F$ and simulates at ~0 and $f_s/4$ (note $f_s = K{\cdot}f_s$):
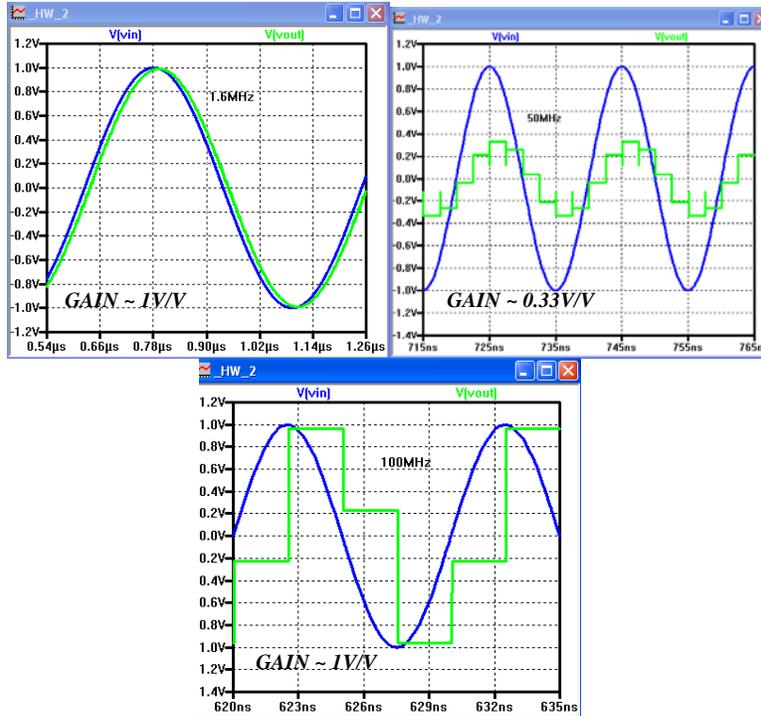
So for $f_{in} << f_s$ we can approximate the response as a low-pass RC filter. When the input frequency increases to where f_{in} is no longer $<< f_s$ we can use the frequency response in F-4 to determine the approximate response seen the simulation results.

Kaijun Li

Problem 2.10

In your own words, why the ϕ_2 switches are shut off after the ϕ_1 switches in the S/H seen in Fig. 2.39?

The topology seen in Fig. 2.39 is a fully differential sample and hold circuit.
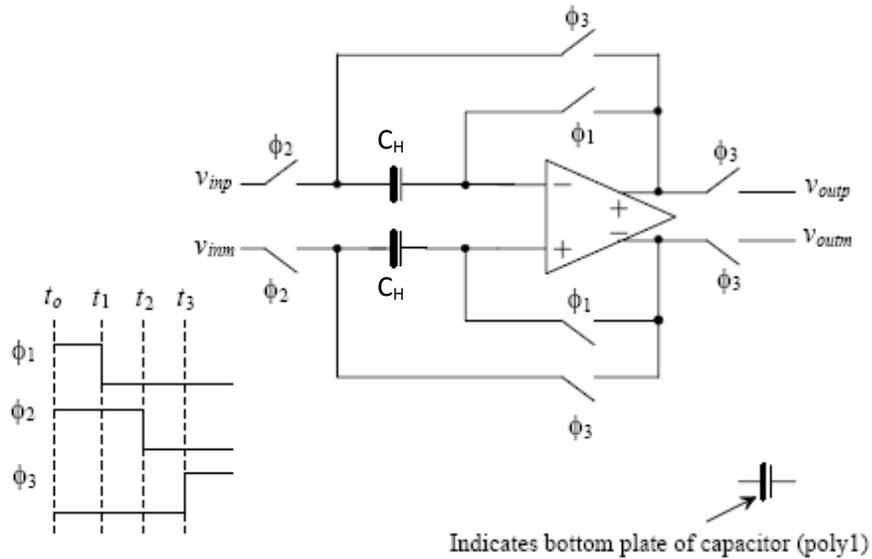
Fig. 2.39 Fully-differential S/H differential topology

The reason why ϕ_2 switches are shut off after the ϕ_1 switches is that when ϕ_2 switches are shut off, the charge injected from ϕ_2 sees capacitor C_H as high impedance. In the other words, if the ϕ_2 switches are shut off first, the inverting input node of the op-amp connects the top plate of C_H to the positive output node of the op-amp, and this makes the impedance seen from the bottom plate of C_H a low impedance. So if the ϕ_2 switches are shut off first, the charge injected from ϕ_2 switches not only goes into input node v_{inp}, v_{inm}, but into hold capacitor C_H, which means when ϕ_1 switches are shut off, the charge transferred into output node will be input dependent.

2.11) *Sketch the op-amp's open loop response, both magnitude and phase, specified by Eq. (2.59).*

Solution:
Equation 2.59 gives the open-loop frequency response of an op-amp with a single dominant pole.

$$A_{OL}(f) = \frac{A_{OLDC}}{1 + j.\dfrac{f}{f_{3dB}}} \qquad \text{Eq. (2.59)}$$

For more details about the derivation of this equation, refer to pg.680 of *CMOS: Circuit Design , Layout and Simulation* book.

We are asked to sketch the op-amp's magnitude and phase response plots versus input frequency. To do this, lets find the magnitude of the transfer function.
Taking magnitude of the above equation we get,

$$Magnitude = \frac{|A_{OLDC}|}{\sqrt{1^2 + \left(\dfrac{f}{f_{3dB}}\right)^2}}$$

Magnitude Resposne
To plot the magnitude response, we calculate the magnitude at a few frequencies and plot it against input frequency.

- At DC or at f=0, magnitude of op-amp's open loop response is just A_{OLDC} .

- For input frequencies less than f_{3dB} , we can consider $\dfrac{f}{f_{3dB}} = 0$. Therefore, magnitude

still remains at A_{OLDC} .
- Therefore, we can see that as we get very close to f_{3dB} , the magnitude response starts to decrease. And once the input frequency exceeds f_{3dB} the magnitude response starts to rolloff at a rate of -20 dB/dec. The -20 dB/dec rolloff comes due to the fact that at higher frequencies, the magnitude response can be written as,

$$Magnitude @ Hi-frequencies = \frac{|A_{OLDC}|}{\sqrt{\left(\dfrac{f}{f_{3dB}}\right)^2}} = \frac{|A_{OLDC}|}{\dfrac{f}{f_{3dB}}} = |A_{OLDC}|.\frac{f_{3dB}}{f}$$

Now, to plot the magnitude in frequency domain on a log plot, we calculate magnitude as equal to $20\cdot\log\left(|A_{OLDC}|\cdot\dfrac{f_{3dB}}{f}\right) = 20\cdot\log(|A_{OLDC}|) + 20\cdot\log\left(\dfrac{f_{3dB}}{f}\right)$.

As the frequency increases up in a decade ($f = 10\cdot f_{3dB}$), magnitude of the op-amp's open loop response will be equal to

$$20 \cdot \log\left(\left|A_{OLDC}\right|\right) + 20 \cdot \log\left(\frac{f_{3dB}}{10 \cdot f_{3dB}}\right) = 20 \cdot \log\left(\left|A_{OLDC}\right|\right) + 20 \cdot \log\left(\frac{1}{10}\right) = 20 \cdot \log\left(\left|A_{OLDC}\right|\right) - 20$$

Therefore, for every decade increase in input frequency, the magnitude of the op-amp's open loop response will fall at the rate of -20dB/decade. Sketching the magnitude response of the open-loop gain looks like:
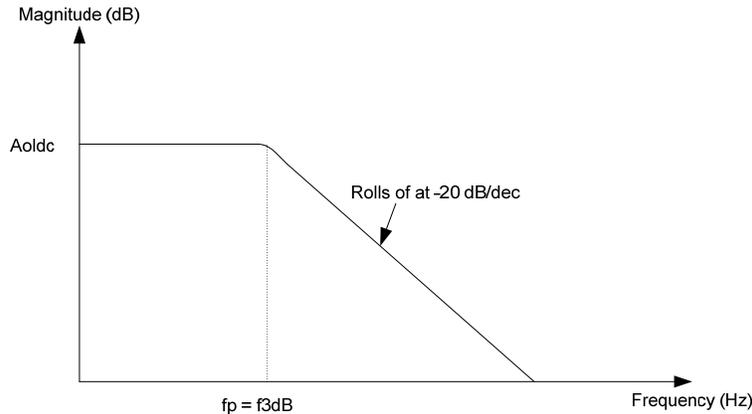
Figure 1: Magnitude Response of an Op-Amp

Phase Response:

Calculating the phase of eq 2.59 we get,

$$\angle = \tan^{-1}\left(\frac{0}{A_{OLDC}}\right) - \tan^{-1}\left(\frac{\frac{f}{f_{3dB}}}{1}\right) = -\tan^{-1}\left(\frac{f}{f_{3dB}}\right).$$

- At DC, we see that the phase response of the op-amp's open loop response is 0°.
- At $f = f_{3dB}$, the phase response is 45°.
- For higher frequencies, the phase response reaches its peak value of -90°.

Using these values, the phase response of the op-amp is sketched below:
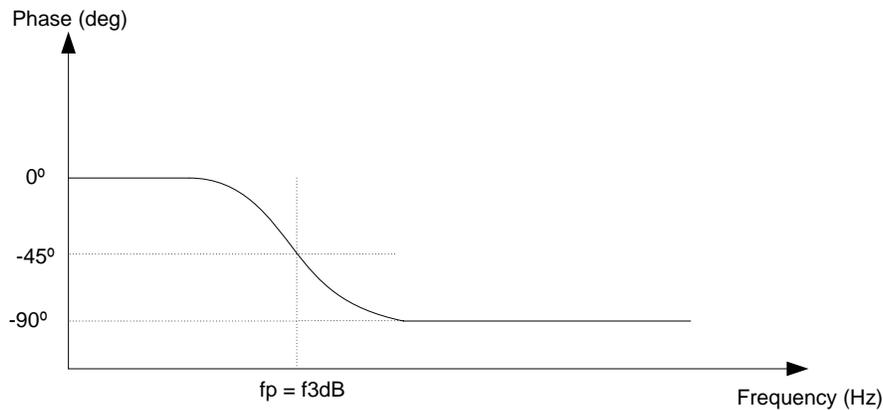
Figure 2: Phase Response of an Op-Amp

Avinash Rajagiri
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Since an ideal op-amp has a single dominant pole, like a RC response we can see that the gain will rolloff at -20dB/decade once the first pole kicks in at f_{3dB}. Also, due to this pole we will have a phase shift of 90° in the phase response of the circuit.

Solution by Jake Baker

2.12 What is the voltage across C_F in Fig. 2.41 in terms of the input-referred offset and noise? Verify your answer with simulations commenting on the deviation of the frequency behavior of the input-referred noise to the frequency response of the voltage across the capacitor.

Solution: Figure 2.41 including the input referred noise, $V_{inoise}^2(f)$, power spectral density (PSD with units of V^2/Hz) and op-amp offset voltage is reproduced below for convenience. When the ϕ_1 switches are closed the op-amp is in the voltage follower configuration and so the voltage across C_F, assuming large op-amp gain so the $+$ and $-$ op-amp inputs are driven to the same voltage, is

$$V_{CF} = v_{in} - [V_{CM} + V_{OS} + v_{inoise}(t)] \text{ for } t \leq t_1$$

This isn't really important since the ϕ_3 switch connected to the output of the op-amp is open and thus v_{out} is isolated from the op-amp.
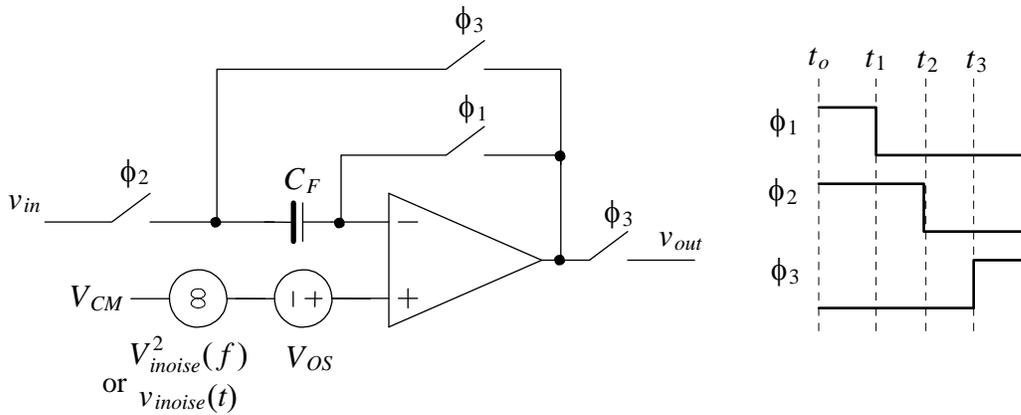
Figure 2.41 S/H with input-referred offset and noise shown.

At t_3, when the ϕ_3 switches close, the voltage on the inputs of the op-amp is

$$V_{CM} + V_{OS} + v_{inoise}(t_3)$$

The output voltage for $t_3 \leq t \leq t_3 + T_s/2$ (when the ϕ_3 switches are closed) is

$$v_{out}(t) = v_{in}(t_3) - v_{inoise}(t_3) + v_{inoise}(t)$$

and the voltage on the inputs of the op-amp is

$$V_{CM} + V_{OS} + v_{inoise}(t)$$

The voltage across C_F during this time is

$$V_{CF} = v_{in}(t_3) - v_{inoise}(t_3) + v_{inoise}(t) - [V_{CM} + V_{OS} + v_{inoise}(t)]$$

or

$$V_{CF} = v_{in}(t_3) - v_{inoise}(t_3) - V_{CM} - V_{OS}$$

In other words the voltage across C_F doesn't vary for $t_3 \leq t \leq t_3 + T_s/2$ (when the ϕ_3 switches are closed). The DC component of the noise (offset) is removed from v_{out} and stored on C_F as seen in this equation. The higher the frequency of the noise (relative to $1/T_s$) the less benefit we get from autozeroing.

If we could, somehow, get the voltage across C_F to vary with the op-amp's input-referred noise when the ϕ_3 switches are closed then we could remove all of the noise, not just the slow noise, from the S/H's output. This means that the voltage across C_F would vary when the ϕ_3 switches are closed to cancel-out the op-amp's noise.

The simulation used to generate Fig. 2.44 was run and the voltage across C_F is plotted below. A zoomed in view to show the voltage across C_F doesn't vary during $t_3 \leq t \leq t_3 + T_s/2$ (again, when the ϕ_3 switches are closed) is also provided.
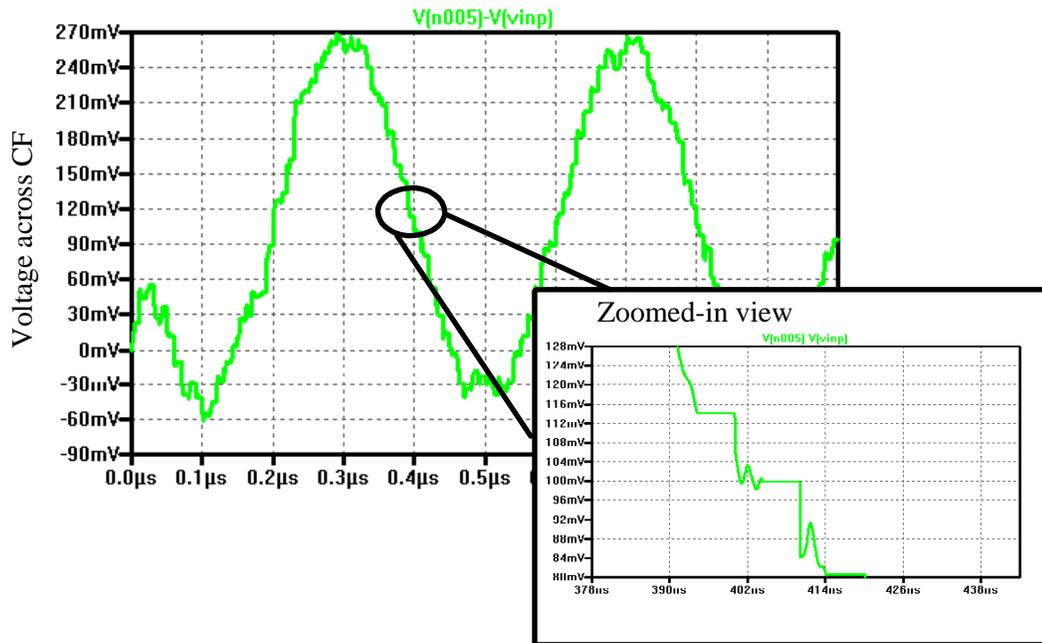
2.13. Provide a quantitative description of how capacitor mismatch will affect the operation of the S/H seen in Fig. 2.46. Verify your descriptions with simulations.

Sol: Consider the S/H topology seen in Fig 2.46. The implementation of this topology is as shown below in Fig. 1.
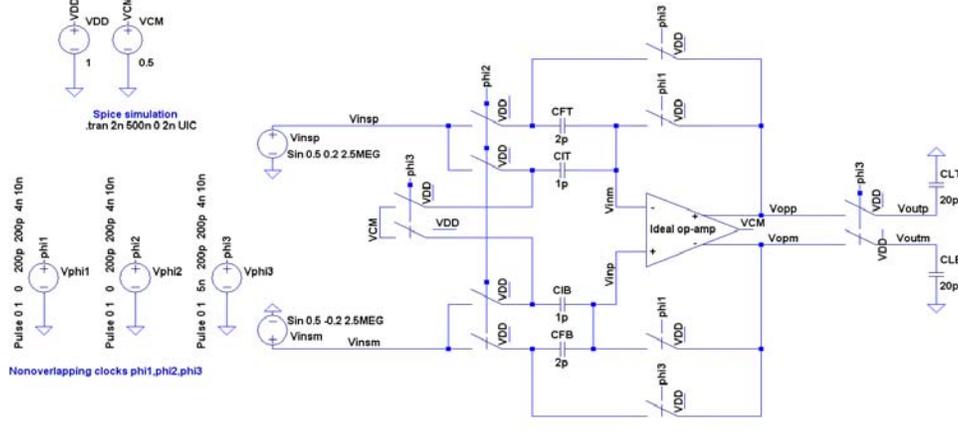
Figure 1. A "Sample/Hold circuit with gain" implementation of topology as in Fig 2.46

The differential gain of this topology when there is no mismatch in the capacitors is $(1 + C_I/C_F)$ from equation 2.84 on page 62 of textbook. The capacitances on the inverting terminal are C_{FT}, C_{IT}. The capacitances on the non inverting terminal are $C_{FB,}$ $C_{IB.}$ C_{FT} and C_{IT} are given by

$$C_{FT} = C_F$$
$$C_{IT} = C_I$$

Let us say there is a mismatch in the capacitances on the non inverting terminal with capacitances on the inverting terminal.

$$C_{FB} = C_F + \Delta C_F$$
$$C_{IB} = C_I + \Delta C_I$$

Then v_{out+} due to v_{in+} (i.e. Vinsp in Fig .1) is using equation 2.83 on page 62 of textbook

$$V_{out+} = (1 + C_I/C_F)(v_{in}+) - (C_I/C_F)V_{CM}$$

Then v_{out-} due to v_{in-} (i.e. Vinsm in Fig .1) is

$$V_{out-} = (1 + C_{IB}/C_{FB})(v_{in}-) - (C_{IB}/C_{FB})V_{CM}$$

$$V_{out-} = \left(1 + \frac{C_I + \Delta C_I}{C_F + \Delta C_F}\right)(v_{in}-) - \left(\frac{C_I + \Delta C_I}{C_F + \Delta C_F}\right)V_{CM}$$

$$V_{out-} = \left(1 + \frac{C_I(1 + \Delta C_I/C_I)}{C_F(1 + \Delta C_F/C_F)}\right)(v_{in}-) - \frac{C_I(1 + \Delta C_I/C_I)}{C_F(1 + \Delta C_F/C_F)}(V_{CM})$$

Assuming the mismatch in capacitances ΔC_F, ΔC_B is very small compared to C_F, C_B we can use Taylor series expansion to expand $(1 + \Delta C_F/C_F)^{-1}$ and neglecting higher order terms in the expansion we derive the below equation.

$$\left(1+\Delta C_F/C_F\right)^{-1} = 1-\left(\Delta C_F/C_F\right)$$

Based on above formula and reducing v_{out-} term we get

$$V_{out-} = \left(1+\frac{C_I\left(1+\Delta C_I/C_I\right)\left(1-\left(\Delta C_F/C_F\right)\right)}{C_F}\right)\left(V_{in}-\right)-\left(\frac{C_I\left(1+\Delta C_I/C_I\right)\left(1-\left(\Delta C_F/C_F\right)\right)}{C_F}\left(V_{CM}\right)\right)$$

Further simplifying we get

$$V_{out-} = \left(1+\frac{C_I}{C_F}\right)\left(V_{in}-\right)-\left(\left(\frac{C_I}{C_F}\right)V_{CM}\right)+\left(\frac{\Delta C_I}{C_F}\right)\left(V_{in}-\right)-\left(\frac{C_I\times\Delta C_F}{C_F^2}\right)\left(V_{in}-\right)-\left(\frac{C_I\times\Delta C_I}{C_F^2}\right)\left(V_{CM}\right)+\left(\frac{C_I\times\Delta C_F}{C_F^2}\right)\left(V_{CM}\right)$$

$$\left(V_{out}+\right)-\left(V_{out}-\right) = \left(1+\frac{C_I}{C_F}\right)\left(\left(V_{in}+\right)-\left(V_{in}-\right)\right)-\left(\frac{\Delta C_I}{C_F}\right)\left(V_{in}-\right)+\left(\frac{C_I\times\Delta C_F}{C_F^2}\right)\left(V_{in}-\right)+\left(\frac{C_I\times\Delta C_I}{C_F^2}\right)\left(V_{CM}\right)-\left(\frac{C_I\times\Delta C_F}{C_F^2}\right)\left(V_{CM}\right) \quad (1)$$

From equation (1) it is seen that if $\Delta C_I=0$ and $\Delta C_F=0$ then

$$\left(V_{out}+\right)-\left(V_{out}-\right) = \left(1+\frac{C_I}{C_F}\right)\left(\left(V_{in}+\right)-\left(V_{in}-\right)\right) \quad (2)$$

For simplified analysis assume $C_I=C_F$

$$\left(V_{out}+\right)-\left(V_{out}-\right) = 2\left(\left(V_{in}+\right)-\left(V_{in}-\right)\right)-\left(\frac{\Delta C_I}{C_F}\right)\left(V_{in}-\right)+\left(\frac{\Delta C_F}{C_F}\right)\left(V_{in}-\right)+\left(\frac{\Delta C_I}{C_I}\right)\left(V_{CM}\right)-\left(\frac{\Delta C_F}{C_F}\right)\left(V_{CM}\right) \quad (3)$$

Now let us analyze the following cases.
Case 1: If $\Delta C_I=\Delta C_F$ then

$$\left(V_{out}+\right)-\left(V_{out}-\right) = 2\left(\left(V_{in}+\right)-\left(V_{in}-\right)\right) \quad (4)$$

Now let us verify the simulation and confirm the theoretical gain matches with the gain from simulation. In this example $C_{FT}=1p$, $C_{IT}=1p$, $C_{FB}=1.1p$, $C_{IB}=1.1p$ i.e $\Delta C_I=\Delta C_F=0.1p$. If the differential input i.e. the difference between Vinsp and Vinsm in Fig. 1. is 400mV as shown in Fig. 2., the differential output is 800mV i.e. twice the differential input.
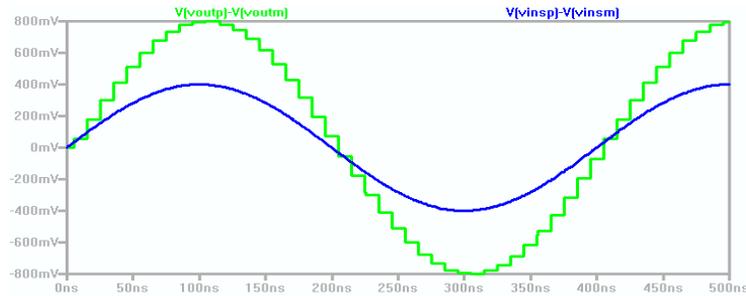

Figure 2. Simulation output when $\Delta C_I=\Delta C_F$

Case 2: If $\Delta C_F = 0$ and $\Delta C_I \neq 0$ then

$$\left(V_{out+}\right) - \left(V_{out-}\right) = 2\left(\left(V_{in+}\right) - \left(V_{in-}\right)\right) - \left(\frac{\Delta C_I}{C_I}\right)\left(V_{in-}\right) + \left(\frac{\Delta C_I}{C_I}\right)\left(V_{CM}\right) \qquad (5)$$

Now let us verify the simulation and theory. In this example C_{FT}=1p,C_{IT}=1p, C_{FB}=1p,C_{IB}=1.1p i.e $\Delta C_I = 0.1p$ and $\Delta C_F = 0$. V_{in-} has an amplitude of 200mV. Substituting these values in (5) we get

V_{out+}- V_{out-}= 2x400mV - (0.1/1)(200mV) + (0.1/1)500mV=830mV, the simulated output is 835 mV.
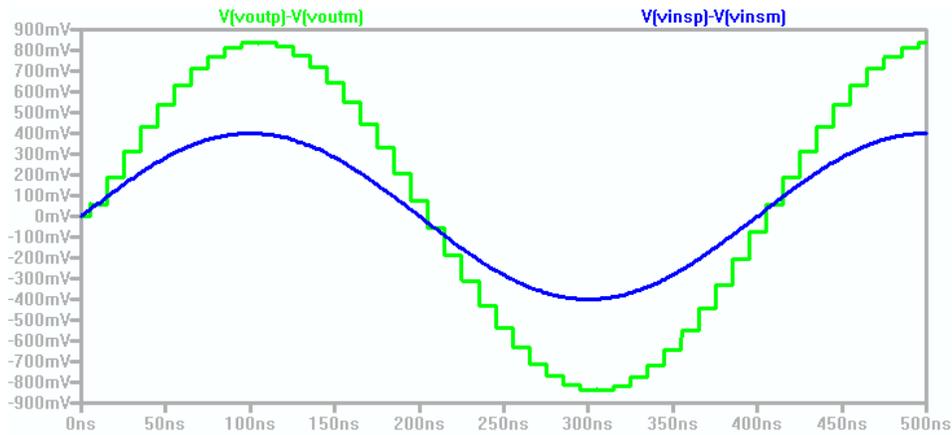
Figure 3. Simulation output when $\Delta C_F = 0$ and ΔC_I =+10%

Case 3: If $\Delta C_I = 0$ and $\Delta C_F \neq 0$ then

$$\left(V_{out+}\right) - \left(V_{out-}\right) = 2\left(\left(V_{in+}\right) - \left(V_{in-}\right)\right) + \left(\frac{\Delta C_F}{C_F}\right)\left(V_{in-}\right) - \left(\frac{\Delta C_F}{C_F}\right)\left(V_{CM}\right) \qquad (6)$$

The calculated value in this case for 10% mismatch in C_F is 730mV. The simulation value in this case is 725mV.
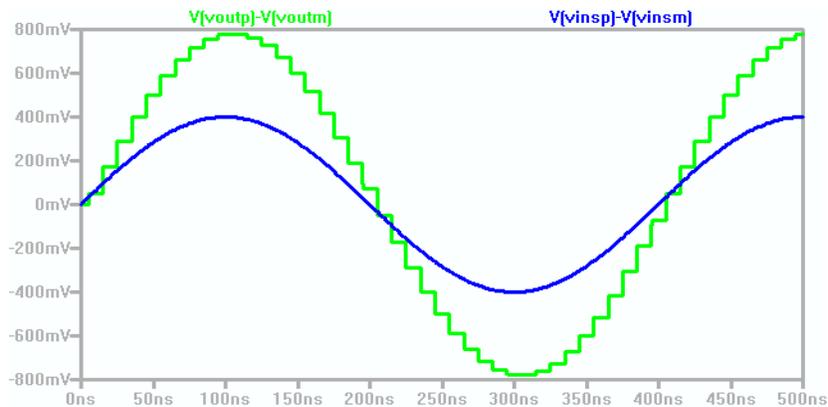
Figure 4. Simulation output when $\Delta C_I = 0$ and ΔC_F =+10%

Solution by Jake Baker

2.14 Is it possible to design a S/H with a gain of 0.5? How can this be done or why can't it be done? Use simulations to verify your answer.

Solution: Yes, it's possible. Consider the modification of Fig. 2.46 seen below. In this figure we have connected the C_F capacitors to V_{CM} instead of the inputs and we've made $C_F = 2C_I$. Below this figure is the simulation output using Fig. 2.48 but with the modified circuit seen below.
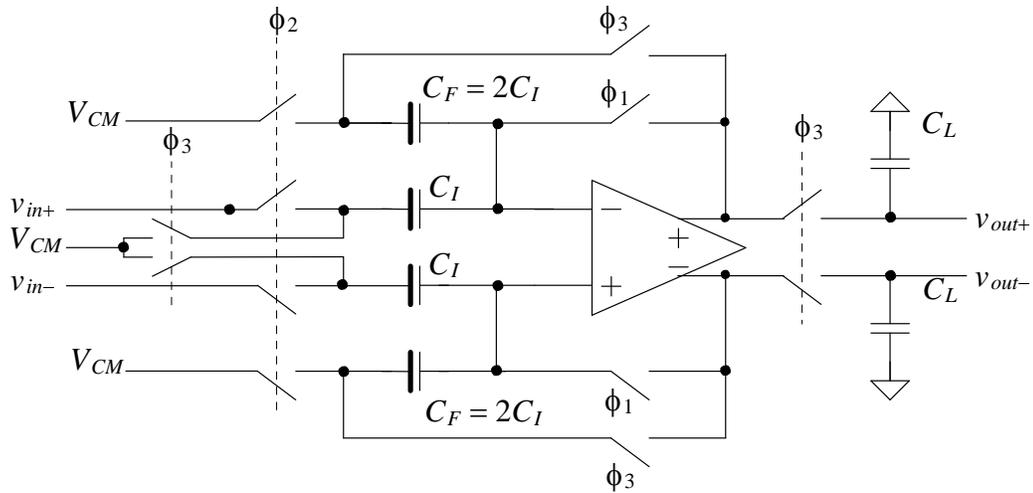
A S/H with gain of 0.5.
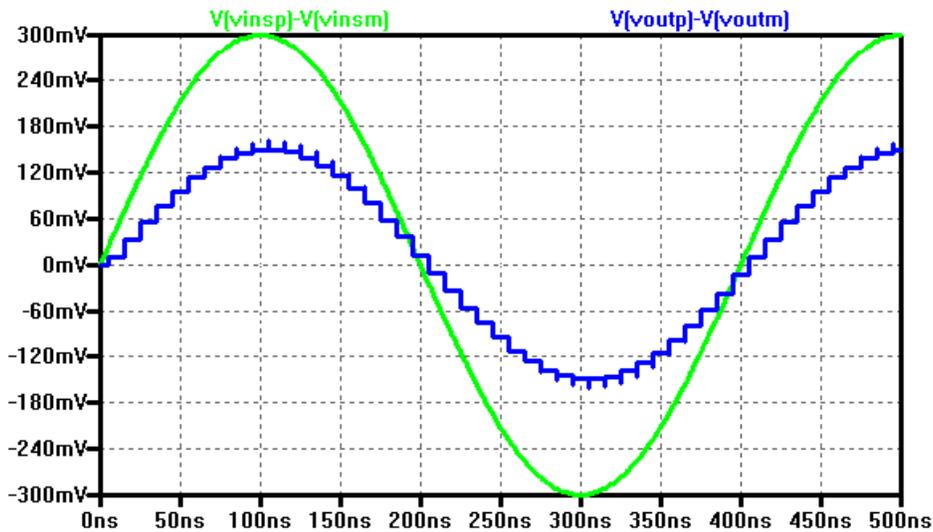
Simulating the circuit seen above using the parameters used to generate Fig. 2.48.

To determine the equation governing the operation of this circuit let's follow the methods used in Sec. 2.2. First,

$$Q_{I,F}^{\phi_1} = C_I \cdot (v_{in} - V_{CM} \pm V_{OS}) + C_F \cdot (V_{CM} - V_{CM} \pm V_{OS})$$

and when the ϕ_3 switches turn on

$$Q_I^{\phi_3} = C_I \cdot (V_{CM} - V_{CM} \pm V_{OS})$$

and

$$Q_F^{\phi_3} = C_F \cdot (v_{out} - V_{CM} \pm V_{OS})$$

Knowing charge must be conserved

$$Q_F^{\phi_3} = C_F \cdot (v_{out} - V_{CM} \pm V_{OS}) =$$

$$= \overbrace{C_F \cdot (\pm V_{OS})}^{Q_F^{\phi_1}} + \overbrace{C_I \cdot (v_{in} - V_{CM} \pm V_{OS})}^{Q_I^{\phi_1}} - \overbrace{C_I \cdot (V_{CM} - V_{CM} \pm V_{OS})}^{Q_I^{\phi_3}}$$

or

$$v_{out} = \frac{C_I}{C_F} \cdot v_{in} - \frac{C_I}{C_F} \cdot V_{CM} + V_{CM}$$

For a fully-differential topology the last two terms are common to both the inverting and non-inverting inputs of the S/H, or

$$v_{out+} - v_{out-} = \left[\frac{C_I}{C_F} \cdot v_{in+} - \frac{C_I}{C_F} \cdot V_{CM} + V_{CM} \right] - \left[\frac{C_I}{C_F} \cdot v_{in-} - \frac{C_I}{C_F} \cdot V_{CM} + V_{CM} \right]$$

so we can write

$$v_{out+} - v_{out-} = \frac{C_I}{C_F} \cdot (v_{in+} - v_{in-})$$

A block diagram is seen below.
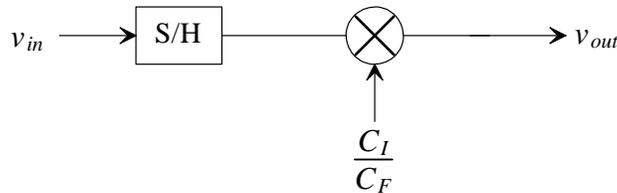
2.15 For the first entry ($v_1 =$ input, $v_2 = v_{CM}$) in Table 2.2 derive the frequency response, magnitude and phase, of the DAI. Use simulations at a few frequencies to verify your derivations.

Solution:

For $v_1 =$ input, $v_2 = v_{CM}$, the z-domain transfer function of the DAI shown in <u>Table 2.2 in [1]</u>, or

1) when output connected to ϕ_1 ,

$$H_1(z) = \frac{C_I}{C_F} \cdot \frac{z^{-1}}{1 - z^{-1}}$$ (1)

2) when output connected to ϕ_2 ,

$$H_2(z) = \frac{C_I}{C_F} \cdot \frac{z^{-1/2}}{1 - z^{-1}}$$ (2)

To evaluate the frequency response of the DAI, we can use <u>Eq. 1.37 in [1]</u>, or

$$z = e^{j2\pi \cdot \frac{f}{f_s}}$$ (3)

Rewriting Eqs. 1 and 2 using Eq. 3 gives

1) when output connected to ϕ_1 ,

$$H_1(f) = \frac{C_I}{C_F} \cdot \frac{e^{-j2\pi f/f_s}}{1 - e^{-j2\pi f/f_s}}$$ (4)

2) when output connected to ϕ_2

$$H_2(f) = \frac{C_I}{C_F} \cdot \frac{e^{-j\pi f/f_s}}{1 - e^{-j2\pi f/f_s}}$$ (5)

Now let us derive the magnitude and phase responses of $H_1(f)$ and $H_2(f)$, respectively.

Geng Zheng

I. Frequency Response of $H_1(f)$

We can get started by multiplying both the numerator and denominator of Eq. 4 by $e^{j2\pi f/f_s}$, or

$$H_1(f)=\frac{C_I}{C_F}\cdot\frac{e^{-j2\pi f/f_s}}{1-e^{-j2\pi f/f_s}}\cdot\frac{e^{j2\pi f/f_s}}{e^{j2\pi f/f_s}}=\frac{C_I}{C_F}\cdot\frac{1}{e^{j2\pi f/f_s}-1} \tag{6}$$

Using Euler's formula

$$e^{jk}=\cos k+j\cdot\sin k \tag{7}$$

we can rewrite Eq. 6 as

$$H_1(f)=\frac{C_I}{C_F}\cdot\frac{1}{\left[\cos(2\pi f/f_s)-1\right]+j\left[\sin(2\pi f/f_s)\right]} \tag{8}$$

which is in the form

$$\frac{1}{a+jb} \tag{9}$$

And we know that, after reviewing Eqs. 1.59 and 1.60 in Section 1.2.5 of [1], the magnitude of Eq. 8 is

$$\left|\frac{1}{a+jb}\right|=\frac{1}{\sqrt{a^2+b^2}} \tag{10}$$

Thus the magnitude of $H_1(f)$,

$$\begin{aligned}\left|H_1(f)\right|&=\frac{C_I}{C_F}\cdot\frac{1}{\sqrt{\left[\cos(2\pi f/f_s)-1\right]^2+\left[\sin(2\pi f/f_s)\right]^2}}\\&=\frac{C_I}{C_F}\cdot\frac{1}{\sqrt{\left[\cos(2\pi f/f_s)\right]^2+1-2\cos(2\pi f/f_s)+\left[\sin(2\pi f/f_s)\right]^2}}\\&=\frac{C_I}{C_F}\cdot\frac{1}{\sqrt{2\cdot\left[1-\cos(2\pi f/f_s)\right]}}\end{aligned} \tag{11}$$

or

$$\left|H_1(f)\right|=\frac{C_I}{C_F}\cdot\frac{1}{2\cdot\left|\sin\left(\pi\dfrac{f}{f_s}\right)\right|} \tag{12}$$

We can evaluate the phase response directly from z-plane plot by picking an arbitrary frequency f, and by using Eq. 1.51 in [1], or

$$\angle H(f) = \angle \text{ of zero} - \angle \text{ of pole} \tag{13}$$

After reviewing Eq. 1, we know that there is no zero for $H_1(f)$. Thus $\angle$ of zero is 0. Fig. 1 shows the z-plane representation for $H_1(f)$ which we use to find $\angle$ of pole .
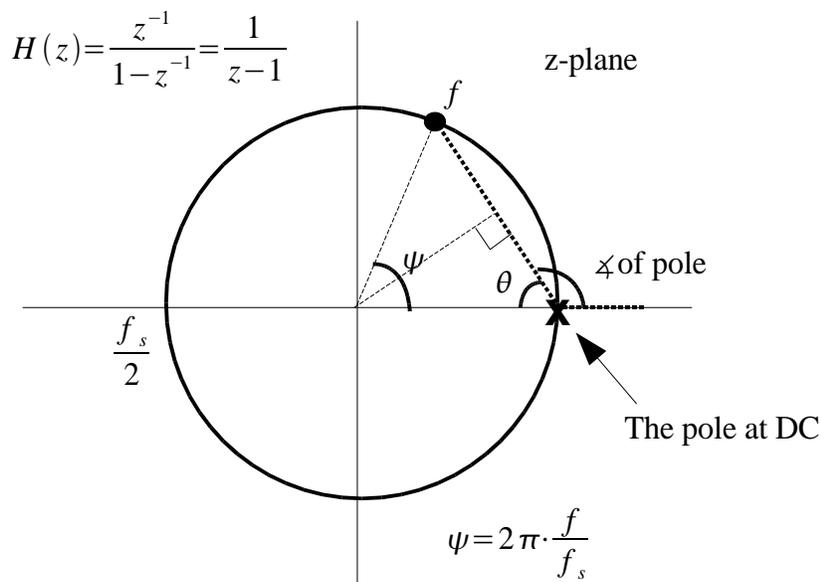
Figure 1 The z-plane representation for $H_1(f)$

From Fig. 1 we see that

$$\angle \text{ of pole} = \pi - \theta \tag{14}$$

where

$$\theta = \frac{\pi}{2} - \frac{\psi}{2} \tag{15}$$

and

$$\psi = 2\pi \cdot \frac{f}{f_s} \tag{16}$$

Using Eqs. 14 and 15, we can rewrite Eq. 13 as

$$\angle \text{ of pole} = \pi - \left(\frac{\pi}{2} - \frac{\psi}{2}\right) = \pi - \left(\frac{\pi}{2} - \frac{1}{2} \cdot 2\pi \cdot \frac{f}{f_s}\right)$$
$$= \pi \cdot \frac{f}{f_s} + \frac{\pi}{2} \tag{17}$$

Applying Eq. 12, we have

$$\angle H_1(f)=0-\left(\pi\cdot\frac{f}{f_s}+\frac{\pi}{2}\right) \tag{18}$$

or the phase response of $H_1(f)$ is

$$\angle H_1(f)=-\left(\pi\cdot\frac{f}{f_s}-\frac{\pi}{2}\right) \tag{19}$$

II. Frequency Response of $H_2(f)$

Again, let us get started by multiplying both the numerator and denominator of Eq. 5 by $e^{j2\pi f/f_s}$, or

$$H_2(f)=\frac{C_I}{C_F}\cdot\frac{e^{-j\pi f/f_s}}{1-e^{-j2\pi f/f_s}}\cdot\frac{e^{j2\pi f/f_s}}{e^{j2\pi f/f_s}}=\frac{C_I}{C_F}\cdot\frac{e^{j\pi f/f_s}}{e^{j2\pi f/f_s}-1} \tag{20}$$

Before going any further, comparing Eq. 20 with Eq. 6 in Part I, we see that the denominators in both equations are the same. Let's define

$$H_{2a}(f)=e^{j\pi f/f_s} \tag{21}$$

and

$$H_{2b}(f)=\frac{C_I}{C_F}\cdot\frac{1}{e^{j2\pi f/f_s}-1} \tag{22}$$

So that

$$H_2(f)=H_{2a}(f)\cdot H_{2b}(f) \tag{23}$$

$$\left|H_2(f)\right|=\left|H_{2a}(f)\right|\cdot\left|H_{2b}(f)\right| \tag{24}$$

$$\angle H_2(f)=\angle H_{2a}(f)+\angle H_{2b}(f) \tag{25}$$

Since

$$e^{j\pi f/f_s}\rightarrow 1\angle\left(\pi\cdot\frac{f}{f_s}\right) \tag{26}$$

the magnitude of $H_{2a}(f)$ is simply 1 and its phase response is $\pi\cdot\frac{f}{f_s}$. $H_{2b}(f)$, Eq. 22, is the

same as $H_1(f)$ in Part I so we can simply use the result from Part I, or

$$\left| H_{2b}(f) \right| = \left| H_1(f) \right| = \frac{C_I}{C_F} \cdot \frac{1}{2 \cdot \left| \sin\left(\pi \frac{f}{f_s}\right) \right|} \tag{27}$$

$$\measuredangle H_{2b}(f) = \measuredangle H_1(f) = -\pi \cdot \frac{f}{f_s} - \frac{\pi}{2} \tag{28}$$

Plugging the magnitude and phase responses of $H_{2a}(f)$ and $H_{2b}(f)$ into Eqs. 24 and 25, we get the magnitude response of $H_2(f)$

$$\left| H_2(f) \right| = (1) \cdot \left(\frac{C_I}{C_F} \cdot \frac{1}{2 \cdot \left| \sin\left(\pi \frac{f}{f_s}\right) \right|} \right) = \frac{C_I}{C_F} \cdot \frac{1}{2 \cdot \left| \sin\left(\pi \frac{f}{f_s}\right) \right|} \tag{29}$$

and the phase response of $H_2(f)$

$$\measuredangle H_2(f) = \left(\pi \cdot \frac{f}{f_s} \right) - \left(\pi \cdot \frac{f}{f_s} + \frac{\pi}{2} \right) \tag{30}$$
$$= 2\pi \cdot \frac{f}{f_s} - \frac{\pi}{2}$$

III. Simulations

In the simulations, $C_I = C_F = 1\,pF$, VDD = 1 V, and the clock frequency, f_s, is 100 MHz. Table 1 shows the hand calculation results for a few frequencies when the output is connected ϕ_1. Table 2 shows the hand calculation results for a few frequencies when the output is connected ϕ_2.

Frequency	1 kHz	25 MHz	50 MHz
$V_{out,\text{ peak-to-peak}}$	∞	0.71 V	0.5 V
Delay	2.5 ns	7.5 ns	5 ns

Table 1 Hand calculation result when output connected through ϕ_1.

Frequency	1 kHz	25 MHz	50 MHz
$V_{out,\text{ peak-to-peak}}$	∞	0.71 V	0.5 V
Delay	2.5 ns	10 ns	5 ns

Table 2 Hand calculation result when output connected through ϕ_2.

1) Simulations for output connected through ϕ_1.


```
.global VDD GND
VDD VDD 0 DC 1
VSS GND 0 DC 0
VCM VCM 0 DC 0.5
Vin Vin 0 SINE(0.5 0.5 25MEG)
Vphi1 phi1 0 PULSE(0 1 0 200p 200p 4n 10n)
Vphi2 phi2 0 PULSE(0 1 5n 200p 200p 4n 10n)
.tran 0 4u 0 2n UIC
.options plotwinsize=0
```
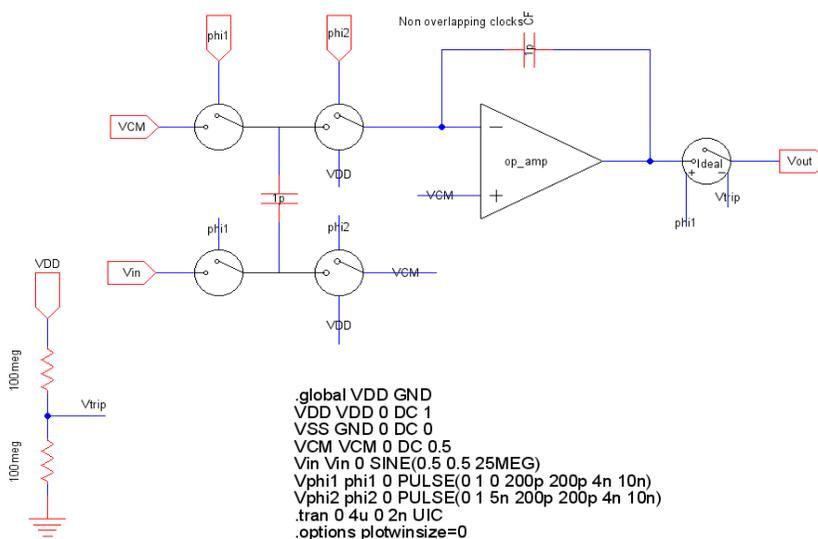
**Figure 2** Schematic for output connected to ϕ_1
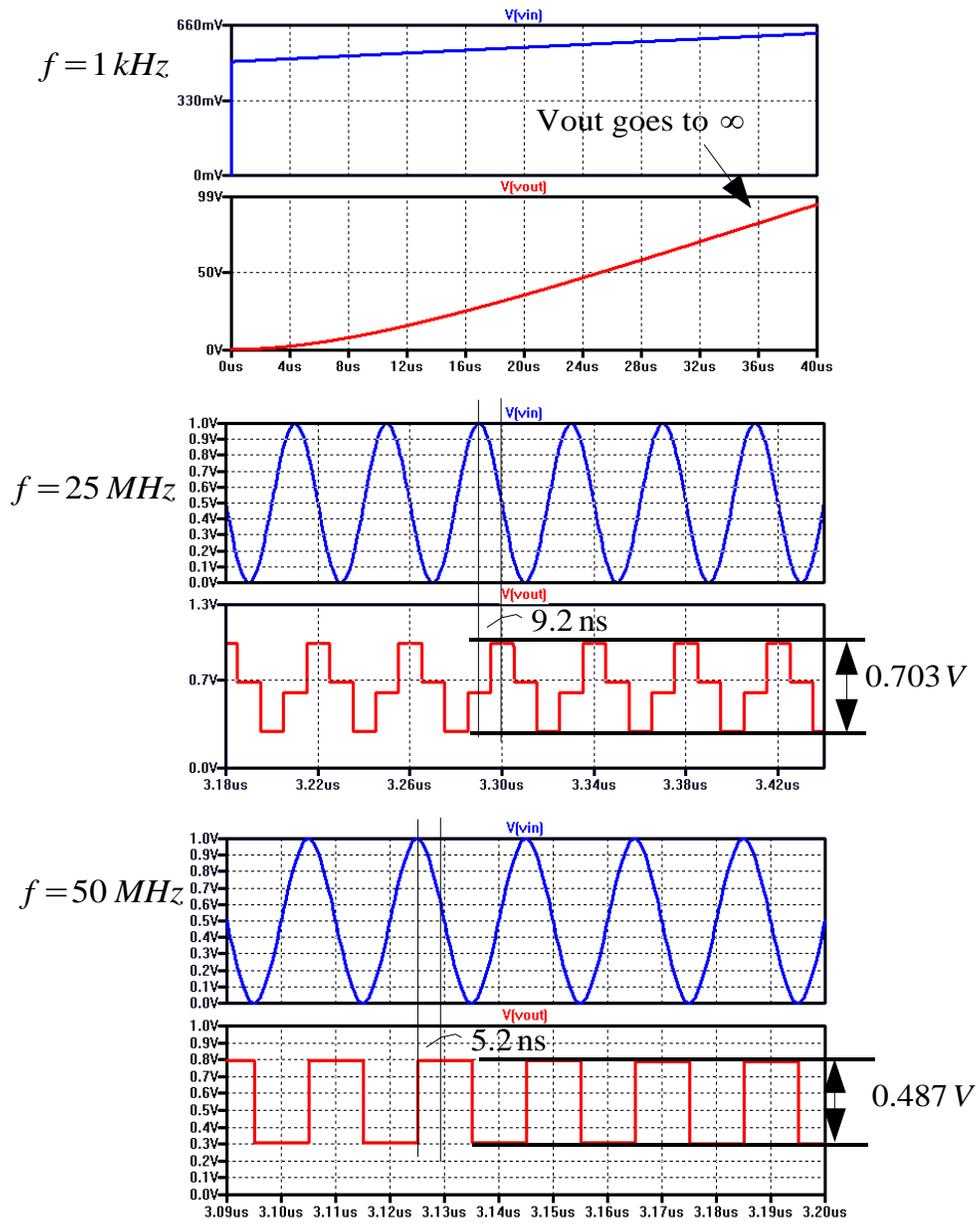
Figure 3 Simulations for output connected to ϕ_1

2) Simulations for output connected through ϕ_2.
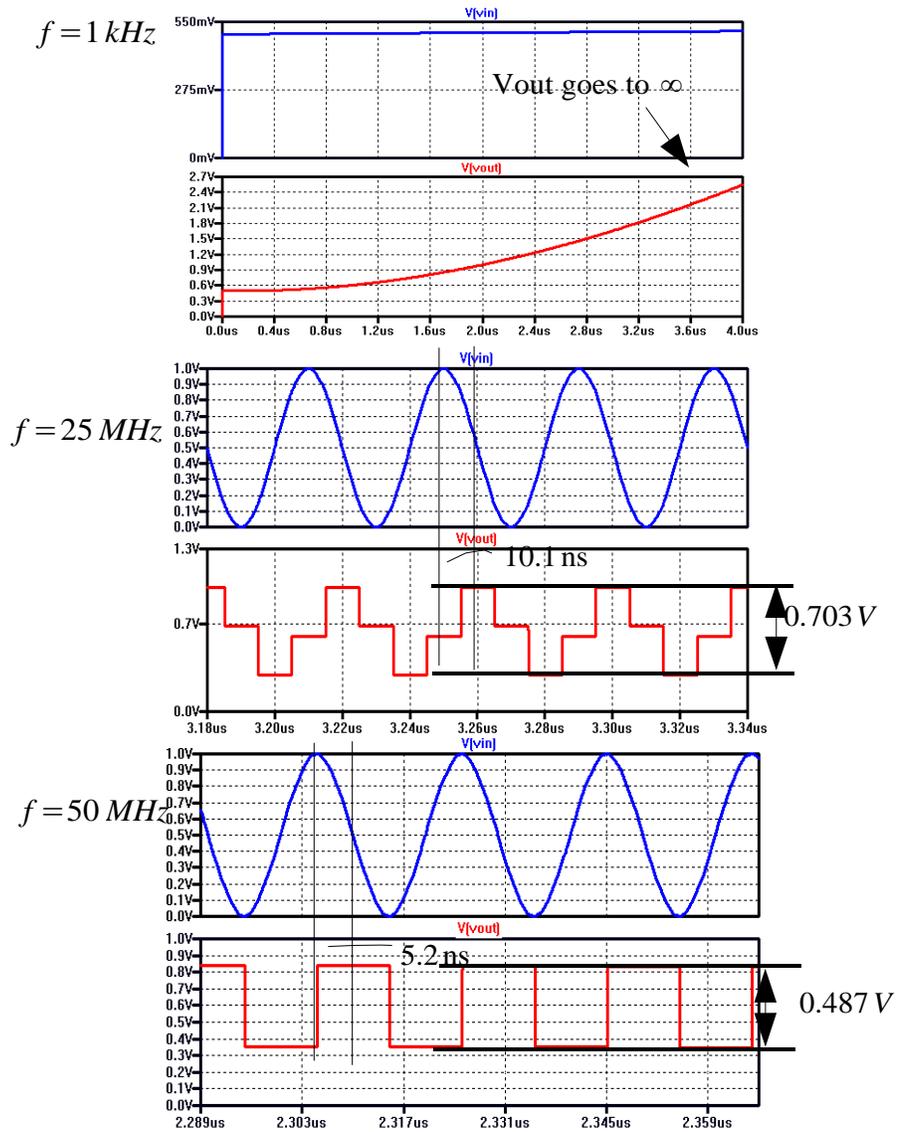

Figure 4 Simulations for output connected to ϕ_2.

Reference:

[1] R. J. Baker, *CMOS Mixed-signal Circuit Design, Second Edition*, Wiley-IEEE, 2009.

Solution by Jake Baker

2.16 Repeat Question 2.15 for the second entry. Here is Question 2.15: For the first entry (v_1 = input, $v_2 = V_{CM}$) in Table 2.2 derive the frequency response, magnitude and phase, of the DAI. Use simulations at a few frequencies to verify your derivations.

Solution:

Both Table 2.2 and Fig. 2.54 are shown below.

Table 2.2 Discrete analog integrator (DAI) input/output relationships.

Input	Output connected to ϕ_1	Output connected to ϕ_2
v_1 = input and $v_2 = V_{CM}$	$\dfrac{z^{-1}}{1 - z^{-1}} \cdot \dfrac{C_I}{C_F}$	$\dfrac{z^{-1/2}}{1 - z^{-1}} \cdot \dfrac{C_I}{C_F}$
v_2 = input and $v_1 = V_{CM}$	$\dfrac{-z^{-1/2}}{1 - z^{-1}} \cdot \dfrac{C_I}{C_F}$	$\dfrac{-1}{1 - z^{-1}} \cdot \dfrac{C_I}{C_F}$
v_1 and v_2 are both inputs	$\dfrac{V_1(z) \cdot z^{-1} - V_2(z) \cdot z^{-1/2}}{1 - z^{-1}} \cdot \dfrac{C_I}{C_F}$	$\dfrac{V_1(z) \cdot z^{-1/2} - V_2(z)}{1 - z^{-1}} \cdot \dfrac{C_I}{C_F}$
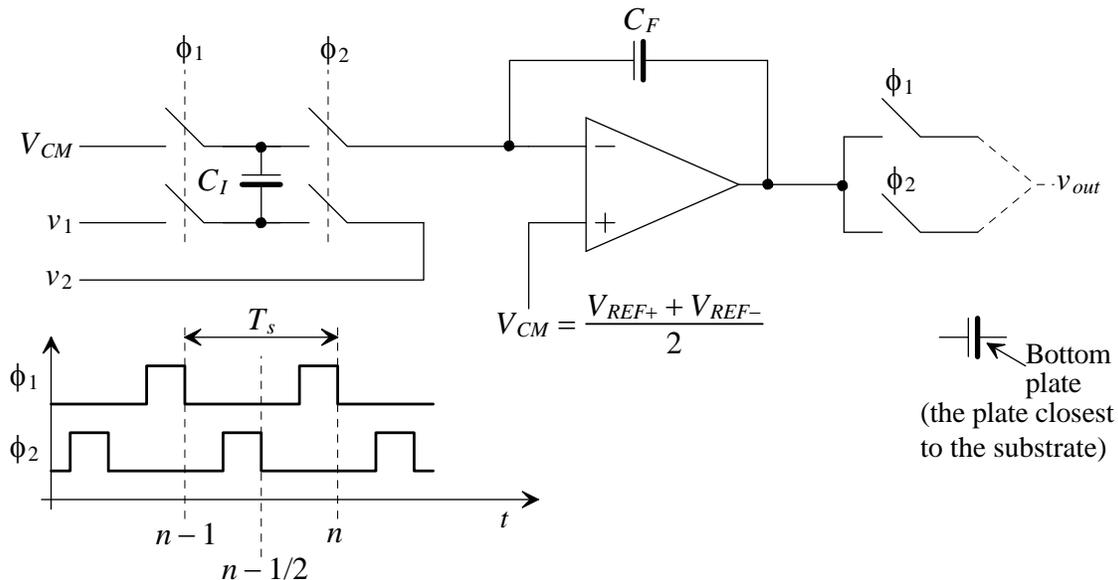
Figure 2.54 Schematic diagram of a discrete analog integrator (DAI).

We'll derive the frequency response for

$$H(z) = \frac{v_{out}(z)}{v_2(z)} = \frac{C_I}{C_F} \cdot \frac{-z^{-1/2}}{1 - z^{-1}} = \frac{C_I}{C_F} \cdot \frac{-z^{1/2}}{z - 1}$$

noting that if we change the numerator from $-z^{-1/2}$ to -1 we simply get a phase shift in the DAI.

The figure below shows the *z*-plane representation for the second entry in the table along with its magnitude and phase responses. To determine equations for the magnitude and phase responses we can write

$$H(z) = \frac{C_I}{C_F} \cdot \frac{-z^{1/2}}{z-1} \rightarrow \overbrace{e^{j\pi} \cdot e^{j\pi\frac{f}{fs}}}^{\text{Phase shift}} \cdot \frac{C_I}{C_F} \cdot \frac{1}{e^{j2\pi\frac{f}{fs}} - 1} = e^{j\left(\pi + \pi\frac{f}{fs}\right)} \cdot \frac{\frac{C_I}{C_F}}{(-1 + \cos 2\pi\frac{f}{fs}) + j\sin 2\pi\frac{f}{fs}}$$

noting $\left| e^{j\left(\pi + \pi\frac{f}{fs}\right)} \right| = 1$ and $\angle e^{j\left(\pi + \pi\frac{f}{fs}\right)} = \pi + \pi\frac{f}{fs}$. We can now write

$$|H(f)| = \frac{\frac{C_I}{C_F}}{\sqrt{\left(-1 + \cos 2\pi\frac{f}{fs}\right)^2 + \left(\sin 2\pi\frac{f}{fs}\right)^2}} = \frac{\frac{C_I}{C_F}}{\sqrt{2(1 - \cos 2\pi\frac{f}{fs})}}$$

or

$$|H(f)| = \frac{C_I}{C_F} \cdot \frac{1}{2\left|\sin \pi\frac{f}{fs}\right|}$$

Evaluating the phase response,

$$\angle H(f) = \overbrace{\pi}^{\text{From inversion}} + \overbrace{\pi\frac{f}{fs}}^{\text{From zero}} - \overbrace{\left(\pi\frac{f}{fs} + \frac{\pi}{2}\right)}^{\text{From pole}} = +90 \text{ (degrees) for } 0 < f < f_s$$

Noting that the phase shift, as mentioned above, for the second case

$$H(z) = \frac{-1}{1 - z^{-1}} \cdot \frac{C_I}{C_F}$$

$$H(z) = \frac{C_I}{C_F} \cdot \frac{-z^{-1/2}}{1 - z^{-1}} = \frac{C_I}{C_F} \cdot \frac{-z^{1/2}}{z-1}$$
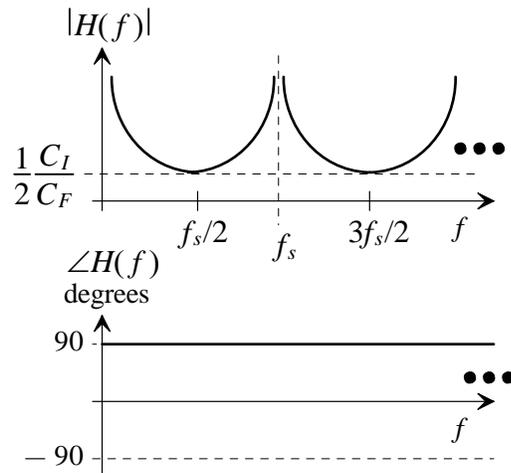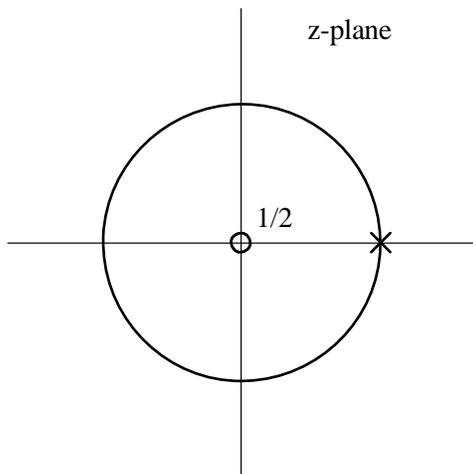
is

$$\angle H(f) = \pi - \pi\frac{f}{f_s} - \frac{\pi}{2} = \frac{\pi}{2} - \pi\frac{f}{f_s}$$

To show that these equations are correct lets use an f_s of 100 MHz, $C_I = C_F = 1\ pF$ and an input frequency of 5 MHz. The simulation schematic is seen below. The magnitude of the output is

$$|H(f)| = \frac{1}{2\left|\sin\pi\frac{5}{100}\right|} = 3.2$$

For a peak input amplitude of 10 mV the output amplitude will be 32 mV. The phase shift for the first case is exactly $+$ 90 degrees (output leading the input) while it's approximately 90 degrees (to be exact it's $90 - 90 \cdot 5/100 = 85.5$ degrees). Note how the intial voltage on the output of the integrator shifts the output voltage.
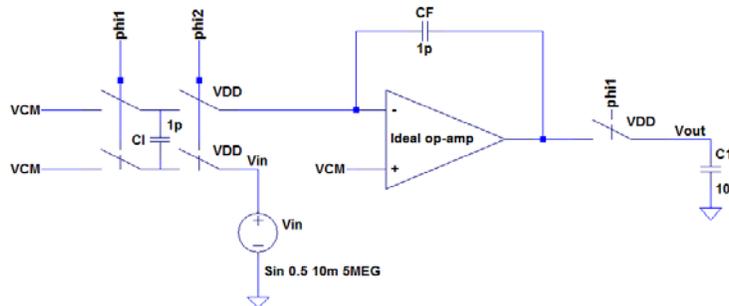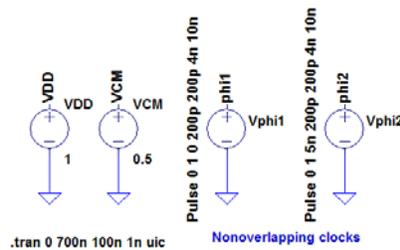

$$H(z) = \frac{-z^{1/2}}{z-1}$$ Output through phi1 switches

$$H(z) = \frac{-1}{z-1}$$ and through phi2 switches
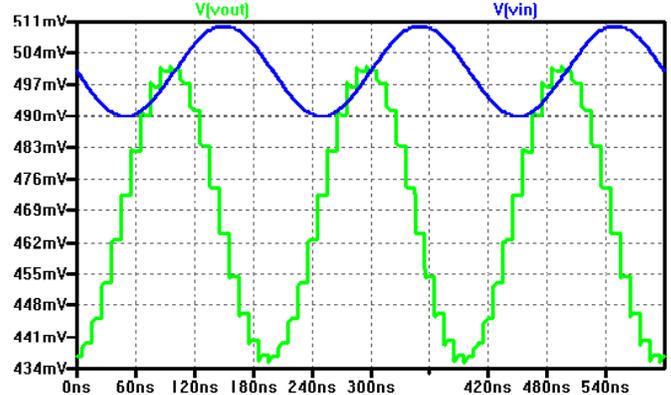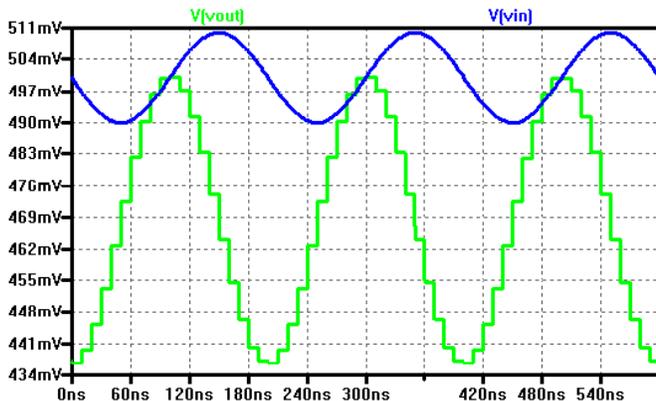
2.17) **For the third entry** $(v_1 = input, v_2 = input)$ **in Table 2.2 derive the frequency response, magnitude and phase, of the DAI. Use simulations at a few frequencies to verify your derivations.**

Solution

$v_1 = input, v_2 = input$. Output connected to Φ_1. Connecting to output to Φ_1 or Φ_2 just delays the output by $T_s/2$, it will not have any affect on the magnitude response. We shall see that in the derivations below:

Case I

The transfer function of the Discrete Analog Integrator (DAI) shown in figure 2.54 with both $v_1 and v_2$ going to inputs is $V_{Out}(z) = \dfrac{V_1(z).z^{-1} - V_2(z).z^{-1/2}}{1 - z^{-1}} \cdot \dfrac{C_I}{C_F}$ **– (1)**

Splitting the transfer function into an addition of two terms, we get

$$V_{Out}(z) = \frac{C_I}{C_F} \cdot \left[\left(\frac{z^{-1}}{1 - z^{-1}} \right) \cdot V_1(z) - \left(\frac{z^{-1/2}}{1 - z^{-1}} \right) \cdot V_2(z) \right] \text{– (2)}$$

Setting, $\left(\dfrac{z^{-1}}{1 - z^{-1}} \right) = P(z)$ and $\left(\dfrac{z^{-1/2}}{1 - z^{-1}} \right) = Q(z)$, we can rewrite the equation 2 as,

$$V_{Out}(z) = \frac{C_I}{C_F} \cdot \left[P(z) \cdot V_1(z) - Q(z) \cdot V_2(z) \right] \text{– (3)}$$

Lets synthesize $P(z)$ and $Q(z)$ separately, we get

$$P(z) = \frac{z^{-1}}{1 - z^{-1}} = \frac{\frac{1}{z}}{1 - \frac{1}{z}} = \frac{\frac{1}{z}}{\frac{z-1}{z}} = \frac{1}{z-1} = \frac{1}{e^{j \cdot 2 \cdot \pi \cdot \frac{f}{f_s}} - 1} = \frac{1}{\cos\left(2 \cdot \pi \cdot \frac{f}{f_s}\right) + j \cdot \sin\left(2 \cdot \pi \cdot \frac{f}{f_s}\right) - 1}$$

$$P(z) = \frac{1}{\left\{\cos\left(2 \cdot \pi \cdot \frac{f}{f_s}\right) - 1\right\} + j \cdot \sin\left(2 \cdot \pi \cdot \frac{f}{f_s}\right)} \text{– (4)}$$

$$Q(z) = \frac{z^{-1/2}}{1 - z^{-1}} = \frac{\frac{1}{z^{1/2}}}{1 - \frac{1}{z}} = \frac{\frac{1}{z^{1/2}}}{\frac{z-1}{z}} = \frac{z^{1/2}}{z-1} = \frac{e^{j\pi \cdot \frac{f}{f_s}}}{e^{j \cdot 2 \cdot \pi \cdot \frac{f}{f_s}} - 1} = \frac{\cos\left(\pi \cdot \frac{f}{f_s}\right) + j \cdot \sin\left(\pi \cdot \frac{f}{f_s}\right)}{\left\{\cos\left(2 \cdot \pi \cdot \frac{f}{f_s}\right) - 1\right\} + j \cdot \sin\left(2 \cdot \pi \cdot \frac{f}{f_s}\right)}$$

– (5)

Substituting $P(z)$ and $Q(z)$ back in equation 3 for V_{Out} we get the frequency response of the system to be,

$$V_{Out}(f) = \frac{C_I}{C_F} \cdot \left[\frac{1}{\left\{\cos\left(2 \cdot \pi \cdot \frac{f}{f_s}\right) - 1\right\} + j \cdot \sin\left(2 \cdot \pi \cdot \frac{f}{f_s}\right)} \cdot V_1(z) - \frac{\cos\left(\pi \cdot \frac{f}{f_s}\right) + j \cdot \sin\left(\pi \cdot \frac{f}{f_s}\right)}{\left\{\cos\left(2 \cdot \pi \cdot \frac{f}{f_s}\right) - 1\right\} + j \cdot \sin\left(2 \cdot \pi \cdot \frac{f}{f_s}\right)} \cdot V_2(z) \right]$$

– (6)

To find the magnitude and phase response and verify with schematic, lets assume that both the input capacitor and feedback capacitor are equal. Also, to simplify the algebra, lets assume that both V_1 and V_2 inputs are equal.

$$\frac{V_{Out}(z)}{V_{1,2}(z)} = 1 \cdot \left[\frac{1 - \cos\left(\pi \cdot \frac{f}{f_s}\right) - j \cdot \sin\left(\pi \cdot \frac{f}{f_s}\right)}{\left\{\cos\left(2 \cdot \pi \cdot \frac{f}{f_s}\right) - 1\right\} + j \cdot \sin\left(2 \cdot \pi \cdot \frac{f}{f_s}\right)} \right] = -1 \cdot \left[\frac{\left\{\cos\left(\pi \cdot \frac{f}{f_s}\right) - 1\right\} + j \cdot \sin\left(\pi \cdot \frac{f}{f_s}\right)}{\left\{\cos\left(2 \cdot \pi \cdot \frac{f}{f_s}\right) - 1\right\} + j \cdot \sin\left(2 \cdot \pi \cdot \frac{f}{f_s}\right)} \right]$$

– (7)

Magnitude response

$$\left|\frac{V_{Out}(z)}{V_{1,2}(z)}\right| = \frac{\sqrt{\left\{\cos\left(\pi \cdot \frac{f}{f_s}\right) - 1\right\}^2 + \sin^2\left(\pi \cdot \frac{f}{f_s}\right)}}{\sqrt{\left\{\cos\left(2 \cdot \pi \cdot \frac{f}{f_s}\right) - 1\right\}^2 + \sin^2\left(2 \cdot \pi \cdot \frac{f}{f_s}\right)}} = \frac{\sqrt{2 - 2 \cdot \cos\left(\frac{\pi \cdot f}{f_s}\right)}}{\sqrt{2 - 2 \cdot \cos\left(\frac{2\pi \cdot f}{f_s}\right)}} = \frac{\sqrt{2 \cdot 2 \cdot \sin^2\left(\frac{\pi}{2} \frac{f}{f_s}\right)}}{\sqrt{2 \cdot 2 \cdot \sin^2\left(\pi \cdot \frac{f}{f_s}\right)}}$$

– (8)

$$\left|\frac{V_{Out}(z)}{V_{1,2}(z)}\right| = \frac{2 \cdot \sin\left(\frac{\pi}{2} \frac{f}{f_s}\right)}{2 \cdot \sin\left(\pi \cdot \frac{f}{f_s}\right)}$$ **– (9)** is the magnitude response of the Discrete Analog

Integrator with both the inputs $v_1 and v_2$.

Phase response
Lets now derive the phase response of the transfer function of the given DAI, transfer function given is,

$$\frac{V_{Out}(z)}{V_{1,2}(z)} = -\frac{C_I}{C_F} \cdot \left[\frac{\left\{\cos\left(\pi \cdot \frac{f}{f_s}\right) - 1\right\} + j \cdot \sin\left(\pi \cdot \frac{f}{f_s}\right)}{\left\{\cos\left(2 \cdot \pi \cdot \frac{f}{f_s}\right) - 1\right\} + j \cdot \sin\left(2 \cdot \pi \cdot \frac{f}{f_s}\right)} \right]$$ **– (9)** this function can be

rewritten as, $$\frac{V_{Out}(z)}{V_{1,2}(z)} = -\frac{C_I}{C_F} \cdot \left[\frac{-2 \cdot \sin^2\left(\frac{\pi}{2} \cdot \frac{f}{f_s}\right) + j \cdot 2 \cdot \sin\left(\frac{\pi}{2} \cdot \frac{f}{f_s}\right) \cdot \cos\left(\frac{\pi}{2} \cdot \frac{f}{f_s}\right)}{-2 \cdot \sin^2\left(\pi \cdot \frac{f}{f_s}\right) + j \cdot 2 \cdot \sin\left(\pi \cdot \frac{f}{f_s}\right) \cdot \cos\left(\pi \cdot \frac{f}{f_s}\right)} \right]$$ **– (10)**

Now, we can find the phase response of the above transfer function easily,

$$\angle = 180° + \tan^{-1}\left(\frac{2 \cdot \sin\left(\frac{\pi}{2} \cdot \frac{f}{f_s}\right) \cdot \cos\left(\frac{\pi}{2} \cdot \frac{f}{f_s}\right)}{-2 \cdot \sin^2\left(\frac{\pi}{2} \cdot \frac{f}{f_s}\right)}\right) - \tan^{-1}\left(\frac{2 \cdot \sin\left(\pi \cdot \frac{f}{f_s}\right) \cdot \cos\left(\pi \cdot \frac{f}{f_s}\right)}{-2 \cdot \sin^2\left(\pi \cdot \frac{f}{f_s}\right)}\right) - (11)$$

$$\angle = 180° - \left(\frac{\pi}{2} - \frac{\pi}{2} \cdot \frac{f}{f_s}\right) + \left(\frac{\pi}{2} - \pi \cdot \frac{f}{f_s}\right) = 180° + \frac{\pi}{2} \cdot \frac{f}{f_s} - \pi \cdot \frac{f}{f_s} \quad - (12)$$

$$\angle = 180° - \frac{\pi}{2} \cdot \frac{f}{f_s} \quad - (13)$$

Simulations

Let's verify the above derivations by simulating the DAI with equal inputs V1 and V2. This circuit will be clocked at 100MHz, therefore $f_s = 100MHz$. Also notice that both the capacitors are set to 1pF so the gain across is just $\frac{C_I}{C_F} = 1$. The schematic for the circuit is given below,
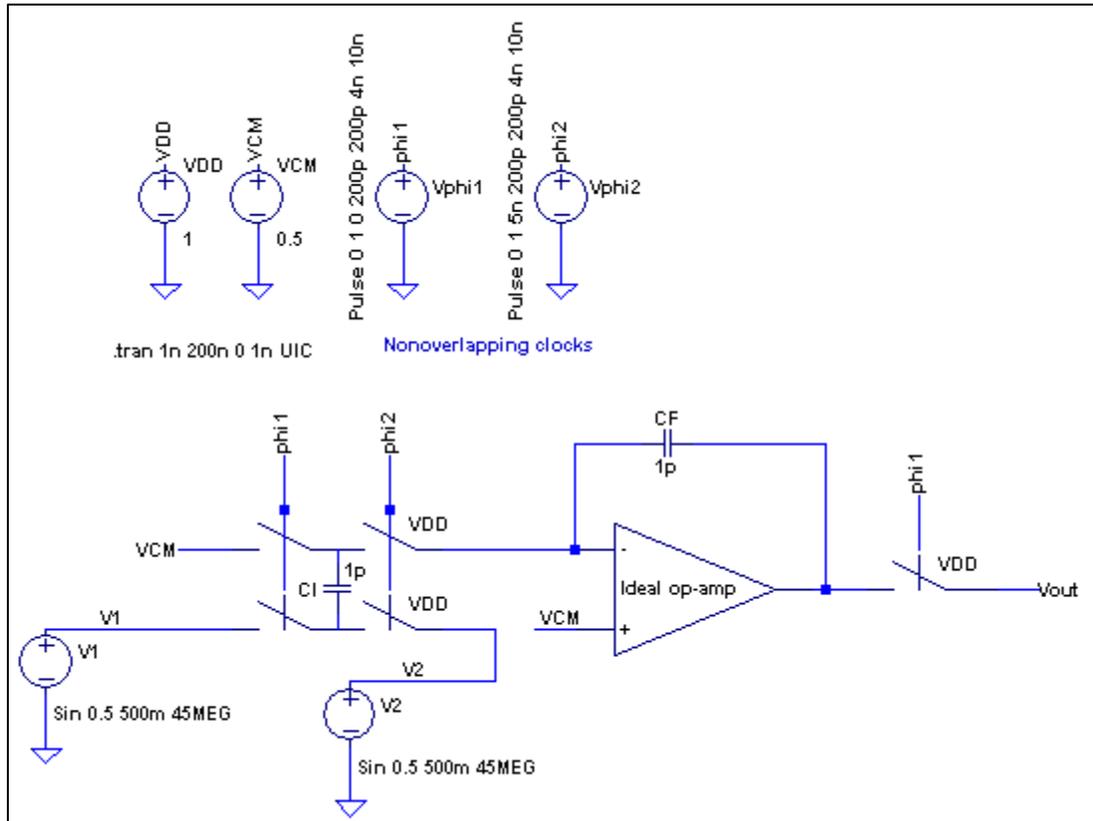

Figure 1: Circuit implementation of a DAI

@ Input frequency = 5MHz $(\sim DC)$
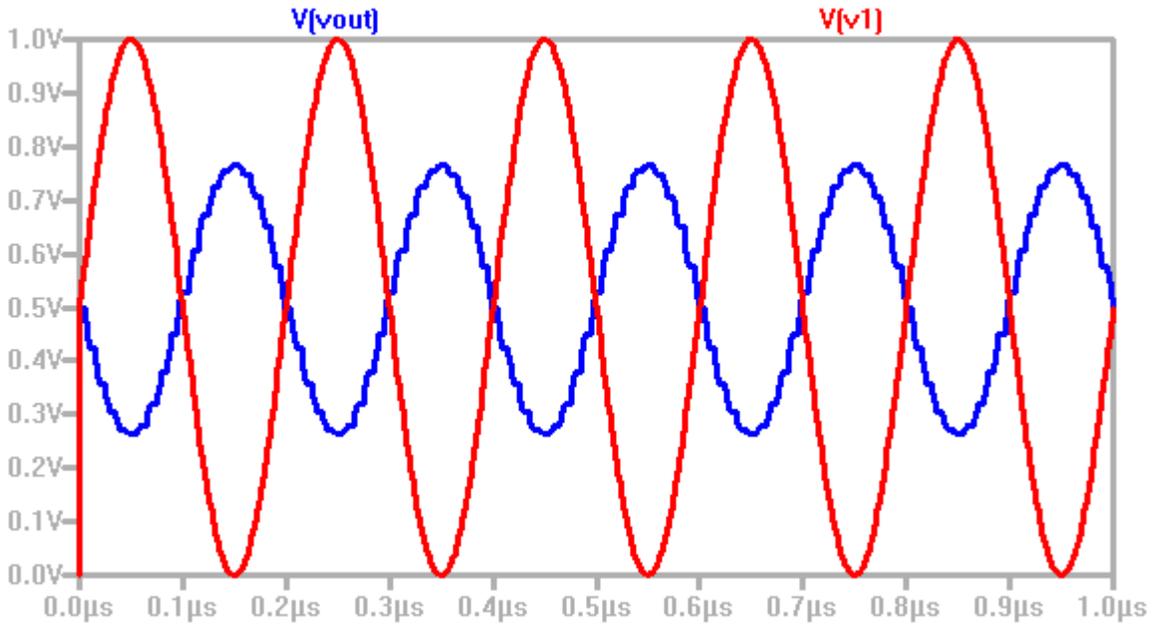
Simulated Vout = 500.462mV. Hand calculated Vout = 501.5mV

@ Input frequency = 45MHz $\left(\sim \dfrac{f_s}{2}\right)$
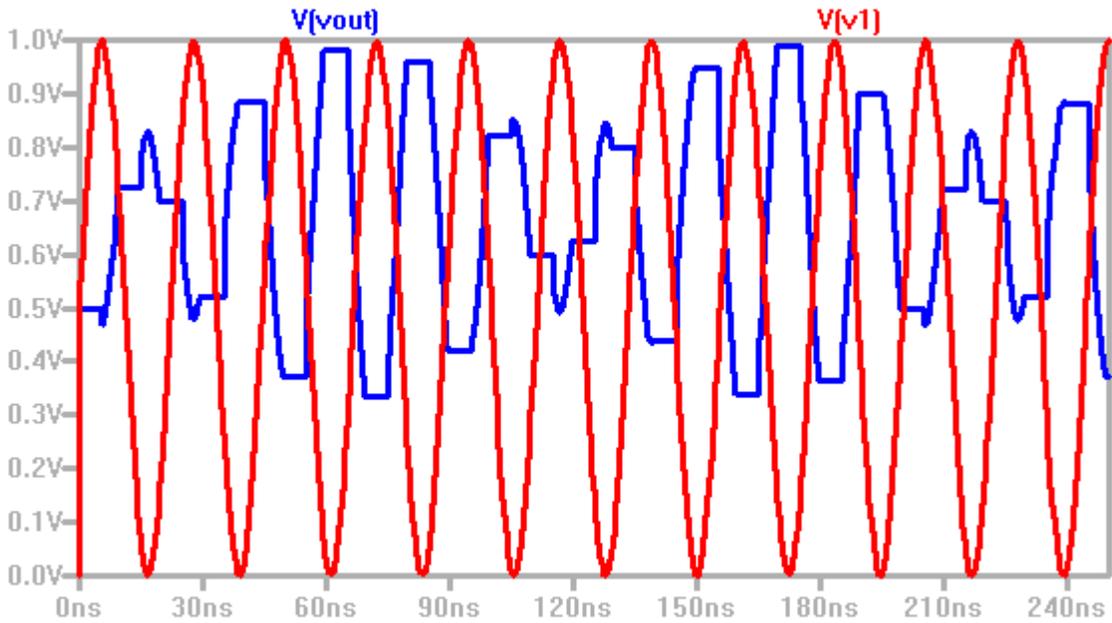
Simulated Vout = 648.93mV. Hand calculated Vout = 657mV

@ Input frequency = 100MHz $\left(f_s\right)$
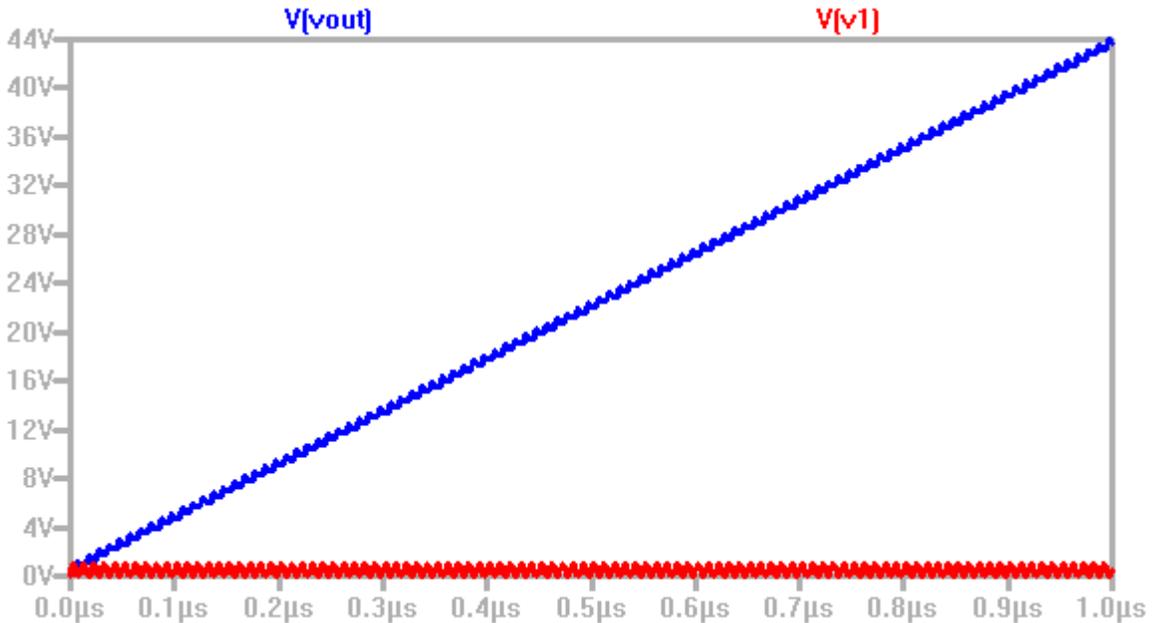
Simulated Vout keeps increasing. Hand calculated Vout = infinite!

From equation 2, we notice that the transfer function of the DAI is just a sum of two integrating circuits discussed in chapter1. Similar to the integrator circuit, the output goes to infinity of blows up at fs frequency as seen in the figure above.

Therefore, we see that our frequency response values match pretty close the simulation results seen above.

Case II

$v_1 = input, v_2 = input$, but now the output is connected to Φ_2 instead of Φ_1. As mentioned earlier, this should just delay the output of the DAI while the magnitude response remain unaffected. Lets verify,

$$V_{Out}(z) = \frac{V_1(z).z^{-1/2} - V_2(z)}{1 - z^{-1}} \cdot \frac{C_I}{C_F} - \textbf{(14)}$$ is the transfer function. Following the steps similar to the derivations in *Case I*, we get

$$V_{Out}(z) = \frac{C_I}{C_F} \cdot \left[\left(\frac{z^{-1/2}}{1 - z^{-1}} \right) \cdot V_1(z) - \left(\frac{1}{1 - z^{-1}} \right) \cdot V_2(z) \right] - \textbf{(15)}$$

Setting, $\left(\frac{z^{-1/2}}{1 - z^{-1}} \right) = P(z)$ and $\left(\frac{1}{1 - z^{-1}} \right) = Q(z)$, we can rewrite the above equation as,

$$V_{Out}(z) = \frac{C_I}{C_F} \cdot \left[P(z) \cdot V_1(z) - Q(z) \cdot V_2(z) \right] - \textbf{(16)}$$

Lets synthesize $P(z)$ and $Q(z)$ separately, we get

$$P(z) = \frac{z^{-1/2}}{1-z^{-1}} = \frac{\frac{1}{z^{1/2}}}{1-\frac{1}{z}} = \frac{\frac{1}{z^{1/2}}}{\frac{z-1}{z}} = \frac{z^{1/2}}{z-1} = \frac{e^{j\pi\cdot\frac{f}{f_s}}}{e^{j\cdot2\cdot\pi\cdot\frac{f}{f_s}}-1} = \frac{e^{j\pi\cdot\frac{f}{f_s}}}{\left\{\cos\left(2\cdot\pi\cdot\frac{f}{f_s}\right)-1\right\}+j\cdot\sin\left(2\cdot\pi\cdot\frac{f}{f_s}\right)}$$

− (17)

$$Q(z) = \frac{1}{1-z^{-1}} = \frac{1}{1-\frac{1}{z}} = \frac{1}{\frac{z-1}{z}} = \frac{z}{z-1} = \frac{e^{j2\pi\cdot\frac{f}{f_s}}}{e^{j\cdot2\cdot\pi\cdot\frac{f}{f_s}}-1} = \frac{e^{j2\pi\cdot\frac{f}{f_s}}}{\left\{\cos\left(2\cdot\pi\cdot\frac{f}{f_s}\right)-1\right\}+j\cdot\sin\left(2\cdot\pi\cdot\frac{f}{f_s}\right)}$$

− (18)

Substituting $P(z)$ and $Q(z)$ back in equation for V_{Out} we get the frequency response of the system to be,

$$V_{Out}(f) = \frac{C_I}{C_F}\cdot\left[\frac{e^{j\pi\cdot\frac{f}{f_s}}}{\left\{\cos\left(2\cdot\pi\cdot\frac{f}{f_s}\right)-1\right\}+j\cdot\sin\left(2\cdot\pi\cdot\frac{f}{f_s}\right)}\cdot V_1(z) - \frac{e^{j2\pi\cdot\frac{f}{f_s}}}{\left\{\cos\left(2\cdot\pi\cdot\frac{f}{f_s}\right)-1\right\}+j\cdot\sin\left(2\cdot\pi\cdot\frac{f}{f_s}\right)}\cdot V_2(z)\right]$$

− (19)

To find the magnitude and phase response and verify with schematic, lets assume that both the input capacitor and feedback capacitor are equal. Also, to simplify the algebra, lets assume that both V_1 and V_2 inputs are equal.

$$\frac{V_{Out}(z)}{V_{1,2}(z)} = 1\cdot\left[\frac{e^{j\pi\cdot\frac{f}{f_s}}}{\left\{\cos\left(2\cdot\pi\cdot\frac{f}{f_s}\right)-1\right\}+j\cdot\sin\left(2\cdot\pi\cdot\frac{f}{f_s}\right)} - \frac{e^{j2\pi\cdot\frac{f}{f_s}}}{\left\{\cos\left(2\cdot\pi\cdot\frac{f}{f_s}\right)-1\right\}+j\cdot\sin\left(2\cdot\pi\cdot\frac{f}{f_s}\right)}\right]$$

− (20)

$$\frac{V_{Out}(z)}{V_{1,2}(z)} = e^{j\pi\cdot\frac{f}{f_s}}\cdot\left[\frac{1}{\left\{\cos\left(2\cdot\pi\cdot\frac{f}{f_s}\right)-1\right\}+j\cdot\sin\left(2\cdot\pi\cdot\frac{f}{f_s}\right)} - \frac{e^{j\pi\cdot\frac{f}{f_s}}}{\left\{\cos\left(2\cdot\pi\cdot\frac{f}{f_s}\right)-1\right\}+j\cdot\sin\left(2\cdot\pi\cdot\frac{f}{f_s}\right)}\right]$$

− (21)

The term $e^{j\pi\cdot\frac{f}{f_s}}$ is factored out in the expression above because, we know $\left|e^{j\pi\cdot\frac{f}{f_s}}\right|=1$ and

$\angle e^{j\pi\cdot\frac{f}{f_s}} = \pi\cdot\frac{f}{f_s}$. Also, the rest of the expression above is similar to the previous case and therefore we can now see that by connecting the output Vout to Φ_2 just delays the output by Ts/2 . It has no effect on the magnitude of the output, only phase will vary.

Therefore, using the result derived in the previous case, magnitude of the above expression is,

$$\left| \frac{V_{Out}(z)}{V_{1,2}(z)} \right| = 1 \cdot \frac{2 \cdot \sin\left(\dfrac{\pi}{2} \dfrac{f}{f_s} \right)}{2 \cdot \sin\left(\pi \cdot \dfrac{f}{f_s} \right)} \quad \textbf{– (22)} \quad \text{is the magnitude response of the Discrete Analog}$$

Integrator with both the inputs V1 and V2 and output is sampled using Φ_2.

Lets now derive the phase response of the transfer function of the given DAI, transfer function given is,

$$\frac{V_{Out}(z)}{V_{1,2}(z)} = -e^{j\pi \cdot \frac{f}{f_s}} \cdot \left[\frac{\left\{ \cos\left(\pi \cdot \dfrac{f}{f_s} \right) - 1 \right\} + j \cdot \sin\left(\pi \cdot \dfrac{f}{f_s} \right)}{\left\{ \cos\left(2 \cdot \pi \cdot \dfrac{f}{f_s} \right) - 1 \right\} + j \cdot \sin\left(2 \cdot \pi \cdot \dfrac{f}{f_s} \right)} \right] \quad \textbf{– (23)}$$

this function can be rewritten as,

$$\frac{V_{Out}(z)}{V_{1,2}(z)} = -e^{j\pi \cdot \frac{f}{f_s}} \cdot \left[\frac{-2 \cdot \sin^2\left(\dfrac{\pi}{2} \cdot \dfrac{f}{f_s} \right) + j \cdot 2 \cdot \sin\left(\dfrac{\pi}{2} \cdot \dfrac{f}{f_s} \right) \cdot \cos\left(\dfrac{\pi}{2} \cdot \dfrac{f}{f_s} \right)}{-2 \cdot \sin^2\left(\pi \cdot \dfrac{f}{f_s} \right) + j \cdot 2 \cdot \sin\left(\pi \cdot \dfrac{f}{f_s} \right) \cdot \cos\left(\pi \cdot \dfrac{f}{f_s} \right)} \right] \quad \textbf{– (24)}$$

Now, we can find the phase response of the above transfer function easily,

$$\angle = 180° + \pi \cdot \frac{f}{f_s} + \tan^{-1}\left(\frac{2 \cdot \sin\left(\dfrac{\pi}{2} \cdot \dfrac{f}{f_s} \right) \cdot \cos\left(\dfrac{\pi}{2} \cdot \dfrac{f}{f_s} \right)}{-2 \cdot \sin^2\left(\dfrac{\pi}{2} \cdot \dfrac{f}{f_s} \right)} \right) - \tan^{-1}\left(\frac{2 \cdot \sin\left(\pi \cdot \dfrac{f}{f_s} \right) \cdot \cos\left(\pi \cdot \dfrac{f}{f_s} \right)}{-2 \cdot \sin^2\left(\pi \cdot \dfrac{f}{f_s} \right)} \right)$$

– (25)

$$\angle = 180° + \pi \cdot \frac{f}{f_s} - \left(\frac{\pi}{2} - \frac{\pi}{2} \cdot \frac{f}{f_s} \right) + \left(\frac{\pi}{2} - \pi \cdot \frac{f}{f_s} \right) = 180° + \pi \cdot \frac{f}{f_s} + \frac{\pi}{2} \cdot \frac{f}{f_s} - \pi \cdot \frac{f}{f_s} \quad \textbf{– (26)}$$

$$\angle = 180° + \frac{\pi}{2} \cdot \frac{f}{f_s} \quad \textbf{– (27)}, \text{ therefore we can see that compared to the phase response of}$$

previous case, the output is just a delayed version; it is delayed by Ts/2 or by $-180°$.

Simulations

   Similar to the simulations performed in case I, here we can vary the input signal frequency and check the output response. Notice that the output is now clocked on Φ_2 instead of Φ_1
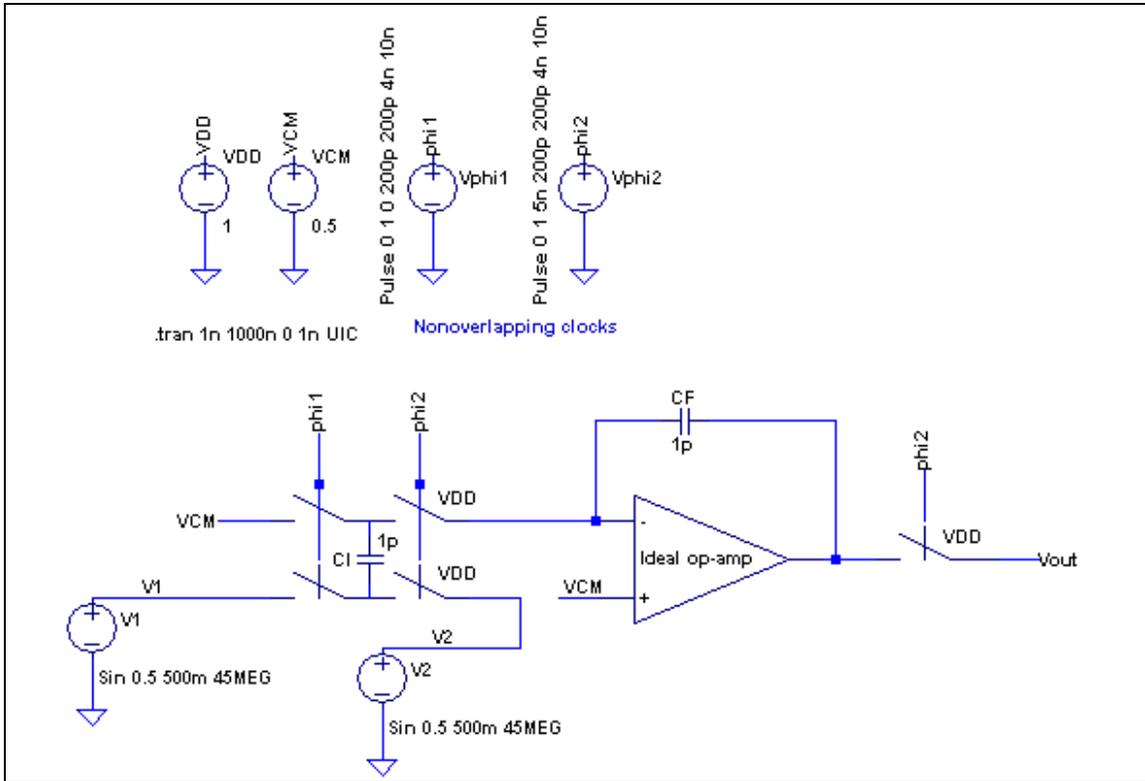

Figure 2: DAI, but now the output is connected to Φ2 instead of Φ1

@ Input frequency = 5MHz $(\sim DC)$
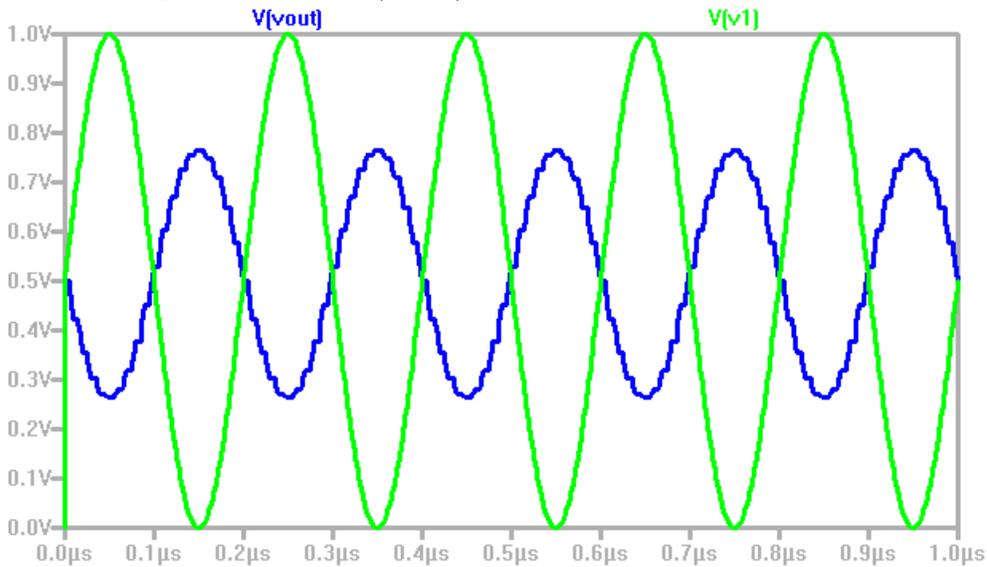
Simulated Vout = 500.416mV. Hand calculated Vout = 501.5mV
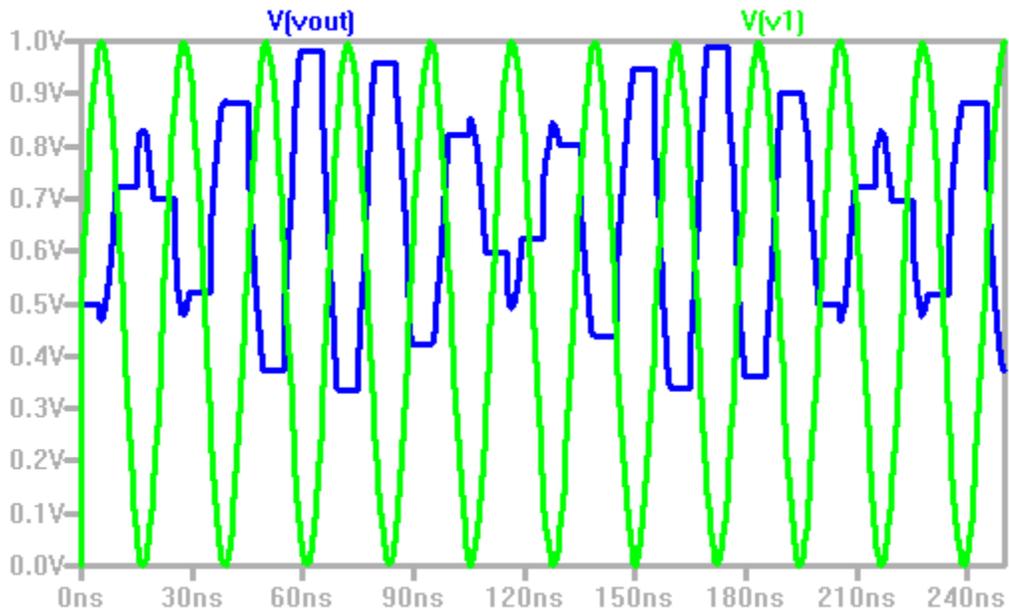
Avinash Rajagiri
Spring 2009

@ Input frequency = 45MHz $\left(\sim \dfrac{f_s}{2} \right)$

Simulated Vout = 648.93mV. Hand calculated Vout = 657mV

@ Input frequency = 100MHz (f_s)
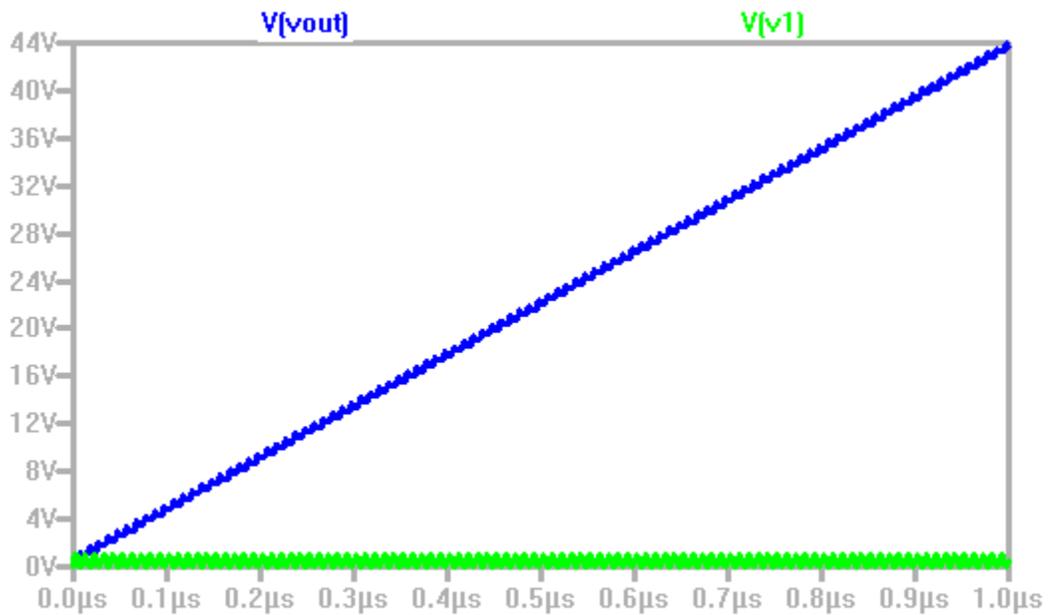
Simulated Vout keeps increasing. Hand calculated Vout = infinite!

The simulation results from spice match with the hand calculated magnitude response.

The DAI has a response similar to the magnitude response of an integrator covered in chapter 1. The circuit just passes the input signal at lower frequencies and as we keep going higher in frequency, the DAI starts to act like an accumulator and has a peak value at fs frequency, where the magnitude blows up. The magnitude response of the discrete analog integrator looks like a response of an integrator circuit from chapter 1, but with a delay of Ts/2.
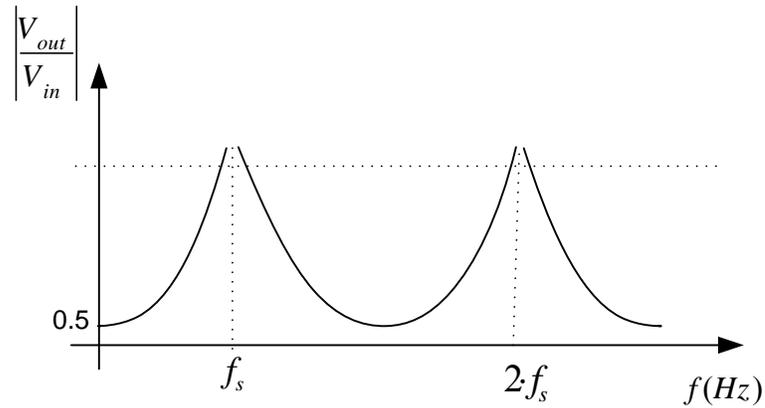

Figure 3: Magnitude resposne of an DAI

Kaijun Li
Problem 2.18
Does the DAI use CDS? Why or why not? Use simulations to support your answers.

To answer yes or no to this question, we should investigate on the charge transfer when the switches are turned on and off.

To simplify the math, we set v_2 to be V_{CM}. When ϕ_1 switches are closed, the charge on C_I is
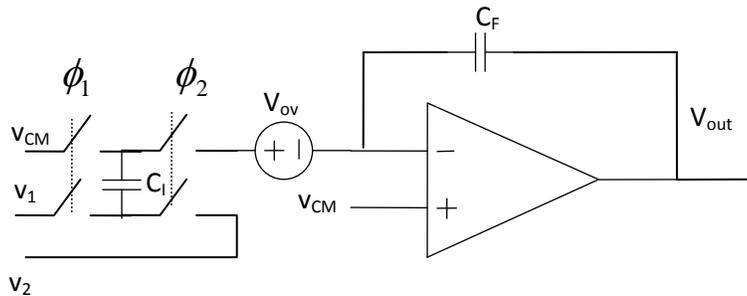

Fig. 1 Discrete analog integrator (DAI).

$Q_1=CI(v_1-V_{CM})$. When ϕ_2 switches are closed, the charge on C_I is $Q_{2,1}=C_I(V_{CM}+V_{ov}-V_{CM})=C_IV_{ov}$, and the charge on C_F is $Q_{2,2}=C_F(\Delta V_{out}-V_{CM})$. Due to charge reservation, $Q_1=Q_{2,1}+Q_{2,2}$, and this means that $CI(v_1-V_{CM})=C_IV_{ov}+C_F(\Delta V_{out}-V_{CM})$, which is $V_{out}(1-z^{-1})=CI/C_F(V_{in}-V_{ov})$. Therefore, the offset is not cancelled out in DAI, and DAI doesn't use CDS.
The simulation results are shown as follows.