Problem 16.1

Below in figure 1 is a simplified circuit representation of a memory cell.
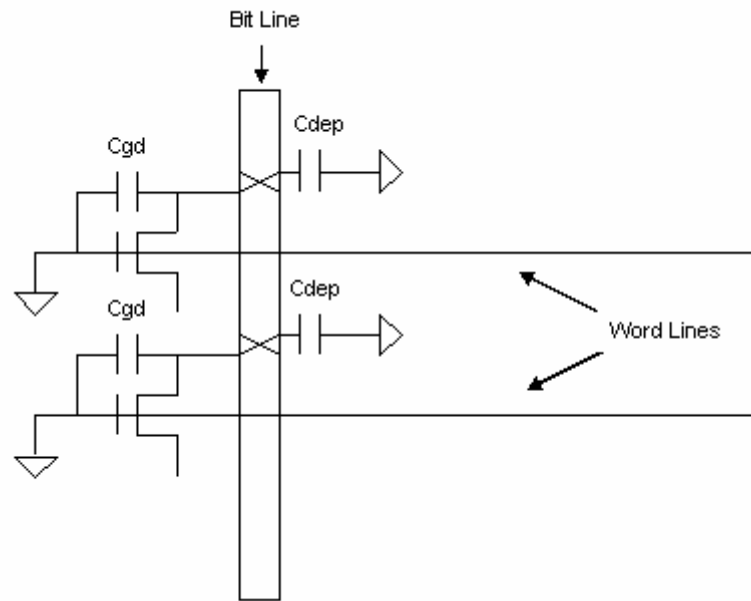

Figure 1.

There are 256 word lines => 256 MOSFETs. When the word lines are at ground, Cgd and Cdep are in parallel as seen below in figure 2.
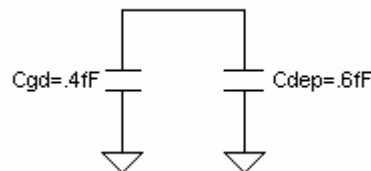

Figure2.

The Capacitance for each Mosfet is .4f+.6f = 1fF.
If the bit line is the same dimensions as in Figure 16.2 and the Capacitance from Metal 1 to Substrate is $100\frac{aF}{\mu m^2}$, then using equations 16.1 and 16.3 :

$$C_{col-sub} = .1\mu m * 100\mu m * 100\frac{aF}{\mu m^2} = 1fF$$

and the total Capacitance is:

$$C_{col} = 256 * 1fF + 1fF = 257fF.$$

Problem 16.2

Assuming the capacitors are equilibrated to the same voltage of 0.5 V, when the sense_N signal goes high both M1 and M2 transistors will be in the saturation region and an Ids current will begin to flow in both transistors. We can approximate the behavior of the transistors as that of resistors. We then can look at the circuit as two discharging RC circuits. The voltage equation for a discharging RC circuit is
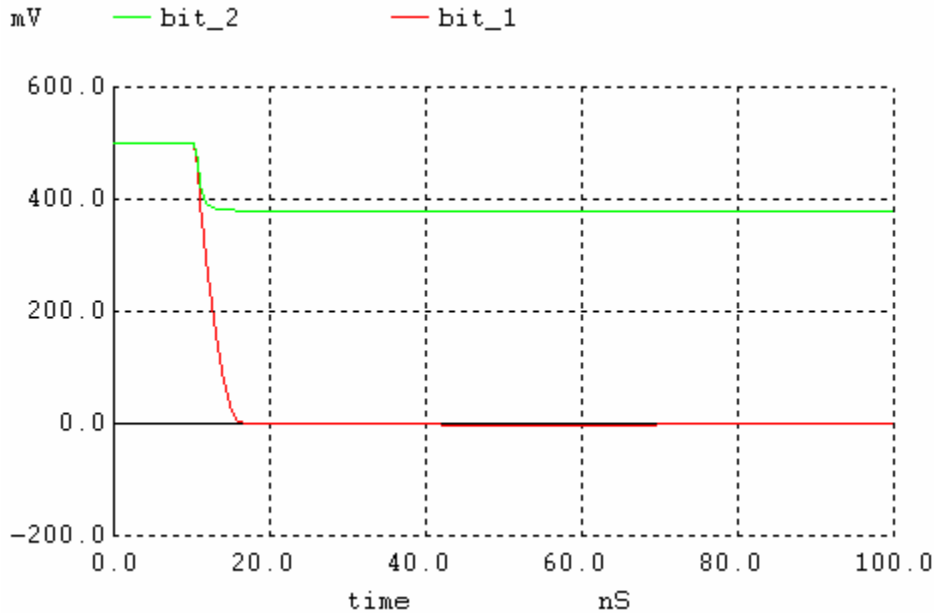
$$V(t) = V_i e^{-t/RC}. \qquad \text{Eq 1}$$

Where Vi is the initial voltage of the capacitor (.5V) and V(t) is the transient value of the voltage at the drain of each transistor. Solving for t results in

$$T = -\ln|V(t)/V_i| \; RC \qquad \text{Eq 2}$$

Looking at this equation we can see that the circuit with the larger capacitance will take longer to discharge.

Now, looking back at the original circuit we can conclude that the 100f F capacitor will discharge quicker, which in turn will shut off the M2 transistor. With the M2 transitor off, the 120 fF capacitor will stop discharging while the 100fF capacitor will continue to discharge to ground.

To calculate the initial capacitor voltage difference needed for metastability we will use the I-V capacitor equation
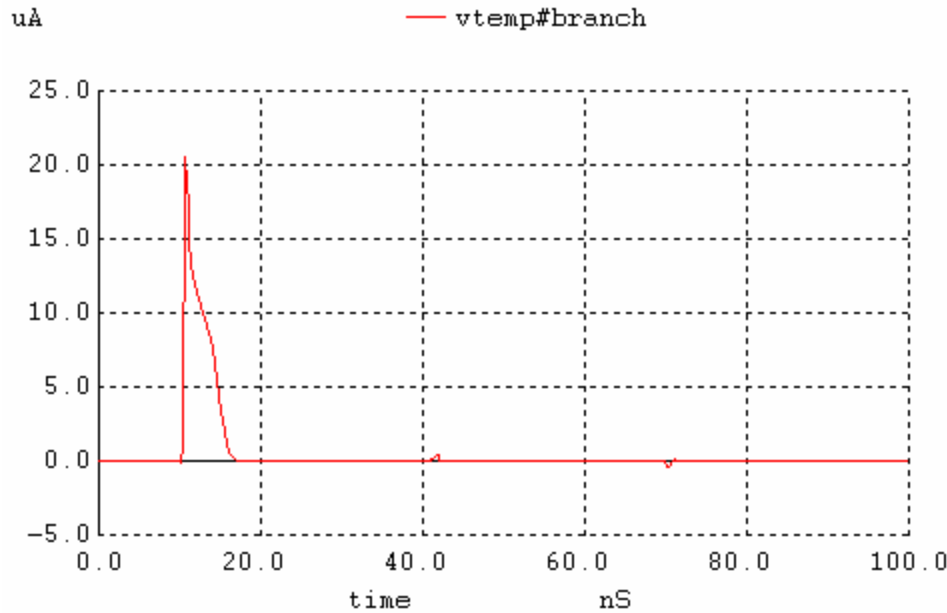
$$I(t) = C\Delta v/\Delta t \qquad \text{Eq 3}$$

For the circuit to enter metastability, both transistors will move from strong-inversion down through the triode region and eventually meet and stay at a certain V_{DS} voltage.
Solving equation 3 for voltage and adding the initially capacitor voltages we get,

$$V1(t) = V1_{init} - t(I_{D1}/C_1) \qquad \text{Eq 4}$$
$$V2(t) = V2_{init} - t(I_{D2}/C_2) \qquad \text{Eq 5}$$

I_{D1} and I_{D2} can be taken from the first simulation. Looking at the plot, as the M1 transistor shuts off I_{D1} goes from 20uA to 0. We will use 10uA for I_{D1} and I_{D2}.
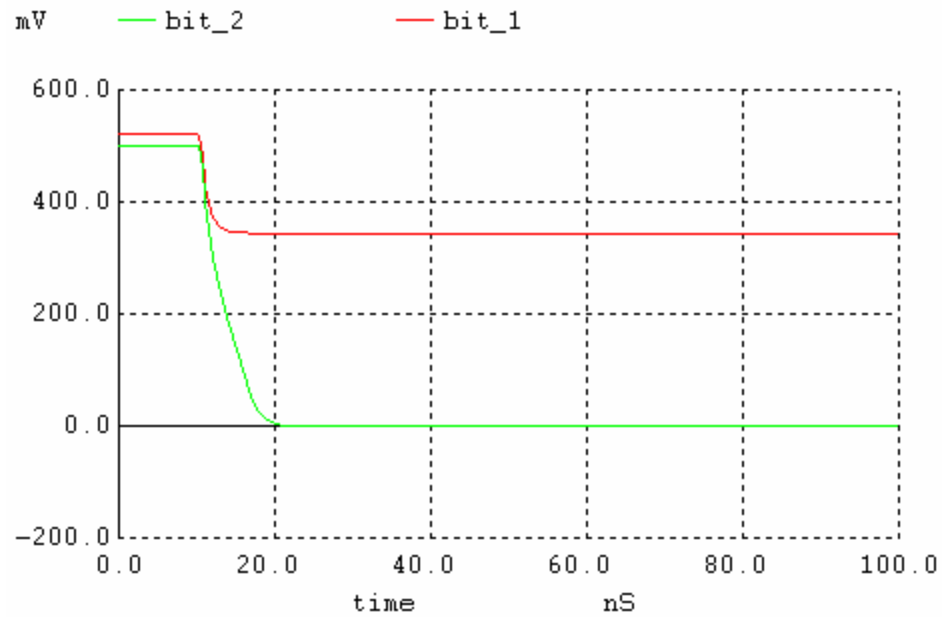

uA   — vtemp#branch

Lets assume that the voltage where $V1_{DS}$ and $V2_{DS}$ meet is above the threshold voltage , 400mV.
Now lets plug that into equation 5 and solve for t since we know that $V2_{init}$ is 0.5V.

$$T = -(V2 - V2_{init})(C_2/I_{D2}) = -(0.4 - 0.5)(120fF/10u) = 1.2ns$$

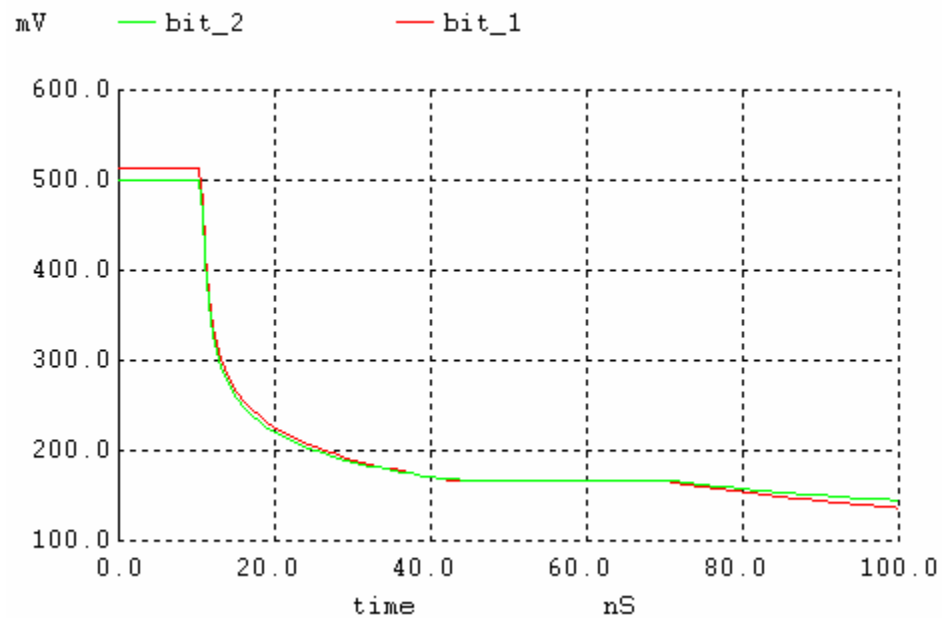Now lets rearrange equation 4 and solve for $V1_{init}$

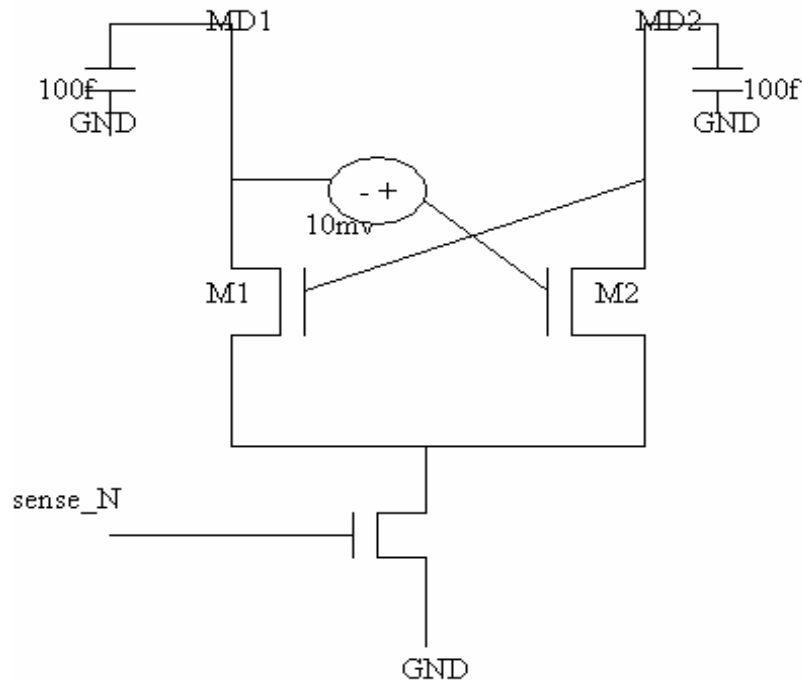$$V1_{init} = V1(t) + t(I_{D1}/C_1) = 0.4 + (1.2n)(10u/100f) = .52V$$

Simulating with this initial voltage of capacitor one give us the plot below.
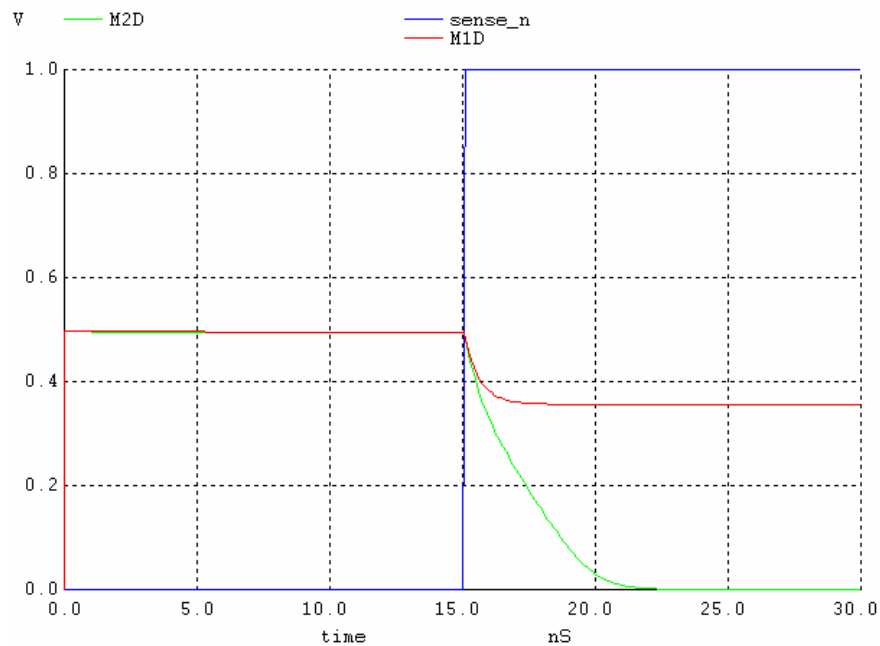
This is not metastability but gets us close, with a little trial and error of plugging numbers in Spice and simulating we find that we get metastability when V1init = 0.5142. This is shown in the plot below.

Problem 16.3

Before turning sense_N signal both the drains of M1 (100fF capacitor) and M2 (100fF capacitor) are charged to 0.5v.When sense_N is turned ON both M1 and M2 starts conducting. Since the voltage required on drain of M1 to turn on M2 is 10mv less than the voltage required to turn on M1.Therefor M1 turns off faster than M2 making M2 in ON state for more time pulling the drain voltage of M2 to ground.Therefore M2's capacitor will fully discharge to ground.

Spice File:

```
** Assignemt  16.3a ***
.control
destroy all
run
plot M1D M2D sense_n
.endc
.option scale=50n
.tran 100p 30n 0 100p UIC
VNSA    sense_n        0      DC      0       PULSE 0 1 15n
Ccol0  M1D    0       100f   IC=0.5
Ccol1  M2D    0       100f   IC=0.5
M1     M1D    M2D     NLAT    0       NMOS L=1 W=10
M2     M2D    Vgm2    NLAT    0       NMOS L=1 W=10
VGM    Vgm2   M1D     DC      0.01
MPD    NLAT   sense_n         0       0       NMOS L=1 W=10
```

To calculate the voltage difference on capacitor in order to cause metastability, discharge times for both M1 and M2 should be equal

Discharge time of M1 is approximated to Tdis =CVd/Id
Where Vd is drain voltage, C is the capacitance and Id is drain current

Tdism1=100*Xm1/Id1 ; Id1(short channel current)= Vsat$_1$ .W$_1$.Cox'$_1$.(Vgs$_1$-Vthn$_1$-Vdsat$_1$)
where Xm1 is voltage across the 100fF capacitor on M1in order to cause metastability.

Discharge time of M2 is approximated to Tdis =CVd/Id

Tdism2=100*0.5/Id2; Id2(short channel current)= Vsat$_2$ .W$_2$.Cox'$_2$.(Vgs$_2$-Vthn$_2$-Vdsat$_2$)

Therefore Tdism1=Tdism2

From the circuit

100*Xm1/(Vgs$_1$-Vthn$_1$-Vdsat$_1$) = 120*0.5/(Vgs$_2$-Vthn$_2$-Vdsat$_2$);
Where Vgs$_2$ = Xm1+10mv, Vthn=280mv and Vdsat=50mv

Solving the equation gives Xm1=0.492
Therefore voltage difference to create metastabilty=0.5-0.492 = 8mv.

Simulation shown for Xm1=0.4895v , where as calculated value for Xm1= 0.492v
Voltage difference to create metastabilty using simulation is =0.5-0.4895 = 10.5mv

Spice File:
```
*** Assignemt 16.3b ***
.control
destroy all
run
plot M1D M2D sense_n
.endc
.option scale=50n
.tran 100p 30n 0 100p UIC
VNSA    sense_n     0       DC      0       PULSE 0 1 15n
Ccol0   M1D     0       100f    IC=0.4895
Ccol1   M2D     0       100f    IC=0.5
M1      M1D     M2D     NLAT    0       NMOS L=1 W=10
M2      M2D     Vgm2    NLAT    0       NMOS L=1 W=10
VGM     Vgm2    M1D     DC      0.01
MPD     NLAT    sense_n     0       0       NMOS L=1 W=10
```

Problem 16.4

Examining Fig 16.17 we see that there will be a voltage drop along the metal line labeled NLAT when the sense amplifiers fire. Re-sketch this metal line as reistors in between each NSA. If the voltage drop along the line is significant (the length of the line is very long) errors can result. Would we make things better by using individual MOSFET's on the bottom of each NSA connected to sense_N? Why or why not?
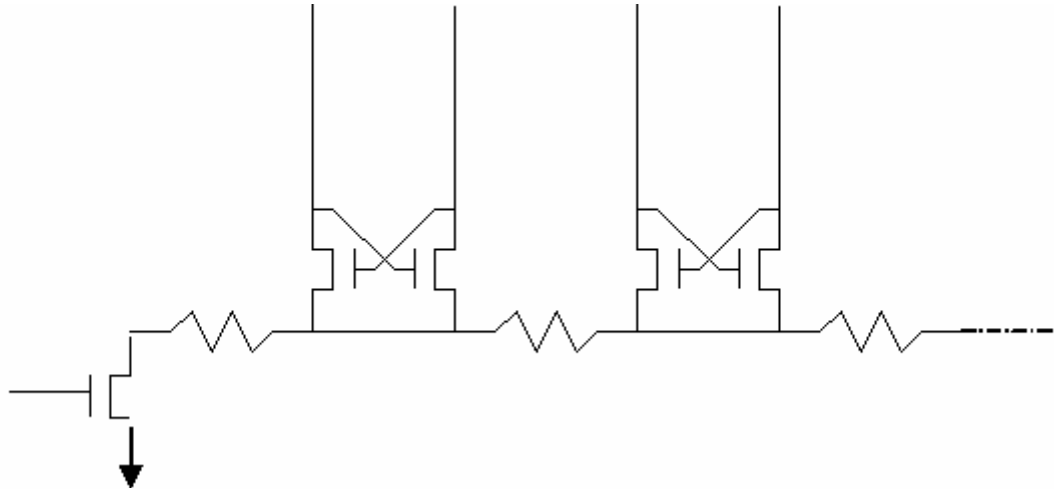

Figure 16.17 redrawn to show resistive NLAT metal line

No, we would not make things better by using individual MOSFETS's on the bottom of each NSA. We would still have the same problem, only it will be shifted to the metal line that is connected to ground instead of the NLAT line. Even worse, the layout size has now increased due to the extra transistors.
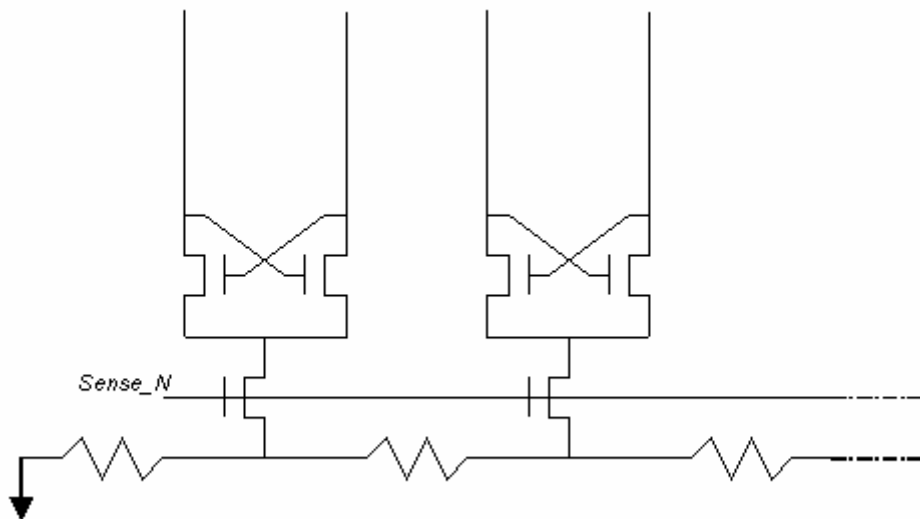

Figure 16.17 redrawn to show individual sense_N mosfets connected to each sense amp.

Problem 16.5
Given that there are 1024 column lines.
Resistance of the cell along the word line= 2 ohms/each cell
Capacitance w.r.t. ground=500aF/each cell
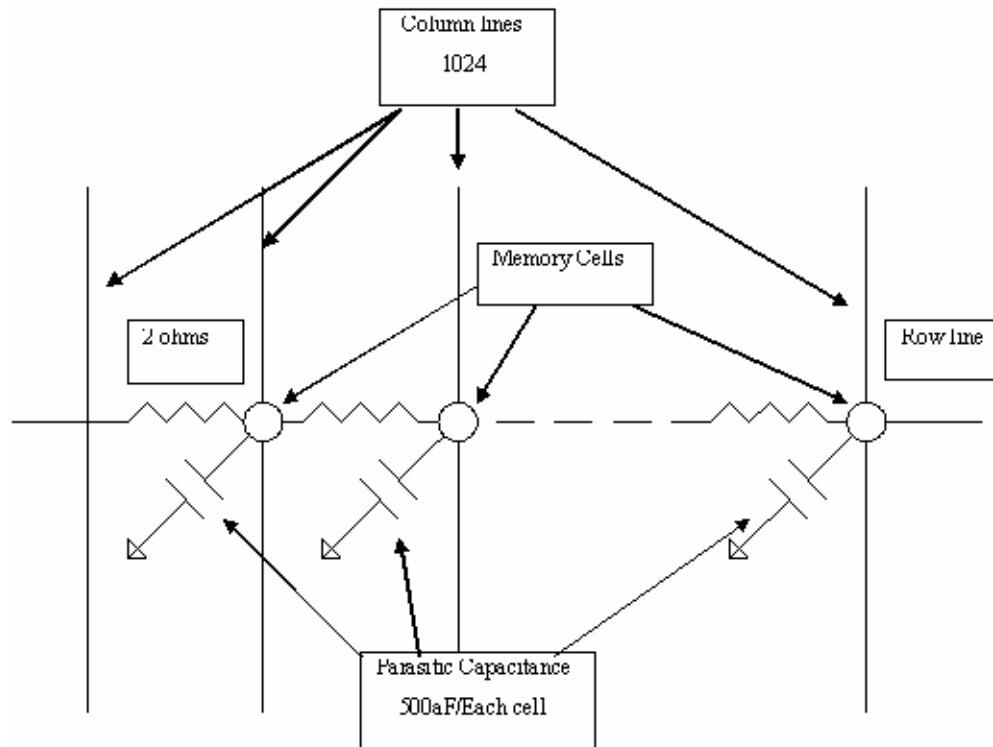Elmore delay for a distributed RC line is given by
Time delay=
.35 x (number column lines)2 x (resistance/each cell)x(capacitance per each cell)
=0.35 x $(1024)^2$ x (2 ohms) x (500aF)
=0.3668 ns
=366.8 ps.

Column lines
1024

Memory Cells

2 ohms

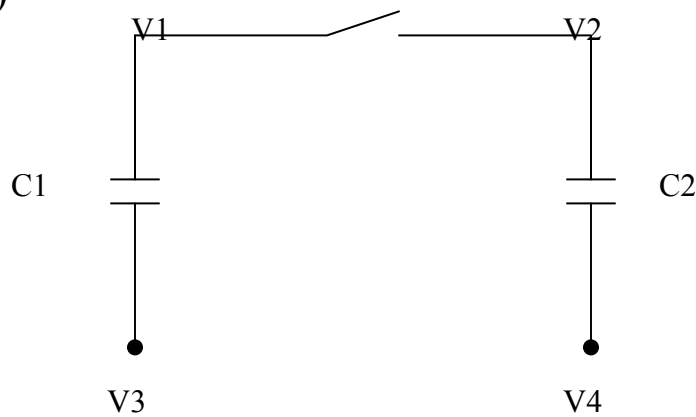Row line

Parasitic Capacitance
500aF/Each cell

For practical reasons, the worst case delay must be considered. The equivalent circuit can be
drawn as below using total resistance and total capacitance, which are 2048 ohms and 512 pF,
respectively.

R=2048 ohms

C=512 fF

Equivalent
Circuit

Equivalent Circuit for the Schematic shown above.

16.6)

The Initial charge on each capacitor when the switch is open is given by

$Q1 = C1 (V1 – V3)$ $\qquad$ $Q2 = C2 (V2 – V4)$

When the switch is closed, there is a charge sharing between the two capacitors and the final voltage is given by

$(V_{final} - V3) C1 + (V_{final} - V4) C2 = C1 (V1 – V3) + C2 (V2 – V4)$

On solving the above equation we get

$V_{final} = [C1V1 + C2V2] / [C1 + C2]$

Problem 16.7)

While comparing the circuits found in figures 16.32 and 16.72, it was found that the differences in operation were extremely small. Therefore there are not any merits or disadvantages of either topology.

The netlists are found below in figures 1 & 2.

```
*** Problem 16.7 --Figure 16.72 --CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
let IDD=-VDD#branch
plot IDD ylimit -50u 150u
print mean(IDD)
*plot Inp Inm clock
plot Outp Outm
plot vtest1#branch vtest2#branch ylimit -50u 50u
.endc

.option scale=50n

.tran 100p 40n 0 100p UIC

VDD     VDD    0        DC      1
Vinp    Inp    0        DC      0         PULSE 0.25 0.45 0 0 0 20n 40n
Vinm    Inm    0        DC      0.35
Vclock  clock  0        DC      0         PULSE 0  1 10n 0 0 10n 20n
Vtest1  s1     0        DC      0
Vtest2  s2     0        DC      0

R1      Inp    gb1      100k
R2      Inm    gb2      100k

MN1     d1     Outp     s1      0         NMOS L=1 W=10
MN2     d2     Outm     s2      0         NMOS L=1 W=10

MP1     Outm   clock    VDD     VDD       PMOS L=1 W=30
MP2     Outm   Outp     VDD     VDD       PMOS L=1 W=30
MP3     Outp   Outm     VDD     VDD       PMOS L=1 W=30
MP4     Outp   clock    VDD     VDD       PMOS L=1 W=30

MS1     Outm   clock    db1     0         NMOS L=1 W=10
MS2     Outp   clock    db2     0         NMOS L=1 W=10

MB1     db1    gb1      d1      0         NMOS L=1 W=10
MB2     db2    gb2      d2      0         NMOS L=1 W=10
```
Figure 1: Netlist for figure 16.72 of problem 16.7

```
*** Figure 16.32 CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
let IDD=-VDD#branch
plot IDD ylimit -50u 150u
print mean(IDD)
plot Inp Inm clock
plot Outp Outm
plot vtest1#branch vtest2#branch ylimit -50u 50u
.endc

.option scale=50n

.tran 100p 40n 0 100p UIC

VDD     VDD     0       DC      1
Vinp    Inp     0       DC      0       PULSE .25 .45 0 0 0 20n 40n
Vinm    Inm     0       DC      0.35
Vclock  clock   0       DC      0       PULSE 0  1 10n 0 0 10n 20n
Vtest1  sb1     0       DC      0
Vtest2  sb2     0       DC      0

R1      Inp     gb1     100k
R2      Inm     gb2     100k

MN1     d1      Outp    db1     0       NMOS L=1 W=10
MN2     d2      Outm    db2     0       NMOS L=1 W=10

MP1     Outm    clock   VDD     VDD     PMOS L=1 W=30
MP2     Outm    Outp    VDD     VDD     PMOS L=1 W=30
MP3     Outp    Outm    VDD     VDD     PMOS L=1 W=30
MP4     Outp    clock   VDD     VDD     PMOS L=1 W=30

MS1     Outm    clock   d1      0       NMOS L=1 W=10
MS2     Outp    clock   d2      0       NMOS L=1 W=10

MB1     db1     gb1     sb1     0       NMOS L=1 W=10
MB2     db2     gb2     sb2     0       NMOS L=1 W=10
```
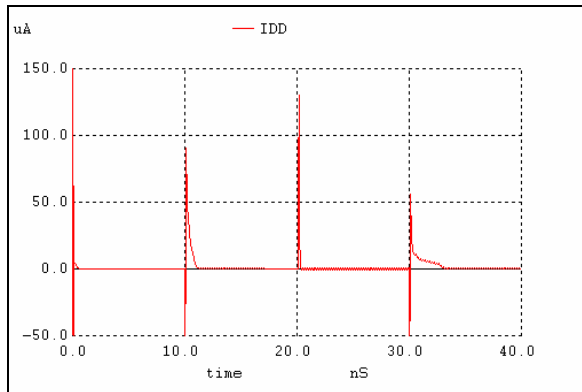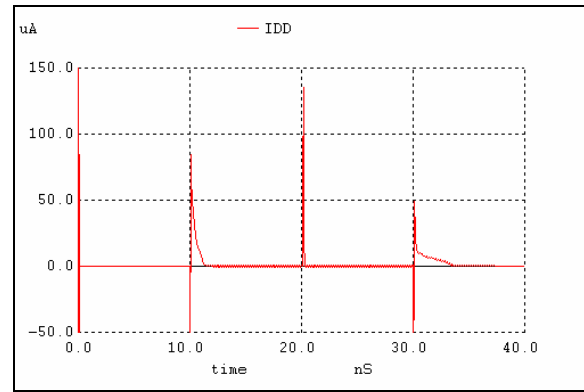**Figure 2: Netlist for figure 16.32 used to compare against problem 16.7**

Figure 16.32: total circuit current
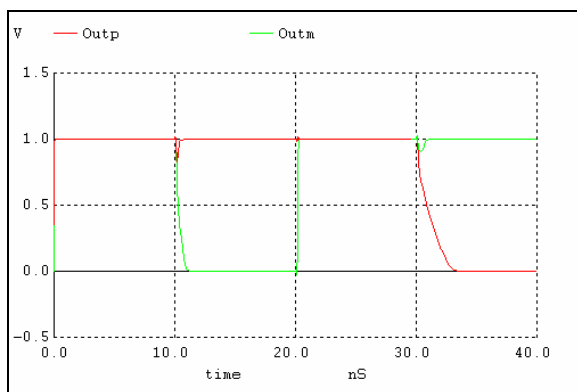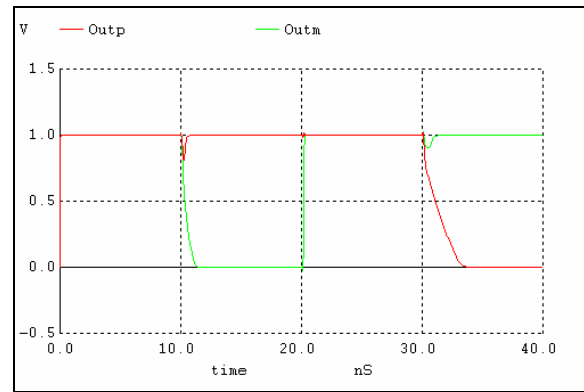

Problem 16.7: total circuit current

Figure 16.32: Voutm & Voutp vs time

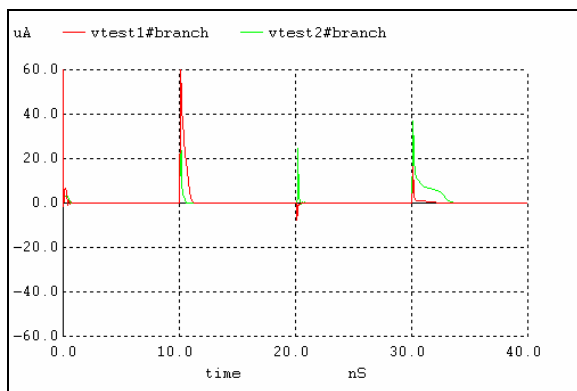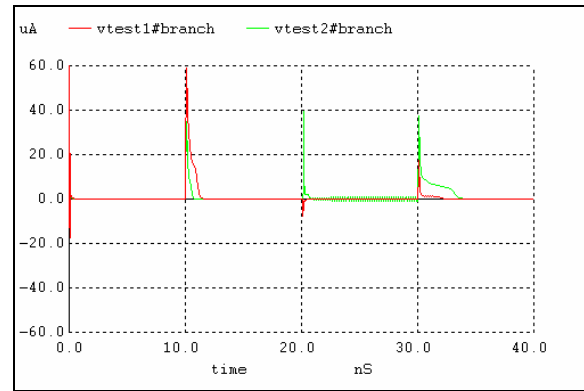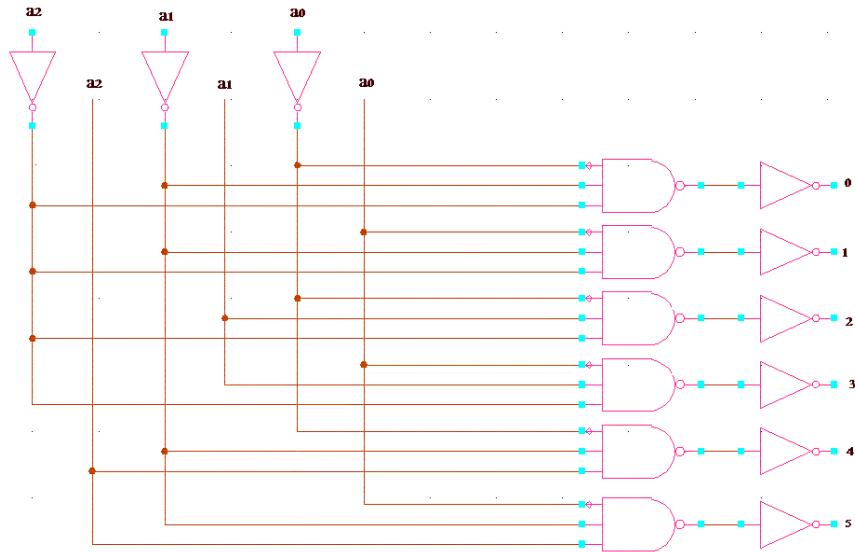**Problem 16.7: Voutm & Voutp vs time**

Figure 16.32: current through each leg of comparator

Problem 16.7: current through each leg of comparator

Solution 16.8:

 The Following static column decoder consists of 6 Nand gates and inverters that can be implemented to decode the desired address for figure 16.73. The outputs of the decoder are connected to the gates of the I/O lines.

16.9) The I/O lines in the previous problem won't swing to full logic levels. In order to restore a full VDD level on these lines and to speed up the signals a helper *flip-flop* is used. Sketch a possible implementation of the helper flip-flop. Why can it be used to speed up the signals?

An implementation of a helper flip-flop (HFF) would be the circuit in Fig 16.35 (shown below).
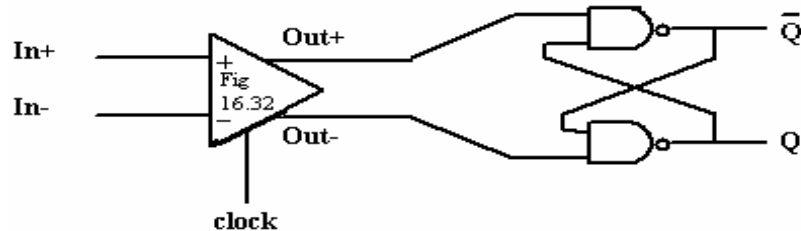

Fig 16.35

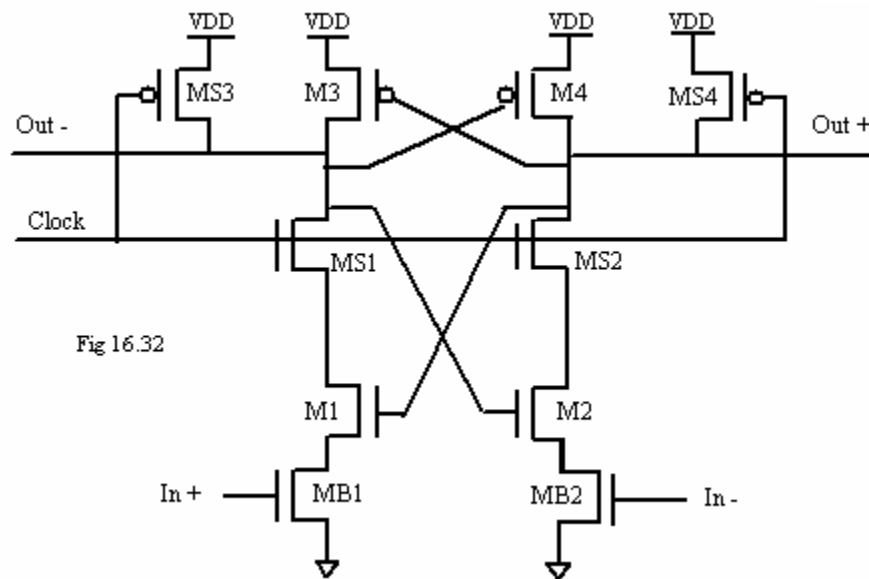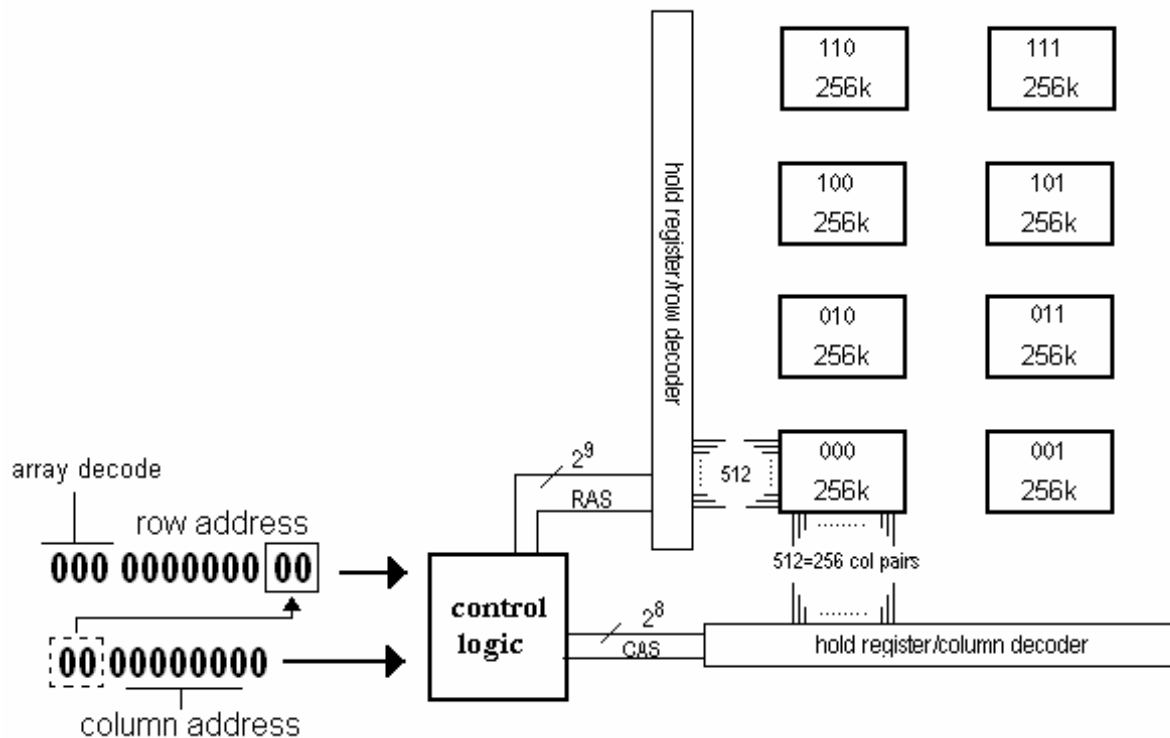The following is the sense amp circuit used in Fig 16.32 (shown below).

The reason the sense amp in Fig 16.32 is used with the SR flip-flop as an implementation of HFF, is as follows. This particular sense amp has good sensitivity and gain. As long as the inputs are $> V_{thn}$ a path to ground is provided to give correct logic signals and have no dynamic nodes. The addition of the SR flip-flop ensures that the outputs will only change on the rising edge of the clock. This allows the circuit implementation to behave like a flip-flop with the sensing capabilities. The way the HFF speeds the signals up is due to the good sensitivity in combination with signals being restored to full logic levels allowing the circuit to make quicker transitions.

Problem 16.10)

Solution:
A 2Mbit memory has 2 million memory cells, to access each cell we would need 21 address pins, (2^{21}=2Meg). This is a x2 part which will give us two bits for each address so we need 20 address pins to access all 2 Meg of data. We multiplex the 10 input pins for both the row and column address. To do this we generate a clock signal, often called RAS, to clock the row address into a hold register to be decoded later and then sent out to open the selected row. We then generate a clock signal, often called CAS, to clock the column address into a hold register to be decoded and sent out to the selected column pair. We subdivide the 2 Meg into 8-256k subarrays, (8 * 256k=2Meg) and use the 3 MSB from the row address to select which subarray we will be accessing. The remaining 7 bits are used from the row address along with the 2 MSB from the column address, (2^9=512). The remaining 8 bits are used for the column select, (2^8=256 column pairs).
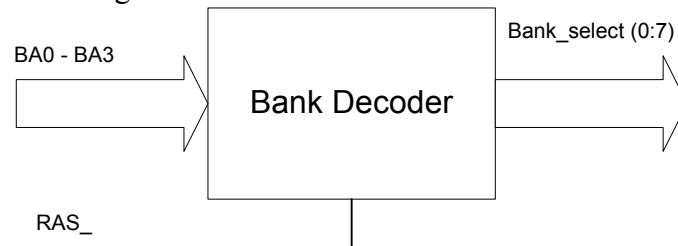
Block diagram:

EE597 **HW 16.11**   **Dong Pan**

16.11. A memory with 2M bit 2 DQ. Configed as 8*256K. (1024 row, 512 col, folded)
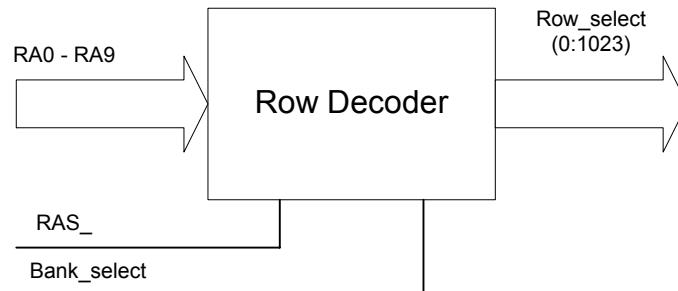1) How many I/O line is needed for each array?
2) How big is a page of data?
3) Sketch a decoding scheme.
4) Assume 3 bits is globally decoded and others are locally decoded. How many these bit needed to be routed to each array?
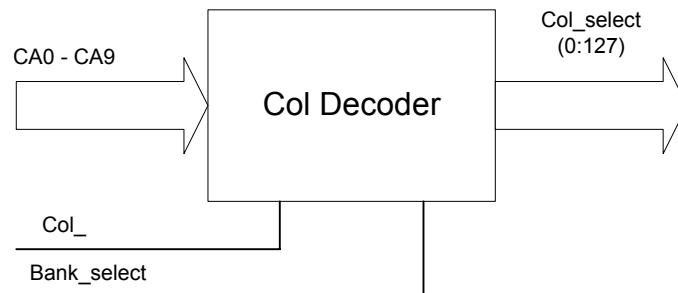
Solution:
1) Each array need 2 sets of I/O line. Total 4 I/O lines (I/O1, I/O1_, I/O2, I/O2_)
2) A page of data is defined as the number of bits when one row open.
      Total 512 col or 256 col/col_ set signals opened for this circuit. So a page is equal to 256 bits or 128 words (each word has 2 bits)
3) a. Bank decoder. 3 to 8 global decoder

BA0 - BA3 → **Bank Decoder** → Bank_select (0:7)
RAS_

b. Row decoder. 10 to 1024 decoder for each bank

RA0 - RA9 → **Row Decoder** → Row_select (0:1023)
RAS_
Bank_select

c. Col/Col_ select decoder: 7 to 128 decoder for each bank

CA0 - CA9 → **Col Decoder** → Col_select (0:127)
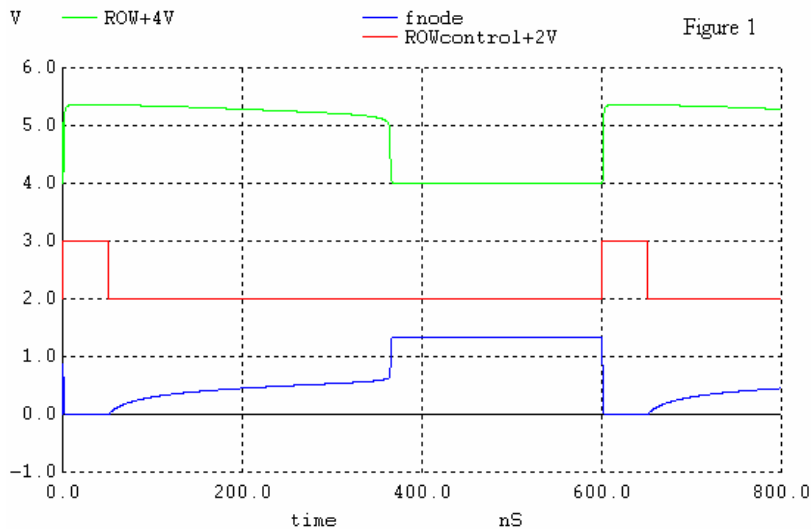Col_
Bank_select

4) Total 18 bits needed to be routed to each array.
      Include 10 Row address bits, 7 Col address bit, one Bank select signal.

Problem 16.12

The design of Figure 16.74 works fine when you are turning on the word line as long as the proper device sizes are chosen. The problem with the design is when you turn off the word line. The drain of M1 and M3 will be in a floating state (labeled fnode in the Spice example). This floating node will be known to be at its worse case when you have just finished accessing the row because it will start off at ground. The node is going to be somewhat unpredictable. Any dip in the word line voltage will turn on M3 and start to charge the floating Node. This creates a condition where the Node will increase upward until it reaches the critical voltage to turn the word line off fully. Also the Node voltage moving upward at all will start this chain of events also. In any case the word line will not turn off in a reasonable amount of time and the unpredictability in the design is unacceptable.

In Figure 1 the design is demonstrated using Spice. The ROWcontrol signal starts off high turning the word line on. When the ROWcontrol signal transitions low we want the word line to turn off. This is not immediately the case. The word line (labeled ROW in the Spice Example) takes more than 300nS to switch for my chosen device sizes. At 600nS the ROWcontrol has no problem bringing the word line high again. With the device size, word line resistance, and word line capacitances that I chose it takes around 2ns for the ROWcontrol signal to bring the word line high.

Figure 1

Spice Net List:

```
*** Problem 16.12 Solution ***
.control
destroy all
run
plot ROWcontrol+2V ROW+4V fnode
.endc
.option scale=150n
.tran 500p 800n 0 500p UIC
VCCP    VCCP    0        DC      1.35
```

```
VDD     VDD    0     DC    1
Von     ROWcontrol       0       DC      0       PULSE 0 1 0 0 0
50n 600n
C1       Crow   0   500f ic = 0
Rrow    ROW    Crow    2048
M1      fnode      ROWcontrol 0      0       NMOS L=1 W=5
M2      ROW      fnode     0      0       NMOS L=1 W=30
M3      fnode      ROW      VCCP    VCCP    PMOS L=1 W=5
M4      ROW      fnode     VCCP    VCCP    PMOS L=1 W=60
```

Name: P.K.Irkar
Prob:16.13

Simulate the operation of the SRAM cell seen in fig. 16.48. Use the 50 nm process with Nmos of 10/1 and PMOS of 20/1. Is it wise to have the access MOSFETS the same size as the latch MOSFETS? Why or why not? Use simulations to verify your answers.

Solution:
SRAM memory cell is a cross coupled connection of invertors. The cross coupled invertors form a +ve feedback circuit, forcing the outputs in opposite directions. When the word/row line is low, both access transistors are off and the datum in the cell is latched, as long as power is applied to the cell.

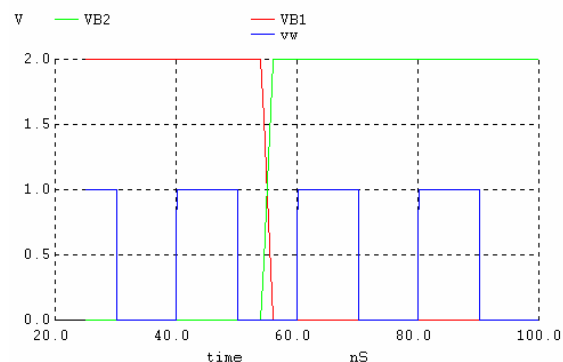The simulation of the SRAM cell shown in fig. 16.48. is as follows:
Notations: B1 – bit , B2- bit bar, Q1- o/p of M1, Q2- o/p of M2, W- word line control
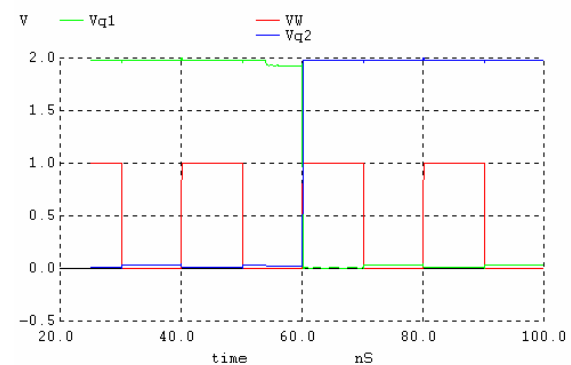**Netlist 1:**

```
\* SRAM cell
* SPICE command scripts
.control
destroy all
run
plot VW Vq1 Vq2 VB1 VB2
.endc
*Access devices
MA1 VB1 VW Vq1 0 NMOS     W=40     L=1
MA2 VB2 VW Vq2 0 NMOS     W=40     L=1
*Nmos devices
M1 Vq1   Vq2 0 0  NMOS     W=10     L=1
M2 Vq2   Vq1 0 0  NMOS     W=10     L=1
*Pmos devices
M3 Vq1   Vq2 VDD VDD  PMOS      W=20     L=1
M4 Vq2   Vq1 VDD VDD  PMOS      W=20     L=1

VDD VDD 0 DC 5
Vb1 Vb1 0 PULSE (0 5V 2NS 2NS 2NS 50NS 100NS)
Vb2 Vb2 0 PULSE (5v 0 2NS 2NS 2NS 50NS 100NS)
VCLK VW 0 DC 0 PULSE 0 5 0 .1N .1N 10N 20N
.TRAN 2NS 100NS 25Ns
.options scale=50nm
* BSIM4 models
.end
```
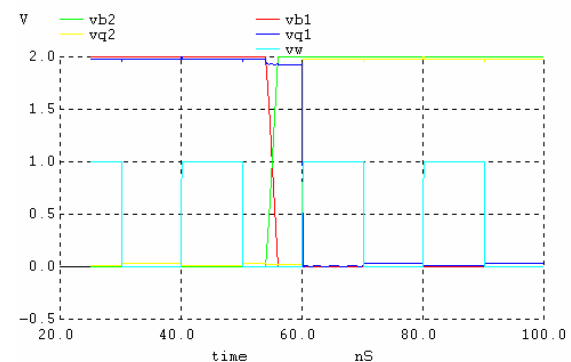
Simulation results: Control signals – word line (Vw) and bit line signals (Vb1,Vb2)

Output signals: VQ1 and VQ2

Outputs with input control signals:

Is it wise to have the access MOSFETs the same size as the latch MOSFETs?

Ans: No, it is not good to have same sizes of access and latch transistors because the effective resistance of the pass transistor is too large to allow overwriting the cell. So if the W/L ratio of access transistor is approximately four times of the latch transistor's W/L ratio, the data on the bit lines are written to the cell.

Simulation with Matched access and latch transistors:

Netlist 2: Only change in Netlist is put the equal W/L's of access and latch transistor

```
*Access devices
MA1 VB1 VW Vq1 0 NMOS      W=10      L=1
MA2 VB2 VW Vq2 0 NMOS      W=10      L=1
*Nmos devices
M1 Vq1    Vq2 0 0  NMOS      W=10      L=1
M2 Vq2    Vq1 0 0  NMOS      W=10      L=1
```
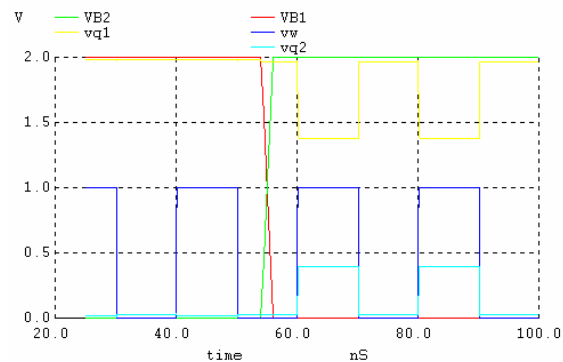
The following simulation result shows that even though the bit /bit bar are flipped, the outputs are not changed. So it needs to be overwritten to flip the data on cell

Netlist 3: Making the access transistors approximately four times than latch transistor

```
*Access devices
MA1 VB1 VW Vq1 0 NMOS      W=40      L=1
MA2 VB2 VW Vq2 0 NMOS      W=40      L=1
*Nmos devices
M1 Vq1    Vq2 0 0  NMOS      W=10      L=1
M2 Vq2    Vq1 0 0  NMOS      W=10      L=1
```
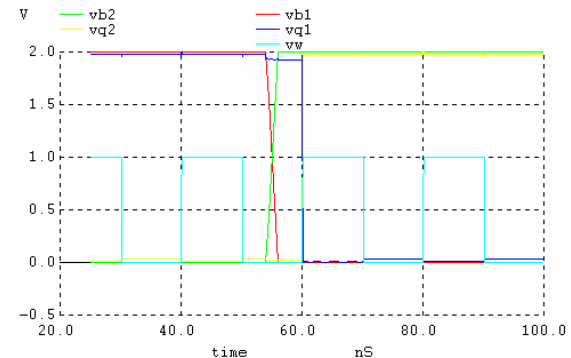
The following simulation result shows that the change in output with respective of bit line and word line control signals .
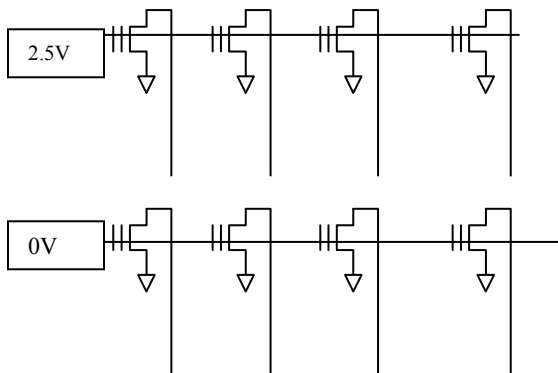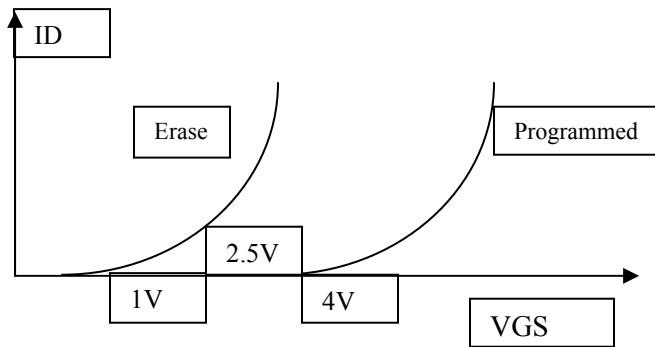
16.14

Suppose an array of EPROM cells, see Fig16.57, consisting of two row lines and four bit lines is designed, Further assume $V_{THN, Erased} = 1V$ and $V_{THN, Prog} = 4V$. Will there be any problems reading the memory out of the array if and unused row line is grounded while the accessed row line is driven to 5V? Explain why or why not.

Solution:

It is desired that the unused row line is grounded so that the transistors are turned off.

If the accessed row line is drive to 5V, then transistors on both erased and programmed bits are fully turned on, the current difference between the two is insignificant. Therefore, we can not tell which bit is erased or programmed. So, yes, there would be problem if the accessed row line is driven to 5V. Therefore chose 2.5V as accessed row line voltage is desired in order to read. See figure below, When the VGS is at 2.5V, I_{erased} is much greater than the $I_{programmed}$. If we chose the middle point of I_{erased} and $I_{programmed}$, that is $(I_{erased} + I_{programmed}) / 2$, the bit is erased if voltage is logic 0, and the bit is programmed if the voltage is logic 1.
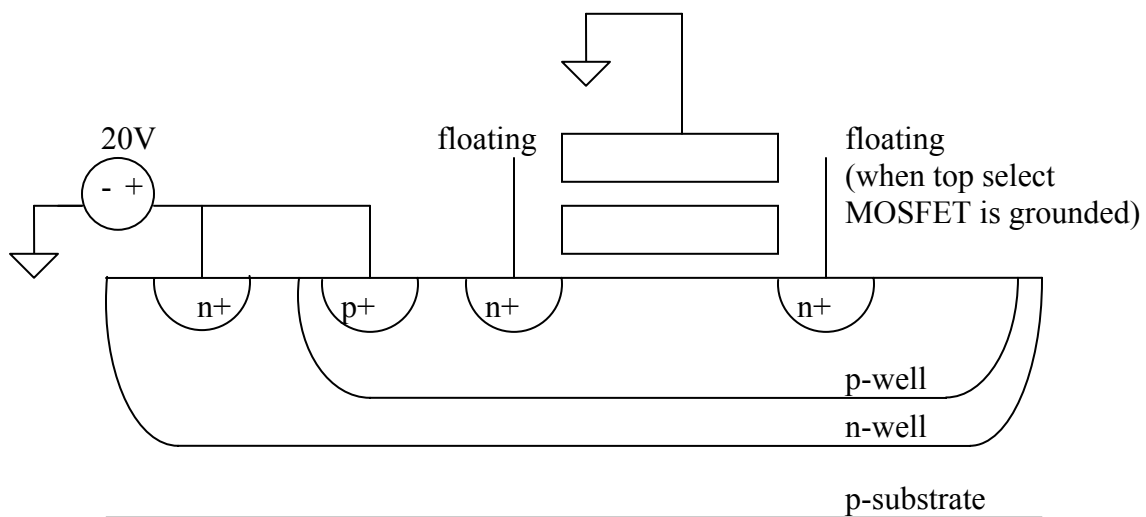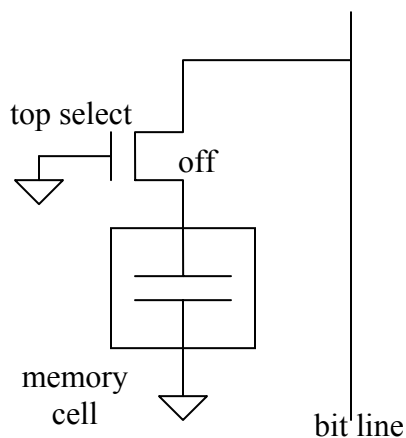
16.15

It was suggested that the n-well in a NAND flash memory cell should be at GND at all times except during the erase. This is actually a better biasing condition than pumping the n-well up to +20V. There will be less loading of the HV pump and less programming current. There is also no danger of forward biasing the np junction of the nwell/pwell.

Problem 16.16

The top select MOSFET is needed in a NAND Flash memory cell. One of two reasons is that forward bias is prevented between the p-well and n+ drain when 20V is applied to the p-well during the erase process. To do this, we need to ground the gate of the top select MOSFET.

The other advantage is that it lowers the capacitance loading on the bit line because the bit line does not connect to the memory cell when the top select MOSFET is off.

16.17)

To program a flash memory cell the gate should be pulled to +20V,drain at ground, while source is floated. The n+ connection to the n well may be connected to +20V, but in order to minimize the power both the n+ connection to n well and p+ connection to p well are pulled down to ground. Fig 1. shows the required conditions to program the cell.

In order to program the flash cell connected to RA3 with n+ source connection pulled to ground, the gate of RA3 is connected to +20V. The drain of the cell is connected to 0V by pulling the bit line to ground. The gates of RA0-RA2 and select_top transistors are connected to 5V and 20V respectively. This ensures that those transistors get turned on. The source of RA3 is floated by connecting the gate of the select_bot transistor to ground. This will not turn on the select_bot transistor and hence floats the source of the RA3.
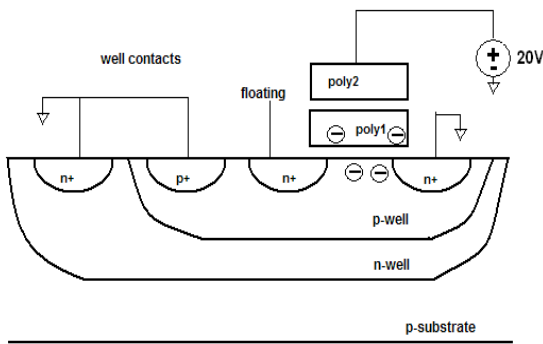
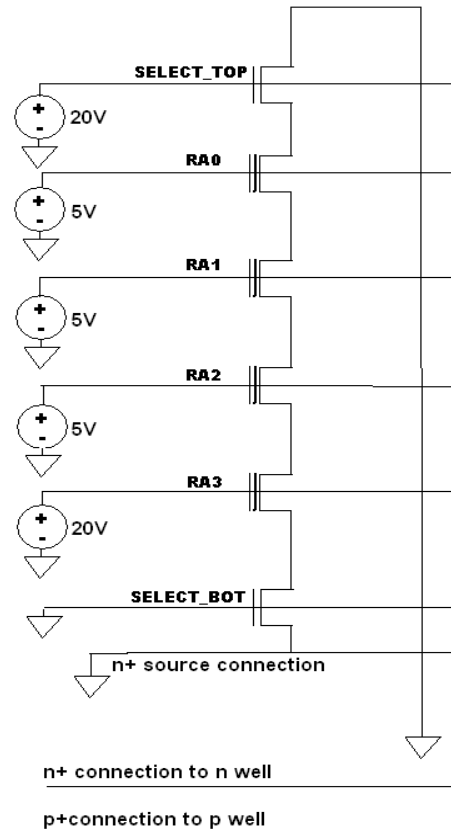Fig 1. Programming a flash cell.

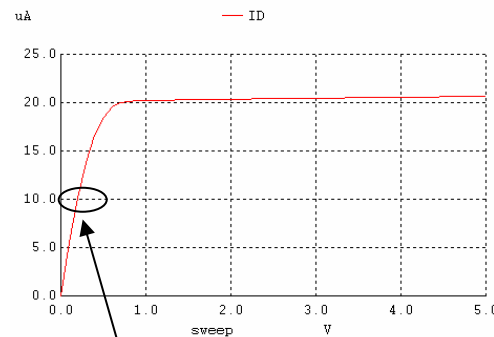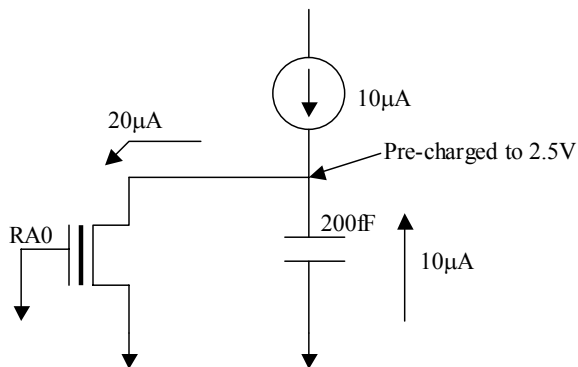Fig2. Programming RA3 in flash memory

16.18

a. Per fig. 16.62, to program just the MOSFET RA0, RA1 - RA3 need not necessarily be at 5V. But, any voltage higher than 5V, may trigger FNT, thereby causing them to be Programmed. Therfore the gates of RA1 – RA3 can be left at 0V or 5V.

b. Yes, RA1 - RA3 can remain grounded (if only RA0 needs to be programmed).

c. Since grounding RA1 - RA3 does not impact RA0 being written to, they can remain at 0V.

d. If RA1 is to be programmed, RA0 has to be at 5V. Else, RA1 cannot be written to (accessed). If RA0 stays at 0V, then RA1 cannot have charge transfer via FNT, and if RA0 is driven high (to 20V), we program that Xr. Hence, 5V (or whichever voltage enable us to turn the Xr, but not cause FNT) is what RA0 needs to be driven to.

Problem 16.19

If the flash cell is Erased:
The bit line is initially equilibrated to 2.5V. When the sensing begins, the erased flash cell draws 20μA. Only 10μA is available from the current source, so 10μA flows up through the bit line and the bit line discharges towards ground. The final bit line voltage is a few hundred mV above ground (the V_{DS} corresponding to 10μA on the V_{DS}-I_{DS} curve).

Bitline discharges to

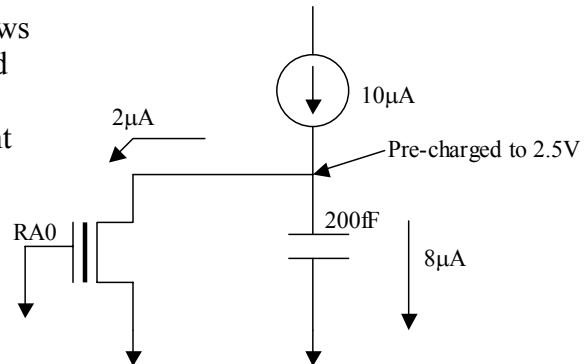The time for the data on the bit line to settle can be determined from:

$$\frac{I}{C} = \frac{\Delta V}{\Delta t} \Rightarrow \Delta t = \frac{(\Delta V * C)}{I} \Rightarrow \Delta t = \frac{((2.5V - .2V) * 200\,fF)}{10\,\mu A} = 46ns$$

(Note V_{final} is estimated at 200mV).

<u>If the flash cell is Programmed:</u>
When the sensing begins, the programmed flash
cell draws only 2μA. The remaining 8μA flows
through the bit line until the bit line is charged
up towards V_{DD}. The final bit line voltage
corresponds to the V_{DS} required for the current
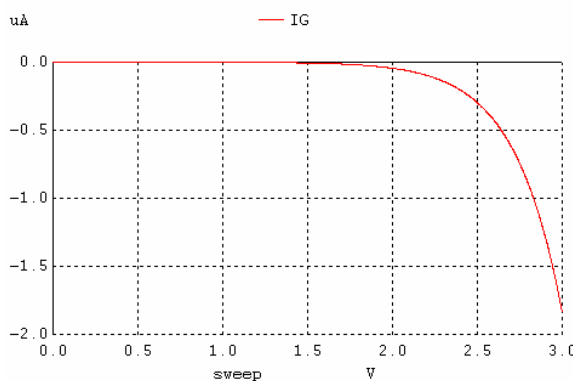source to provide only 2μA.

To determine the time required for data
to settle on the bit line, $V_{final} = 4.9V$
is assumed.

$$\Delta t = \frac{(\Delta V * C)}{I} \Rightarrow \Delta t = \frac{((4.9V - 2.5V) * 200\,fF)}{8\,\mu A} = 60ns$$

16.20

Erasing the memory cell by applying a positive potential to the drain and grounding the
gate of the MOSFET, does cause a negative current to flow through the gate. This works
because electrons will travel off the gate, through the oxide and to the drain, (or since
they are connected the bitline.) This is equivalent to driving current from the drain into
the channel and out the gate, (hence the negative current in the figure below.)


```
*** PROBLEM 16.20

.control
destroy all
run
let IG=-VGS#branch
plot IG
.endc

.option scale=50n

.DC VDS 0 3 1m

VGS  VGS  0  DC  0
VDS  VDS  0  DC  0

M1  VDS  VGS  OpenS  0  NMOS L=1 W=10
RopenS    OpenS  0   1G

* BSIM4 models
```