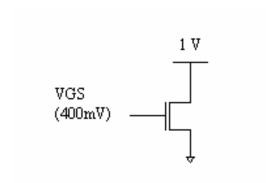
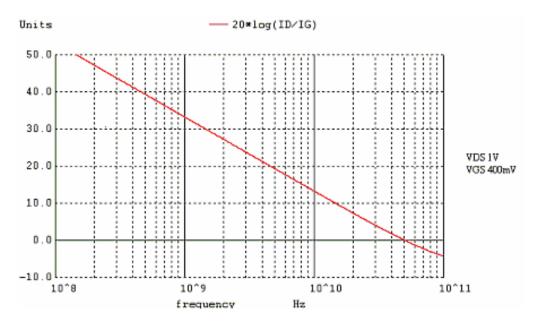
Problem 26.1 Dennis Montierth

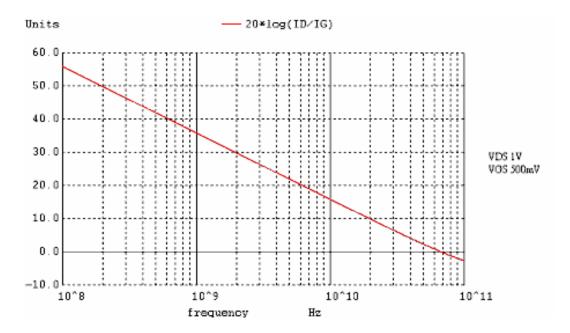
Using simulations determine the transition frequencies for the NMOS and PMOS devices seen in Fig. 26.1 at the nominal operating conditions indicated in the figure. Show that by increasing the MOSFET's overdrive voltage the transition frequencies increase.

### NMOS:





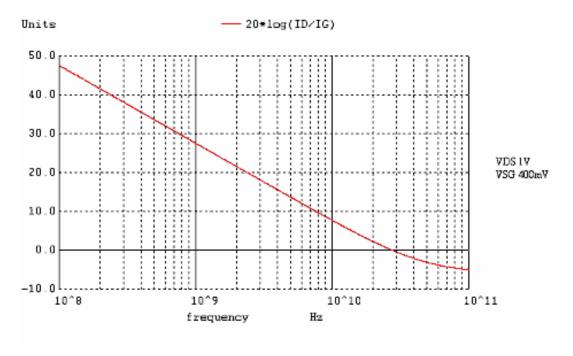
Here I have used the nominal operating conditions to plot the transition frequency. The transition frequency as shown in this plot is around 50 GHz. Increasing the overdrive voltage is the same as increasing VGS. I will now increase VGS to 500mV to show that as the overdrive voltage increases, so does the transition frequency of the MOSFET.



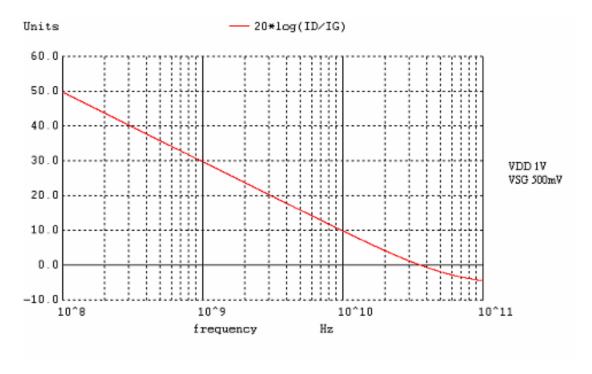
You can see that the transition frequency has increased to around 70 GHz.

### PMOS:

I am going to repeat the previous example for the PMOS. The same explanations apply.



Transition frequency is around 30 GHz.



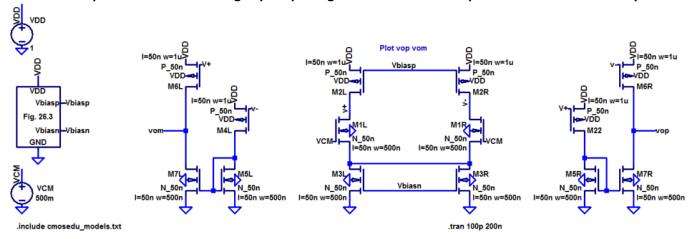
Transition frequency moved closer to 40 GHz.

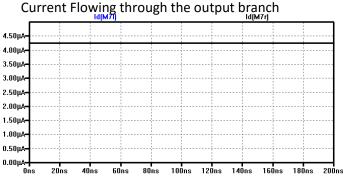
Net List for First PMOS graph:

\* 50nm BSIM4 models

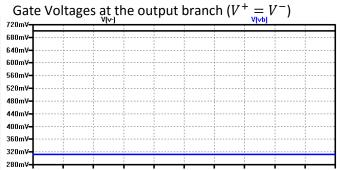
```
*** Problem 26.1 ***
.control
destroy all
let ID=mag(VDS#branch)
let IG=mag(VGS#branch)
plot 20*log(ID/IG)
.endc
.option scale=50n
       DEC 1000 10MEG 1000G
.AC
VDS
       VDS
              0
                      DC
VGS
       VGS
              0
                      DC
                             600m
                                    AC
                                            1
M1
       VDS
              VGS
                      0
                             VDD
                                     PMOS L=1 W=20
```

26.2 Simulate the operation of the two-stage op-amp in Fig. 26.2. Show that the quiescent current in the output





Notice how the current through the output branch is 4.25uA. This is caused by the gate voltages at the output branch which are shown in the plot to the right.



Notice how the PMOS gate voltage is ~700mV. This means that the  $V_{sg}$  of the PMOS device is 300mV. Also notice that the NMOS  $V_{gs}$  is ~300mV.

### Does this affect the speed of the output buffer? Why or why not?

Yes, the speed of the output buffer is affected by the low quiescent current / gate bias voltage! The standard  $V_{sg}$  and  $V_{gs}$  voltage is 400mV ( $V_{biasn}$  is set to 400mV). Decreasing the  $V_{gs,sg}$  of the output branch means that the overdrive voltage  $V_{ov}$  is decreased! Decreasing  $V_{ov}$  will decrease the transcondondcutance ( $g_m$ ) of the output branch which decreases the transition frequency  $f_T$ ! This issue is demonstrated in book problem 26.1.

Problem 26.3 Kostas Moutafis

Plot reference current against resistor value for the BMR seen in Fig. 26.3. Use simulations to determine the IREF for each value of resistance.

### **Solution:**

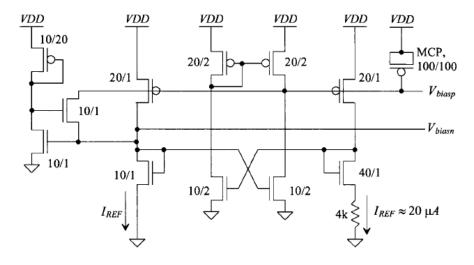
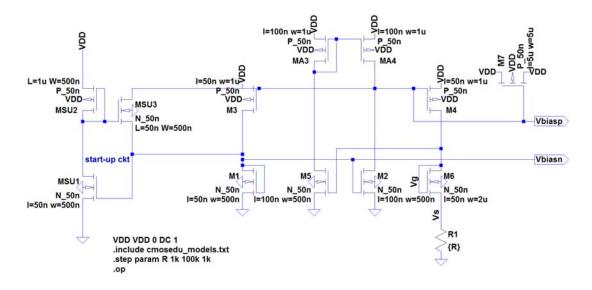


Figure 26.3: Biasing circuit used in chapter 26

We expect the reference current to decrease as we increase the value of the resistor. However, when the gate source voltage of the 40/1 NMOS reaches the threshold voltage (around 280mV), the current will stop changing (much) as we increase the resistance.

To prove what mentioned above we will run a ".step param" for the value of the resistance as seen in the figure below.



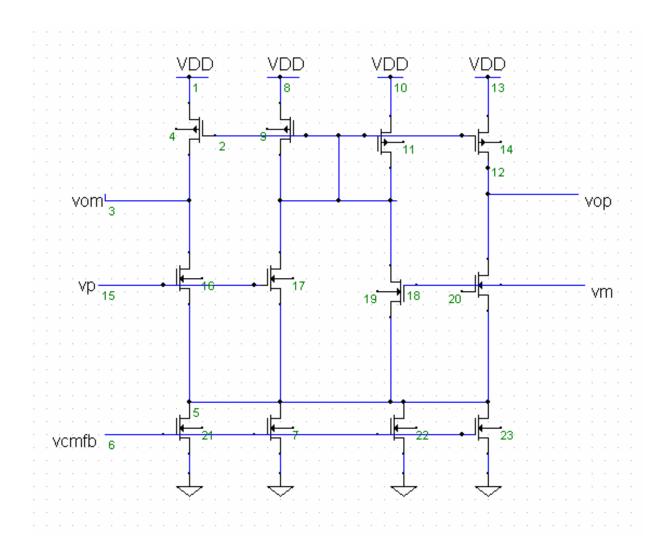


As we can see in the simulation above, the current will decrease as we increase the value of the resistance. We can also see, that the current stays almost constant when the Vgs of the 40/1 NMOS reaches the threshold voltage, which is the case when  $R > 10k\Omega$ .

If we want to find the exact  $I_{REF}$  values for different values of the resistance we can either use the attached cursor for the Id(M6) curve or do operating point [.op] analysis for specific R values. Either way we get the same results. We summarize some of them in the following table.

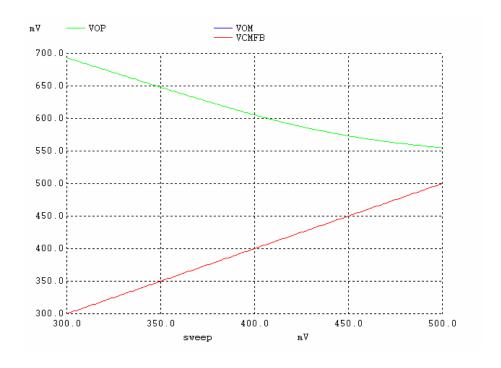
Resistance	$I_{ m REF}$
1k	154μΑ
2k	58μΑ
4k	20μΑ
8k	8.4μΑ
10k	6.5μΑ
20k	3μΑ
40k	1.65μΑ
80k	1.11μΑ
100k	0.97μΑ

Problem 26.4)
Comment on the benefits and /or concerns with the CMFB input connections seen in the fig 26.61. Use simulations to support your answers. Note the similarity to the way CMFB was implemented in fig 26.17.



In the above fully differential amplifier, if the  $v_{cmfb}$  is connected as shown in the circuit diagram the gain will be less than one. We can visualize it as similar to the common source amplifier configuration with gate drain connected load where the gain is approximately equal to one. (gain=resistance seen from the drain/ resistance seen from the source)

The simulation results are shown in the next page:



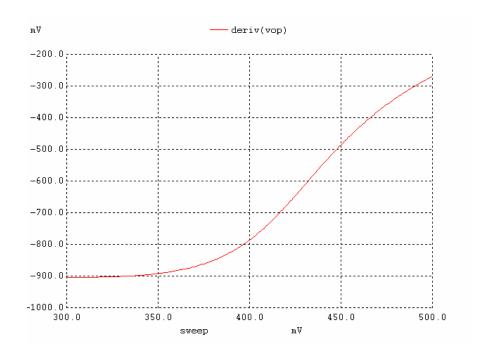
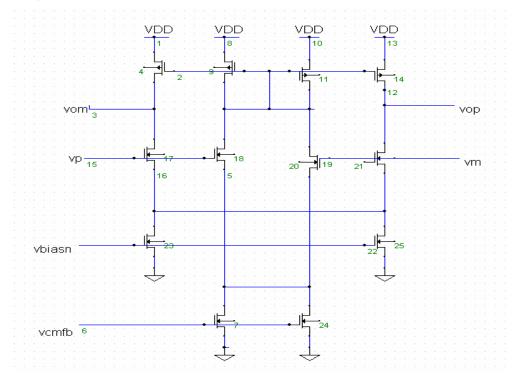
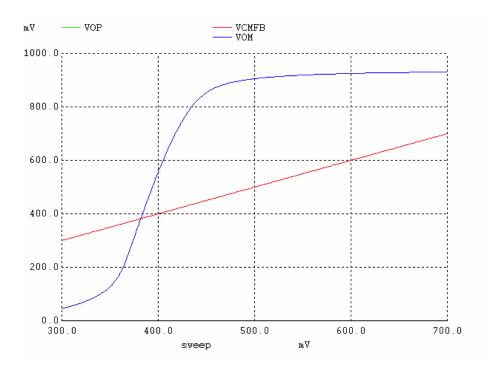
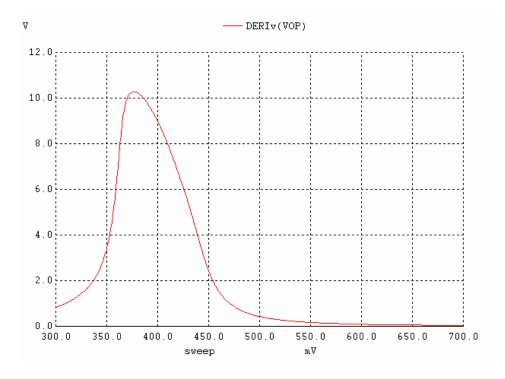


Fig 26.x.2)



In the above circuit configuration driving the two tail NMOS devices with common mode feedback voltage results in having more gain than the previous configuration. Notice that vop and vom are high impedance nodes. The only concern here is that increasing the gain may result in instability.

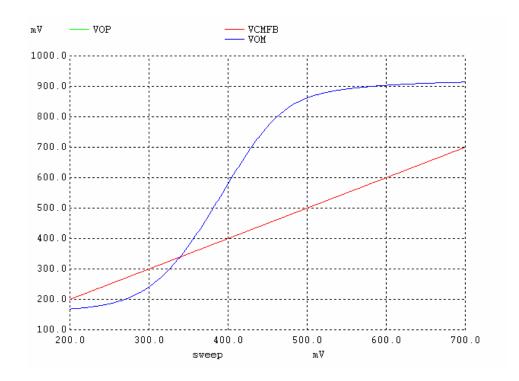


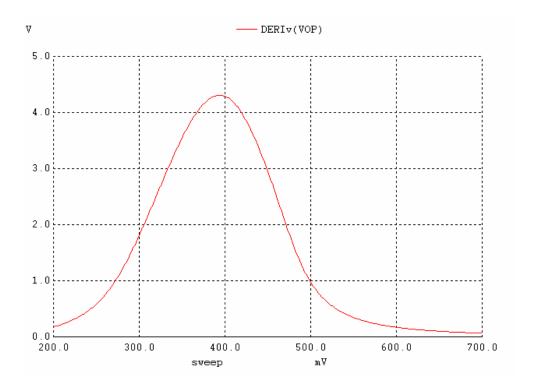


NOTE: Gain can be further reduced (halved) if the CMFB signal to the diff amp is driving only single NMOS device in the tail current source instead of two as seen in above figure.

Now we simulate the same above circuit but with the CMFB signal applied to only a single NMOS tail current device. We expect the gain to reduce by half.

The simulation results are shown below;





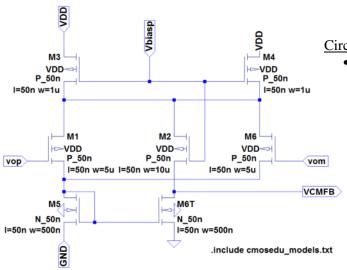
As seen the gain has reduced approximately by a factor of two.

```
The SPICE netlist is given below:
.control
destroy all
run
plot VCMFB VOP VOM
.endc
.option scale=50n
.dc VCMFB 0.3 0.7 1m
*.tran 1u 1000u UIC
VDD VDD 0
                 DC
                      1
VP
     VP
           0
                 DC
                      0.5
VM
     VM
           0
                 DC
                      0.5
VCMFB
           VCMFB
                            DC
                                  0
                      0
Xbias vbiasn vbiasp VDD
                      bias
M1L
     VN
           VCMFB
                      0
                            0
                                  NMOS W=10 L=1
M2L VOM VP
                 VN
                      0
                            NMOS W=10 L=1
M3L
     VOM VGD VDD
                     VDD PMOS W=20 L=1
M4L VGD VGD VDD VDD PMOS W=20 L=1
```

```
M5L
     VGD VP
               VN
                     0
                          NMOS W=10 L=1
M6L
     VN
          VCMFB
                     0
                                NMOS W=10 L=1
M1R VN
          VCMFB
                     0
                          0
                                NMOS W=10 L=1
                VN
M2R VOP
          VM
                     0
                           NMOS W=10 L=1
          VGD VDD
M3R VOP
                    VDD
                          PMOS W=20 L=1
M4R VGD VGD VDD VDD PMOS W=20 L=1
M5R VGD
          VM
                VN
                     0
                           NMOS W=10 L=1
     VN
          VCMFB
M6R
                     0
                          0
                                NMOS W=10 L=1
.subckt bias vbiasn vbiasp VDD
     Vbiasn Vbiasn 0
                          NMOS L=1 W=10
M1
                     0
M2
     Vreg Vreg Vr
                     0
                          NMOS L=1 W=40
     Vbiasn Vbiasp VDD VDD PMOS L=1 W=20
M3
          Vbiasp VDD VDD PMOS L=1 W=20
M4
     Vreg
Rbias Vr
          0
                4k
*amplifier
     Vamp Vreg 0
                     0
                           NMOS L=2 W=10
MA1
MA2 Vbiasp Vbiasn 0
                     0
                           NMOS L=2 W=10
MA3 Vamp Vamp VDD VDD
                          PMOS L=2 W=20
MA4 Vbiasp Vamp VDD VDD
                          PMOS L=2 W=20
*start-up stuff
MSU1 Vsur
          Vbiasn 0
                     0
                           NMOS L=1 W=10
         Vsur
MSU2 Vsur
                VDD VDD
                          PMOS L=20 W=10
MSU3 Vbiasp Vsur
               Vbiasn 0
                          NMOS L=1 W=10
```

.ends

**26.5** Verify, using simulations, that the circuit in Fig. 26.9 does indeed amplify the difference between  $V_{biasp}$  and the average on the + inputs of the amplifier. Common on the operation of the circuit, making sure it is clear that the limitations, uses, and operation of the amplifier are understood. - Joey Yurgelon



### **Circuit Operation:**

• When the two inputs  $(V_{om} \text{ and } V_{op})$  are equal to  $V_{biasp}$  there exists 20 uA flowing through M2, and 10 uA flowing in M1/M6 due to their halved widths. When the average of the two inputs increase, the current in M5 begins to decrease due to the reduced  $V_{sg}$  voltages on the inputs. This reduction in  $V_{sg}$  causes the current in M5 to decrease, and subsequently, increase the current in the M2 branch. This, increase in current, will drive  $V_{CMFB}$  upwards in an attempted to pull the outputs of the diff. amp back to  $V_{biasp}$ 

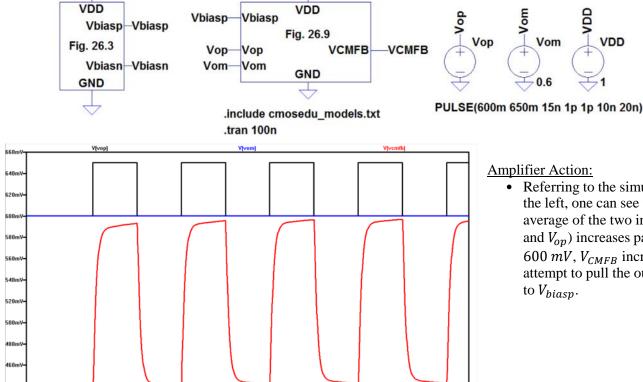
### **Circuit Limitations:**

VDD

10ns

20ns

• Two issues become apparent with this design. As with any system with feedback, we have to take notice of stability. In this case, capacitors may need to be added at the outputs of the diff. amp to help compensate the CMFB loop. The other issue exists with the limited input common-mode range. Notice that the inputs are connected to PMOS devices. If one input strays past the other with a certain  $V_{OS}$ , we will see one of the PMOS devices shut off preventing proper amplifier action.



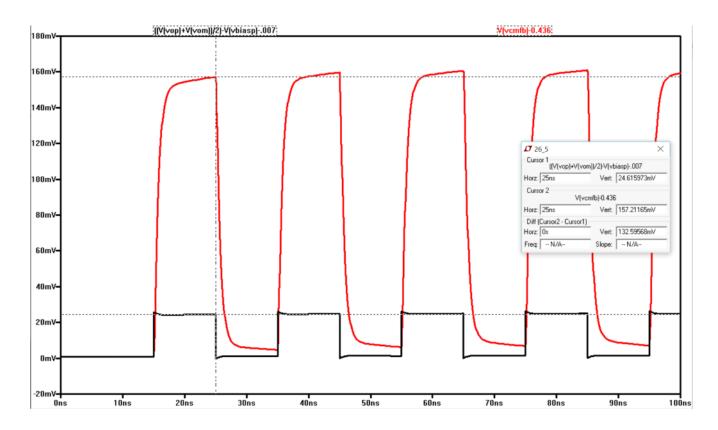
VDD

Referring to the simulation to the left, one can see that when average of the two inputs  $(V_{om})$ and  $V_{op}$ ) increases past  $V_{biasp}$  at  $600 \, mV, \, V_{CMFB}$  increases in an attempt to pull the outputs back

60ns

50ns

40ns



• To further illustrate the amplification action, one can see to left that with a 50 mV pulse on one of the inputs, we see an average of around 25 mV between the two inputs. This is then amplified by the CMFB amplifier by roughtly x6.5.

Problem 26.6 Kostas Moutafis

Simulate the operation of the CMFB circuit in Fig 26.16

### **Solution:**

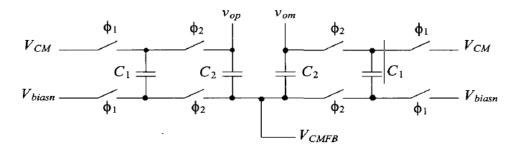


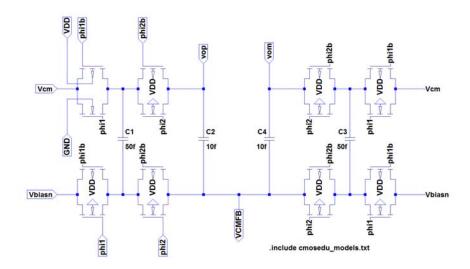
Figure 26.16: A switched-capacitor CMFB circuit.

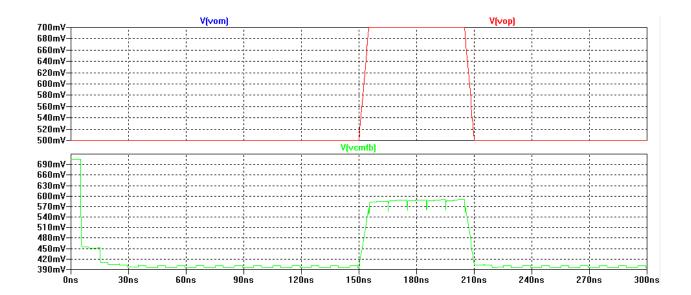
 $V_{CMFB}$  will go to the tail of the amplifier. When  $(V_{op} + V_{om})/2$  is getting higher than  $V_{CM}$  (here 500mV),  $V_{CMFB}$  will go up trying to bring the output voltages of the amplifier down again.

To prove what mentioned above we will use the following spice schematic.



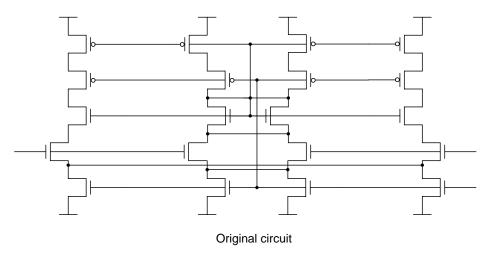
The schematic of the "SC\_CMFB\_P26.6" symbol can be seen below.



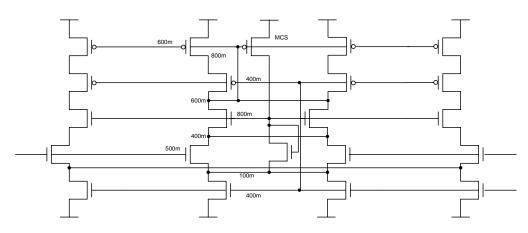


As we can see in the simulation above, at 150ns  $(V_{op} + V_{om})/2$  goes up from 500mV to 700mV resulting in  $V_{CMFB}$  going up from 400mV to 600mV. When the outputs of the amplifier come back to 500mV,  $V_{CMFB}$  will also return to its initial value.

# 26.7) Is VDD divided up evenly between the drain-source voltages of the MOSFETS in the Figure 26.19? Suggest a better method to better divide VDD between the MOSFETS used in the diff amp.



Voltage breakdown is already shown in figure 26.19



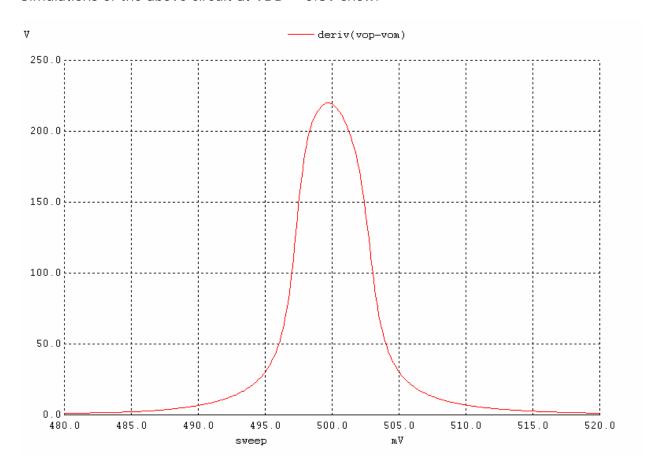
**Modified Circuit** 

Voltage breakdown at drains and gates are shown above.

By using a current source (MCS) and a diode connected transistor to set the bias points, the Vds of all transistors can be kept at 200 mV. Some would argue that this consumes more current. However, if you are making more than one opamp, then this bias point could be propagated to other amplifiers.

The original circuit didn't have an equal amount of VDD shared throughout each of the transistors. That is some the transistors had 200mV Vds, one had 400mV and the other NMOSs had 100mV of Vds. However by using the current source through a transistor an equal amount of Vds (i.e. 200mV) will across all of the Vds. This enables the opamp to work at even lower VDDs.

Simulations of the above circuit at VDD = 0.8V show:



The gain is a little bit lowered but this is somewhat expected but much better than the normal simulation at such a low VDD.

#### Problem 26.8

Suggest a simple method to speed up the step response of the op-amp in Fig. 26.22 in the circuit seen in Fig. 26.24. Verify the validity of your suggestion using SPICE simulations.

A simple method for decreasing the step-response time is to increase the gate width of the transistors of both the input diff-pairs and also the output buffers. The original simulation shows:

Figure 1: Original Simulation of Large Signal Step-Response

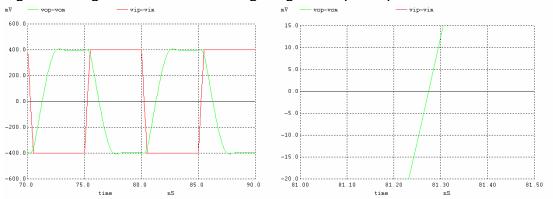
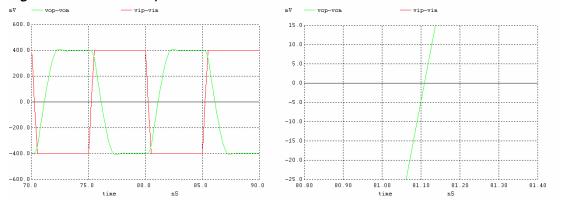
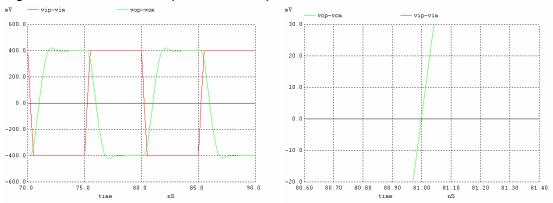


Figure 2: Widened Input FETs and Buffer FETs



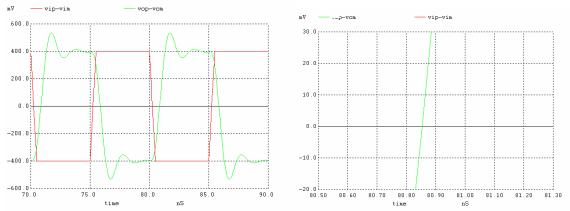
Note the zero-crossing of Figure 1 versus Figure 2. Figure 2 is approximately 200ps quicker than Figure 1. Another, and more effective, way to decrease the step time is to reduce the compensation capacitance. In this example, the capacitance was lowered from 50pF to 25pF.

Figure 3: Reduced Compensation Capacitance



The side effect of reduced step response time is ringing. For example, if the compensation capacitance was reduced to 10pF, Figure 4 would result.

Figure 4: Further Reduced Compensation Capacitance



### Kloy Debban

26.9 Suggest an alternative method to the one seen in Fig. 26.32 for controlling the output buffer's current. Using the modification regenterate the results seen in Fig. 26.36.

If we simply make M5N wider, it's output resistance is small, and the problem of the buffer drawing too much current and the outputs not reaching the rails is not solved. Alternative methods for controlling the output buffers current include, changing the gate voltage of M5N to Vcm, replacing M5N with a PMOS, or replacing M5N with a resistor. Changing M5N's gate voltage and replacing it with a PMOS, both result in a decreased output swing. Therefore we will investigate replacing M5N with a resistor. Figure 1 below is the same as 26.32 except it uses a resistor control the current in the output buffer.

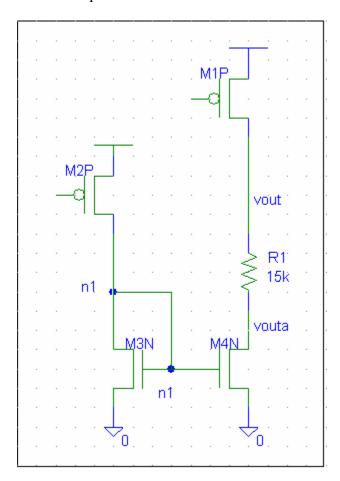
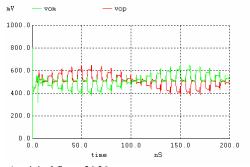
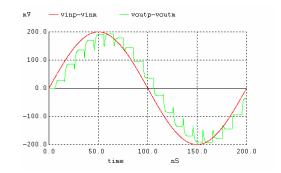


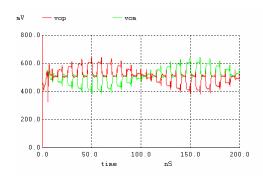
Figure 1.

M5N was replaced with a  $15k\Omega$  resistor. Below in Figure 2 is the comparison of the original figure 26.36,(a) and the one generated by replacing M5N with the  $15k\Omega$  resistor, (b.)









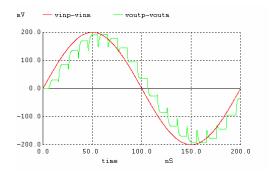


Figure 2

There is not much difference in the figures. They work pretty much the same. The only problem with adding the resistor, as opposed to the MOSFET, is that the layout area with the resistor would be larger.

***p26.9								
.control								
destroy all	destroy all							
run								
**plot phi	1+2.5 phi2-	+1.25 phi3						
plot vinp-v	vinm voutp	-voutm						
plot vop v	om							
.endc								
tran 100n	200n UIC							
options so								
vdd	vdd	0	DC	1				
vau vem	vau vcm	0	DC	500m				
VCIII	VCIII	U	DC	500111				
* clock signals								
Vphi1	phi l	0	DC	0				
	PULSE 1	0 5n 0 0 5	n 10n					
Vphi2	phi2	0	DC	0				
	PULSE 1	0 5.2n 0 0	5n 10n					
Vphi3	phi3	0	DC	0				
	PULSE 0	1 5.4n 0 0 4	4n 10n					

* input sig	gnals				
vinp		0	DC	0	SIN
500m 100		5MEG	D.C.	0	CDI
vinm		0 5MEC	DC	0	SIN
500m -100	Jm	5MEG			
* op-amp	call				
xopamp	vop	vom	vp	vm	VDD
	vcm	opamp			
· ·,					
* capacito Ct	rs t1		250f		
Cb	b1	vm	250f		
Cb	D1	vp	2301		
Coutp	voutp	0	250f		
Coutm	voutm	0	250f		
	T switches				
M1	vinp		t1	0	
	NMOS L=				
M2	vinm		b1	0	
	NMOS L=	=1 W=10			
M3	t1	nhi3	vop	0	
1413	NMOS L=		vop	U	
M4	b1		vom	0	
	NMOS L=		. 0111	-	

b.) M5N is replace by the  $15k\Omega$  resistor.

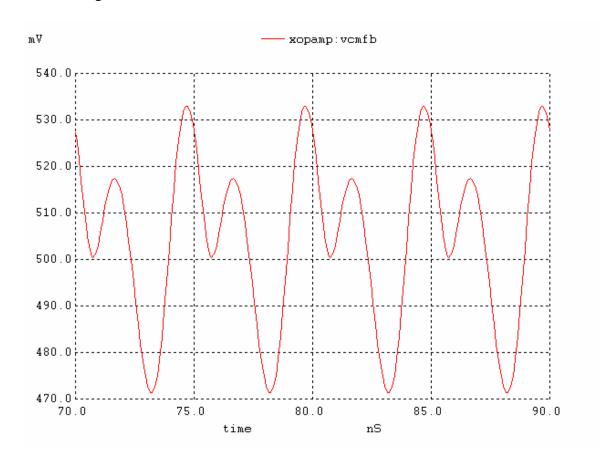
M5	vm	phi l	vop	0		M4R	n2R vm NMOS L=1 W=10	nlt	0
M6	NMOS L=	=1 W=10 phi1	vom	0		M5R	n3 n3 NMOS L=1 W=10	n2	0
1.10	NMOS L	1	, 0111	v		M6R	vop n3 NMOS L=1 W=10	n2R	0
M7	vop NMOS L=	phi3	voutp	0		M7R	n3 vbiasn PMOS L=1 W=20	n4	VDD
M8	vom NMOS L=	phi3	voutm	0		M8R	vop vbiasn PMOS L=1 W=20	n4R	VDD
* op-amp		1 11 10				M9R	n4 n3 PMOS L=1 W=20	VDD	VDD
1 1						M10R	n4R n3	VDD	VDD
.subckt op	VDD	vop vcm	vom	vp	vm		PMOS L=1 W=20		
Xbias Xdiffamp	vbiasn	vbiasp vom1	VDD	bias vm		M1L	n1b vbiasn NMOS L=1 W=10	0	0
Aumamp	vbiasn diffamp	cr	vp cl	vemfb	vdd	M2L	nlt vbiasn NMOS L=1 W=10	0	0
Xbuffr Xbuffl	vop1 vom1	vom1	vom	VDD VDD	buff buff	M3L	n2 vp NMOS L=1 W=10	n1b	0
cc1	vom	vop1 cr	vop 50f	VDD	oun	M4L	n2L vp	nlt	0
cc2 xcmfb	vop vop	cl vom	50f vcm	vcmfb		M5L	NMOS L=1 W=10 n3 n3	n2	0
.ends	vbiasp	vdd	cmfb			M6L	NMOS L=1 W=10 vom n3	n2L	0
.subckt cr		vop	vom	vcm		M7L	NMOS L=1 W=10 n3 vbiasn	n4	VDD
Ra1	vemfb vop	vbiasp vdd vcma	l 20k			M8L	PMOS L=1 W=20 vom vbiasn	n4L	VDD
Ca1 Ra2	vop vom	vema vema	10f 20k			M9L	PMOS L=1 W=20 n4 n3	VDD	VDD
Ca2	vom	vema	10f			M10L	PMOS L=1 W=20 n4L n3	VDD	VDD
Mp1	vss PMOS L=	vbiasp 1 W=20	VDD	VDD		.ends	PMOS L=1 W=20		
Mp2	n1 PMOS L=	vcma 1 W=20	VSS	VDD					
Mp3	vcmfb PMOS L=	vcm 1 W=20	VSS	VDD		.subckt bia	s vbiasn vbiasp VDD		
Mn1	n1 NMOS L=	n1	0	0		M1	Vbiasn Vbiasn NMOS L=1 W=10	0	0
Mn2			0	0		M2	Vreg Vreg	Vr	0
	vemfb NMOS I =	n1 =1 W=10	Ü			1412			
.ends	vemfb NMOS L=					M3	NMOS L=1 W=40 Vbiasn Vbiasp	VDD	VDD
			vm	vout	VDD		NMOS L=1 W=40 Vbiasn Vbiasp PMOS L=1 W=20 Vreg Vbiasp	VDD VDD	VDD VDD
.ends	NMOS L=	=1 W=10 vp vp		vout VDD	VDD	M3 M4 Rbias	NMOS L=1 W=40 Vbiasn Vbiasp PMOS L=1 W=20 Vreg Vbiasp PMOS L=1 W=20 Vr 0		
.ends	buff  vout PMOS L=	vp vp vp vp vw=1 W=40 vm	vm		VDD	M3 M4	NMOS L=1 W=40 Vbiasn Vbiasp PMOS L=1 W=20 Vreg Vbiasp PMOS L=1 W=20 Vr 0	VDD	
.ends .subckt M1p	buff vout PMOS L= n1 PMOS L= n1	vp vp vp:1 W=40 vm :1 W=20 n1	vm VDD	VDD	VDD	M3 M4 Rbias *amplifier	NMOS L=1 W=40 Vbiasn Vbiasp PMOS L=1 W=20 Vreg Vbiasp PMOS L=1 W=20 Vr 0  Vamp Vreg NMOS L=2 W=10 Vbiasp Vbiasn	VDD 4k	VDD
.ends .subckt M1p M2p	buff  vout PMOS L= n1 PMOS L= n1 NMOS L= vouta	vp vp vp vl W=40 vm vl W=20 n1 =1 W=10 n1	vm VDD VDD	VDD VDD	VDD	M3 M4 Rbias *amplifier MA1	NMOS L=1 W=40 Vbiasn Vbiasp PMOS L=1 W=20 Vreg Vbiasp PMOS L=1 W=20 Vr 0  Vamp Vreg NMOS L=2 W=10 Vbiasp Vbiasn NMOS L=2 W=10 Vamp Vamp Vamp Vamp	VDD 4k 0	VDD 0
.ends .subckt M1p M2p M3n	buff  vout PMOS L= n1 PMOS L= n1 NMOS L= vouta NMOS L= vout	vp vp vp v1 W=40 vm v1 W=20 n1 =1 W=10 n1 =1 W=20 vdd	vm VDD VDD	VDD VDD 0	VDD	M3 M4 Rbias *amplifier MA1 MA2	NMOS L=1 W=40 Vbiasn Vbiasp PMOS L=1 W=20 Vreg Vbiasp PMOS L=1 W=20 Vr 0  Vamp Vreg NMOS L=2 W=10 Vbiasp Vbiasn NMOS L=2 W=10 Vamp Vamp PMOS L=2 W=20 Vbiasp Vamp PMOS L=2 W=20 Vbiasp Vamp	VDD 4k 0	VDD 0 0
.ends .subckt M1p M2p M3n M4n **M5n	buff  vout PMOS L= n1 PMOS L= n1 NMOS L= vouta NMOS L= vout NMOS L=	vp vp vp v1 W=40 vm v1 W=20 n1 =1 W=10 n1 =1 W=20 vdd	vm VDD VDD 0	VDD VDD 0	VDD	M3 M4 Rbias *amplifier MA1 MA2 MA3 MA4	NMOS L=1 W=40 Vbiasn Vbiasp PMOS L=1 W=20 Vreg Vbiasp PMOS L=1 W=20 Vr 0  Vamp Vreg NMOS L=2 W=10 Vbiasp Vbiasn NMOS L=2 W=10 Vamp Vamp PMOS L=2 W=20 Vbiasp Vamp PMOS L=2 W=20 Vbiasp Vamp PMOS L=2 W=20	VDD 4k 0 0 VDD	VDD  0 0 VDD
.ends .subckt M1p M2p M3n M4n	buff  vout PMOS L= n1 PMOS L= n1 NMOS L= vouta NMOS L= vout NMOS L=	vp vp vp v1 W=40 vm v1 W=20 n1 =1 W=10 n1 =1 W=20 vdd	vm VDD VDD 0	VDD VDD 0	VDD	M3 M4 Rbias *amplifier MA1 MA2 MA3	NMOS L=1 W=40 Vbiasn Vbiasp PMOS L=1 W=20 Vreg Vbiasp PMOS L=1 W=20 Vr 0  Vamp Vreg NMOS L=2 W=10 Vbiasp Vbiasn NMOS L=2 W=10 Vamp Vamp PMOS L=2 W=20 Vbiasp Vamp PMOS L=2 W=20 Vbiasp Vamp PMOS L=2 W=20	VDD 4k 0 0 VDD	VDD  0 0 VDD
.ends .subckt M1p M2p M3n M4n **M5n	buff  vout PMOS L= n1 PMOS L= n1 NMOS L= vouta NMOS L= vout NMOS L= vouta State Vout NMOS L= vouta State Vout NMOS L= vouta 15k	vp vp vp vl W=40 vm vl W=20 n1 =1 W=10 n1 =1 W=20 vdd =1 W=10	vm VDD VDD 0 vouta	VDD VDD 0 0 0 vp	vm	M3 M4 Rbias *amplifier MA1 MA2 MA3 MA4 *start-up s	NMOS L=1 W=40 Vbiasn Vbiasp PMOS L=1 W=20 Vreg Vbiasp PMOS L=1 W=20 Vr 0  Vamp Vreg NMOS L=2 W=10 Vbiasp Vbiasn NMOS L=2 W=10 Vamp Vamp PMOS L=2 W=20 Vbiasp Vamp Vsur Vbiasn NMOS L=1 W=10 Vsur Vsur	VDD 4k 0 0 VDD VDD	VDD  0  0  VDD  VDD
.ends .subckt M1p M2p M3n M4n **M5n R1 vout .ends .subckt	buff  vout PMOS L= n1 PMOS L= n1 NMOS L= vouta NMOS L= vout NMOS L= vout Shoot	vp vp vp vl W=40 vm i-1 W=20 n1 =1 W=10 n1 =1 W=20 vdd =1 W=10	vm VDD VDD 0 0 vouta vom n2L	VDD VDD 0 0 0 vp		M3 M4 Rbias *amplifier MA1 MA2 MA3 MA4 *start-up s MSU1	NMOS L=1 W=40 Vbiasn Vbiasp PMOS L=1 W=20 Vreg Vbiasp PMOS L=1 W=20 Vr 0  Vamp Vreg NMOS L=2 W=10 Vbiasp Vbiasn NMOS L=2 W=10 Vamp Vamp PMOS L=2 W=20 Vbiasp Vamp PMOS L=2 W=20 tuff Vsur Vbiasn NMOS L=1 W=10 Vsur Vsur PMOS L=20 W=10 Vbiasp Vsur	VDD 4k 0 0 VDD VDD VDD	VDD  0 0 VDD  VDD  0
.ends .subckt M1p M2p M3n M4n **M5n R1 vout .ends .subckt M1R	buff  vout PMOS L= n1 PMOS L= n1 NMOS L= vouta NMOS L= vout NMOS L= vout SMOS L= vout NMOS L=	vp vp vp vw vm vl vl vl vl vl vl vl vl vl vl vl vl vl	vm VDD VDD 0 0 vouta vom n2L 0	VDD VDD 0 0 0 vp vcmfb 0	vm	M3 M4 Rbias *amplifier MA1 MA2 MA3 MA4 *start-up s MSU1 MSU2	NMOS L=1 W=40 Vbiasn Vbiasp PMOS L=1 W=20 Vreg Vbiasp PMOS L=1 W=20 Vr 0  Vamp Vreg NMOS L=2 W=10 Vbiasp Vbiasn NMOS L=2 W=10 Vamp Vamp PMOS L=2 W=20 Vbiasp Vamp NMOS L=2 W=20 Vbiasp Vamp	VDD 4k 0 0 VDD VDD 0 VDD	VDD  0 0 VDD  VDD  0 VDD
.ends .subckt M1p M2p M3n M4n **M5n R1 vout .ends .subckt	buff  vout PMOS L= n1 PMOS L= n1 NMOS L= vouta NMOS L= vout NMOS L= vout SMOS L= vout NMOS L= vout	vp vp vp vp v1 W=40 vm v1 W=20 n1 =1 W=10 n1 =1 W=10 vdd =1 W=10 vdd =1 W=10 vop n2R vcmfb =1 W=10 vbiasn	vm VDD VDD 0 0 vouta vom n2L	VDD VDD 0 0 0 vp	vm	M3 M4 Rbias *amplifier MA1 MA2 MA3 MA4 *start-up s MSU1 MSU2 MSU3 .ends	NMOS L=1 W=40 Vbiasn Vbiasp PMOS L=1 W=20 Vreg Vbiasp PMOS L=1 W=20 Vr 0  Vamp Vreg NMOS L=2 W=10 Vbiasp Vbiasn NMOS L=2 W=10 Vamp Vamp PMOS L=2 W=20 Vbiasp Vamp PMOS L=2 W=20 tuff Vsur Vbiasn NMOS L=1 W=10 Vsur Vsur PMOS L=20 W=10 Vbiasp Vsur	VDD 4k 0 0 VDD VDD 0 VDD	VDD  0 0 VDD  VDD  0 VDD
.ends .subckt M1p M2p M3n M4n **M5n R1 vout .ends .subckt M1R	buff  vout PMOS L= n1 PMOS L= n1 NMOS L= vouta NMOS L= vout NMOS L= vout SMOS L= vout NMOS L= vout NMOS L= vout NMOS L= n1b NMOS L= n1b	vp vp vp vp vl W=40 vm vl W=20 n1 vl W=20 n1 vl W=10 vdd vdd vdd vdd vdd ver vbiasn ver ver ver vbiasn vm	vm VDD VDD 0 0 vouta vom n2L 0	VDD VDD 0 0 0 vp vcmfb 0	vm	M3 M4 Rbias *amplifier MA1 MA2 MA3 MA4 *start-up s MSU1 MSU2 MSU3 .ends	NMOS L=1 W=40 Vbiasn Vbiasp PMOS L=1 W=20 Vreg Vbiasp PMOS L=1 W=20 Vr 0  Vamp Vreg NMOS L=2 W=10 Vbiasp Vbiasn NMOS L=2 W=10 Vamp Vamp PMOS L=2 W=20 Vbiasp Vamp PMOS L=2 W=20 tuff Vsur Vbiasn NMOS L=1 W=10 Vsur Vsur PMOS L=2 W=20 Vsur Vsur NMOS L=1 W=10 Vsur Vsur PMOS L=2 W=10 Vsur Vsur PMOS L=2 W=10	VDD 4k 0 0 VDD VDD 0 VDD	VDD  0 0 VDD  VDD  0 VDD

### Problem 26.10)

Is the CMFB loop stable in the op-amp of Fig. 26.40? Use the large signal test circuit seen in Fig.26.24 ( at a slower frequency) and simulations to look at the stability of the loop. Suggest and verify with simulations methods to improve the stability of the CMFB loop.

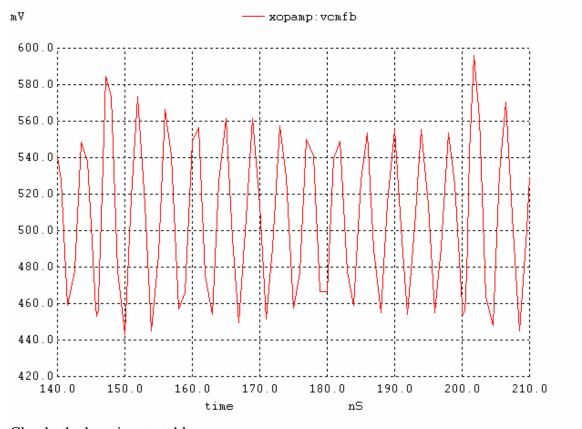
The simulation results of the opamp of Fig 26.40 are shown below.

The CMFB signal is shown below:



As we can see from the simulations the CMFB signal is bouncing all around the place and is not stable. Ideally we would like our CMFB signal to stay close to 500mV. But from the figure we see that CMFB signal is bouncing between 470mV-530mV.

At slower frequency the simulation results are shown below:



Clearly the loop is not stable.

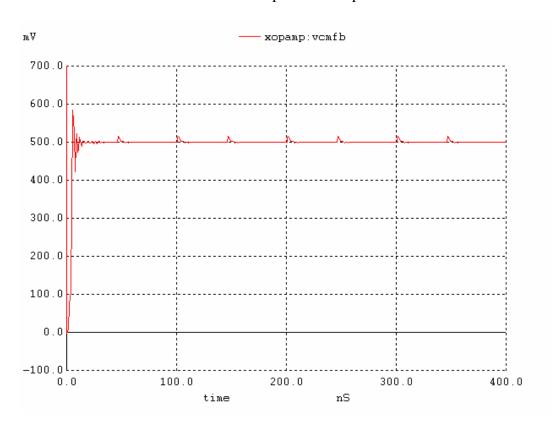
We can increase the stability of the loop by two methods.

- 1. Increase the size of compensation capacitors.
- 2. Reduce the gain of the CMFB signal by increasing the length of the MOSFET to which the CMFB signal is applied.

The disadvantages would be sluggish response, less control and slows the circuit speed.

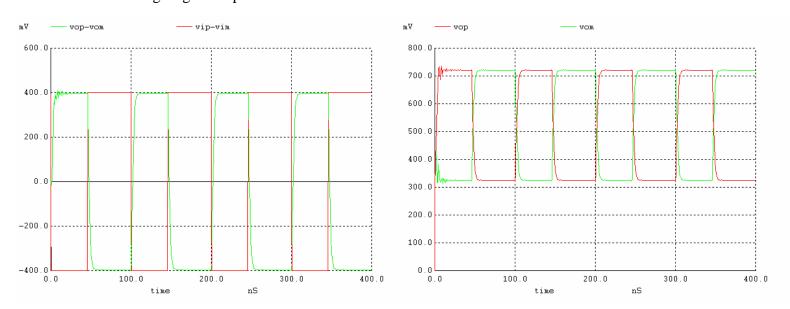
We can also look at the combination of both of the above methods inorder to stablize the loop.

The simulation results with increased compensation capacitors are shown below:

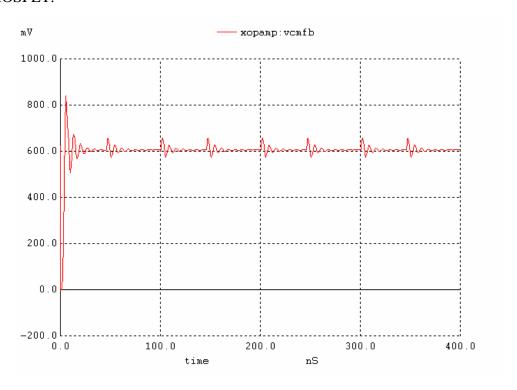


We can see that the CMFB signal is now close to the desired 500mV.

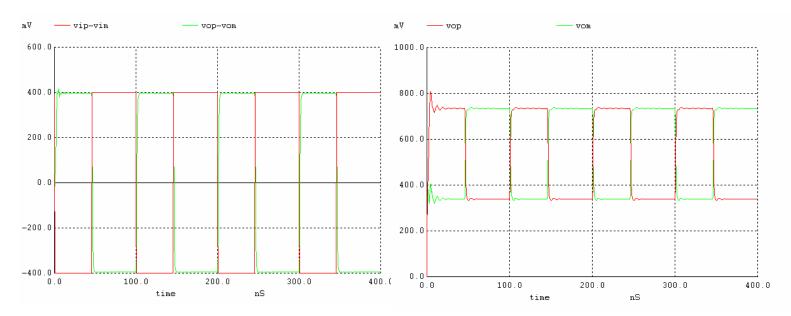
The large signal response is shown below:



Now we look at the simulation results of stabilizing the loop by increasing the length of the MOSFET.

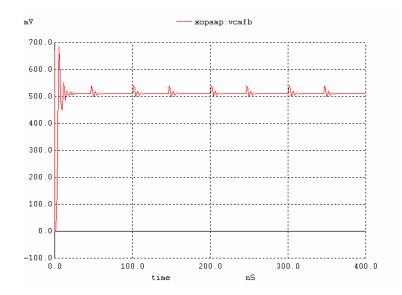


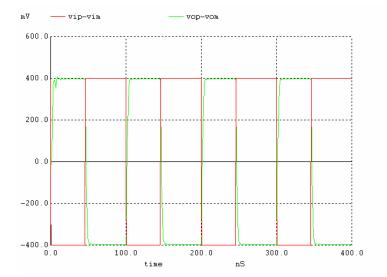
The large signal response is plotted below:

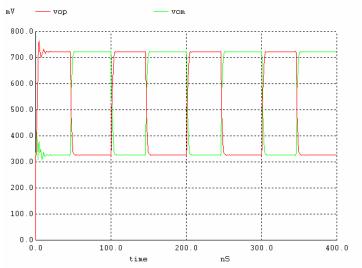


The trade off would be increase in settling time, less control. And sluggish response.

We can also use the combination of both and try to stabilize the loop. The simulation results using the combination of both of the techniques of stabilizing the loop are shown below:







Problem 26.11 Kostas Moutafis

Is the CMFB loop stable in the op-amp of Fig. 26.43? Use the large-signal test circuit seen in Fig. 26.24 (at a slower frequency) and simulations to look at the stability of this loop. Suggest, and verify with simulations, methods to improve the stability of the CMFB loop.

### **Solution:**

We will use the large-signal test circuit seen in Fig. 26.24 at a slower frequency, say 50MHz (was 100MHz), for the op-amp of Fig. 26.43.

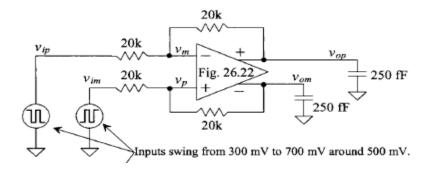


Figure 26.24: Step response of the op-amp driving 250 fF capacitors and 20k feedback resistors.

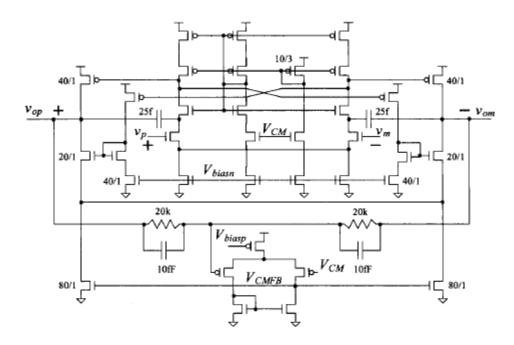
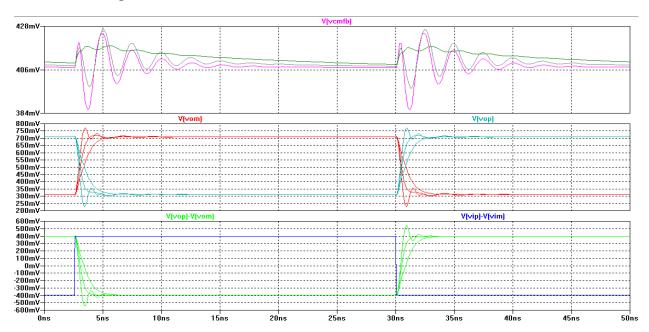


Figure 26.43 Providing CMFB through just the output buffer.

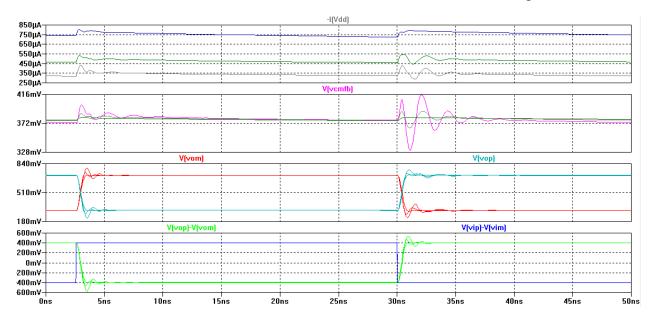
As we can see in Fig.26.43,  $V_{CMFB}$  is used as gate voltage for the triode-operating NMOS devices at the output buffer of the amplifier. The compensation capacitors have been reduced from 50fF to 25fF, because the forward differential path compensation doesn't include the CMFB path.

Our circuit is stable, but can get even more stable if we increase the values of the compensation capacitors back to 50fF. This increase may not be needed if there are not any process shifts and temperature variations, but it's always better to overcompensate than having an unstable op-amp.

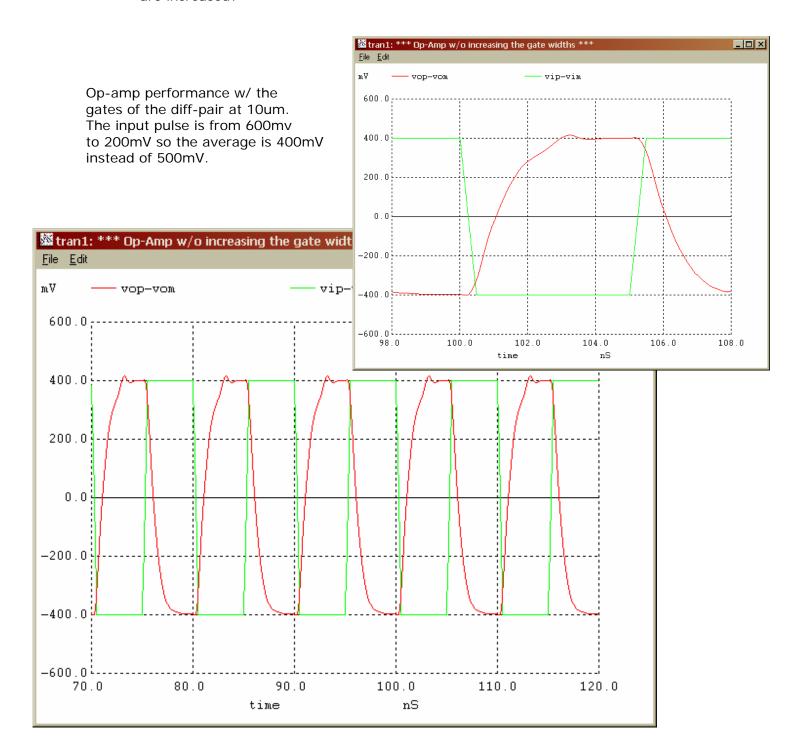
In the following simulations we see the individual output signals as well as the differential ones. We also see the differential inputs and the CMFB signal for C = 10fF, 25fF and 50fF. It is clear that as the compensate capacitor increases the circuit becomes more stable at the cost of increased settling time.

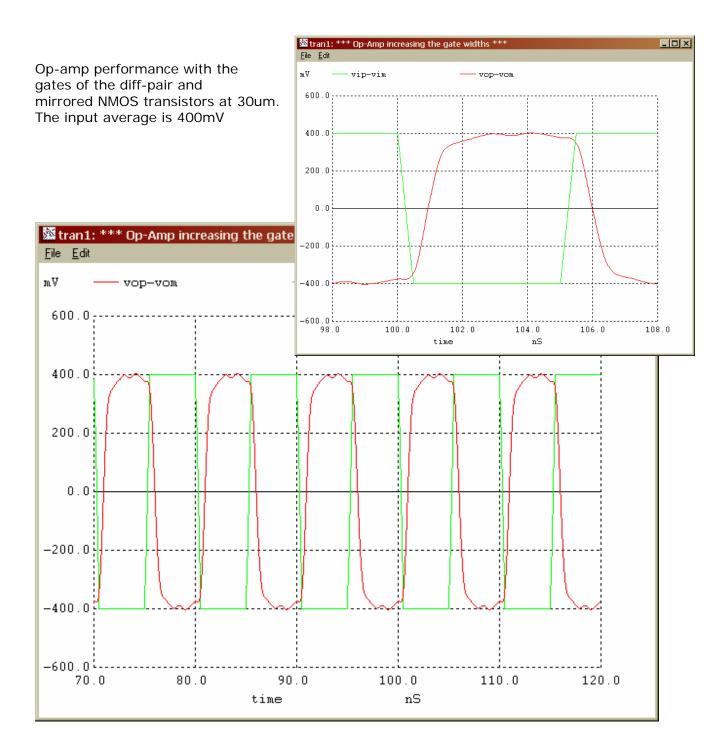


Another way to increase stability is to increase the widths at the output buffer of our amplifier. In the following simulation we change the compensation capacitor to 10fF (was 25fF) and we compare the stability performance of our circuit for widths multiplied by 1, 2 and 4. As we can see in the simulation below we make our circuit more stable at the cost of extra power.

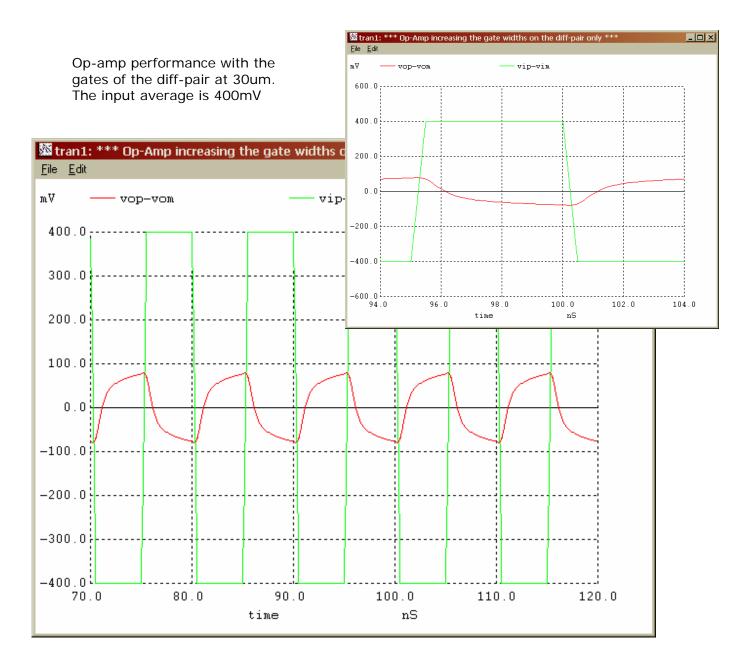


26.12) As discussed at the end of the chapter, Fig.26.59 and the associated discussion, the input common-mode voltage dropping below  $V_{\text{CM}}$  can shut off the op-amp's input diff-amp and cause problems. The diff-amp's NMOS devices have a nominal  $V_{\text{GS}}$  of 400 mV leaving only 100mV across the diff-amp's tail current. Show, using the op-amp in Fig.26.39 in the configuration seen in Fig. 26.24 with an input common-mode voltage less than 500 mV (the input pulse waveforms average to a voltage less than VCM), the resulting problems. Show that increasing the widths of the NMOS diff-pair (and the mirrored NMOS in the bias circuit with gates tied to  $V_{\text{CM}}$ ) from 10 to 30 helps to increase the operating range (four MOSFET's width's are increased from 10 to 30). What happens if only the diff-pair's widths (two MOSFETs) are increased?





We can see that we get better performance from the op-amp by reducing the Vgs of the diff-pair.



By only increasing the widths of the diff-pair we see that the outputs can't swing full rail and the diff-pair has moved into the triode region. By increasing both the diff-pairs width along with the current mirror this allows the drains and sources of the biasing circuit to adjust to the appropriate level.

\*\*\* Op-Amp Performance \*\*\* .control destroy all run plot vop-vom vip-vim .endc .option scale=50n rshunt=1e11 .tran 100p 120n 70n 100p UIC VDD VDD 0 DC vcm vcm 0 DC 500m 0 DC PULSE 600m 200m 0 500p 500p 4.5n 10n vip vip 0 vim DC 0 PULSE 200m 600m 0 500p 500p 4.5n 10n vim 0 Rf1 20k vop vm Rf2 20k vom vp Ri1 vip vm 20k Ri2 20k vim νp 250f Clr vop 0 cll vom 250f VDD xopamp vop vom vρ vm vcm opamp .subckt opamp vop vom νp vm VDD vcm Xbias vbiasn vbiasp **VDD** bias Xdiffampvop1 vom1 vm vcmfb vbiasn cl vdd diffamp vp cr vcm VDD buff Xbuffr vop1 vom1 vom Xbuffl VDD buff vom1 vop1 vop cc1 vom cr 50f cc2 vop cl 50f vbiasp vdd cmfb xcmfb vop vom vcmfb vcm .ends .subckt cmfb vop vom vcm vcmfb vbiasp vdd Ra1 vcma 20k vop Ca1 vop vcma 10f Ra2 20k vom vcma Ca2 vom vcma 10f VDD PMOS L=1 W=20 VDD Mp1 VSS vbiasp Mp2 n1 vcma VSS VDD PMOS L=1 W=20 Mp3 vcmfb vcm VSS VDD PMOS L=1 W=20 Mn1 0 NMOS L=1 W=10 n1 n1 0 Mn2 vcmfb 0 NMOS L=1 W=10 n1 0 .ends .subckt buff vout VDD vm vp vout VDD VDD PMOS L=1 W=40 M1p vp VDD PMOS L=1 W=20 М2р n1 vm **VDD** M3n 0 NMOS L=1 W=10 n1 0 n1 M4n vout vdd n2 0 NMOS L=1 W=10 0 NMOS L=1 W=20 M5n n2 n1 0 .ends

.subckt diffamp vop

vom

vp

vm

vcmfb vbiasn n2R

n2L

vcm

vdd

M2R	n1t	vbiasn	0	0	NMOS L=1 W=10
M4R	n2R	vm	n1t	0	NMOS L=1 W=10
M6R	vop	vws	n2R	0	NMOS L=1 W=10
M8R	vop	vbiasn	n4R	VDD	PMOS L=1 W=20
M10R	n4R	vws	VDD	VDD	PMOS L=1 W=20
M1R	n1ws	vcmfb	0	0	NMOS L=1 W=10
M1L	n1ws	vbiasn	0	0	NMOS L=1 W=10
M3R	n2ws	vcm	n1ws	0	NMOS L=1 W=10
M3L	n2ws	vcm	n1ws	0	NMOS L=1 W=10
M5R	vws	vws	n2ws	0	NMOS L=1 W=10
M5L	vws	vws	n2ws	0	NMOS L=1 W=10
M7R	vws	vbiasn	vd7	VDD	PMOS L=1 W=20
M7L	vws	vbiasn	vd7	VDD	PMOS L=1 W=20
M9R	vd7	vws	VDD	VDD	PMOS L=1 W=20
M9L	vd7	vws	VDD	VDD	PMOS L=1 W=20
M2L	n1t	vbiasn	0	0	NMOS L=1 W=10
M4L	n2L	vp	n1t	0	NMOS L=1 W=10
M6L	vom	vws	n2L	0	NMOS L=1 W=10
M8L	vom	vbiasn	n4L	VDD	PMOS L=1 W=20
M10L	n4L	vws	VDD	VDD	PMOS L=1 W=20
.ends					
.subckt	bias vbia	sn vbiasp	VDD		
M1	Vbiasn	Vbiasn	0	0	NMOS L=1 W=10
M2	Vreg	Vreg	Vr	0	NMOS L=1 W=40
M3	Vbiasn	Vbiasp	VDD	VDD	PMOS L=1 W=20
M4	Vreg	Vbiasp	VDD	VDD	PMOS L=1 W=20
Rbias	Vr	0	4k		
*amplifi MA1 MA2 MA3 MA4	er Vamp Vbiasp Vamp Vbiasp	Vreg Vbiasn Vamp Vamp	0 0 VDD VDD	0 0 VDD VDD	NMOS L=2 W=10 NMOS L=2 W=10 PMOS L=2 W=20 PMOS L=2 W=20
*start-u MSU1 MSU2 MSU3	p stuff Vsur Vsur Vbiasp	Vbiasn Vsur Vsur	0 VDD Vbiasn	0 VDD 0	NMOS L=1 W=10 PMOS L=20 W=10 NMOS L=1 W=10

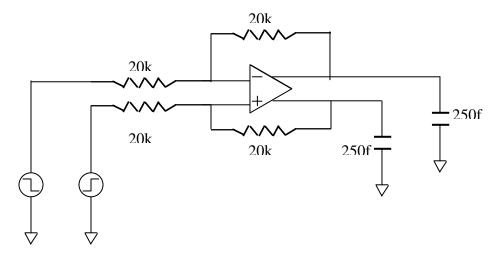
.ends

## 26.13) Repeat problem 26.12 for the op-amp in Fig 26.40. What happens if the input common-mode voltage becomes greater than 500mV?

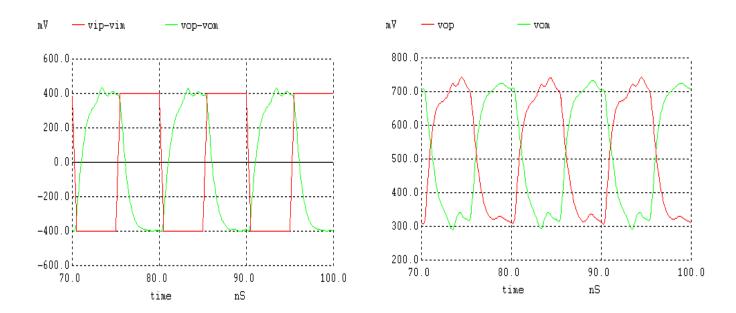
### Soln[Ravi]:

When the input common-mode voltage drops below  $V_{CM}$ , the voltage across diffamp's tail current [in the two external paths] drops. When the common-mode voltage reaches 400 mV, the diff-amp's NMOS devices fail to maintain the same current as in other branches and this causes problems.

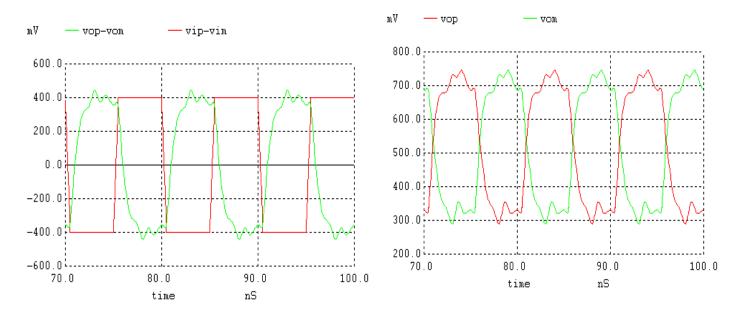
The op-amp in Fig. 26.40 is used in the following configuration.



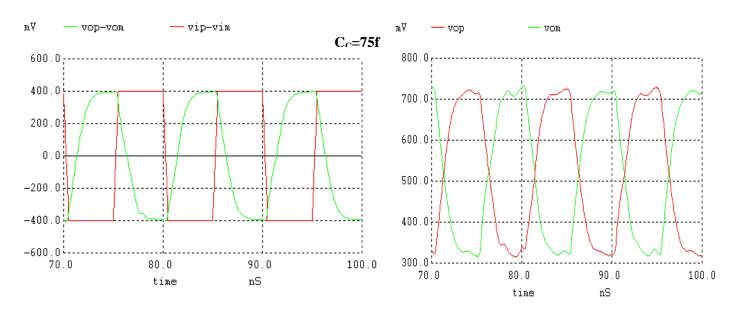
The gain of the CMFB circuit in fig. 26.40 is reduced for stability concerns in all the simulations shown below. With input common-mode voltage of 400mV [inputs swinging from 300mV to 500mV], the step response of the opamp is shown below.



The step response with increasing the widths of the NMOS diff-pair and the mirrored NMOS from 10 to 30 is shown below.[inputs swinging from 200mV to 600mV]



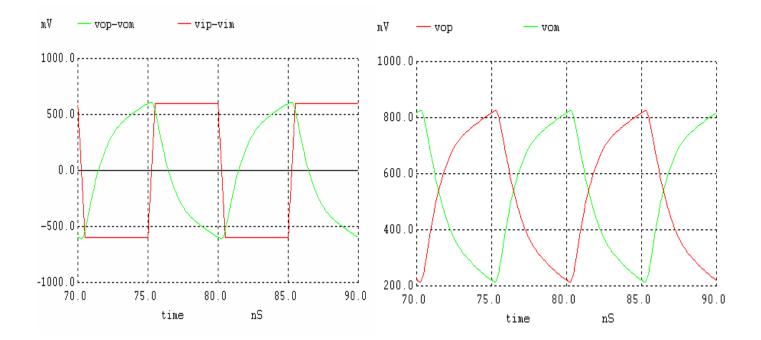
Increasing the widths of the NMOS increases their  $g_m$  values and hence the unity gain frequency is further pushed to the right in the frequency response, reducing the phase margin [unstable]. Below is the step response with a *compensation capacitor of 75f* [increases stability of the op-amp].



Clearly the op-amp is response has improved with increasing the widths of the four NMOS.

If we increase the widths of the two NMOS diff-pair only from 10 to 30, then the diff-pair will move into triode region. So, the biasing circuit will not work properly.

The step-response of the op-amp when the input common-mode voltage is greater than 500mV is shown below. The input is swinging from 300mV to 900mV [common mode voltage of 600mV].



### **NETLIST**

\*\*\* Prob 26.13 \*\*\*

```
.control
destroy all
run
plot vop vom
plot vip-vim vop-vom
.endc
.option scale=50n
.tran 100p 100n 70n 100p UIC
VDD
       VDD
               0
                      DC
                              1
vcm
       vcm
               0
                      DC
                              500m
               0
                      DC
                              0
                                     PULSE 900m 300m 0 500p 500p 4.5n 10n
vip
       vip
                                     PULSE 300m 900m 0 500p 500p 4.5n 10n
vim
       vim
               0
                      DC
                              0
                      20k
Rf1
       vop
               vm
Rf2
                      20k
       vom
               vp
Ri1
                      20k
       vip
               vm
Ri2
       vim
               vp
                      20k
Clr
       vop
               0
                      250f
cll
       vom
               0
                      250f
xopamp vop
                      vp
                              vm
                                     VDD
                                             vcm
                                                    opamp
               vom
.subckt opamp
                                             VDD
                                                    vcm
               vop
                      vom
                                     vm
                              vp
Xbias
       vbiasn
               vbiasp
                      VDD
                              bias
Xdiffamp
               vop1
                      vom1
                                             vbiasn cr
                                                            cl
                                                                    vemfb vem
                                                                                   vdd
                              vp
                                     vm
       diffamp
Xbuffr vop1
                      vom
                              VDD
                                     buff
               vom1
                              VDD
Xbuffl vom1
               vop1
                                     buff
                      vop
cc1
                      50f
       vom
               cr
                      50f
cc2
       vop
               cl
                                     vbiasp
xcmfb
       vop
               vom
                      vcm
                              vcmfb
                                             vdd
                                                    cmfb
.ends
.subckt cmfb
               vop
                      vom
                              vcm
                                     vcmfb
                                             vbiasp vdd
Ra1
       vop
               vcma
                      20k
Ca1
                      10f
       vop
               vcma
                      20k
Ra2
       vom
               vcma
Ca2
               vcma
                      10f
       vom
                              VDD
                                     PMOS L=1 W=40
Mp1
                      VDD
               vbiasp
       VSS
Mp2
       n1
               vcma
                      VSS
                              VDD
                                     PMOS L=1 W=40
Mp3
       vcmfb
                              VDD
                                     PMOS L=1 W=40
               vcm
                      VSS
Mn1
                      0
                              0
                                     NMOS L=1 W=20
       n1
               n1
Mn2
       vcmfb
               n1
                      0
                              0
                                     NMOS L=1 W=20
.ends
.subckt buff
                                     VDD
               vp
                      vm
                              vout
                              VDD
                                     PMOS L=1 W=40
M1p
       vout
                      VDD
               vp
M2p
       n1
               vm
                      VDD
                              VDD
                                     PMOS L=1 W=20
M3n
       n1
               n1
                      0
                              0
                                     NMOS L=1 W=10
M4n
                      0
                              0
                                     NMOS L=1 W=20
       vouta
               n1
                                     NMOS L=1 W=10
M5n
       vout
               vdd
                      vouta
                              0
```

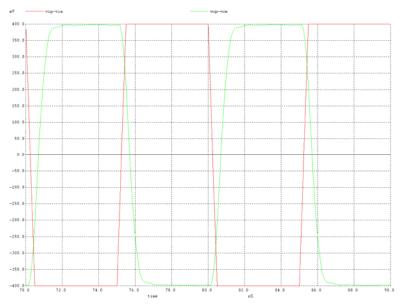
.subckt	diffamp	vop	vom	vp	vm	vbiasn	n2R	n2L	vemfb	vcm	vdd
M2R M4R M6R M8R M10R	n1t n2R vop vop n4R	vbiasn vm n3 vws n3	0 n1t n2R n4R VDD	0 0 0 VDD VDD	NMOS I NMOS I PMOS I	L=1 W=1 L=1 W=1 L=1 W=1 L=1 W=2 L=1 W=2	0 0 0				
M1R M1LL M1LR M3R M3L M5L M7R M7L M9L	n1ws n1b n1b vws n2 n3 vws n3	vbiasn vcmfb vbiasn vcm vcm n3 vws vws n3	0 0 0 n1ws n1b n2 VDD n4 VDD	0 0 0 0 0 0 VDD VDD VDD	NMOS I NMOS I NMOS I NMOS I PMOS I PMOS I	L=1 W=1 L=2 W=1 L=2 W=1 L=1 W=1 L=1 W=1 L=3 W=1 L=1 W=2 L=1 W=2	0 0 0 0 0 0				
M2L M4L M6L M8L M10L	n1t n2L vom vom n4L	vbiasn vp n3 vws n3	0 n1t n2L n4L VDD	0 0 0 VDD VDD	NMOS I NMOS I PMOS I	L=1 W=1 L=1 W=1 L=1 W=1 L=1 W=2 L=1 W=2	0 0 0				
.ends											
.subckt l	oias vbias	sn vbiasp	VDD								
M1 M2 M3 M4	Vreg	Vbiasn Vreg Vbiasp Vbiasp	Vr VDD	0 0 VDD VDD	NMOS I PMOS I	L=1 W=1 L=1 W=4 L=1 W=2 L=1 W=2	0				
Rbias	Vr	0	4k								
*amplifi MA1 MA2 MA3 MA4	Vamp Vbiasp Vamp	Vreg Vbiasn Vamp Vamp	VDD	0 0 VDD VDD	NMOS I PMOS I	L=2 W=1 L=2 W=1 L=2 W=2 L=2 W=2	0				
*start-up MSU1 MSU2 MSU3	Vsur	Vbiasn Vsur Vsur	0 VDD Vbiasn	0 VDD 0	PMOS I	L=1 W= L=20 W= L=1 W=	=10				

.end

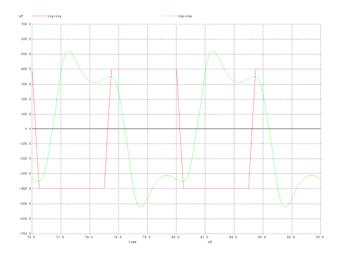
\* 50nm BSIM4 models

Repeat problem 26.12 for the op-amp in Fig. 26.43. What happens if the input common-mode voltage becomes greater than 500 mV? Why does the op-amp in Fig. 26.40 perform better with variations in the input common-mode voltage than the op-amp in Fig. 26.43?

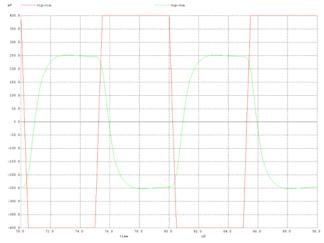
As mentioned in the problem and the discussion associated with Fig. 26.59, we know that when the input common-mode voltage goes well below 500 mV the diff-amp will not work properly and will result in unreliable output. To further analyze this on the circuit seen in figure 26.43, lets look at the large signal response. First let's run the circuit with the input common-mode at 500 mV.



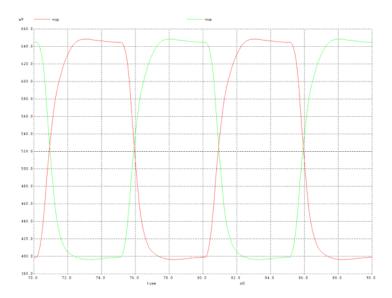
In the figure above, we see the output differential signal settling to the approximately the desired value in about 3 nS. Now let's drop the input common-mode below 500 mV. In the figure below we see that there is overshoot on the output differential signal. If we continue to drop the common-mode input voltage we will continue to see the overshoot and also the value that the output settles to is below the desired voltage. This is because the tail mosfets will move into triode and possibly even the current source transistors. This will lessen the current drive of the op-amp.



If we move in the other direction with the common-mode voltage going above 500 mV we get the behavior seen in the figure below.

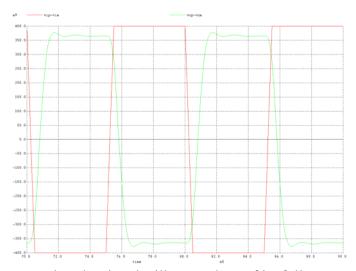


In the figure above we see that when the input common-mode voltage is above 500 mV the output doesn't achieve full levels. If we apply opposing input signals with values varying from 800mV to 400 mV we get the output signals seen in the following plot.

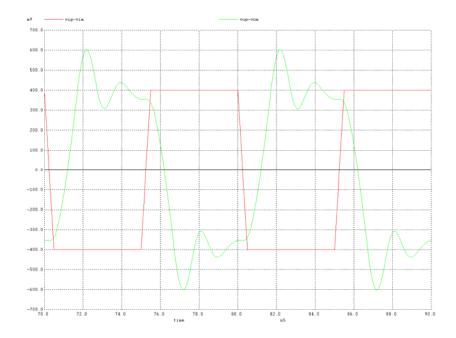


We see that the output does go to 400 mV but doesn't reach 800 mV and is clamped at  $\sim 650 \text{ mV}$ .

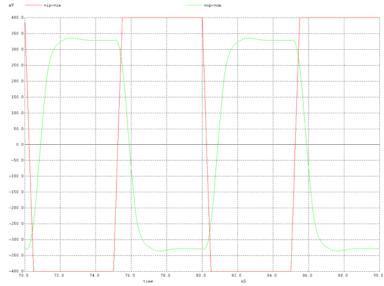
If we increase the width of the diff-amp pair from 10 to 30 as well as the mirrored NMOS of the bias circuit, we get the following plot when the input common-mode is above 500 mV.



This is an improvement but the signal still stops short of its full expected value. The wider widths still don't help when the input common mode is below 500 mV as seen in the figure below. In fact the overshoot appears to be worse.



If we only increase the widths of the diff-amp and not the mirrored bias transistors we significantly reduce the overshoot but have a lower final value. (Vcm input < 500 mV)



If only the diff-amp pair widths are increased when the input common-mode is above 500 mV the output signal is drastically reduced.

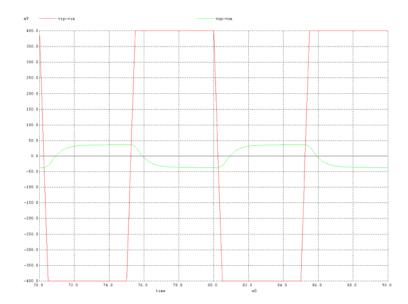


Figure 26.40 will respond better to variations on the input common-mode because it has common-mode feedback directly to the bias circuit whereas the circuit in figure 26.43 has the common mode feedback through the output buffer. This allows the outputs of the diff-amp to have more control on the PMOS transistors in the output buffer.

### **Problem 26.15**

#### **Problem:**

Design and simulate the operation of an op-amp using gain-enhancement (Fig 26.42) and having an open-loop DC gain greater than 2,000 based on the topologies seen in Figs. 26.40 and 26.43. Simulate the operation of your design and generate outputs like those seen in Fig 26.44.

#### **Solution**:

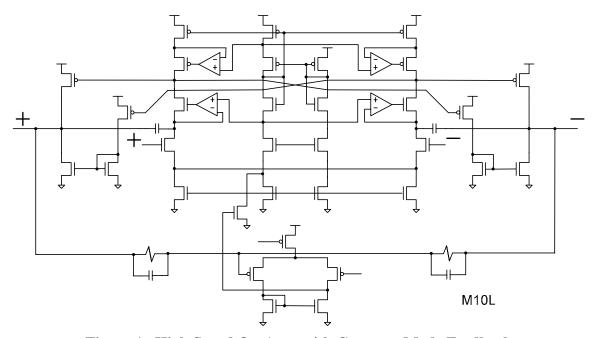


Figure 1. High Speed Op-Amp with Common Mode Feedback

M8L M7L

Figure 1 shows the addition of gain enhancement amplifiers with op-amp from Fig 26.40. The gain enhancement amplifiers effectively increase the output resistance (and thus the gain) of the diff-amp by factor of the GE amp's gain. The gain of the GE amp is on the order of 10V/V and the gain of this op-amp (see Fig 26.44) is about 400V/V. Therefore we can expect that the gain of the op-amp should be approximately 4kV/V with the GE amps added. The gain of the GE amps can be further increased without effecting the speed of the op-amp by increasing the length of these transistors (the GE amps L was increased to 4 for this design).

There are two issues to consider when using GE amps to increase the gain of any opamp. The first is power consumption. Four GE amps are needed each of which draws up to 30uA of current (a potential total increase of M30uA). The second issue is stability. M5n M4L Because of the high gain output common mode variations can easily cause the CMFB to negatively effect performance. 20% is especially a problem when the CMFB is done through the output buffer as in Fig 26.44.

To reduce the effect of CMFB on the op-amp it is a good idea to reduce the loop gain of the CMFB. Reducing the gain of the CMFB loop also helps to improve the settling M1LR time of the op-amp when the inputs are toggling. The two problems with reducing the

M1 Vbiasp

M9L

M5L

M<sub>3</sub>L

M<sub>1</sub>L

20k

gain of the CMFB are a potential output common mode offset and a slowing of the feedback response (it might not effect the outputs fast enough). Reducing the gain of the CMFB loop can be done by increasing length of transistor M1LR (notice from Fig1 that L=4 for this design).

Finally, the compensation capacitor sizing must be considered when tuning the AC response of the op-amp. If not enough compensation capacitance is present the outputs will overshoot and ring (especially when input-referred offsets are introduced). If too much compensation cap is present then the overall response will slow down and resemble an RC response. For this design 50uF caps were used to compensate the diffamp and 75uF caps were used to compensate each GE amp.

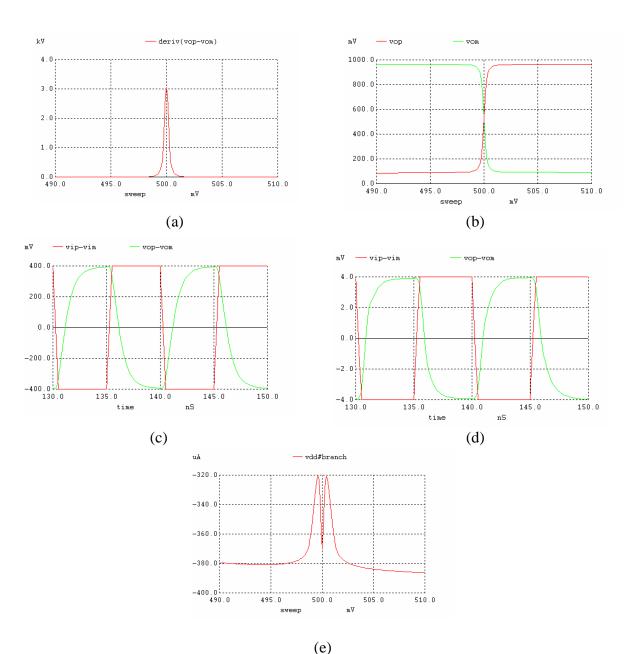


Figure 2. (a) DC Gain (b) Output Switching (c) Large AC Response (d) Small AC Response (e) Power Consumption

Fig 2a shows the open-loop DC gain of the op-amp in Fig 1. Nearly as expected the GE amps have increased the gain by a factor of 10. The gain comes in at about 3kV/V. Fig 2b shows the output switching for a linearly increasing input voltage. Notice the rail-to-rail class AB action while the inputs are switching. It is noticeable that the output common mode voltage is slightly offset from VCM (~540mV) due to the adjustments made to the CMFB loop gain. Fig 2e shows the current drawn by the entire op-amp which is not insignificantly increased from the original op-amp in Fig 26.40.

Fig 2c shows the large signal AC response of the op-amp from Fig 1. The 50% rise and fall time is much better than 1ns. Fig 2d shows the small signal AC response of this op-amp. The response is nearly identical to the large signal response with the exception that the overall swing is 4mV compared to 400mV. This is a result of effective compensation.

### **Netlist:**

*** Midterm_DC CMOS: Circuit Design, Layout, and Simulation ***											
.control destroy all run plot i(vdd) plot vop vom plot vop-vom plot deriv(vo plot xopamp: *print all *print .endc	ı p-vom)										
.option scale	=50n rshunt=1	e12									
.dc *.op **.tran 1m 1	vin UIC	490m	510m	.1m							
VDD	VDD	0	DC								
VDD vcm	VDD vcm	0	DC DC	1 500m							
vin	vin	0	DC	500m							
xopamp	vop	vom	vin	vcm	VDD	vcm	opamp				
.subckt opam	p vop	vom	vp	vm	VDD	vcm					
Xbias	vbiasn	vbiasp	VDD	bias							
Xdiffamp	vop1	vom1	vp	vm	vbiasn	vbiasp	cr	cl	vemfb vem	vdd	diffamp
Xbuffr	vop1	vom1	vom	vbiasn	vc	vemfb	VDD	buff			
Xbuffl cc1	vom1 vom	vop1 cr	vop 50f	vbiasn	vc	vemfb	VDD	buff			
cc2	vom	cl	50f								
xcmfb	vop	vom	vem	vemfb	vbiasp	vdd	cmfb				
.ends											
.subckt cmfb	vop	vom	vcm	vemfb	vbiasp vdd						
Ra1	vop	vcma	20k								
Ca1	vop	vema	10f								
Ra2	vom	vcma	20k								
Ca2	vom	vema	10f								
Mp1	vss	vbiasp	VDD	VDD	PMOS L=1	1 W=20					
Mp2	n1	vcma	VSS	VDD	PMOS L=1						
Mp3	vemfb	vcm	vss	VDD	PMOS L=1						
Mn1	n1	n1	0	0	NMOS L=						
Mn2 .ends	vemfb	n1	0	0	NMOS L=	1 W=10					
.enus											
.subckt	buff	vp	vm	vout	vbiasn	vc	vemfb	VDD			
M1p	vout	vp	VDD	VDD	PMOS L=1						
M2p	n1	vm	VDD	VDD	PMOS L=1						
M3n	n1	n1	0	0	NMOS L=						
M4n M5n	vout n2	VDD n1	n2 0	0	NMOS L= NMOS L=						
ends.	114	11.1	U	U	MINIOS L=	1 11-20					

.subckt	diffamp	vop	vom	vp	vm	vbiasn	vbiasp	n2R	n2L	vemfb vem	vdd
M2R	n1t	vbiasn	0	0	NMOS L=1	W=10					
M4R	n2R	vm	n1t	0	NMOS L=1						
M6R	vop	g6R	n2R	0	NMOS L=1						
M8R	vop	g8R	n4R	VDD	PMOS L=1						
M10R	n4R	n3	VDD	VDD	PMOS L=1						
WITOK	1141X	113	VDD	VDD	r MOS L-1	W -20					
MID		add a sec	0	0	NIMOG I I	W 10					
M1R	n1ws	vbiasn	0	0	NMOS L=1						
M1L	n1b	vbiasn	0	0	NMOS L=2						
M1LR	n1b	vemfb	0	0	NMOS L=4	W=10					
M3R	n2ws	vcm	n1ws	0	NMOS L=1	W=10					
M3L	n2	vcm	n1b	0	NMOS L=1	W=10					
M5R	vws	vws	n2ws	0	NMOS L=1						
M5L	n3	n3	n2	0	NMOS L=1						
M7R	vws	vws	VDD	VDD	PMOS L=3						
M7L	n3	vws	n4	VDD	PMOS L=1						
M9L	n4	n3	VDD	VDD	PMOS L=1	W=20					
						*** 40					
M2L	n1t	vbiasn	0	0	NMOS L=1						
M4L	n2L	vp	n1t	0	NMOS L=1	W=10					
M6L	vom	g6L	n2L	0	NMOS L=1	W=10					
M8L	vom	g8L	n4L	VDD	PMOS L=1	W=20					
M10L	n4L	n3	VDD	VDD	PMOS L=1						
- *		-				-					
XnampL	VDD	vbiasn	g8L	n4	n4L	namp					
XnampR	VDD	vbiasn	g8R	n4	n4R	namp					
XpampL	VDD	vbiasp	g6L	n2	n2L	pamp					
XpampR	VDD			n2	n2R						
мрашрк	עטי	vbiasp	g6R	114	1141	pamp					
.subckt	pamp	VDD	vbiasp	vout	vn	vm					
					vp pMOS I -4						
M1	vps	vbiasp	VDD	VDD	PMOS L=4						
M2	Vsp	vbiasp	VDD	VDD	PMOS L=4						
M3	Vms	vbiasp	VDD	VDD	PMOS L=4	W=10					
M4	0	vp	vps	VDD	PMOS L=4	W=10					
M5	n1	vps	vsp	VDD	PMOS L=4	W=10					
M6	vout	vms	vsp	VDD	PMOS L=4	W=10					
M7	0	vm	vms	VDD	PMOS L=4						
M8	n1	n1	0	0	NMOS L=4						
M9		n1	0	0							
	vout			U	NMOS L=4	W-10					
cc	vout	0	75f								
.ends											
.subckt	namp	VDD	vbiasn	vout	vp	vm					
M1	VDD	vp	vps	0	NMOS L=4						
M2	n1	n1	VDD	VDD	PMOS L=4						
M3	vout	n1	VDD	VDD	PMOS L=4						
M4	VDD	vm	vms	0	NMOS L=4						
M5	n1	vps	VSS	0	NMOS L=4						
M6	vout	vms	VSS	0	NMOS L=4	W=10					
M7	vps	vbiasn	0	0	NMOS L=4	W=10					
M8	vss	vbiasn	0	0	NMOS L=4						
M9	vms	vbiasn	0	0	NMOS L=4						
cc	vout	0	75f	*							
.ends	·out	9	7.51								
.5											
.ends											
.subckt bias v	biasn vbiasp V	'DD									
M1	Vbiasn	Vbiasn	0	0	NMOS L=1	W=10					
M2	Vreg	Vreg	Vr	0	NMOS L=1						
M3	Vbiasn	Vbiasp	VDD	VDD	PMOS L=1						
M4	Vreg	Vbiasp	VDD	VDD	PMOS L=1						
		· Omsp			1.1.00 L-1	20					
Rbias	Vr	0	4k								
*amplifier											
MA1	Vamp	Vreg	0	0	NMOS L=2						
MA2	Vbiasp	Vbiasn	0	0	NMOS L=2						
MA3	Vamp	Vamp	VDD	VDD	PMOS L=2						
MA4	Vbiasp	Vamp	VDD	VDD	PMOS L=2						
	r	r.				-					
*start-up stuff	f										
MSU1	Vsur	Vbiasn	0	0	NMOS L=1	W=10					
MSU2	Vsur	Vsur	VDD	VDD	PMOS L=20						
MSU3	Vbiasp	Vsur	Vbiasn	0	NMOS L=1						
	, ошор			~							
.ends											

## Solution to problem 26\_16:

From figure Fig: 1 shown below, the sizes of the added drain gate connected MOSFET is set to W/L = 10/50. in order to make the OP-AMP more stable feedback MOSFET(M1LL) length is increased to 3 I,e W/L = 10/3. Advantages of this op-amp is its good for lower VDD operations and disadvantage is it burns more power.

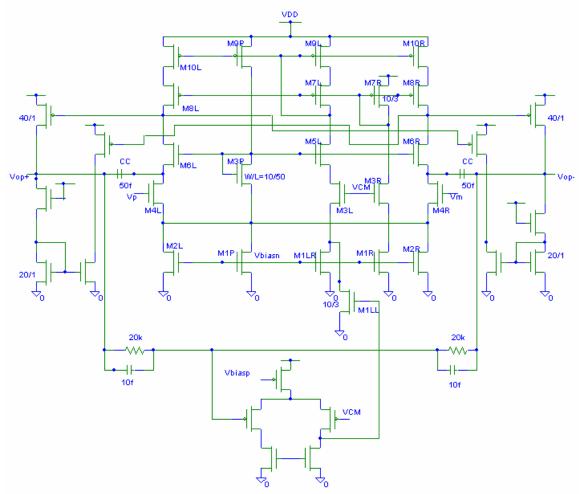


Fig:1 Op-Amp with better biasing for lower VDD operations

# Spice simulations:

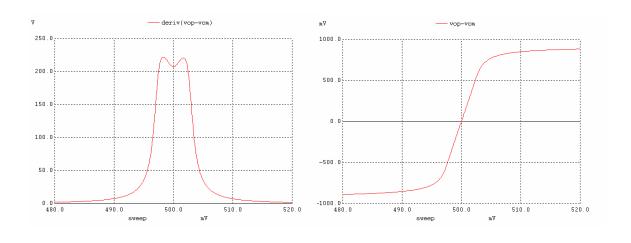
\*\*\* Problem 26.16\_DC and small signal simulations\*\*\*

```
destroy all
run
plot i(vdd)
plot vop vom
plot vop-vom
plot deriv(vop-vom)
.option scale=50n rshunt=1e9
                    480m
                              520m
.dc
         vin
                                        .1m
          VDD
                              DC
VDD
                   0
vcm
          vcm
                              DC
                                        500m
```

.control

vin	vin	0	DC	500m							
xopamp	vop	vom	vin	vcm	VDD	vcm	opamp				
.subckt op Xbias Xdiffamp Xbuffr Xbuffl cc1 cc2	vbiasn	vop vbiasp vom1 vom1 vop1 cr cl	vom VDD vp vom vop 60f 60f	vp bias vm VDD VDD	vm vbiasn buff buff	VDD cr	vcm cl	vemfb	vcm	vdd	diffamp
xcmfb .ends	vop	vom	vcm	vemfb	vbiasp	vdd	cmfb				
.subckt ci Ra1 Ca1 Ra2 Ca2	nfb vop vop vom vom	vop vcma vcma vcma vcma	vom 20k 10f 20k 10f	vem	vcmfb	vbiasp vo	dd				
Mp1 Mp2 Mp3 Mn1 Mn2	vss n1 vcmfb n1 vcmfb	vbiasp vcma vcm n1	VDD vss vss 0	VDD VDD VDD 0	PMOS L PMOS L NMOS L	=1 W=20 =1 W=20 =1 W=20 =1 W=10 =1 W=10					
.ends	1 66				I/DD						
.subckt M1p M2p M3n M4n M5n .ends	buff vout n1 n1 vouta vout	vp vp vm n1 n1 vdd	vm VDD VDD 0 0 vouta	vout VDD VDD 0 0	PMOS L NMOS L NMOS L	=1 W=40 =1 W=20 =1 W=10 =1 W=20 =1 W=10					
.subckt	diffamp	vop	vom	vp	vm	vbiasn	n2R	n2L	vcmfb	vcm	vdd
M2R M4R M6R M8R M10R M1R M1LL M1LR M1LP M3R M3P M3L M5L M7R M7L M9P M2L M4L M4L	n1t n2R vop vop n4R n1ws n1b n1ta vws n3P n2 n3 vws n3 n4 n3P	vbiasn vm n3p vws n3 vbiasn vcmfb vbiasn vbiasn vcm n3P vcm n3p vws vws n3 vws vws n3	0 n1t n2R n4R VDD  0 0 0 0 0 n1ws n1ta n1b n2 VDD n4 VDD vDD vDD 0 n1t n2L	0 0 0 VDD VDD 0 0 0 0 0 0 VDD VDD VDD VD	NMOS L PMOS L PMOS L NMOS L NMOS L NMOS L NMOS L NMOS L NMOS L PMOS L PMOS L PMOS L PMOS L PMOS L PMOS L NMOS L NMOS L NMOS L NMOS L	=1 W=10 =1 W=10 =1 W=10 =1 W=20 =1 W=20 =1 W=20 ==1 W=10 ==2 W=10 ==1 W=10 ==1 W=10 ==1 W=10 ==1 W=10 ==1 W=20 ==1 W=20 ==1 W=20 ==1 W=10 ==1 W=10 ==1 W=10 ==1 W=10 ==1 W=10					
M8L M10L .ends	vom n4L	vws n3	n4L VDD	VDD VDD		=1 W=20 =1 W=20					
M1	Vbiasn	Vbiasn	0	0		=1 W=10					
M2 M3	Vreg Vbiasn	Vreg Vbiasp	Vr VDD	0 VDD		=1 W=40 =1 W=20					

M4	Vreg	Vbiasp	VDD	VDD	PMOS L=1 W=20
Rbias	Vr	0	4k		
*amplifier					
MA1	Vamp	Vreg	0	0	NMOS L=2 W=10
MA2	Vbiasp	Vbiasn	0	0	NMOS L=2 W=10
MA3	Vamp	Vamp	VDD	VDD	PMOS L=2 W=20
MA4	Vbiasp	Vamp	VDD	VDD	PMOS L=2 W=20
*start-up s	tuff				
MSU1	Vsur	Vbiasn	0	0	NMOS L=1 W=10
MSU2	Vsur	Vsur	VDD	VDD	PMOS L=20 W=10
MSU3 .ends	Vbiasp	Vsur	Vbiasn	0	NMOS L=1 W=10



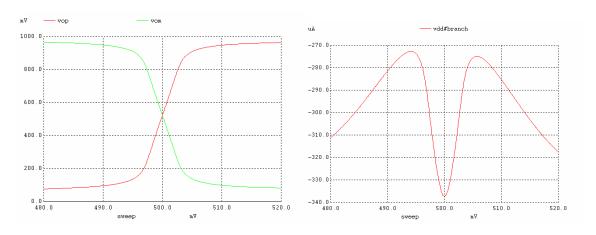


Fig 2: Dc behavior, small signal gain and currnt burnt in opamp

\*\*\* Problem 26.16\_large signal Simulation \*\*\*

.control destroy all run plot vop vom plot vip-vim vop-vom .endc

VDD	VDD	0	DC	1							
vcm	vcm	0	DC	500m							
vip	vip	0	DC	0	PULSE 7	00m 300m	0 500p 500	op 4.5n 10n			
vim	vim	0	DC	0			0 500p 500				
,		Ü	20	Ü	102020	00 <b>111</b> / 00 <b>111</b>	o boop boo	P 1011			
Rf1	vop	vm	20k								
Rf2	vop vom		20k								
		vp									
Ri1	vip	vm	20k								
Ri2	vim	vp	20k								
Clr	vop	0	250f								
cll	vom	0	250f								
xopamp	vop	vom	vp	vm	VDD	vcm	opamp				
.subckt op	oamp	vop	vom	vp	vm	VDD	vcm				
Xbias	vbiasn	vbiasp	VDD	bias							
Xdiffamp	vop1	vom1	vp	vm	vbiasn	cr	cl	vemfb	vcm	vdd	diffamp
Xbuffr	vop1	vom1	vom	VDD	buff						
Xbuffl	vom1	vop1	vop	VDD	buff						
cc1	vom	cr	60f								
cc2	vop	cl	60f								
xcmfb	vop vop	vom	vcm	vcmfb	vbiasp	vdd	cmfb				
	vop	VOIII	VCIII	veillib	voiasp	vuu	CIIIIO				
.ends											
1.1.	a				a	1.	1.1				
.subckt cr		vop	vom	vcm	vcmfb	vbiasp vo	aa				
Ra1	vop	vcma	20k								
Ca1	vop	vcma	10f								
Ra2	vom	vcma	20k								
Ca2	vom	vcma	10f								
Mp1	VSS	vbiasp	VDD	VDD	PMOS L:	=1 W=20					
Mp2	n1	vema	VSS	VDD	PMOS L:	=1 W=20					
Mp3	vcmfb	vcm	VSS	VDD	PMOS L:						
Mn1	n1	n1	0	0	NMOS L						
Mn2	vemfb	n1	0	0	NMOS L						
	VCIIIIO	111	U	U	NWIOS L	-1 <b>VV</b> -10					
.ends											
anh alst	buff	****	****	v.out	VDD						
.subckt		vp	vm	vout	VDD	1 117 40					
M1p	vout	vp	VDD	VDD	PMOS L:						
M2p	n1	vm	VDD	VDD	PMOS L						
M3n	n1	n1	0	0	NMOS L						
M4n	vouta	n1	0	0	NMOS L	=1 W=20					
M5n	vout	vdd	vouta	0	NMOS L	=1 W=10					
.ends											
.subckt	diffamp	vop	vom	vp	vm	vbiasn	n2R	n2L	vcmfb	vcm	vdd
	•	-		•							
M2R	n1t	vbiasn	0	0	NMOS L	=1 W=10					
M4R	n2R	vm	n1t	0	NMOS L						
M6R	vop	n3p	n2R	0	NMOS L						
M8R	vop	vws	n4R	VDD	PMOS L						
M10R	n4R	n3	VDD	VDD	PMOS L						
WITOK	11+1	113	VDD	VDD	I WOS L-	-1 <b>VV</b> -20					
M1R	n1ws	vbiasn	0	0	NMOS L	_1 W_10					
M1LL	n1b	vemfb	0	0	NMOS L						
M1LR	n1b	vbiasn	0	0	NMOS L						
M1LP	n1t	vbiasn	0	0	NMOS L						
M3R	vws	vcm	n1ws	0	NMOS L						
M3P	n3P	n3P	n1t	0		=50 W=10					
M3L	n2	vcm	n1b	0	NMOS L	=1 W=10					
M5L	n3	n3p	n2	0	NMOS L	=1 W=10					
M7R	vws	vws	VDD	VDD	PMOS L=	=3 W=10					
M7L	n3	vws	n4	VDD	PMOS L:	=1 W=20					
M9L	n4	n3	VDD	VDD	PMOS L:						
M9P	n3P	n3	VDD	VDD	PMOS L:						
	-	-	. =	. =		=-					
M2L	n1t	vbiasn	0	0	NMOS L	=1 W=10					
			-	-	LOD L	3					

M4L M6L M8L M10L	n2L vom vom n4L	vp n3p vws n3	n1t n2L n4L VDD	0 0 VDD VDD	NMOS L=1 W=10 NMOS L=1 W=10 PMOS L=1 W=20 PMOS L=1 W=20
.ends	ias vbiasn v	biasp VDD	)		
M1 M2 M3 M4	Vbiasn Vreg Vbiasn Vreg	Vbiasn Vreg Vbiasp Vbiasp	0 Vr VDD VDD	0 0 VDD VDD	NMOS L=1 W=10 NMOS L=1 W=40 PMOS L=1 W=20 PMOS L=1 W=20
Rbias	Vr	0	4k		
*amplifie					
MA1	Vamp	Vreg	0	0	NMOS L=2 W=10
MA2	Vbiasp	Vbiasn	0	0	NMOS L=2 W=10
MA3	Vamp	Vamp	VDD	VDD	PMOS L=2 W=20
MA4	Vbiasp	Vamp	VDD	VDD	PMOS L=2 W=20
*start-up	stuff				
MSU1	Vsur	Vbiasn	0	0	NMOS L=1 W=10
MSU2	Vsur	Vsur	VDD	VDD	PMOS L=20 W=10
MSU3	Vbiasp	Vsur	Vbiasn	0	NMOS L=1 W=10
.ends					

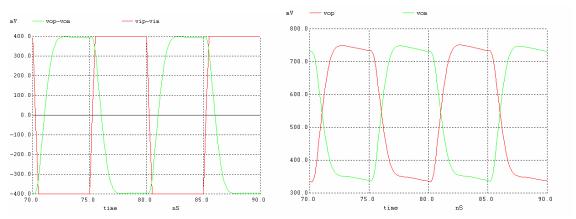


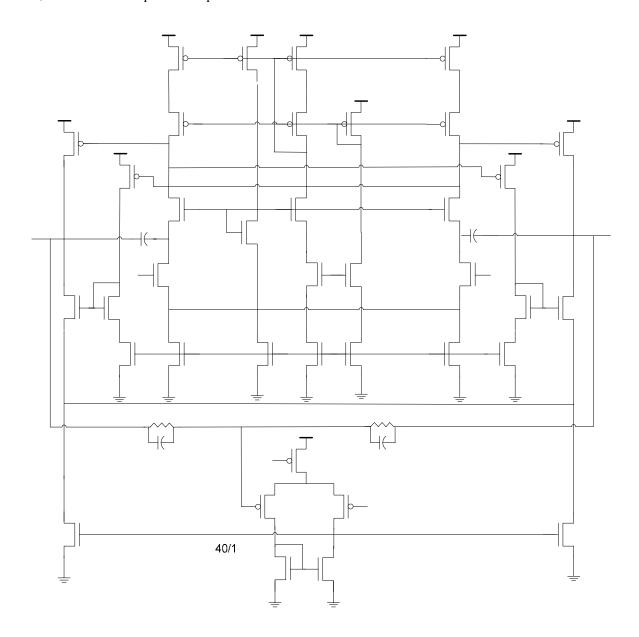
Fig 3:Large signal Step response of OP-Amp

## **Problem 26.17**

## Repeat problem 26.16 for the op-amp in Fig. 26.43

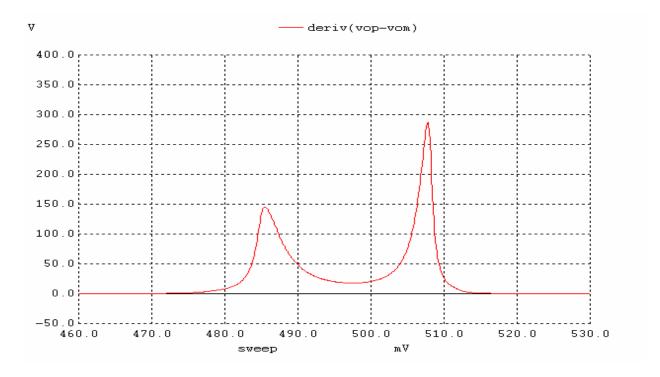
The gate drain connected NMOS has 20uA current flowing through it at all times. Since the current flowing through this NMOS is constant, its  $V_{GS}$  will be constant, thus helping in keeping the diff-pair NMOS's from going into triode.

Ideally the voltage across the NMOS is equal to the sum of  $V_{GS}$  and  $V_{DS,sat}$  of other NMOS devices, i.e., 450mv (400mv+50mv). For that amount of  $V_{GS}$ , a NMOS of size 4/1 will carry a current of 20uA. This equation applies perfectly well for long channel devices. For short channel devices, simulations show that a size of 4/1 doesn't work. Instead, a size of 20/20 helps in better performance.



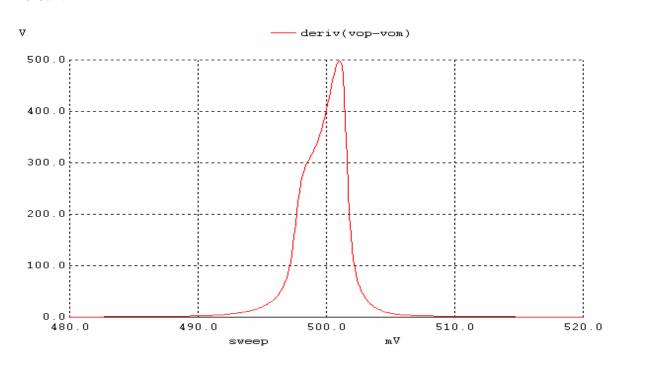
Vop + W/L

This is the DC gain observed by using NMOS of size 4/1

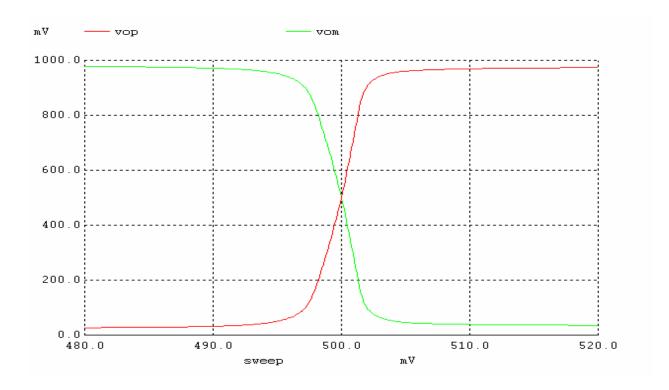


When an NMOS of size 20/20 is used, there is an increase in DC gain of the circuit up to 550. The attached simulation figures show the DC response and the large signal response of the circuit with the 20/20 NMOS.

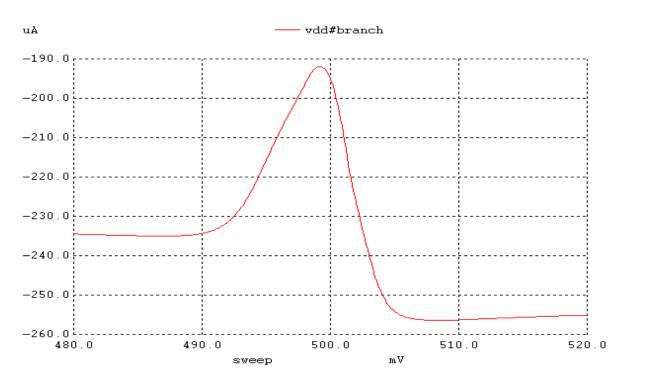
#### DC Gain:



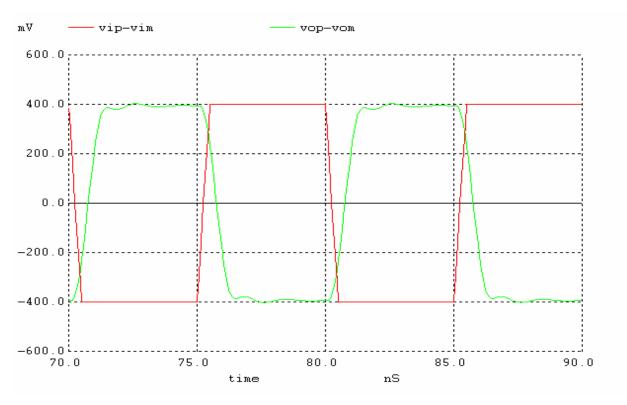
The outputs almost pull up to the rails.

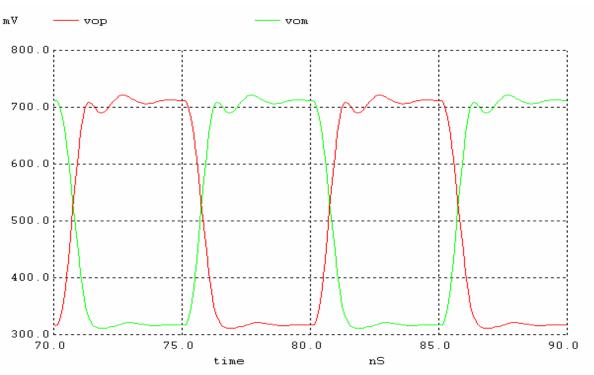


With this circuit, the power consumed in the circuit is higher, as expected.



# Large signal response:





```
*** P26_17 DC ***
.control
destroy all
run
plot i(vdd)
plot vop vom
plot vop-vom
plot deriv(vop-vom)
.endc
.option scale=50n rshunt=1e9
                           520m
.dc
                  480m
                                    .1 m
VDD
         VDD
                 0
                           DC
                                    1
                           DC
                                    500m
vcm
         vcm
                 0
         vin
                 0
                           DC
                                    500m
vin
                                            VDD
xopamp
        vop
                 vom
                           vin
                                    vcm
                                                     vcm
                                                              opamp
                                                     VDD
.subckt opamp
                  vop
                           vom
                                    vp
                                            vm
                                                               vcm
                  vbiasp
Xbias
         vbiasn
                           VDD
                                    bias
Xdiffamp vop1
                                                                                vdd
                                                                                         diffamp
                 vom1
                           vp
                                    vm
                                            vbiasn
                                                     cr
                                                              cl
                                                                       vcm
Xbuffr
                                                               VDD
         vop1
                 vom1
                           vom
                                    vbiasn
                                                     vcmfb
                                                                       buff
                                            vc
Xbuffl
                                                               VDD
         vom1
                 vop1
                           vop
                                    vbiasn
                                            vc
                                                     vcmfb
                                                                       buff
                           25f
cc1
         vom
                 cr
                           25f
cc2
         vop
                 cl
xcmfb
                                                     vdd
                                                              cmfb
         vop
                 vom
                           vcm
                                    vcmfb
                                            vbiasp
.ends
.subckt cmfb
                                    vcm
                                            vcmfb
                                                     vbiasp vdd
                  vop
                           vom
Ra1
                  vcma
                           20k
         vop
Ca1
                           10f
         vop
                  vcma
Ra2
                  vcma
                           20k
         vom
Ca2
         vom
                  vcma
                           10f
Mp1
                  vbiasp
                           VDD
                                    VDD
                                            PMOS L=1 W=20
         vss
                                    VDD
                                            PMOS L=1 W=20
Mp2
        n1
                  vcma
                           VSS
Mp3
         vcmfb
                  vcm
                                    VDD
                                            PMOS L=1 W=20
                           VSS
                           0
                                    0
                                            NMOS L=1 W=10
Mn1
        n1
                 n1
Mn2
         vcmfb
                 n1
                           0
                                    0
                                            NMOS L=1 W=10
.ends
        buff
                                            vbiasn
                                                               vemfb
                                                                       VDD
.subckt
                                                     vc
                           vm
                                    vont
                 vp
M1p
         vout
                  vp
                           VDD
                                    VDD
                                            PMOS L=1 W=40
                           VDD
                                    VDD
                                            PMOS L=1 W=20
M2p
        n1
                 vm
M3n
        n1
                 n1
                           n2
                                    0
                                            NMOS L=1 W=10
M4n
        n2
                 vhiasn
                           0
                                    0
                                            NMOS L=1 W=40
                                            NMOS L=1 W=20
M5n
         vout
                 n1
                           vc
                                   0
M6n
                 vcmfb
                           0
                                    0
                                            NMOS L=1 W=80
         vc
.ends
.subckt
        diffamp
                                                              n2R
                                                                       n2L
                                                                                         vdd
                 vop
                           vom
                                    vp
                                            vm
                                                     vbiasn
                                                                                vcm
M1
        n4L
                 n3
                           VDD
                                    VDD
                                            PMOS L=1 W=20
                                    VDD
                                            PMOS L=1 W=20
M2
         vom
                  vws
                           n4L
М3
                  VG
                           n2L
                                            NMOS L=1 W=10
         vom
                                    0
                                            NMOS L=1 W=10
M4
         n2L
                  vp
                           n45
                                    0
M5
                                            NMOS L=1 W=10
        n45
                  vbiasn
                                    0
                           VDD
                                    VDD
M6
                                            PMOS L=1 W=20
         n4
                 n3
M7
         n3
                  vws
                           n4
                                    VDD
                                            PMOS L=1 W=20
                                   0
M8
         n3
                  VG
                           n2
                                            NMOS L=1 W=10
M9
         n2
                           n1b
                                    0
                                            NMOS L=1 W=10
                  vcm
M10
        n1b
                 vbiasn
                                    0
                                            NMOS L=1 W=10
                           0
M11
                           VDD
                                    VDD
                                            PMOS L=3 W=10
         vws
                  vws
M12
                          n1ws \\
                                   0
                                            NMOS L=1 W=10
         vws
                  vcm
M13
        n1ws
                  vbiasn
                                    0
                                            NMOS L=1 W=10
                           VDD
                                    VDD
M14
        n4R
                                            PMOS L=1 W=20
                 n3
M15
                  vws
                           n4R
                                    VDD
                                            PMOS L=1 W=20
         vop
M16
                  VG
                          n2R
                                   0
                                            NMOS L=1 W=10
         vop
M17
        n2R
                           n45
                                    0
                                            NMOS L=1 W=10
                  vm
M18
                                    0
                                            NMOS L=1 W=10
         n45
                  vbiasn
                           0
MPT
         VG
                 n3
                           VDD
                                    vDD
                                            PMOS L=1 W=20
MNC
         VG
                  VG
                                   0
                                            NMOS L=20 W=20
                           n45
MNB
         n45
                  vbiasn
                           0
                                    0
                                            NMOS L=1 W=10
```

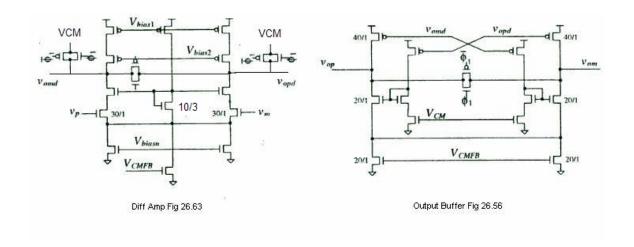
.ends

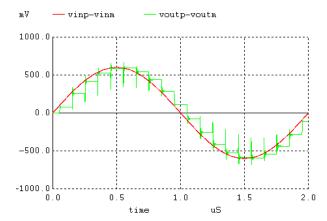
## **Problem 26.18**

Using the diff-amp in Fig 26.63 in the configuration seen in Fig 26.54 (with SC CMFB) and the output buffer in Fig 26.56 (again SC CMFB) regenerate the wave forms seen in Fig 26.60.

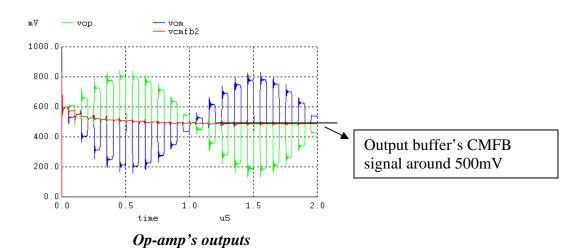
In this topology (comparing to Fig 26.53) we added gate drain connected NMOS (M12) to bias the gates of NMOS devices (M3, M8) at a higher potential than its drain and hence VDD is distributed better in this op-amp. The op-amp can now function at a lower VDD as shown in the simulations below it works fine with VDD=0.9 V.

From the Simulations (below) we can see that the settling time is around 4ns, the outputs are swinging almost around VCM (500mV), the outputs of the diff-amp are swinging around VBIAS1 and the common mode feedback voltage is relatively stable.





Circuit's outputs & inputs

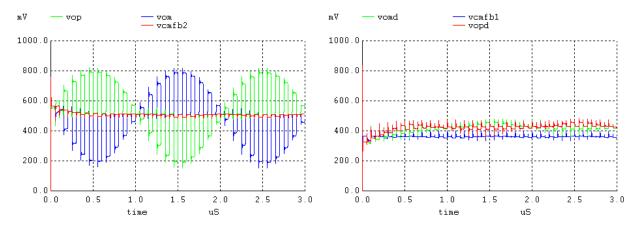


mV — vomd — vemfb1
1000.0
800.0
400.0
200.0
0.0
0.0
0.5
1.0
1.5
2.0

Diff Amp's CMFB signal around 400mV

Diff-amp's outputs

# Op-amp of Fig 26.63 with VDD=0.9V



#### **Net list**

\* Problem 26.18 CMOS: Circuit Design, Layout, and Simulation \*

.control
destroy all
run
plot i(vdd)
plot vopd vomd vcmfb1
plot vcmfb2 vop vom
plot vinp-vinm voutp-voutm
.endc

.options scale=50nm .tran 1n 2000n 0 1n UIC

VDD VDD 0 DC 1 VCM vcm 0 DC 500m

\* Clock Signals

Vphi1 phi1 0 DC 0 Pulse 0 1 0 2n 2n 40n 100n Vphi1b phi1b 0 DC 0 Pulse 1 0 0 2n 2n 40n 100n Vphi2 phi2 0 DC 0 Pulse 0 1 50n 2n 2n 40n 100n Vphi2b phi2b 0 DC 0 Pulse 1 0 50n 2n 2n 40n 100n R1 phi1 0 1MEG R2 phi1b 0 1MEG R3 phi2 0 1MEG R4 phi2b 0 1MEG \* input signals

ii ipat oi	griaio				
vinp	vinp	0	DC	0	SIN 500m 300m
vinm	vinm	0	DC	0	SIN 500m -300m
* capacit	ors				
Ct	t1	vm	250f		
Cb	b1	vp	250f		
Coutp	voutp	0	250f		
Coutm	voutm	0	250f		

* switche	es					
XTGs1	vinp	t1	phi1	phi1b	VDD	TG
XTGs2	vinm	b1	phi1	phi1b	VDD	TG
XTGs3	t1	vop	phi2	phi2b	VDD	TG
XTGs4	b1	vom	phi2	phi2b	VDD	TG
XTGs5	vop	voutp	phi2	phi2b	VDD	TG
VTCc6	vom	voutm	nhi2	nhi2h	VDD	TC

XTGs6	vom	voutm	phi2	phi2b	VDD	TG					
* op-amp											
Xbias	vbiasn	vbiasp	Vbias1	Vbias2	vcm	VDD	bias				
Xdiff	vp	vm	vbias1	vbias2	vbiasn	vcmfb1	vopd	vomd	ccl	ccr	vdd
	diffamp										
Xcmfb1	vcmfb1	vopd	vomd	vbiasn	vbias1	phi1	phi1b	phi2	phi2b	vdd	sccmfb
XTG1	vcm	vp	phi1	phi1b	vdd	TG					

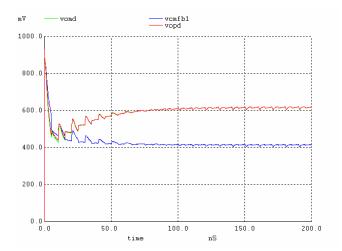
.5MEG

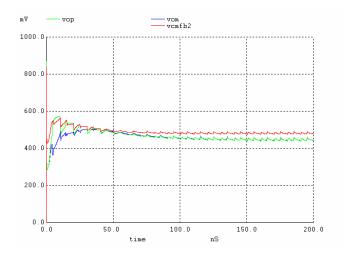
.5MEG

XTG2 XTG3 ccl	vcm vopd vop	vm vomd ccl	phi1 phi1 50f	phi1b phi1b	vdd vdd	TG TG					
ccr	vom	ccr	50f								
Xcmfb2 xbuff	vcmfb2 vopd	vop vomd	vom vcmfb2	vcm vop	vcm vom	phi1 vcm	phi1b vdd	phi2 buffer	phi2b	vdd	sccmfb
XTG4	vop	vom	phi1	phi1b	vdd	TG					
*subcircu .subckt b		vopd	vomd	vcmfb	vop	vom	vcm	vdd			
M1	vop	vomd	VDD	VDD	PMOS L	=1 W=40					
M2 M3	vop vss	n1 vcmfb	vss 0	0 0		=1 W=20 =1 W=20					
M4	n1	vopd	VDD	VDD	PMOS L	=1 W=20					
M5 M6	n1 n2	n1 vcm	n2 0	0 0		=1 W=10 =1 W=10					
M7	n3	vomd	VDD	VDD	PMOS L	=1 W=20					
M8 M9	n3 n4	n3 vcm	n4 0	0 0		=1 W=10 =1 W=10					
M10	vom	vopd	VDD	VDD	PMOS L	.=1 W=40					
M11 M12	vom vss	n3 vcmfb	vss 0	0 0		=1 W=20 =1 W=20					
.ends		VOITILD	Ü								
.subckt d M1	liffamp n1	vp vbias1	vm VDD	vbias1 VDD	vbias2	vbiasn .=1 W=20	vcmfb	vopd	vomd	ccl ccr	vdd
M2	vomd	vbias2	n1	VDD		=1 W=20 =1 W=20					
M3 M4	vomd ccl	vb1 vp	ccl vss	0 0		.=1 W=10 .=1 W=30					
M5	VSS	vbiasn	0	0		=1 W=30 =1 W=10					
M6	n4	vbias1	VDD	VDD		=1 W=20					
M7 M8	vopd vopd	vbias2 vb1	n4 ccr	VDD 0		=1 W=20 =1 W=10					
M9	ccr	vm	vss	0		=1 W=30					
M10 M11	vss vb1	vbiasn vbias1	0 VDD	0 VDD		=1 W=10 =1 W=20					
M12	vb1	vb1	vss	0		=3 W=10					
M13 .ends	VSS	vcmfb	0	0	NMOS L	=1 W=10					
.ends .subckt	sccmfb v	cmfb	vop	vom	vcmfbi	vavgi	phi1	phi1b	phi2	phi2b	vdd
.ends .subckt x1	sccmfb v	rcmfb n1	vop phi1	vom phi1b	vcmfbi vdd	vavgi TG	phi1	phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3	sccmfb v vavgi n1 vom	rcmfb n1 vop n2	vop phi1 phi2 phi2	vom phi1b phi2b phi2b	vcmfbi vdd vdd vdd	vavgi TG TG TG	phi1	phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4	sccmfb v vavgi n1 vom n2	rcmfb n1 vop n2 vavgi	vop phi1 phi2 phi2 phi1	vom phi1b phi2b phi2b phi1b	vcmfbi vdd vdd vdd vdd	vavgi TG TG TG TG	phi1	phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5	sccmfb v vavgi n1 vom n2 vcmfbi n3	rcmfb n1 vop n2 vavgi n3 vcmfb	vop phi1 phi2 phi2 phi1 phi1 phi2	vom phi1b phi2b phi2b phi1b phi1b phi2b	vcmfbi vdd vdd vdd vdd vdd vdd	vavgi TG TG TG TG TG TG	phi1	phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb	rcmfb n1 vop n2 vavgi n3 vcmfb n4	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2	vom phi1b phi2b phi2b phi1b phi1b phi2b phi2b	vcmfbi vdd vdd vdd vdd vdd vdd vdd	vavgi TG TG TG TG TG TG	phi1	phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1	sccmfb v vavgi n1 vom n2 vcmfbi n3	rcmfb n1 vop n2 vavgi n3 vcmfb	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2 phi1 100f	vom phi1b phi2b phi2b phi1b phi1b phi2b	vcmfbi vdd vdd vdd vdd vdd vdd	vavgi TG TG TG TG TG TG	phi1	phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1 vop	remfb n1 vop n2 vavgi n3 vemfb n4 vemfbi n3 vemfb	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2 phi1 100f 250f	vom phi1b phi2b phi2b phi1b phi1b phi2b phi2b	vcmfbi vdd vdd vdd vdd vdd vdd vdd	vavgi TG TG TG TG TG TG	phi1	phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2 C3 C4	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1	remfb n1 vop n2 vavgi n3 vemfb n4 vemfbi n3	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2 phi1 100f	vom phi1b phi2b phi2b phi1b phi1b phi2b phi2b	vcmfbi vdd vdd vdd vdd vdd vdd vdd	vavgi TG TG TG TG TG TG	phi1	phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2 C3 C4 .ends	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1 vop vom n2	remfb n1 vop n2 vavgi n3 vemfb n4 vemfbi n3 vemfb vemfb n4	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2 phi1 100f 250f 250f 100f	vom phi1b phi2b phi2b phi1b phi1b phi2b phi2b phi1b	vcmfbi vdd vdd vdd vdd vdd vdd vdd vdd vdd	vavgi TG TG TG TG TG TG TG	phi1	phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2 C3 C4	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1 vop vom n2	remfb n1 vop n2 vavgi n3 vemfb n4 vemfbi n3 vemfb n4 vemfb in s	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2 phi2 phi1 100f 250f 250f	vom phi1b phi2b phi2b phi1b phi1b phi2b phi2b phi1b	vcmfbi vdd vdd vdd vdd vdd vdd vdd vdd vdd vd	vavgi TG TG TG TG TG TG TG TG	phi1	phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2 C3 C4 .ends .subckt T	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1 vop vom n2	remfb n1 vop n2 vavgi n3 vemfb n4 vemfbi n3 vemfb vemfb n4 in	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2 phi1 100f 250f 250f 100f out	vom phi1b phi2b phi2b phi1b phi1b phi2b phi2b phi1b	vcmfbi vdd vdd vdd vdd vdd vdd vdd vdd vdd vd	vavgi TG TG TG TG TG TG TG	phi1	phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2 C3 C4 .ends .subckt T Mn Mp .ends .subckt	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1 vop vom n2	remfb n1 vop n2 vavgi n3 vemfb n4 vemfbi n3 vemfb n4 vemfb in s	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2 phi2 phi1 100f 250f 250f 100f out	vom phi1b phi2b phi2b phi1b phi2b phi2b phi2b phi2b phi2b pvi2b pvi2b pvi4b pvi4b pvi4b pvi4b vvi4b vvi4b vvi4b	vcmfbi vdd vdd vdd vdd vdd vdd vdd vdd vdd vd	vavgi TG TG TG TG TG TG TG TG TG TG	phi1	phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2 C3 C4 .ends .subckt T Mn Mp .ends .subckt MB1	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1 vop vom n2 	remfb n1 vop n2 vavgi n3 vemfb n4 vemfbi n3 vemfb vemf	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2 phi1 100f 250f 250f 100f out out vbiasp VDD	vom phi1b phi2b phi2b phi1b phi1b phi2b phi2b phi1b s 0 vdd vbias1 VDD	vcmfbi vdd vdd vdd vdd vdd vdd vdd vdd vdd vd	vavgi TG TG TG TG TG TG TG TG TG TG TG		phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2 C3 C4 .ends .subckt T Mn Mp .ends .subckt	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1 vop vom n2	remfb n1 vop n2 vavgi n3 vcmfb n4 vcmfbi n3 vcmfb	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2 phi1 100f 250f 250f 100f out out vbiasp	vom phi1b phi2b phi2b phi1b phi2b phi2b phi2b phi2b phi2b pvi2b pvi2b pvi4b pvi4b pvi4b pvi4b vvi4b vvi4b vvi4b	vcmfbi vdd vdd vdd vdd vdd vdd vdd vdd vdd vd	vavgi TG TG TG TG TG TG TG TG TG TG		phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2 C3 C4 .ends .subckt T Mn Mp .ends .subckt MB1 MB2 MB3 MB4	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1 vop vom n2 TG in in bias nb1 vbias1 vbias1 nb2	remfb n1 vop n2 vavgi n3 vemfb n4 vemfbi n3 vemfb vemf	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2 phi1 100f 250f 250f 100f out out vbiasp VDD nb1 nb2 nb3	vom phi1b phi2b phi2b phi1b phi2b phi2b phi2b phi1b  vodd  vbias1 VDD VDD 0	vcmfbi vdd vdd vdd vdd vdd vdd vdd vdd vdd vd	vavgi TG TG TG TG TG TG TG TG TG TG TG TG =1 W=10 =1 W=10 =1 W=20 =1 W=20 =1 W=30		phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2 C3 C4 .ends .subckt T Mn Mp .ends .subckt MB1 MB2 MB3	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1 vop vom n2 TG in in bias nb1 vbias1 vbias1	vemfb n1 vop n2 vavgi n3 vemfb n4 vemfbi n3 vemfb vemf	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2 phi2 phi1 100f 250f 250f 100f out out vbiasp VDD nb1 nb2	vom phi1b phi2b phi2b phi1b phi2b phi2b phi2b phi2b phi2b pvi2b phi1b	vcmfbi vdd vdd vdd vdd vdd vdd vdd vdd vdd vd	vavgi TG TG TG TG TG TG TG TG TG TG TG =1 W=10 =1 W=10 vcm =1 W=20 =1 W=20 =1 W=10		phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2 C3 C4 .ends .subckt T Mn Mp .ends .subckt MB1 MB2 MB3 MB4 MB5 MB6 MB8	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1 vop vom n2 G in in bias nb1 vbias1 vbias1 vbias2 vbias2 vbias2	remfb n1 vop n2 vavgi n3 vcmfb n4 vcmfbi n3 vcmfb vcmc vbiasn vbias2 vcm	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2 phi1 100f 250f 250f 100f out out vbiasp VDD nb1 nb2 nb3 0 VDD nb5	vom phi1b phi2b phi2b phi1b phi1b phi2b phi1b phi2b phi1b phi2b phiD phi2b phiD phiD 0 vdd vbias1 VDD VDD 0 0 VDD 0 VDD 0	vcmfbi vdd vdd vdd vdd vdd vdd vdd vdd vdd vd	vavgi TG TG TG TG TG TG TG TG TG TG TG TG =1 W=10 =1 W=10 =1 W=20 =1 W=30 =1 W=30 =1 W=30 =1 W=30		phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2 C3 C4 .ends .subckt T Mn Mp .ends .subckt MB1 MB2 MB3 MB4 MB5 MB6	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1 vop vom n2 G in in bias nb1 vbias1 vbias1 nb2 nb3 vbias2	remfb n1 vop n2 vavgi n3 vemfb n4 vemfbi n3 vemfb vemf	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2 phi1 100f 250f 250f 100f out out vbiasp VDD nb1 nb2 nb3 0 VDD	vom phi1b phi2b phi2b phi1b phi2b phi2b phi2b phi2b phi1b s 0 vdd vbias1 VDD VDD 0 0 VDD	vcmfbi vdd vdd vdd vdd vdd vdd vdd vdd vdd vd	vavgi TG TG TG TG TG TG TG TG TG TG TG TG =1 W=10 =1 W=10 =1 W=20 =1 W=20 =1 W=20 =1 W=30 =1 W=10 =1 W=10		phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2 C3 C4 .ends .subckt T Mn Mp .ends .subckt MB1 MB2 MB3 MB4 MB5 MB6 MB8 MB9 M1 M2	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1 vop vom n2 G in in bias nb1 vbias1 vbias1 vbias2 vbias2 vbias2 nb5 Vbiasn Vreg	remfb n1 vop n2 vavgi n3 vcmfb n4 vcmfbi n3 vcmfb vcmrb vbiasn vbias1 vcm vbias1 vcm vbiasn vbias1 vcm vbiasn vbiasn Vreg	vop phi1 phi2 phi2 phi1 phi2 phi2 phi2 phi1 100f 250f 250f 100f out out vbiasp VDD nb1 nb2 nb3 0 VDD nb5 0 0 Vr	vom phi1b phi2b phi2b phi1b phi2b phi2b phi2b phi2b phi2b phi2b phi2b phi2b phiD 0 0 VDD 0 0 VDD 0 0 0 0 0 0 0	vemfbi vdd vdd vdd vdd vdd vdd vdd vdd vdd vd	vavgi TG TG TG TG TG TG TG TG TG TG TG TG TG		phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2 C3 C4 .ends .subckt T Mn Mp .ends .subckt MB1 MB2 MB3 MB4 MB5 MB6 MB8 MB9 M1	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1 vop vom n2 G in in bias nb1 vbias1 vbias1 vbias1 nb2 nb3 vbias2 vbias2 vbias2 vbias5 Vbiasn	remfb n1 vop n2 vavgi n3 vcmfb n4 vcmfbi n3 vcmfb vcmf	vop phi1 phi2 phi2 phi1 phi2 phi2 phi2 phi1 100f 250f 250f 100f out out vbiasp VDD nb1 nb2 nb3 0 VDD nb5 0 0	vom phi1b phi2b phi2b phi1b phi2b phi1b phi2b phi2b phi1b phi2b phi2b phiD phi2b phiD 0 vdd vbias1 VDD VDD 0 0 VDD 0 0 0 0 0 0 0	vcmfbi vdd vdd vdd vdd vdd vdd vdd vdd vdd vd	vavgi TG TG TG TG TG TG TG TG TG TG TG TG TG		phi1b	phi2	phi2b	vdd
.ends .subckt x1 X2 X3 X4 X5 X6 X7 X8 C1 C2 C3 C4 .ends .subckt Mp .ends .subckt MB1 MB2 MB3 MB4 MB5 MB6 MB8 MB9 M1 M2 M3 M4 Rbias	sccmfb v vavgi n1 vom n2 vcmfbi n3 vcmfb n4 n1 vop vom n2  G in in bias nb1 vbias1 vbias1 vbias2 vbias2 vbias2 vbias2 vbias2 Vbiasn Vreg Vbiasn	remfb n1 vop n2 vavgi n3 vcmfb n4 vcmfbi n3 vcmfb vcmfb n4 in s sb vbiasn vbias1 Vbias2 vbias1 vcm vbiasn vbias2 vcm vbiasn vbiasp Vbiasp Vbiasp	vop phi1 phi2 phi2 phi1 phi1 phi2 phi2 phi1 100f 250f 250f 100f  out out vbiasp VDD nb1 nb2 nb3 0 VDD nb5 0 0 Vr VDD	vom phi1b phi2b phi2b phi1b phi2b phi2b phi1b phi2b phi2b phi2b phi2b phi2b phi2b phi2b phiD 0 vdd vbias1 VDD VDD 0 0 VDD 0 0 VDD 0 0 VDD 0 0 VDD	vcmfbi vdd vdd vdd vdd vdd vdd vdd vdd vdd vd	vavgi TG TG TG TG TG TG TG TG TG TG TG TG TG		phi1b	phi2	phi2b	vdd

26.19) A switched-capacitor integrator is an example of a circuit that uses an op-amp that can't have the outputs of its diff-amp or output buffer shorted when  $\Phi_1$  goes high. Using the diff-amp in Fig 26.63 (with SC CMFB) and the output buffer in Fig 26.56 without the switches (again with the SC CMFB) demonstrate the operation of a SC integrator. For examples of fully-differential SC circuits see the second edition of this book entitled *CMOS Mixed-Signal Circuit Design*.

Shown below are the simulation results of the op-amp implementation using figures 26.56 and 26.63.





Simulation showing diff-amp Vopd = Vomd &  $V_{CMFB}$  values.

Simulation results of both stages of op-amp

Below is a modified circuit from Fig 32.3 pg 151 found in second edition *CMOS Mixed Signal Circuit Design book*. The circuit below shows an implementation of a SC integrator using a fully-differential op-amp.

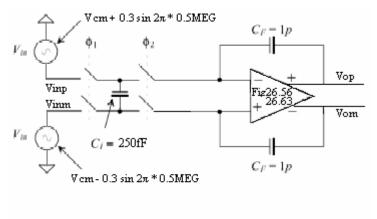
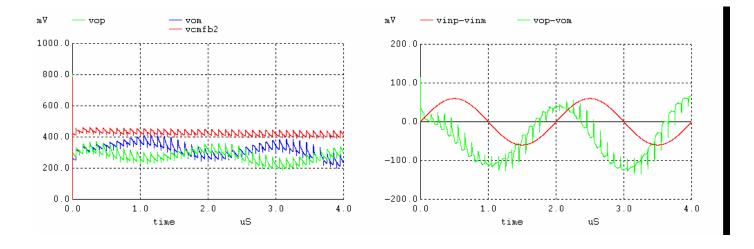


Fig 32.3 Modified as SC integrator for problem 26.19.

Simulation results demonstrating the operation and netlist are provided on next page.

# 26.19) (cont'd)

Simulation results for the SC integrator shown below.



## **Netlist** used in simulations.

.control destroy all run plot vopd vomd vcmfb1 plot vcmfb2 vop vom plot vinp-vinm vop-vom .endc .options scale=50nm .tran 1n 4000n 0 1n UIC VDD VDD 0 DC VCM 0 DC 500m vcm \* Clock Signals Vphi1 phi1 0 DC 0 Pulse 0 1 0 2n 2n 40n 100n Vphi1b phi1b 0 DC 0 Pulse 1  $0 \quad 0 \quad 2n \ 2n \ 40n \ 100n$ Vphi2 phi2 0 DC 0 Pulse 0 1 50n 2n 2n 40n 100n Vphi2b phi2b 0 DC 0 Pulse 1 0 50n 2n 2n 40n 100n R1 phi1 0 1MEG R2 phi1b 0 1MEG R3 phi2 0 1MEG R4 phi2b 0 1MEG \* input signals DC 0 SIN 500m 30m 0.5MEG vinp 0 DC SIN 500m -30m vinm 0.5MEG vinm Ci N1 N2 250f Cf1 vm 1p vop cf2 vom 1p vp \* switches XTGs1 vinp N1 phi1 phi1b VDD TG VDD XTGs2 phi1 phi1b TGvinm N2 phi2 phi2b XTGs3 N1 vm VDD TG XTGs4 VDD TG N2 phi2 phi2b

* op-amp												
Xbias	vbiasn	vbiasp	Vbias1	Vbias2	vcm	VDD	bias					
Xdiff	vp	vm	vbias1	vbias2	vbiasn	vcmfb1	vopd	vomd	ccl	ccr	vdd	diffamp
Xcmfb1	vcmfb1	vopd	vomd	vbiasn	vbias1	phi l	phi1b	phi2	phi2b	vdd	sccmfb	
ccl	vop	ccl	50f									
ccr	vom	ccr	50f									
Xcmfb2	vcmfb2	vop	vom	vcm	vcm	phi l	phi1b	phi2	phi2b	vdd	sccmfb	
xbuff	vopd	vomd	vcmfb2	vop	vom	vcm	vdd	buffer				
. 1 .	٠,											
*subcircu	IIIS											
.subckt b	uffer	vopd	vomd	vemfb	vop	vom	vcm	vdd				
M1	vop	vomd	VDD	VDD		=1 W=40	, 6111	, aa				
M2	vop	n1	VSS	0		_=1 W=20						
M3	VSS	vcmfb	0	0	NMOS I	_=1 W=20						
M4	n1	vopd	VDD	VDD	PMOS L	=1 W=20						
M5	n1	n1	n2	0		_=1 W=10						
M6	n2	vcm	0	0		_=1 W=10						
M7	n3	vomd	VDD	VDD		=1 W=20						
M8	n3	n3	n4	0		_=1 W=10						
M9	n4	vem	0 VDD	0		_1 W=10						
M10	vom	vopd n3	VDD	VDD		=1 W=40						
M11 M12	vom vss	ns vemfb	vss 0	0		=1 W=20 =1 W=20						
ends.	V 55	VCIIIIO	U	U	NIVIOSI	1 W-20						
.cnus												
.subckt d		vp	vm	vbias1	vbias2	vbiasn	vemfb	vopd	vomd	ccl	ccr	vdd
M1	n1	vbias1	VDD	VDD		=1 W=20						
M2	vomd	vbias2	n1	VDD		=1 W=20						
M3	vomd	vdm11	ccl	0		_=1 W=10						
M4	ccl	vp	VSS	0		_=1 W=30						
M5 M6	vss n4	vbiasn vbias1	0 VDD	$_{ m VDD}^{ m 0}$		=1 W=10 =1 W=20						
M7	vopd	vbias1	n4	VDD		=1 W=20						
M8	vopd	vdm11	ccr	0		_1 W=20 _=1 W=10						
M9	ccr	vm	VSS	0		=1 W=30						
M10	VSS	vbiasn	0	0		=1 W=10						
M11	vdm11	vbias1	VDD	VDD		=1 W=20						
M12	vdm11	vdm11	VSS	0		_=1 W=10						
M13	VSS	vcmfb	0	0	NMOS I	_=1 W=10						
.ends												
auk -1-4	aaar- <b>A</b> -	amafla	****	*****		*****	nhi1	mbi11-	mhi2	mhi 21-	v. d.d	
.subckt	scemfb v		vop phi 1	vom phi1b	vemfbi vdd	vavgi TG	phi1	phi1b	phi2	phi2b	vdd	
x1 X2	vavgi n1	nl von	phi2	phi2b	vdd	TG						
X2 X3	vom	vop n2	phi2	phi2b	vdd	TG						
X4	n2	vavgi	phi1	phi1b	vdd	TG						
X5	vemfbi	n3	phi1	phi1b	vdd	TG						
X6	n3	vemfb	phi2	phi2b	vdd	TG						
X7	vemfb	n4	phi2	phi2b	vdd	TG						
X8	n4	vemfbi	phi1	phi1b	vdd	TG						
C1	n1	n3	10f									
C2	vop	vemfb	25f									
C3	vom	vemfb	25f									
C4	n2	n4	10f									
.ends												
.subckt T	G	in	out	s	sb	vdd						
Mn	in	S	out	0		_=1 W=10						
Mp	in	sb	out	vdd		=1 W=10						
.ends												
gub alst	hins	whice	whicen	whica 1	whice?	vone	VDD					
.subckt	bias	vbiasn	vbiasp	vbias1	vbias2	vcm	עטע					
MB1	nb1	vbias1	VDD	VDD	PMOS L	=1 W=20						
MB2	vbias1	Vbias2	nb1	VDD		=1 W=20						
MB3	vbias1	vbias1	nb2	0		=1 W=10						
MB4	nb2	vcm	nb3	0	NMOS I	_=1 W=30						

MB5 MB6 MB8 MB9	nb3 vbias2 vbias2 nb5	vbiasn vbias2 vcm vbiasn	0 VDD nb5 0	0 VDD 0 0	NMOS L=1 W=10 PMOS L=3 W=10 NMOS L=1 W=30 NMOS L=1 W=10
M1 M2 M3 M4	Vbiasn Vreg Vbiasn Vreg	Vbiasn Vreg Vbiasp Vbiasp	0 Vr VDD VDD	0 0 VDD VDD	NMOS L=1 W=10 NMOS L=1 W=40 PMOS L=1 W=20 PMOS L=1 W=20
Rbias	Vr	0	4k		
*amplifier MA1 MA2 MA3 MA4	Vamp Vbiasp Vamp Vbiasp	Vreg Vbiasn Vamp Vamp	0 0 VDD VDD	0 0 VDD VDD	NMOS L=2 W=10 NMOS L=2 W=10 PMOS L=2 W=20 PMOS L=2 W=20
*start-up s MSU1 MSU2 MSU3	tuff Vsur Vsur Vbiasp	Vbiasn Vsur Vsur	0 VDD Vbiasn	0 VDD 0	NMOS L=1 W=10 PMOS L=20 W=10 NMOS L=1 W=10

.ends