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## Homework #8

<Lab>

The image displays the ISE Project Navigator interface for a project named "P.20131013" located at "/csehome/ldj19/ShiftRegis". The main window shows the Verilog code for a 4-bit shift register module, `sr4`.

```
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module sr4(
22     input CLRb,
23     input [1:0] S,
24     input CLK,
25     input SDL,
26     input SDR,
27     input [3:0] D,
28     output [3:0] Q
29 );
30
31 reg[3:0] q;
32 assign Q = q;
33
34 always @(posedge CLK or negedge CLRb) begin
35     if (CLRb == 1'b0) begin
36         q <= 4'b0000;
37     end
38     else begin
39         case (S)
40             2'b00: q <= q;
41             2'b01: q <= (SDR, q[3], q[2], q[1]);
42             2'b10: q <= (q[2], q[1], q[0], SDL);
43             2'b11: q <= D;
44         endcase
45     end
46 end
47
48 endmodule
49
50
```

The right pane shows the simulation results for the `sr4` module. The simulation is titled "Simulation" and shows the values of the signals `Q`, `CLRb`, `S`, `CLK`, `SDL`, `SDR`, and `D` over time. The signals are represented by waveforms, and the values are listed in a table.

Signal	Value
Q[3:0]	1111
CLRb	1
S[1:0]	00
CLK	1
SDL	0
SDR	0
D[3:0]	1111

The simulation results show that the output `Q` is 1111, which matches the input `D`. The simulation is titled "Simulation" and shows the values of the signals `Q`, `CLRb`, `S`, `CLK`, `SDL`, `SDR`, and `D` over time. The signals are represented by waveforms, and the values are listed in a table.

The bottom pane shows the simulation results for the `sr4` module. The simulation is titled "Simulation" and shows the values of the signals `Q`, `CLRb`, `S`, `CLK`, `SDL`, `SDR`, and `D` over time. The signals are represented by waveforms, and the values are listed in a table.

Signal	Value
Q[3:0]	1111
CLRb	1
S[1:0]	00
CLK	1
SDL	0
SDR	0
D[3:0]	1111

The simulation results show that the output `Q` is 1111, which matches the input `D`. The simulation is titled "Simulation" and shows the values of the signals `Q`, `CLRb`, `S`, `CLK`, `SDL`, `SDR`, and `D` over time. The signals are represented by waveforms, and the values are listed in a table.

## <Homework>

위의 lab session 에서 구현했던 4-bit Universal Shift Register 과 유사한 방식으로 8-bit Universal Shift Register 을 Verilog 로 구현해보았습니다. 결과는 다음과 같습니다:

The image displays the ISE Project Navigator and ISim windows, showing the Verilog code for an 8-bit Universal Shift Register and its simulation results.

**ISE Project Navigator (P.20131013) - /csehome/ldj19/ShiftRegister4Bit/ShiftRegister8Bit.v**

```
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module ShiftRegister8Bit(
22     input CLRb,
23     input [1:0] S,
24     input CLK,
25     input SDL,
26     input SDR,
27     input [7:0] D,
28     output [7:0] Q
29 );
30
31 reg[7:0] q;
32 assign Q = q;
33
34 always @(posedge CLK or negedge CLRb) begin
35     if(CLRb == 1'b0) begin
36         q<=8'b00000000;
37     end
38     else begin
39         case(S)
40             2'b00: q<=q;
41             2'b01: q<={SDR, q[7], q[6], q[5], q[4], q[3], q[2], q[1]};
42             2'b10: q<={q[6], q[5], q[4], q[3], q[2], q[1], q[0], SDL};
43             2'b11: q<=D;
44         endcase
45     end
46 end
47 endmodule
48
49
```

**ISE Project Navigator (P.20131013) - /csehome/ldj19/ShiftRegister4Bit/ShiftRegister8Bit.tb**

```
37
38 // Instantiate the Unit Under Test (UUT)
39 ShiftRegister8Bit uut (
40     .CLRb(CLRb),
41     .S(S),
42     .CLK(CLK),
43     .SDL(SDL),
44     .SDR(SDR),
45     .D(D),
46     .Q(Q)
47 );
48
49 always #10 CLK = ~CLK;
50
51 initial begin
52     // Initialize Inputs
53     CLRb = 0;
54     S = 0;
55     CLK = 0;
56     SDL = 0;
57     SDR = 0;
58     D = 0;
59
60     // Wait 100 ns for global reset to finish
61     #100;
62
63     // Add stimulus here
64     #100; //hold
65     CLRb = 1;
66     S = 2'b00;
67     CLK = 0;
68     SDL = 0;
69     SDR = 0;
70     D = 0;
71
72
```

**ISim (P.20131013) - [Default.wcfg]**

Simulation Objects for sr8\_tb

Object Name	Value
Q[7:0]	11111111
CLRb	1
CLK	1
SDL	0
SDR	0
D[7:0]	11111111

Simulation Results (Waveform):

The waveform shows the signals over time (0 ns to 1,000 ns). The signals are: Q[7:0] (11111111), CLRb (1), CLK (1), SDL (0), SDR (0), and D[7:0] (11111111). The simulation completed successfully.