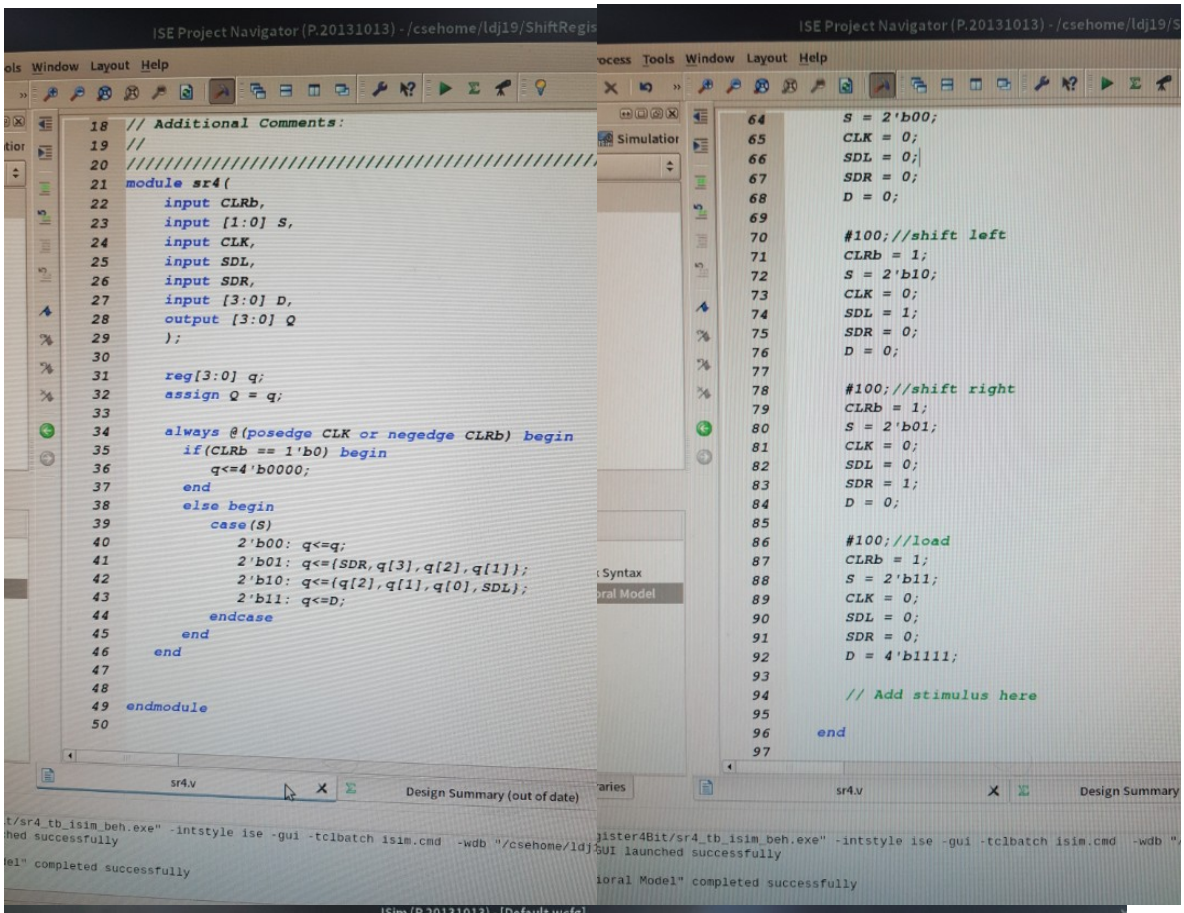
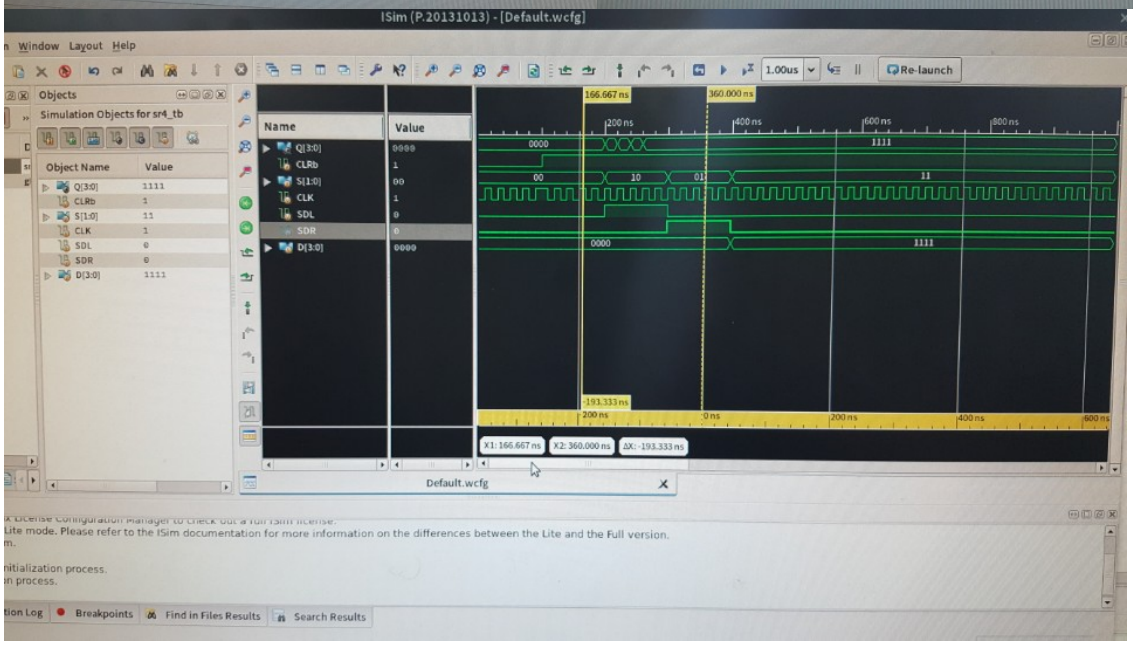
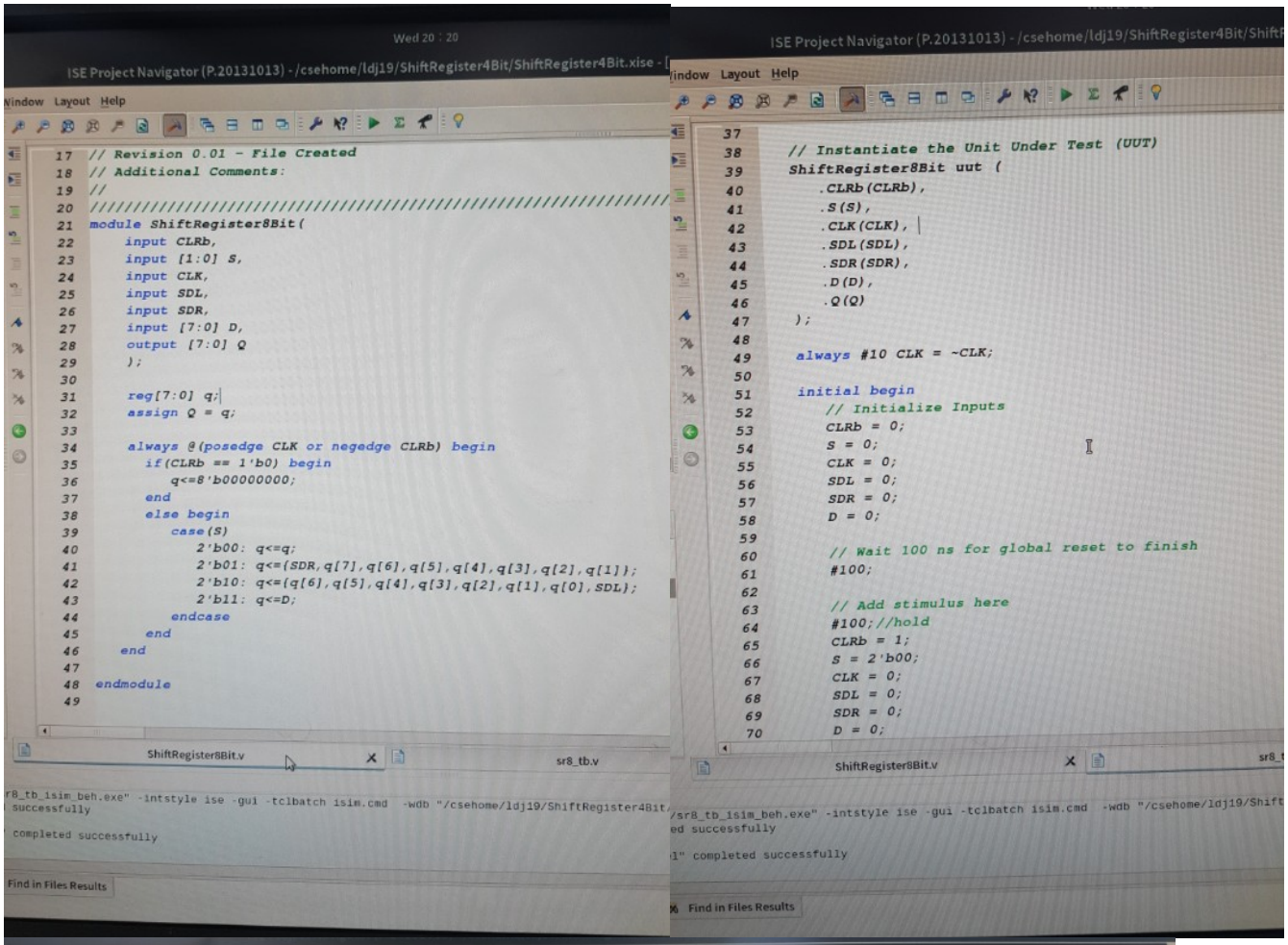
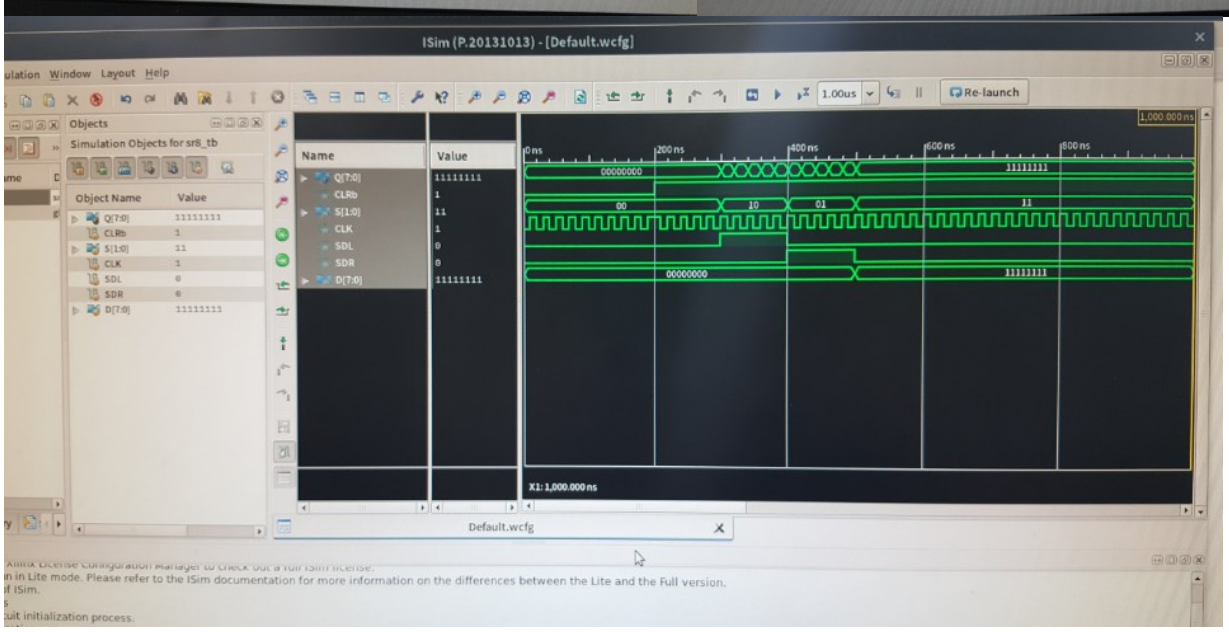
2014-17831 김재원

Homework #8

<Lab>





<Homework>

위의 lab session 에서 구현했던 4-bit Universal Shift Register 과 유사한 방식으로 8-bit Universal Shift Register 을 Verilog 로 구현해보았습니다. 결과는 다음과 같습니다: