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Energy Conservation of Adiabatic ECRL-Based Kogge-Stone Adder Circuits for FFT Applications

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Abstract: Low Power circuits play a significant role in designing large-scale devices with high energy and power consumption. Adiabatic circuits are one such energy-saving circuits that utilize reversible power. Several methodologies used previously infer the use of CMOS circuits for reducing power dissipation in logic circuits. However, CMOS devices hardly manage in maintaining their performance when it comes to fast switching networks. Adiabatic technology is employed to overcome these difficulties, which can further scale down the dissipation of power by charging and discharging. An Efficient Charge Recovery Logic (ECRL) based adiabatic technology is used here to evaluate arithmetic operations in circuits like inverter, full adder, Carry Look-Ahead adder etc. A better chance at reducing delay in digital circuits is illustrated by developing a Kogge-stone Adder, built using the ECRL technology. The developed circuitry is further integrated into a Fast Fourier Transform (FFT), which demonstrates the circuit's enhancement into DSP applications. Not only does this design reduce delay in VLSI switching circuits, but also narrows the power dissipation down to a minimum. This technique proved superior to the existing PFAL technique by demonstrating almost 10% less power dissipation with minimal propagation delay. All the circuits have been simulated at 45 nm technology using the Tanner EDA tool.

Keywords: Full adder; ECRL; carry look-ahead adder; kogge-stone; multiplexer; FFT

1 Introduction

Designing techniques for low power consumption have vastly influenced the current electronic industry trend, due to the increasing demand for compact gadgets such as cellphones, laptops, and several other handheld devices. The microelectronics industry have immensely evolved since transistors were initially designed, which set forth the foundation for such devices. A large number of gadgets were designed by integrating several transistors in them. As the current portable devices necessitate a huge number of logic gates to assemble in a single integrated chip, the area (or) the size of the chip becomes a major concern. Presently, a single IC incorporates fabrication of around 100,000 or even more transistors in it, thusly calling it VLSI (very large scale integration) [1]. Due to the earlier VLSI technologies relying on speed optimization to improve its performance, it has often suffered from portability issues. Reducing the chip