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Dindigul – Palani Highway, Dindigul – 624 002

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VAC

On

VLSI Design Tools-Verilog and VHDL

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Dr.D.SENTHIL KUMARAN, M.E., Ph.D., (MUS).,
Principal
SSM Institute of Engineering and Technology
Kuttathupatti Village, Sindalagundu (Po),
Palani Road, Dindigul - 624 002.



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CIRCULAR

08.01.2020

Department of ECE has planned to conduct Value Added Course for III year students in the title "VLSI Design Tools-Verilog and VHDL" from 11.01.2020 onwards. The main objective of this course involves imparting skills and knowledge related to digital design, hardware description languages, and the implementation of digital circuits. All the students are asked to attend the course without fail and get benefitted

HoD/ECE

Dr.S.Karthigai Lakshmi, Prof/ECE

Olivoigul est again

Dr.D.SENTHIL KUMARAN, M.E., Ph.D., (MUS).,
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Value added Course on VLSI design Tools-Verilog and VHDL7

Date:11.01.2020 to 28.03.2020

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HOD/ECE

Dr.S. KARTHIGAI LAKSHMI

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Value added Course on "VLSI design Tools-Verilog and VHDL"

Date:11.01.2020 to 28.03.2020

Syllabus content

- 1. Introduction to VLSI
- 2. Introduction to Chip Fabrication
- 3. About VLSI Design flow
- 4. VLSI Tool –Verilog Introduction
- 5. Logical Operators and syntax in Verilog

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- 6. VHDL Introduction
- 7. Hands on Verilog coding
- 8. Design of digital logic circuits using Verlilog and VHDL

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Value Added Course Summary 2019-2020

Course Name: VLSI Design tools-Verilog and VHDL

Course Duration: 30 hours

Year Offered: 2019-2020

Course Instructors: Mrs.M.Jeyalakshmi, AP/ECE

Mr.S.R.Ashok Kumar SSMIET,Dindigul

Course Outcome:

On completion of the course, students will be able to understand the process of circuit synthesis, converting high-level descriptions into gate-level or transistor-level representations and gain hands-on experience with Register-Transfer Level (RTL) coding using Verilog and VHDL for describing the behavior of digital systems.

Course Type: Self Framed

Assessment Mode

Attendance: 30 hours

Number of Participants: 40

Scheme of Exam: MCQ

SSM SSM SSM

Course Co-ordinators

Dr.D. SENTHIL KUMARAN, ME., PLD., (BUS)

Principal

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Palani Road, Dindigul - 624 902.

HoD/ECE



Dindigul – Palani Highway, Dindigul – 624 002. Email:ssmietdgl@gmail.com@Website:www.ssmiet.ac.in

Department of Electronics and Communication Engineering

VAC on "VLSI Desig Tools-Verilog and VHDL" Students Namelist

S.No	Register number	Name of the Student
1.	922117106041	KAARTHIC SHANKAR S
2.	922117106042	KALAIARASAN S
3.	922117106043	KARTHIK A
4.	922117106044	KARTHIKEYAN N
5.	922117106045	KAVIYA K
6.	922117106046	KOSHIKHA B
7.	922117106047	LAKSHMI S
8.	922117106048	LAVANYA J
9.	922117106049	LOGA DHARSINI A
10.	922117106050	MANIRAJA P
11.	922117106051	MARUTHARASU V
12.	922117106052	MATHISELVAN R
13.	922117106053	MITHUNAVARSHINI D S
14.	922117106054	MOHAMED IMRAN T
15.	922117106055	MONICA P M
16.	922117106056	MOUNIKA M
17.	922117106057	NAGALAKSHMI N
18.	922117106058	NAGARAJ M
19.	922117106059	NAMPERUMAL M

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Falani Road, Dindigul - 624 002.

922117106060	NANDHA KUMAR M
922117106061	NANDHINI P
922117106062	NAVANEETHA KRISHNAN J
922117106063	NIVETHA V
922117106064	NIVETHITHA T
922117106065	OVIYA S
922117106066	PADMA BHAGAVATHI S A
922117106067	PANDIARAJAN S
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922117106071	PRADEEP RAJA S
922117106072	PRAKASH S
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922117106074	PRAVEEN K
922117106075	PRIYADHARSHINI P (02-02-2000)
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922117106079	RAJKUMAR K
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	922117106061 922117106062 922117106063 922117106064 922117106065 922117106066 922117106067 922117106069 922117106070 922117106071 922117106073 922117106074 922117106075 922117106077 922117106077 922117106078 922117106079

1.M.Jeyalakshmi, AP/ECI

20.

2.S.R.Ashok Kumar/AP/ECE

Faculty Incharges

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HOD/ECE

Dr.S. KARTHIGAI LAKSHMI

Professor & Head Department of ECE SSM Insulure of Engg & Tech Dindiaui - 624 002

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14	922117106054	MOHAMED IMRAN T	I den !
15	922117106055	MONICA P M	P.M. Nomen
16	922117106056	MOUNIKA M	100.1
17	922117106057	NAGALAKSHMI N	Nagelil

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Palani Road, Dindigul - 624 002.

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-	19		NAMPERUMAL M	Nagaraj M
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	20	922117106060	NANDHA KUMAR M	walker
	21	922117106061	NANDHINI P	Vardhinip
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	23	922117106063	NIVETHA V	Nivethay
	24	922117106064	NIVETHITHA T	1 Nivethythe
	25	922117106065	OVIYA S	Donge S
	26	922117106066	PADMA BHAGAVATHI S A	Realin the
244	27	922117106067	PANDIARAJAN S	PO
	28	922117106068	PARALOGA SELVI I	Dandyn
	29	922117106069	PRABHU M	Paralogasella
- 4	30	922117106070 F	PRADEEPA M	M. Pradeep
	31	922117106071 F	PRADEEP RAJA S	1) 1
	32	922117106072 P	PRAKASH S	Ren .
	33	922117106073 P	PRASANNA M	Probome?
	34	922117106074 P	RAVEEN K	D
	35	922117106075 P	RIYADHARSHINI P (02-02-2000)	Prancen K.
	36	922117106076 P	RIYADHARSHINI P (10-08-2000)	Payadhar shirt
	37	922117106077 P	RIYADHARSHINI R (06-09-1999)	Ol mile
AL T	38	922117106078 R	AJALAKSHMI M	Dully .
	39	922117106079 R	AJKUMAR K	Pajalaher
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o' Engineering	Paritient (Faculty Incha	12/200 HOI	other 12020
	willen)		Dr.D.SENTHIL KUMARAN, M.R., Ph.D., (MUS).,	
			Principal	
			SSM Institute of Engineering and Technology Kuttathupatti Village, Sindalagundu (Po),	

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Principal

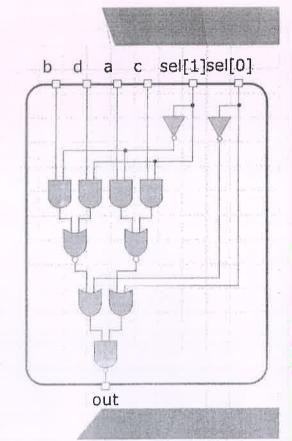
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MUX 4: GATE LEVEL DESIGNING

```
modulemux4(input a,b,c,d, input[1:0] sel, output out);
wire[1:0] sel_b;
not not0( sel_b[0], sel[0] );
not not1( sel_b[1], sel[1] );
wire n0, n1, n2, n3;
and and0( n0, c, sel[1] );
and and1( n1, a, sel_b[1] );
and and2( n2, d, sel[1] );
and and3( n3, b, sel_b[1] );
wirex0, x1;
nor nor0(x0, n0, n1);
nor nor1(x1, n2, n3);
wirey0, y1;
or or0( y0, x0, sel[0] );
or or1( y1, x1, sel_b[0] );
nand nand0( out, y0, y1 );
                                      Courtesy of Arvind http://
endmodule
```

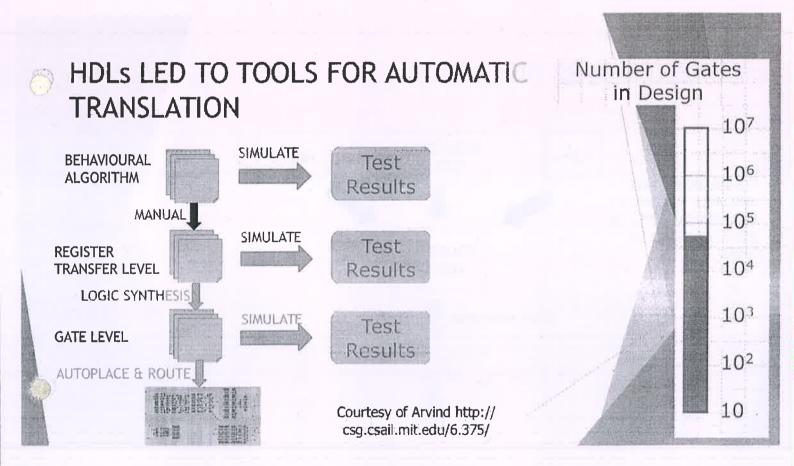
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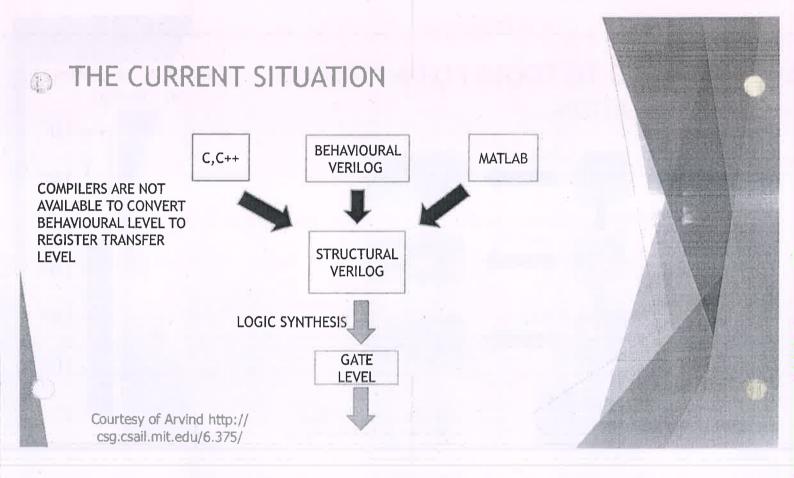
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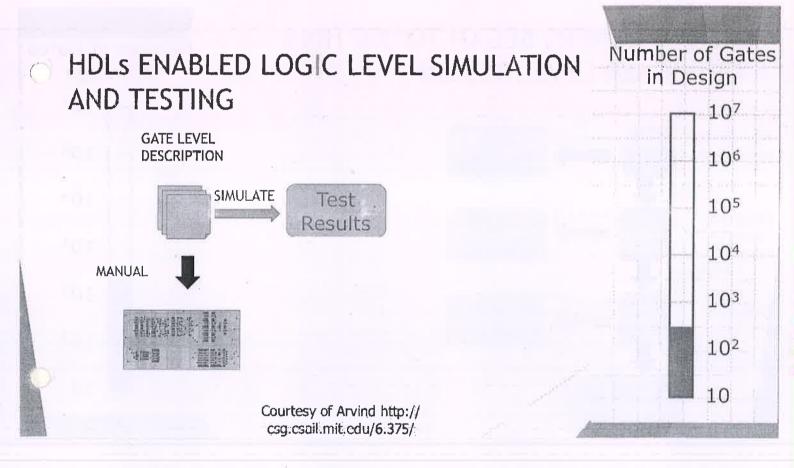


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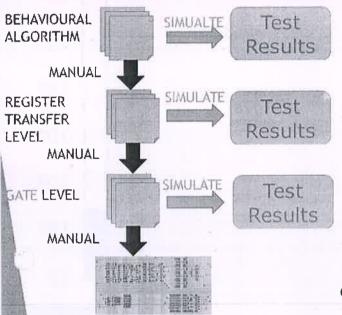


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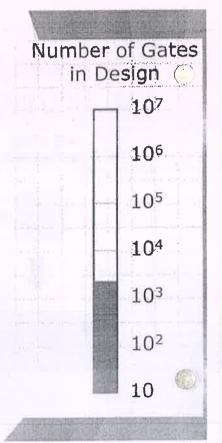
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THEN DESIGNERS BEGAN TO USE HDLs OR HIGHER LEVEL DESIGN



Courtesy of Arvind http://csg.csail.mit.edu/6.375/





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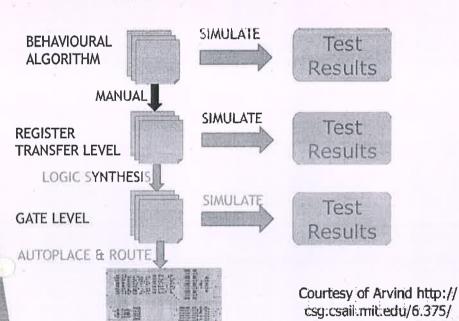
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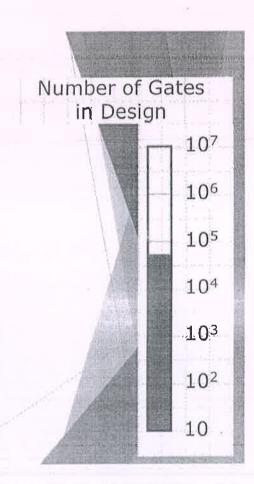
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HDLs LED TO TOOLS FOR AUTOMATIC TRANSLATION





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Value added Course on "VLSI design Tools-Verilog and VHDL" Date:11.01.2020 to 28.03.2020 ASSESSMENT QUESTIONS

1. T	The Verilog is a hardware description language	(3 marks)
	a)Hardware decision language	
	b)Hardware description language	
	c)Software Description language	
2.	is a superset of Verilog.	(3 marks)
	a) Verilog.	
	b)System verilog	
	c)System VHDL	
3. T	he Verilog offers more features than the VHDL.	(3 marks)
	a)Yes	
	b)No	
4. O	perator which precedes the operand is known as	(3 marks)
	,	
	a) Unary	
	b) Binary	
	c)Ternary	
	d)None of the above	
5. T	The wait statement is	(3 marks)
	a) Level sensitive	
	b) Edge sensitive	
	c)Both	
	d)None	

Name: Vikhou.B



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Value added Course on "VLSI design Tools-Verilog and VHDL"

Date:11.01.2020 to 28.03.2020

None: Vixhous

a) Hardware decision language b) Hardware description language c) Software Description language 2. Verilog is a superset of Verilog. a) Verilog. b) System verilog c) System VHDL 3. The Verilog offers more features than the VHDL a) Yes b) No (3 mark	ASSESSME.	NT QUESTIONS
c)Software Description language 2. Verilog is a superset of Verilog. a) Verilog. b)System verilog c)System VHDL 3. The Verilog offers more features than the VHDL a) Yes b)No (3 mark (3 mark		(3 marks)
c)Software Description language 2. Verilog is a superset of Verilog. a) Verilog. b)System verilog c)System VHDL 3. The Verilog offers more features than the VHDL a) Yes b)No (3 mark (3 mark	(b) Hardware description language	
a) Verilog. b)System verilog c)System VHDL 3. The Verilog offers more features than the VHDL a) Yes b) No		
b)System verilog c)System VHDL 3. The Verilog offers more features than the VHDL a)Yes b)No (3 mar)	2. Venlog is a superset of Verilog.	(3 marks)
c)System VHDL 3. The Verilog offers more features than the VHDL a)Yes b)No (3 mar)	a) Verilog.	
3. The Verilog offers more features than the VHDL (3 mar) (3 mar)	b)System verilog	
a)Yes b)No	c)System VHDL	
a)Yes b)No	3. The Verilog offers more features than the VHD	L (3 marks)
	a)Yes	· · · · · · · · · · · · · · · · · · ·
4. Operator which precedes the operand is known as (3 marl	b)No	
	4. Operator which precedes the operand is known	as (3 marks)

a) Unary

Binary (الحل

c)Ternary

d)None of the above

5. The wait statement is

(3 marks)

a) Level sensitive

b) Edge sensitive

Both

d)None

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Value added Course on "VLSI design Tools-Verilog and VHDL"
Date: 11.01.2020 to 28.03.2020

Assessment Marksheet

S.No.	Reg. No.	Name of the Student	Marks
1	922117106041	KAARTHIC SHANKAR S	15
2	922117106042	KALAIARASAN S	15
3	922117106043	KARTHIK A	15
4	922117106044	KARTHIKEYAN N	15
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15	922117106055	MONICA P M	15
16	922117106056	MOUNIKA M	15
17	922117106057	NAGALAKSHMI N	15

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		NAGARAJ M	15
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VAC on "VLSI Desig Tools-Verilog and VHDL"

11/01/2020 To 28/03/2020

FEEDBACK FORM

Name of the Participant:

Vishnu . B

Year/Sem

S.No	Question	Excellent	Good	Satisfactory
1	Did the VAC enlighten your mind			
2	Whether your expectation gets satisfied			
3	Whether the session was interactive			
4	Knowledge gained from this VAC is			
5	Was the VAC well organized			

Comments on session:

Signature of the Participant



SSM INSTITUTE OF ENGINEERING AND TECHNOLOGY

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11/01/2020 To 28/03/2020

Name of the Participant:

Year/Sem

FEEDBACK FORM

S.No	Question	Excellent	Good	Satisfactory
1	Did the VAC enlighten your mind			
2	Whether your expectation gets satisfied			
3	Whether the session was interactive			
4	Knowledge gained from this VAC is			
5	Was the VAC well organized			

Comments on session:

Good

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SSM Institute of Engineering and Technology Kuttathupatti Village, Sindalagundu (Po), Palani Road, Dindigul - 624 002. Signature of the Participant



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VAC on "VLSI Desig Tools-Verilog and VHDL"

11/01/2020 To 28/03/2020

FEEDBACK FORM

Name of the Participant:

Proselohn. M

S.No	Question	Excellent	Good	Satisfactory
1	Did the VAC enlighten your mind			
2	Whether your expectation gets satisfied	1		
3	Whether the session was interactive	1		
4	Knowledge gained from this VAC is			
5	Was the VAC well organized			

Comments on session:

Signature of the Participant

Signature of the Participant



SSM INSTITUTE OF ENGINEERING AND TECHNOLOGY DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VAC on "VLSI Desig Tools-Verilog and VHDL"

on "VLSI Desig Tools-Verilog and VHDL 11/01/2020 To 28/03/2020

FEEDBACK FORM

Name of the Participant: Lavanya. S

Year/Sem

S.No	Question	Excellent	Good	Satisfactory
1	Did the VAC enlighten your mind			
2	Whether your expectation gets satisfied			
3	Whether the session was interactive		/	
4	Knowledge gained from this VAC is			
5	Was the VAC well organized			

Comments on session:

CHOIGUL 624 002

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VAC on "VLSI Desig Tools-Verilog and VHDL"

11/01/2020 To 28/03/2020

FEEDBACK FORM

Name of the Participant:

Year/Sem Excellent Good Question Satisfactory S.No Did the VAC enlighten your mind Whether your expectation gets satisfied 2 3 Whether the session was interactive 4 Knowledge gained from this VAC is Was the VAC well organized 5

Comments on session:

Signature of the Participant



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VAC on "VLSI Desig Tools-Verilog and VHDL"

11/01/2020 To 28/03/2020

FEEDBACK FORM

Name of the Participant: Oviya 3 Year/Sem

S.No	Question	Excellent	Good	Satisfactory
1	Did the VAC enlighten your mind			
2	Whether your expectation gets satisfied			
3	Whether the session was interactive		~	
4	Knowledge gained from this VAC is			
5	Was the VAC well organized			

Comments on session:

in-formative session



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Signature of the Participant

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1.M.Jeyalakshmi , AP/ECE

2.S.R.Ashok Kumar/AP/ECE

Faculty Incharges

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S. Konthill HOD/ECE

DES. KARTHIGAI LAKSIMA.
Professor & Head

Professor & Head
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VAC on "VLSI Desig Tools-Verilog and VHDL"

11/01/2020 To 28/03/2020

FEEDBACK FORM

Name of the Participant:

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Year/Sem

S.No	Question	Excellent	Good	Satisfactory
1	Did the VAC enlighten your mind			
2	Whether your expectation gets satisfied		/	
3	Whether the session was interactive		//	
4	Knowledge gained from this VAC is			
5	Was the VAC well organized			

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Signature of the Participant



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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FEEDBACK FORM

Name of the Participant: Year/Sem :

Mammika. N

S.No	Question	Excellent	Good	Satisfactory
1	Did the VAC enlighten your mind			
2	Whether your expectation gets satisfied			
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5	Was the VAC well organized			

Comments on session:

The state of the s

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SSM Institute of Engineering and Technology Kuttathupatti Village, Sindalagundu (Po), Palani Road, Dindigul - 624 002. Signature of the Participant

Number of Gatas HDLs ENABLED LOGIC LEVEL SIMULATION in Design AND TESTING 107 **GATE LEVEL DESCRIPTION** 106 SIMULATE Test 105 Results 104 MANUAL 10^{3} 10^{2} 10 Courtesy of Arvind http:// csg.csail.mit.edu/6.375/



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CERTIFICATE

THIS CERTIFICATE IS PRESENTED TO

Value Added Course on "VLSI Design tools-Verilog and VHDL"



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Dr.D. Senthil Kumaran Principal

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