



SSM INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, New Delhi / Affiliated to Anna University / Accredited by NAAC)

Dindigul – Palani Highway, Dindigul-624 002

Value added Course on “VLSI design Tools-Verilog and VHDL”

Date :11.01.2020 to 28.03.2020

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S.Karthikai Lakshmi

HOD/ECE

Dr.S. KARTHIGAI LAKSHMI
Professor & Head
Department of ECE
SSM Institute of Engg & Tech
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A.D.Jayaram
Principal

A.D.JAYARAM, M.E.A.M, M.Tech
Principal
SSM Institute of Engineering and Technology
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Syllabus content

1. Introduction to VLSI
2. Introduction to Chip Fabrication
3. About VLSI Design flow
4. VLSI Tool –Verilog Introduction
5. Logical Operators and syntax in Verilog
6. VHDL Introduction
7. Hands on Verilog coding
8. Design of digital logic circuits using Verilog and VHDL



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Date : 11.01.2020 to 28.03.2020

Attendance sheet

S.No.	Reg. No.	Name of the Student	
1	922117106041	KAARTHIC SHANKAR S	KarthickShankar S
2	922117106042	KALAIARASAN S	Kalaiy
3	922117106043	KARTHIK A	Karthik -A
4	922117106044	KARTHIKEYAN N	Karthikeyan
5	922117106045	KAVIYA K	Kaviya .K
6	922117106046	KOSHIKHA B	Koshikha B.
7	922117106047	LAKSHMI S	Lakshmi
8	922117106048	LAVANYA J	Lavanya J
9	922117106049	LOGA DHARSINI A	Loga .Dharsini
10	922117106050	MANIRAJA P	Maniraja
11	922117106051	MARUTHARASU V	Marutharasu
12	922117106052	MATHISELVAN R	Mathi Selv
13	922117106053	MITHUNAVARSHINI D S	Mithunavarshini
14	922117106054	MOHAMED IMRAN T	Mohamed imran T
15	922117106055	MONICA P M	P.M. Monica
16	922117106056	MOUNIKA M	Mounika
17	922117106057	NAGALAKSHMI N	Nagalakshmi

18	922117106058	NAGARAJ M	Nagaraj M
19	922117106059	NAMPERUMAL M	Namperumal M
20	922117106060	NANDHA KUMAR M	Nandha
21	922117106061	NANDHINI P	Nandhini P
22	922117106062	NAVANEETHA KRISHNAN J	Navaneetha
23	922117106063	NIVETHA V	Nivetha V
24	922117106064	NIVETHITHA T	T. Niveditha
25	922117106065	OVIYA S	Oviya S
26	922117106066	PADMA BHAGAVATHI S A	Padma Bhagavathy
27	922117106067	PANDIARAJAN S	Pandiarajan
28	922117106068	PARALOGA SELVI I	Paralogaselvi
29	922117106069	PRABHU M	Prabhu
30	922117106070	PRADEEPA M	M. Pradeepa
31	922117106071	PRADEEP RAJA S	Raja S.
32	922117106072	PRAKASH S	Prahal
33	922117106073	PRASANNA M	Prasanna M
34	922117106074	PRAVEEN K	Praveen k.
35	922117106075	PRIYADHARSHINI P (02-02-2000)	P. Priyadarshini
36	922117106076	PRIYADHARSHINI P (10-08-2000)	Priyadarshini
37	922117106077	PRIYADHARSHINI R (06-09-1999)	Dhanya
38	922117106078	RAJALAKSHMI M	Rajalakshmi
39	922117106079	RAJKUMAR K	Rajkumar
40	18LEECE03	VISHNU B	Vishnu B

Faculty Incharge
HOD/ECE
29/3/2020

29/3/2020
HOD/ECE



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Department of Electronics and Communication Engineering

VAC on “VLSI Desig Tools-Verilog and VHDL”

Students Namelist

S.No	Register number	Name of the Student
1.	922117106041	KAARTHIC SHANKAR S
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31.	922117106071	PRADEEP RAJA S
32.	922117106072	PRAKASH S
33.	922117106073	PRASANNA M
34.	922117106074	PRAVEEN K
35.	922117106075	PRIYADHARSHINI P (02-02-2000)
36.	922117106076	PRIYADHARSHINI P (10-08-2000)
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38.	922117106078	RAJALAKSHMI M
39.	922117106079	RAJKUMAR K
40.	18LEECE03	VISHNU B

1.M.Jeyalakshmi , AP/ECE

2.S.R.Ashok Kumar/AP/ECE

Faculty Incharges

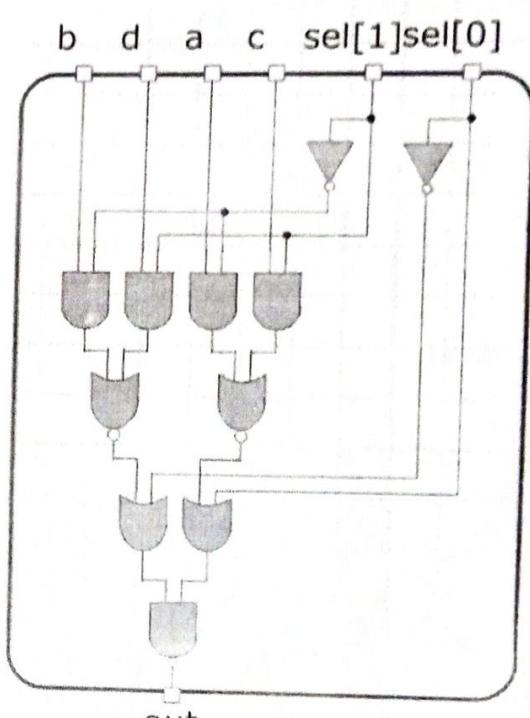
S.Karthigai
HOD/ECE

Dr. S. KARTHIGAI LAKSHMI
Professor & Head
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Dindigul - 624 002

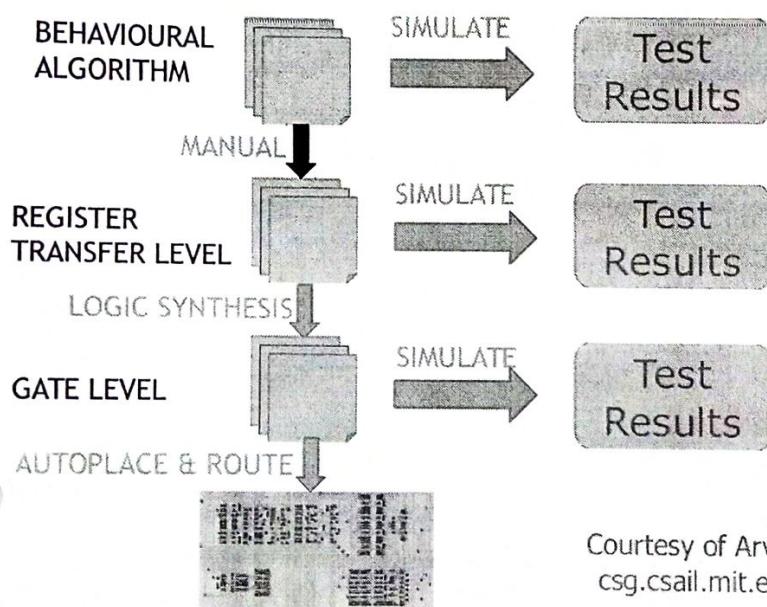
MUX 4 : GATE LEVEL DESIGNING

```
module mux4(input a,b,c,d, input[1:0] sel, output out);
wire[1:0] sel_b;
not not0( sel_b[0], sel[0] );
not not1( sel_b[1], sel[1] );
wire n0, n1, n2, n3;
and and0( n0, c, sel[1] );
and and1( n1, a, sel_b[1] );
and and2( n2, d, sel[1] );
and and3( n3, b, sel_b[1] );
wire x0, x1;
nor nor0( x0, n0, n1 );
nor nor1( x1, n2, n3 );
wire y0, y1;
or or0( y0, x0, sel[0] );
or or1( y1, x1, sel_b[0] );
nand nand0( out, y0, y1 );
endmodule
```

Courtesy of Arvind <http://csg.csail.mit.edu/6.375/>

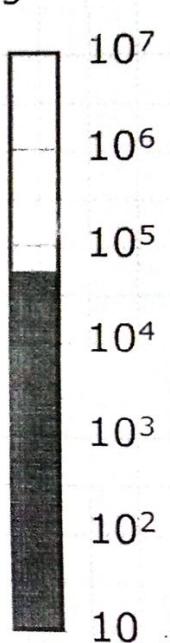


HDLs LED TO TOOLS FOR AUTOMATIC TRANSLATION



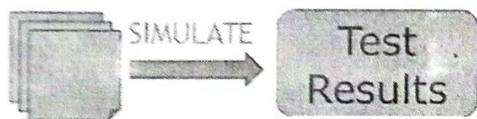
Courtesy of Arvind <http://csg.csail.mit.edu/6.375/>

Number of Gates in Design

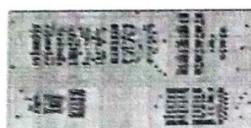


HDLs ENABLED LOGIC LEVEL SIMULATION AND TESTING

GATE LEVEL DESCRIPTION

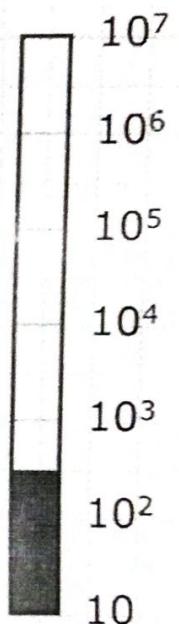


MANUAL

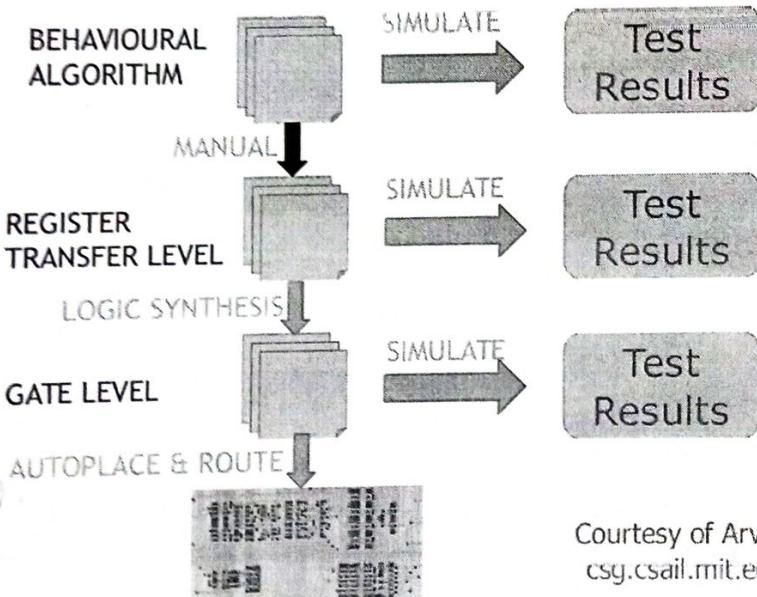


Courtesy of Arvind <http://csg.csail.mit.edu/6.375/>

Number of Gates in Design

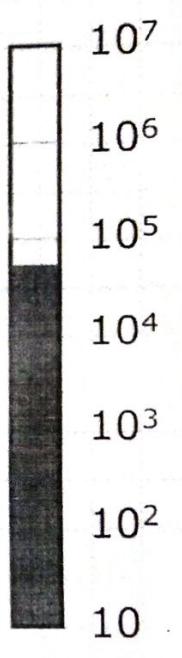


HDLs LED TO TOOLS FOR AUTOMATIC TRANSLATION



Courtesy of Arvind <http://csg.csail.mit.edu/6.375/>

Number of Gates in Design





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Date : 11.01.2020 to 28.03.2020

ASSESSMENT QUESTIONS

1. The Verilog is a hardware description language (3 marks)

- a) Hardware decision language
- b) Hardware description language
- c) Software Description language

2. _____ is a superset of Verilog. (3 marks)

- a) Verilog.
- b) System verilog
- c) System VHDL

3. The Verilog offers more features than the VHDL. (3 marks)

- a) Yes
- b) No

4. Operator which precedes the operand is known as (3 marks)

- a) Unary
- b) Binary
- c) Ternary
- d) None of the above

5. The wait statement is (3 marks)

- a) Level sensitive
- b) Edge sensitive
- c) Both
- d) None

Name : Vishnu .B

(9)



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ASSESSMENT QUESTIONS

Name: Vishnu B (Handwritten)

1. The Verilog is a hardware description language (3 marks)

- a) Hardware decision language
- b) Hardware description language
- c) Software Description language

2. System Verilog is a superset of Verilog. (3 marks)

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- b) System verilog
- c) System VHDL

3. The Verilog offers more features than the VHDL. (3 marks)

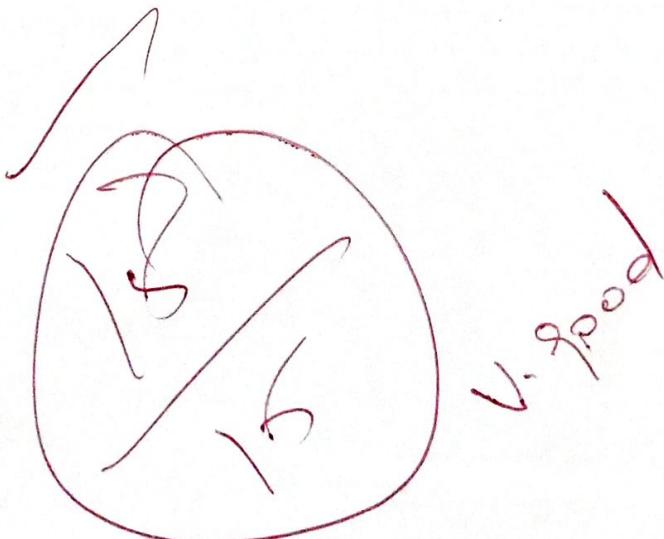
- a) Yes
- b) No

4. Operator which precedes the operand is known as (3 marks)

- a) Unary
- b) Binary
- c) Ternary
- d) None of the above

5. The wait statement is (3 marks)

- a) Level sensitive
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- d) None





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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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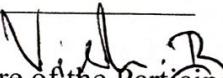
11/01/2020 To 28/03/2020

FEEDBACK FORM

Name of the Participant: **Vishnu B**
Year/Sem :

S.No	Question	Excellent	Good	Satisfactory
1	Did the VAC enlighten your mind	/		
2	Whether your expectation gets satisfied		/	
3	Whether the session was interactive	/		
4	Knowledge gained from this VAC is		/	
5	Was the VAC well organized	/		

Comments on session:


Signature of the Participant



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FEEDBACK FORM

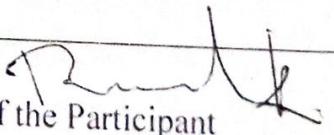
Name of the Participant:
Year/Sem :

Rajkumar. K

S.No	Question	Excellent	Good	Satisfactory
1	Did the VAC enlighten your mind	/		
2	Whether your expectation gets satisfied		/	
3	Whether the session was interactive	/		
4	Knowledge gained from this VAC is	/		
5	Was the VAC well organized	/		

Comments on session:

Good


Signature of the Participant



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
VAC on "VLSI Desig Tools-Verilog and VHDL"

11/01/2020 To 28/03/2020

FEEDBACK FORM

Name of the Participant: *Monika M*

Year/Sem :

S.No	Question	Excellent	Good	Satisfactory
1	Did the VAC enlighten your mind	✓		
2	Whether your expectation gets satisfied		✓	
3	Whether the session was interactive		✓	
4	Knowledge gained from this VAC is		✓	
5	Was the VAC well organized	✓		

Comments on session:

Ni

Monika M
Signature of the Participant



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FEEDBACK FORM

Name of the Participant: *Monika M*

Year/Sem :

S.No	Question	Excellent	Good	Satisfactory
1	Did the VAC enlighten your mind	✓	✓	
2	Whether your expectation gets satisfied		✓	
3	Whether the session was interactive		✓	
4	Knowledge gained from this VAC is		✓	
5	Was the VAC well organized	✓		

Comments on session:

[Signature]

Signature of the Participant



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Assessment Marksheets

S.No.	Reg. No.	Name of the Student	Marks
1	922117106041	KAARTHIC SHANKAR S	15
2	922117106042	KALAIARASAN S	15
3	922117106043	KARTHIK A	15
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15	922117106055	MONICA P M	15
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35	922117106075	PRIYADHARSHINI P (02-02-2000)	15
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38	922117106078	RAJALAKSHMI M	15
39	922117106079	RAJKUMAR K	12
40	18LEECE03	VISHNU B	15

C E R T I F I C A T E

THIS CERTIFICATE IS PRESENTED TO



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11.01.2020 to
28.03.2020

DATE

Dr.D.Senthil Kumaran
Principal

SIGNATURE

C E R T I F I C A T E

THIS CERTIFICATE IS PRESENTED TO

B Manigya.

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28.03.2020

DATE

Du.D.Senthil Kumaran
Principal

SIGNATURE

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Dr.D.Senthil Kumaran
Principal

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