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Original scientific paper

Performance Improvement of SIMD Processor for High-Speed end Devices in IoT Operation Based on Reversible Logic with Hybrid Adder Configuration

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Abstract: The reversible logic function is gaining significant consideration as a style for the logic design by implementing modern Nano and quantum computing with minimal impact on physical entropy. Recent advances in reversible logic allow for computer design applications using advanced quantum computer algorithms. In the literature, significant contributions have been made towards reversible logic gate structures and arithmetic units. However, there are many attempts to dictate the design of Single Instruction-Multiple Data (SIMD) processors. In this research work, a novel programmable reversible logic gate design is verified and a reversible processor design suggests its implementation of SIMD processor. Then, implementing the ripple-carry, carry-select and Kogge-Stone carry look-ahead adders using reversible logic and the performance is compared. The proposed reversible logic-based architecture has a minimum fan out with binary tree structure and minimum logic depth. The simulation result of the proposed design is obtained from Xilinx 14.5 software. From the simulated result, the computational path net delay for 16 × 16 reversible logic with Kogge Stone Adder is 17.247 ns. Compared with 16-bit Kogge Stone Adder, the reversible logic-based 16-bit Kogge Stone Adder gives low power and low time delay. By looking at the speed, energy and area parameters, including fast applications in which two smaller delay and low power adders are required, the effectiveness, including the proper area use of the hybrid adder recommended by it is evaluated.

Keywords: IoT; Kogge-Stone carry look-ahead; quantum; reversible logic; single instruction-multiple data

1 INTRODUCTION

The Internet of Things (IoT) exemplifies a wide range of sensors, computations, and networking that multiply our physical world. As a result, it is shaping up to be one of the most influential technologies in the modern world. IoT is affecting regions spreading over from agriculture [1-3], medical services [4], manufacturing [5] and by empowering unavoidable information assortment to help further investigation. One of IoT's key segments is the sensor hub, normally a little, low-power device with various sensors, remote communication, and an unassuming measure of computation. As these nodes are often set at locations without significant networking or power structures, such as on farms and forests, many sensor nodes are designed to be highly resource-efficient to operate arbitrarily time-efficient automatically. For example, they may work for quite a long time on a little battery [6, 7] and convey through slow and low-power communication networks [8, 9].

While we see development in both data assortment abilities of IoT devices and examination limit on the gathered data, wireless communications' exhibition and power effectiveness have not scaled as much because of actual imperatives. Subsequently, the data assortment limit of low-power IoT gadgets is regularly confined by the upheld data rate and power utilization of its wireless communication module [10-11]. Network advances for IoT devices give a wide spectrum of decisions, traversing from fast and eager for power to moderate and power proficient. One noticeable way to address the communications issue is edge mining, where the IoT nodes themselves play out some calculations to reduce the measure of data to be sent. Some true applications have shown various adders can reduce the data transmission prerequisite by more than 95% [12-15]. In any case, moving calculation to the edge additionally implies the IoT nodes should have critical calculation capacities, which builds the expense and power prerequisites of every node.

In this research work, we present a case reversible logic-based Kogge-Stone carry look-ahead adder for Field-Programmable Gate Arrays (FPGA), improving execution and power effectiveness calculation significantly [16]. Besides, by offloading the calculation initially done at a central server to power-productive FPGAs, this methodology additionally improves the absolute organization's calculation of power proficiency by a significant magnitude [17, 18]. While using redesign hardware such as FPGAs to achieve high performance on the accelerator is not a new idea [19, 20], we provide an instance of a complex adder implementation and in-depth evaluation on performance and power efficiency incorporating wireless communication overhead.

1.1 IoT Applications

The function of IoT devices in different application regions is shown in Fig.1.

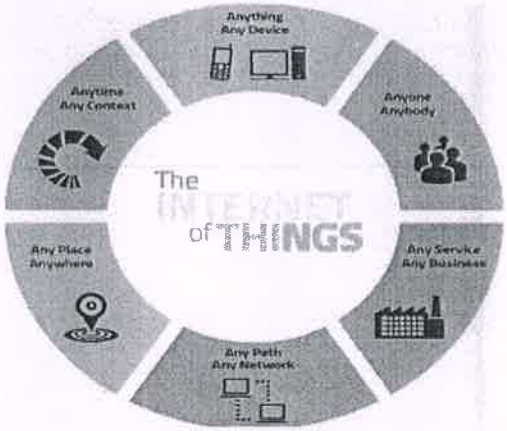

Figure 1 The function of IoT device

The significant destinations for IOT are simply the formation of smart environments/spaces and mindful things (for instance smart vehicle, cities, urban