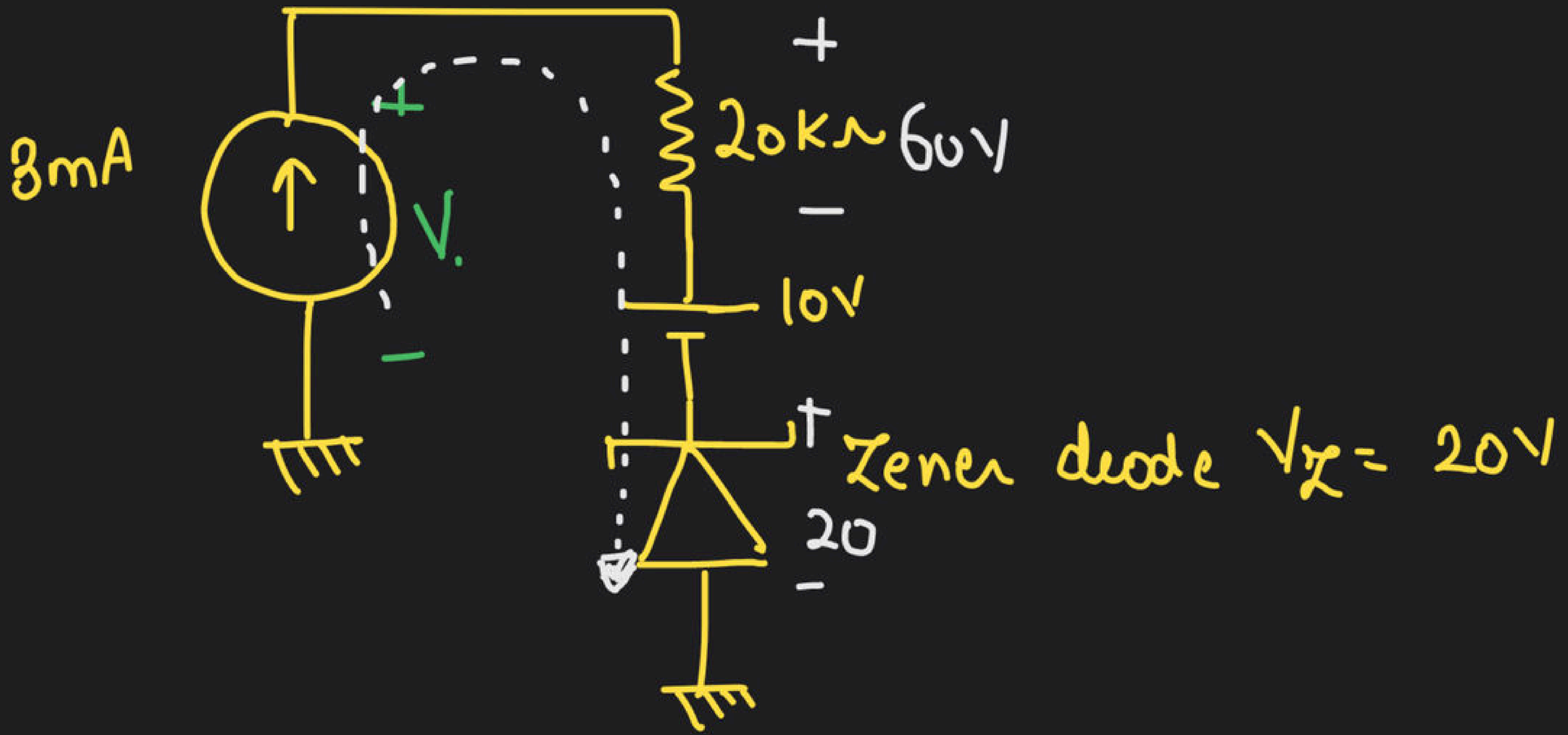
Analog Electronics - LVIII

Lakshya GATE 2023: Course on Analog Electronics for ECE EE IN

Siddharth Sabharwal • Lesson 80 • July 17, 2022


DON'T LET
ONE BAD DAY
MAKE YOU
FEEL LIKE YOU
HAVE A BAD
LIFE.

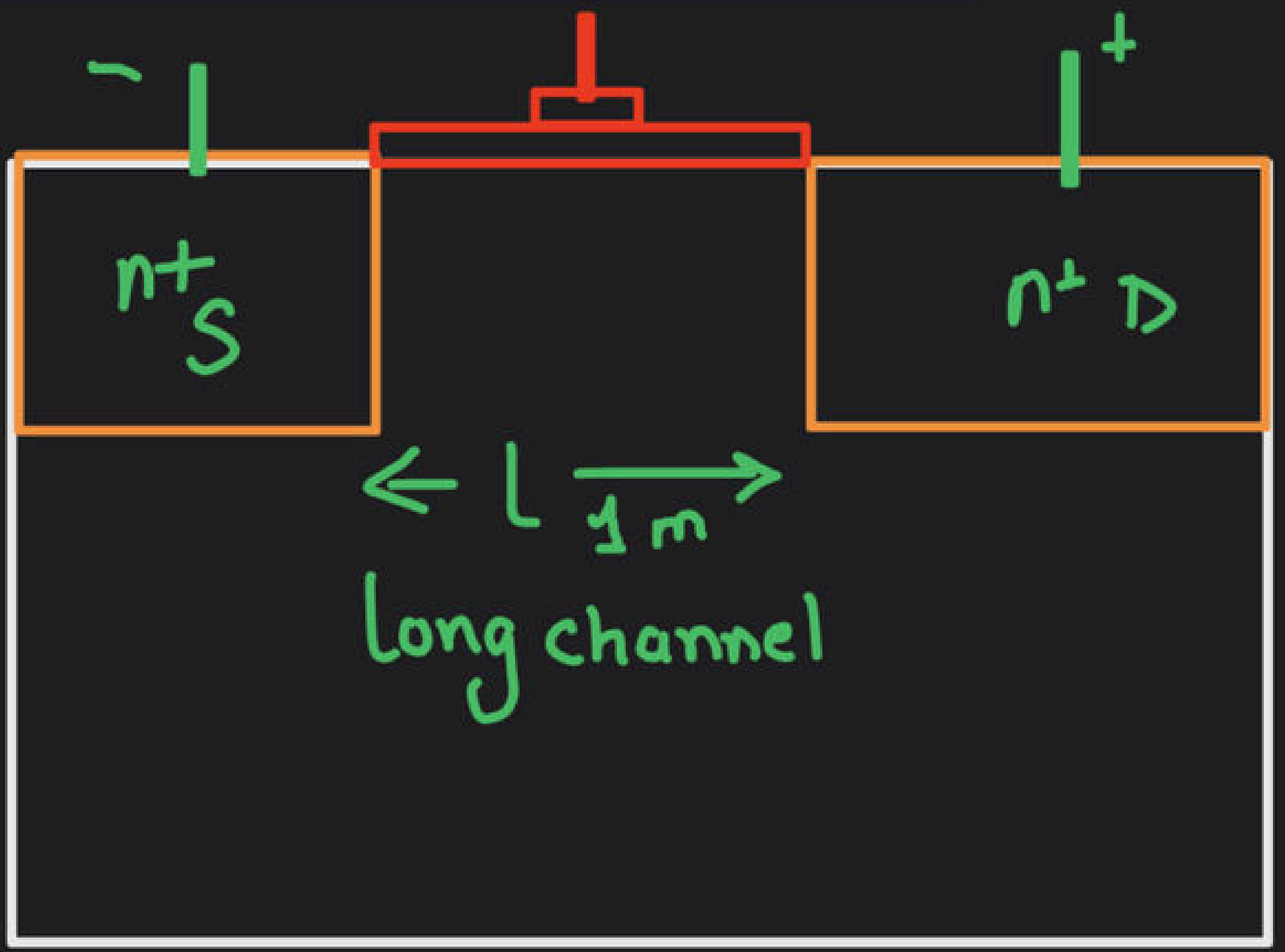
Q 1

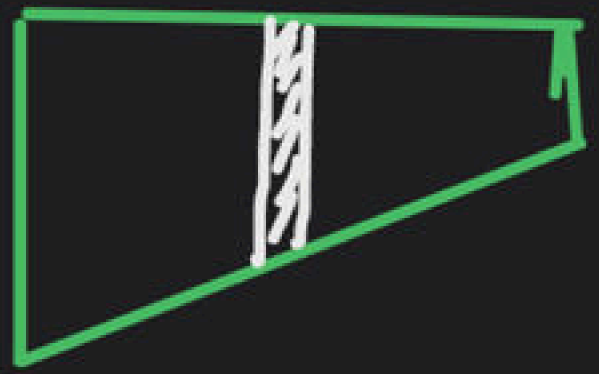


a) 0 b) 30 c) 70 d) 90

Velocity Saturation ⇒

V_{DS}.





$$Q(x) = C\left[V_{GS} - V(x) - V_{th}\right] w \cdot \Delta x$$

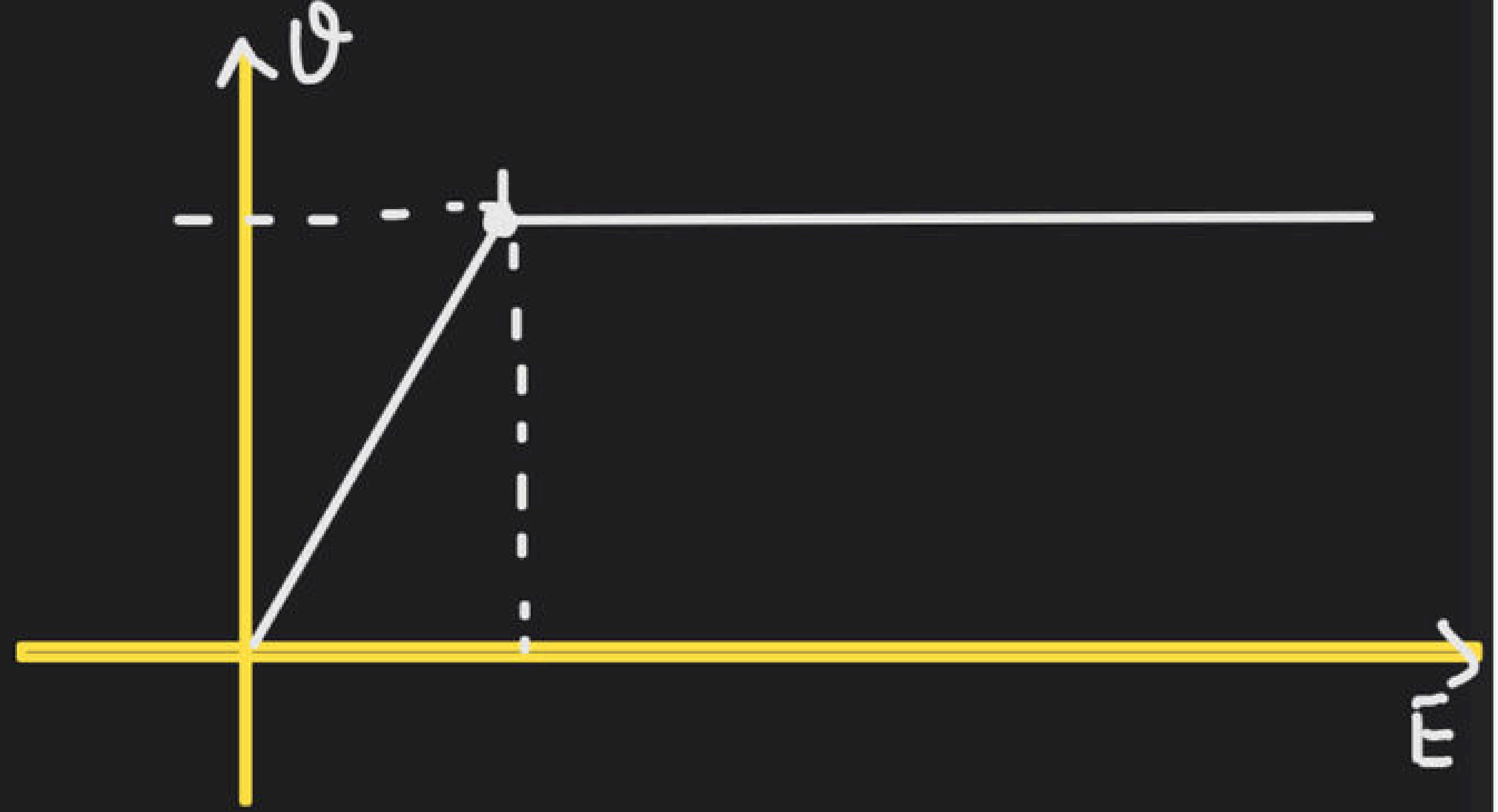
$$I = \frac{dQ}{dt} = C\left[V_{GS} - V(x) - V_{th}\right] w \frac{\Delta x}{\Delta t}$$

$$\boxed{v = \mu E(x)}$$

- due to velocity Sat. the $\frac{\Delta x}{\Delta t}$

i.e. velocity is Const.

why velocity Saturation :- because when channel length reduces then the Electric field in channel obtain a very high value that leads to saturated or fixed velocity of charges



So Now Current of the device

$$I = C\,[V_{GS} - V(x) - V_{th}]\,W \cdot v_{sat}$$

So what happen due to velocity Saturation:-

Reason :- Reducing channel length of device

it leads to

1. when Velocity Sat Occur then the device Current is independent of V_{DS}
2. I_D in saturation {Prop. to $(V_{GS}-V_{th})^2$} but now it is prop to $(V_{GS}-V_{th})$.

3. If we use these Mosfet as amplifier then Gain reduces.

Body effect in MOSFET ⇒ Only for ECE

(NMOS) (Body p)

$$V_{th} = 2\phi_{FP} + \frac{q N_a x_{dT}}{C_{ox}} + \phi_{ms} - \frac{Q_{ox}}{C_{ox}}$$

$$V_{th} = 2\phi_{FP} + \frac{q N_a}{C_{ox}} \sqrt{\frac{2\varepsilon}{q N_a}\left(2\phi_{FP} + V_{SB}\right)} + \phi_{ms} - \frac{Q_{ox}}{C_{ox}}$$

$$g_m = \frac{\partial i_d}{\partial V_{gs}}$$

$$i_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$$

$$\partial i_d / \partial V_{gs} = \mu_n C_{ox} W/L \, (V_{GS} - V_{th})$$

So if the device has body effect then V_{th} depend on V_{SB} also. thus. (i_d in Sat mode)

$$i_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left[V_{GS} - V_{th} \right]^2$$

$$\frac{\partial i_d}{\partial V_{SB}} = \frac{\partial i_d}{\partial V_{th}} \cdot \frac{\partial V_{th}}{\partial V_{SB}} = (-)\mu_n C_{ox} \frac{W}{L} \left[V_{GS} - V_{th} \right] \cdot \frac{qN_a}{C_{ox}} \sqrt{\frac{2\varepsilon}{qN_A}}$$

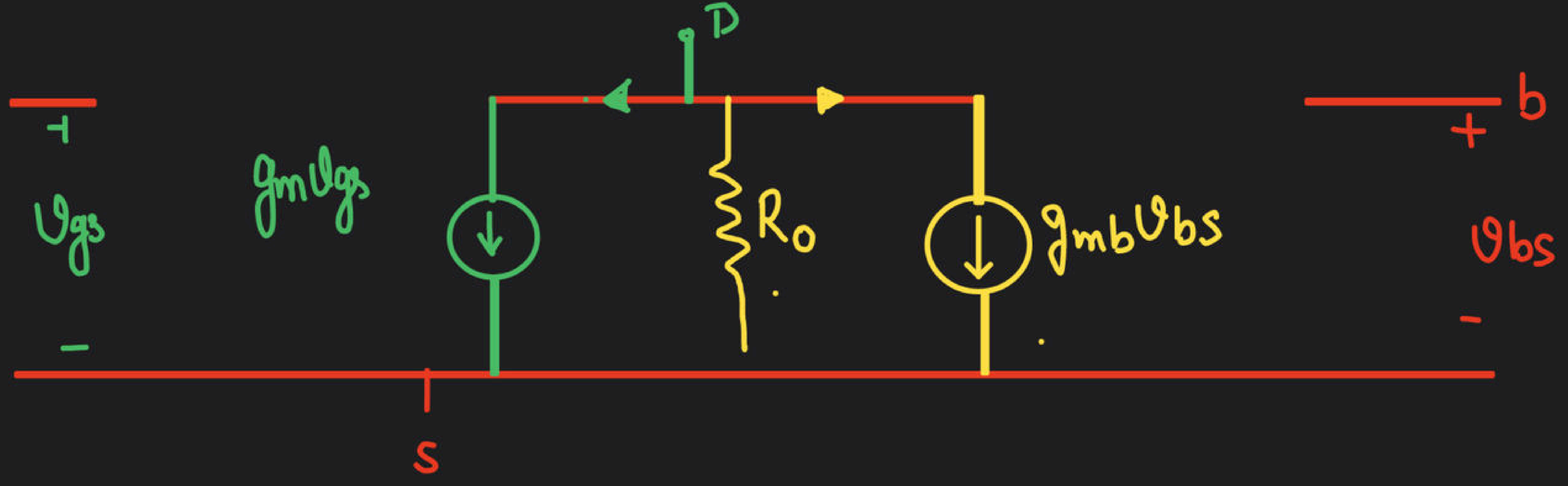
$$\frac{1}{2}(2\phi_{Fp} + V_{SB})^{-1/2}$$

$$\frac{\partial i_d}{\partial V_{SB}} = -g_m \frac{1}{C_{ox}} \sqrt{2\varepsilon qN_A} \; \frac{1}{2}\left(2\phi_{Fp} + V_{SB}\right)^{-1/2}$$

$$\frac{\partial i_d}{\partial V_{bs}} = \boxed{g_m \frac{\sqrt{2qN_a\varepsilon}}{C_{ox}} \frac{1}{2}\left[2\phi_{FP} + V_{SB}\right]^{-1/2} \quad g_{mb}.}$$

Body Gate

Back Gate



N MOS

V_{SB} inc $\rightarrow$ V_{th} inc $\rightarrow$ I_D dec

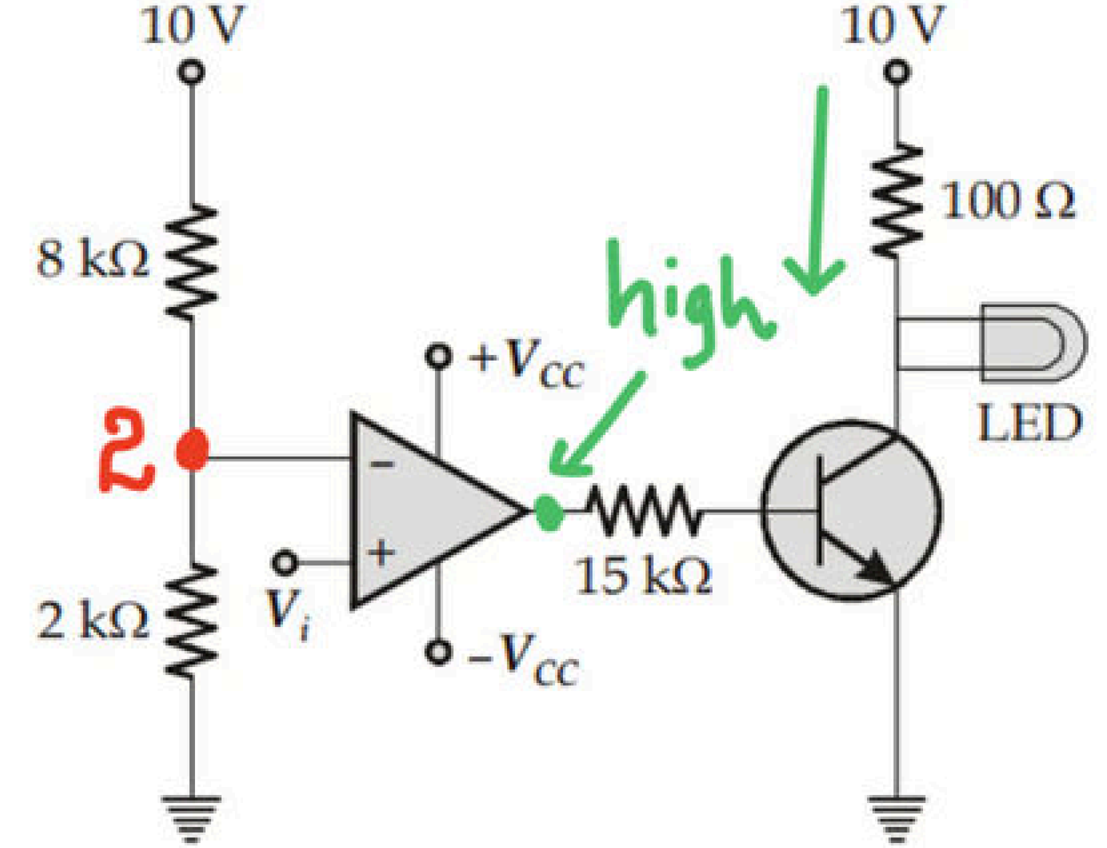
$$\frac{\partial i_d}{\partial v_{SB}} = -ve$$

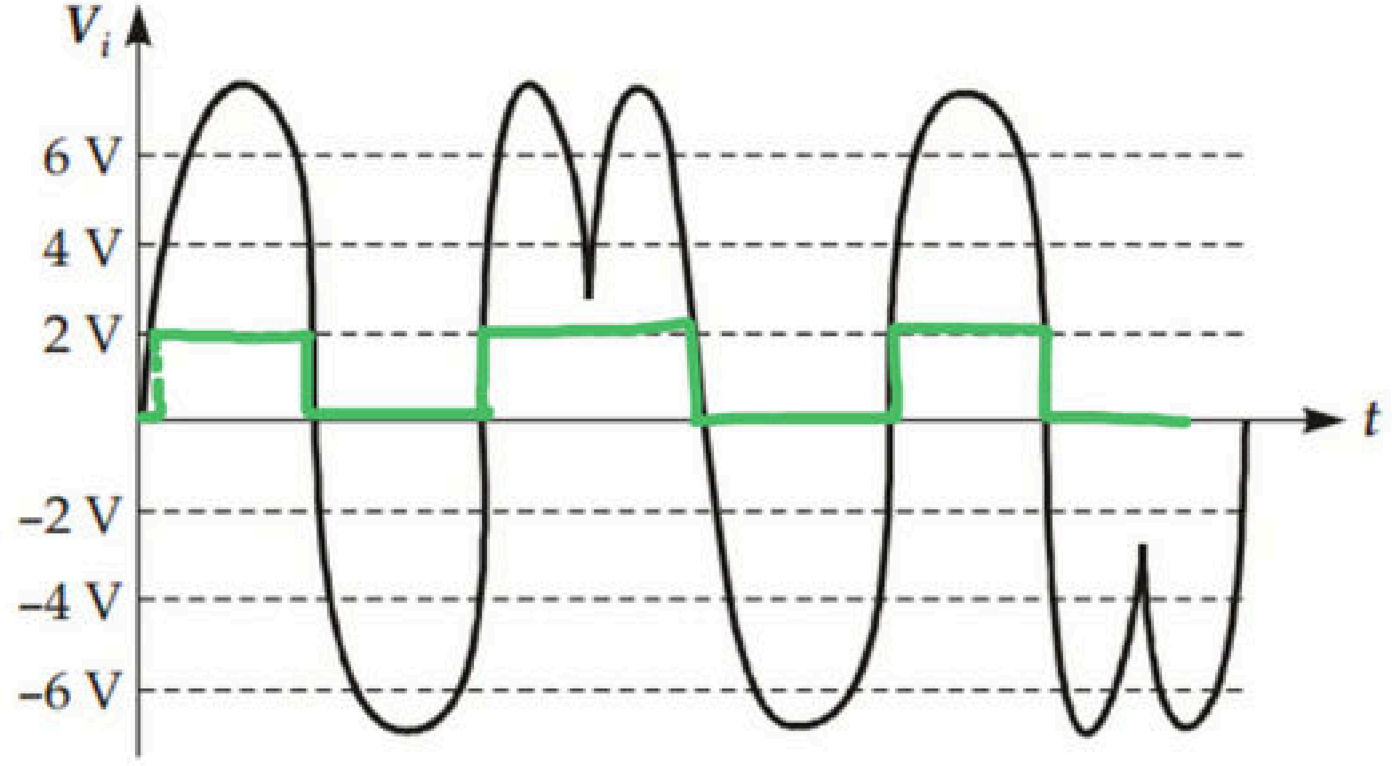
$$\frac{\partial i_d}{\partial v_{bs}} = +v$$

Q
=

Q.66 The following signal V_i of peak voltage 8 V applied to the non-inverting terminal of an ideal op-amp. The transistor has $V_{BE} = 0.7$ V, $\beta = 100$, $V_{LED} = 1.5$ V, $V_{CC} = 10$ V and $-V_{CC} = -10$ V.

$V_i > 2$





The number of times the LED glows is ______ .

[EC-2016 : 1 Mark]

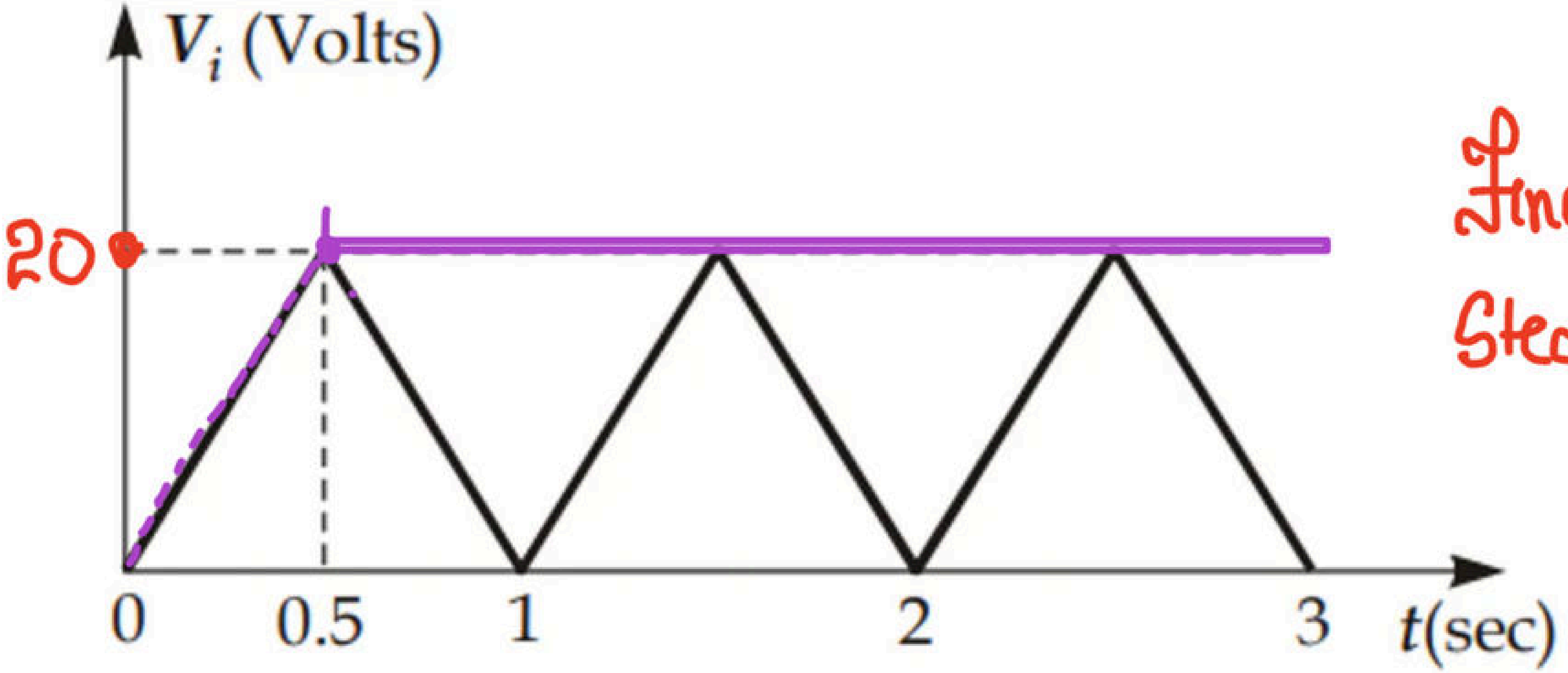
4 a) 3

b) 2

c) 4

d) 5

Q



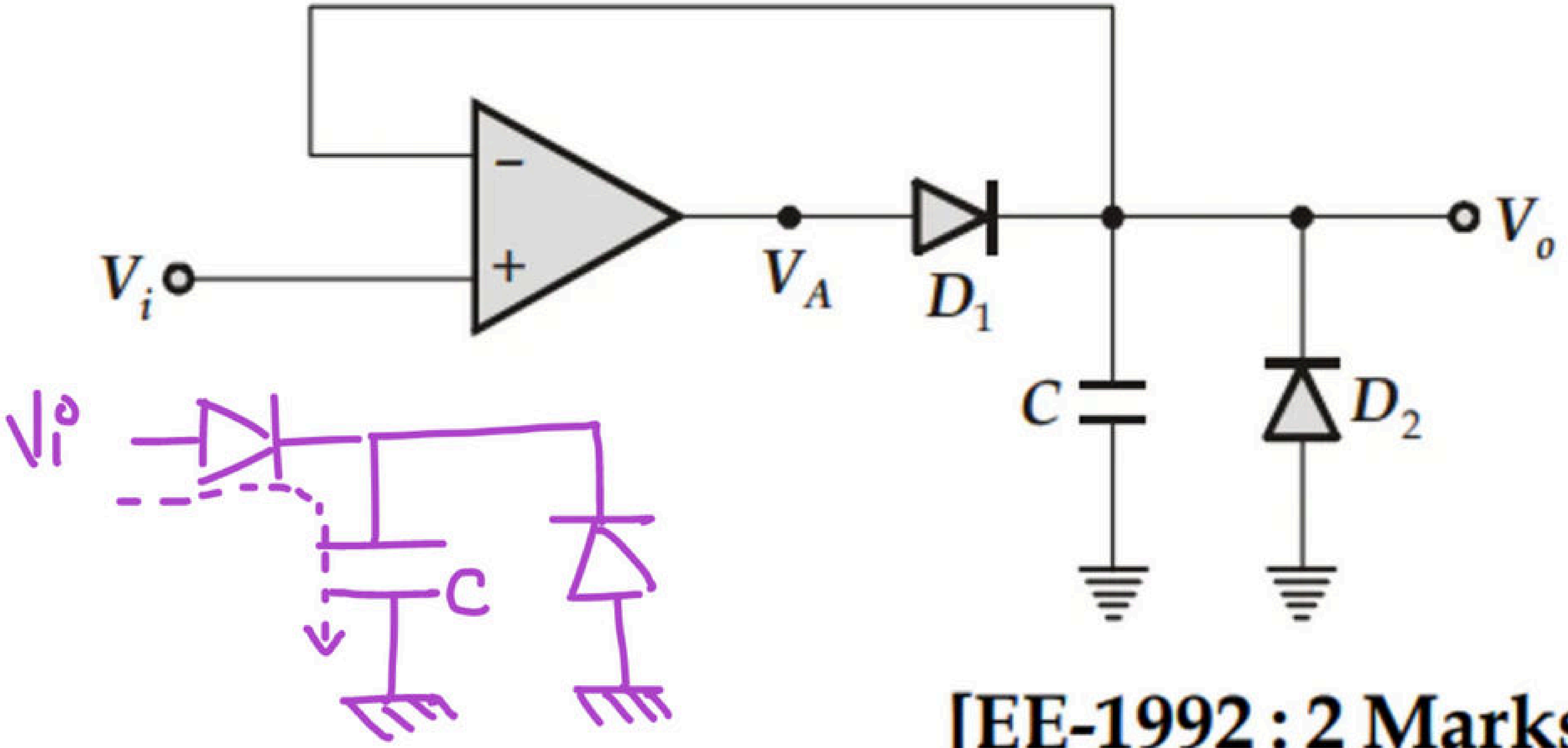
Find avg value of o/p @ Steady state

a) 10

b) 15

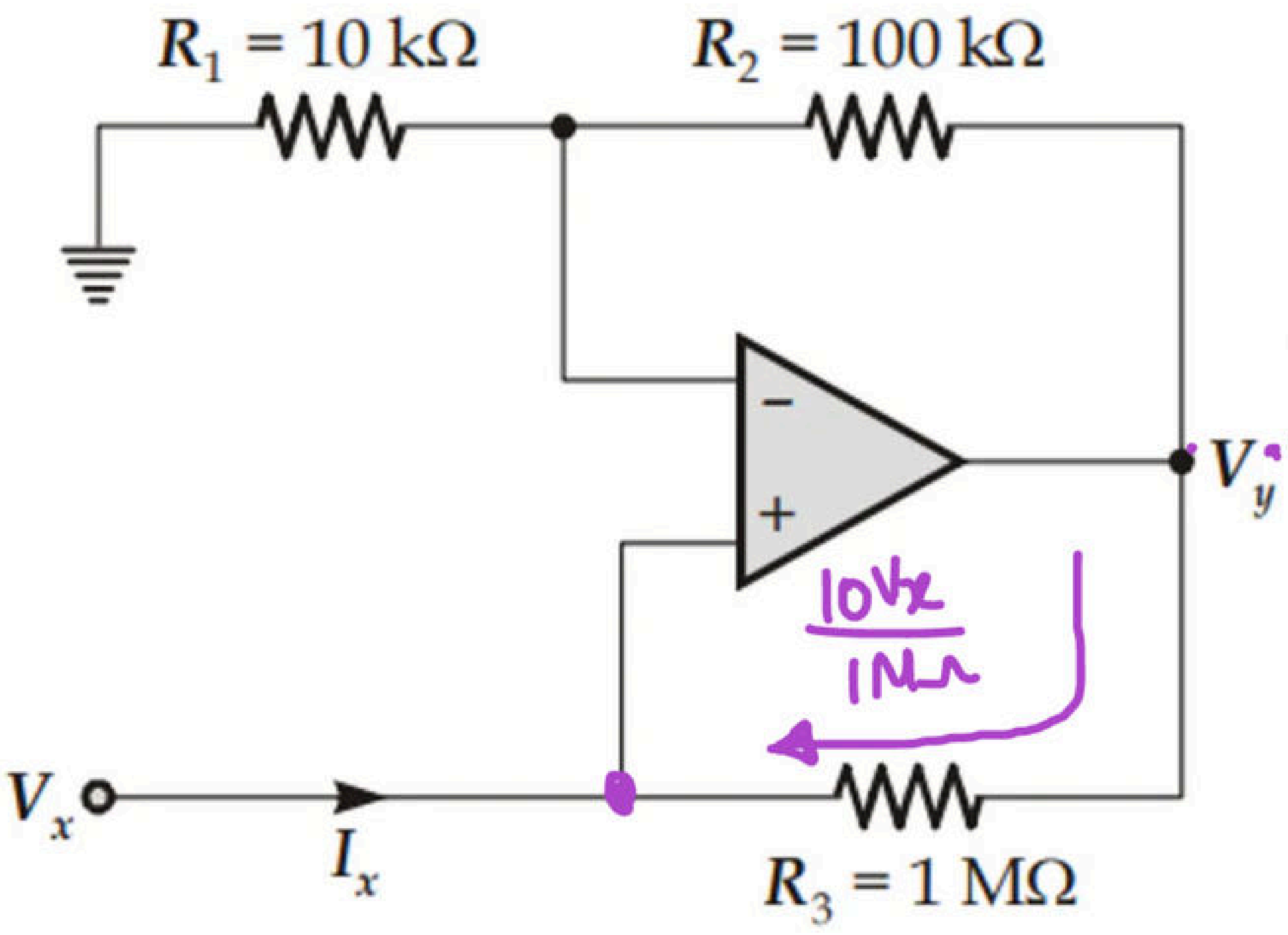
c) 20

d) 25



[EE-1992 : 2 Marks]

The input resistance R_{IN} (= V_x/I_x) of the circuit in figure is



$11V_x$

$\frac{10V_x}{1M\Omega}$

$i_x = -\frac{10V_x}{1M\Omega}$

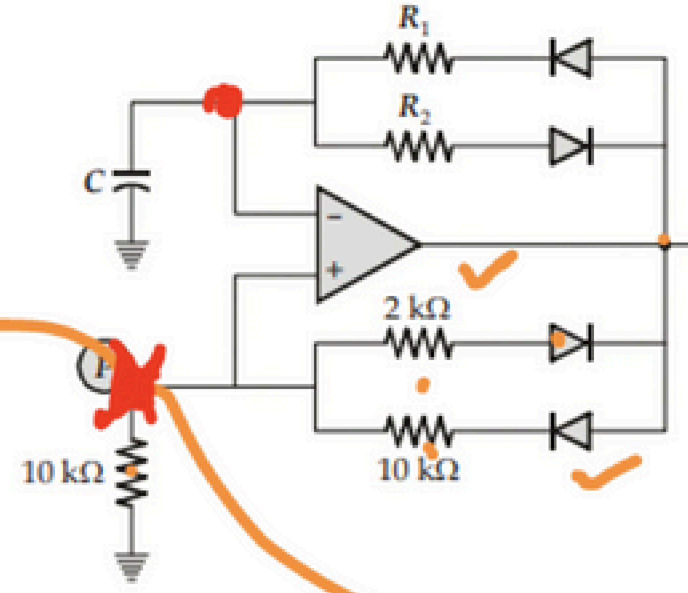
$\frac{V_x}{i_x} = -\frac{10^6}{10}$

(a) +100 kΩ (b) –100 kΩ

(c) +1 MΩ (d) –1 MΩ

[EE-2004 : 2 Marks]

Q.18 A relaxation oscillator is made using op-amp as shown in figure. The supply voltages of the op-amp are ±12 V. The voltage waveform at point *P* will be



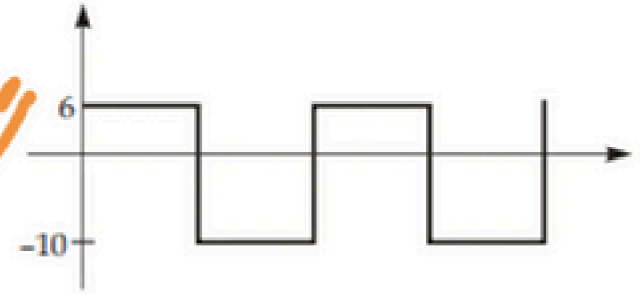
12/-12

$V_p = ?$

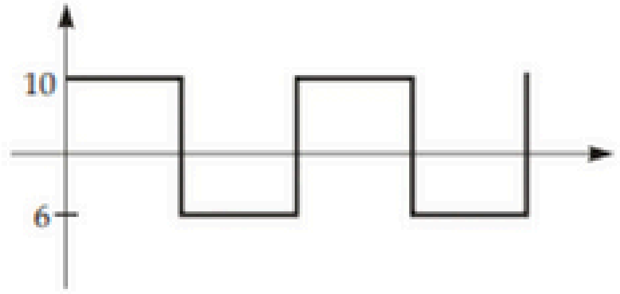
6

-10

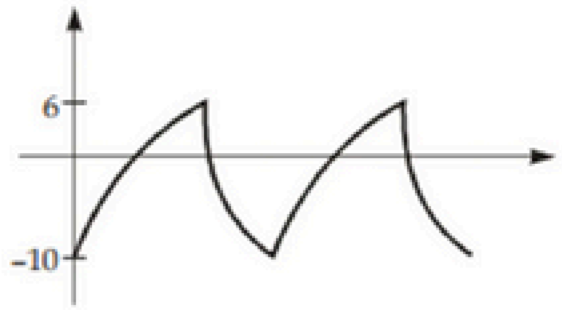
(a)



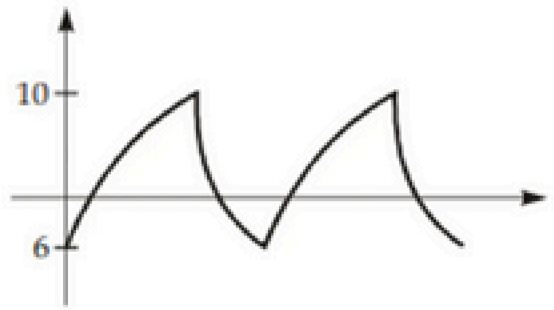
(b)



(c)



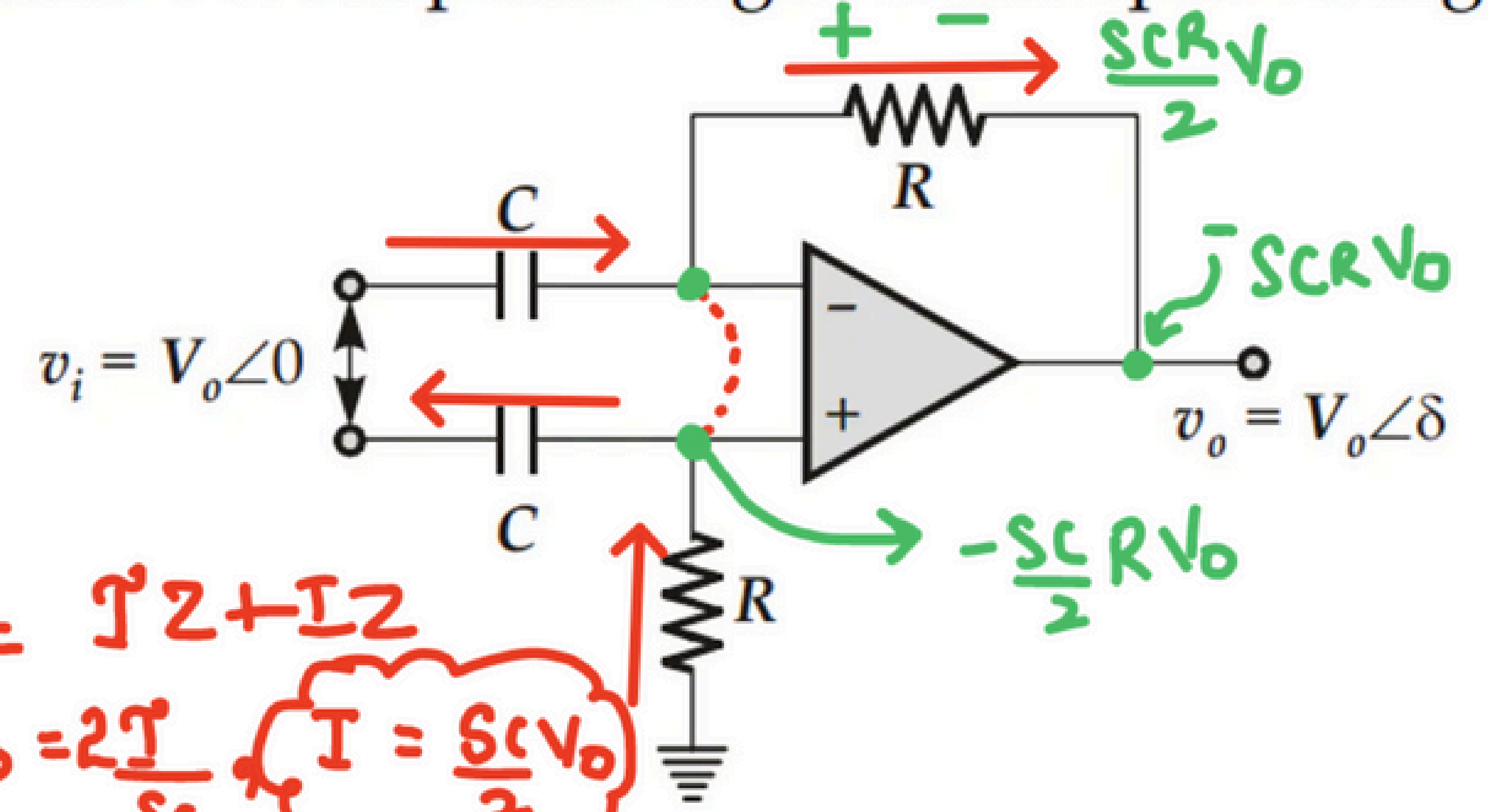
(d)



[EE-2006 : 2 Marks]

Q

Consider the circuit shown in the figure. In this circuit $R = 1\ \text{k}\Omega$, and $C = 1\ \mu\text{F}$. The input voltage is sinusoidal with a frequency of 50 Hz, represented as a phasor with magnitude V_i and phase angle 0 radian as shown in the figure. The output voltage is represented as a phasor with magnitude V_o and phase angle δ (in radian) relative to the phase angle of the input voltage?



$V_o = I'Z + IZ$

$V_o = 2\frac{I}{SC}$ · $I = \frac{SCV_o}{2}$

(a) 0
(b) π
(c) $\frac{\pi}{2}$
(d) $-\frac{\pi}{2}$

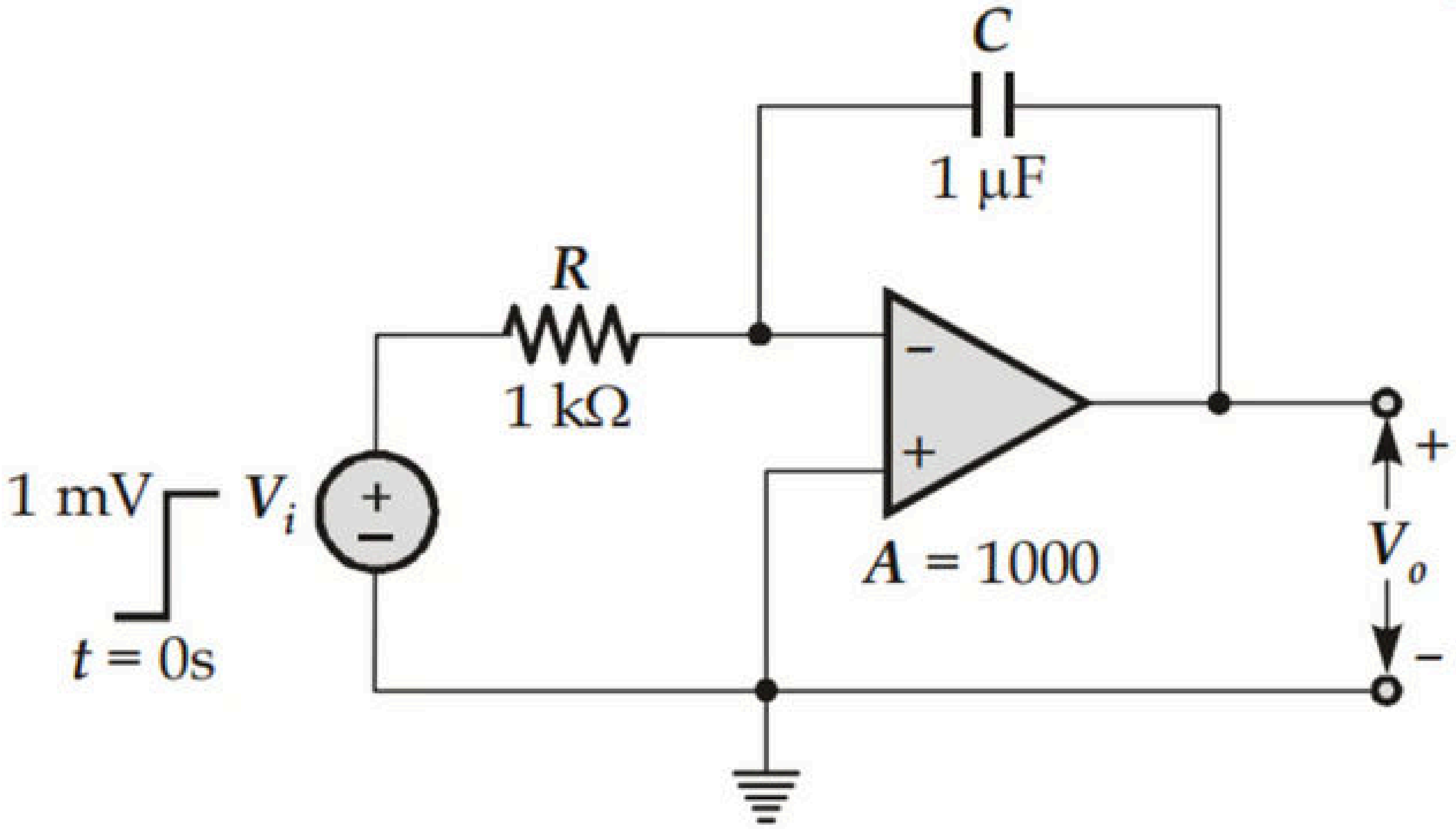
$V_{out} = -SCRV_o$
$= -j\omega CRV_o$
$= -90°$

[EE-2015 : 1 Mark]

Q

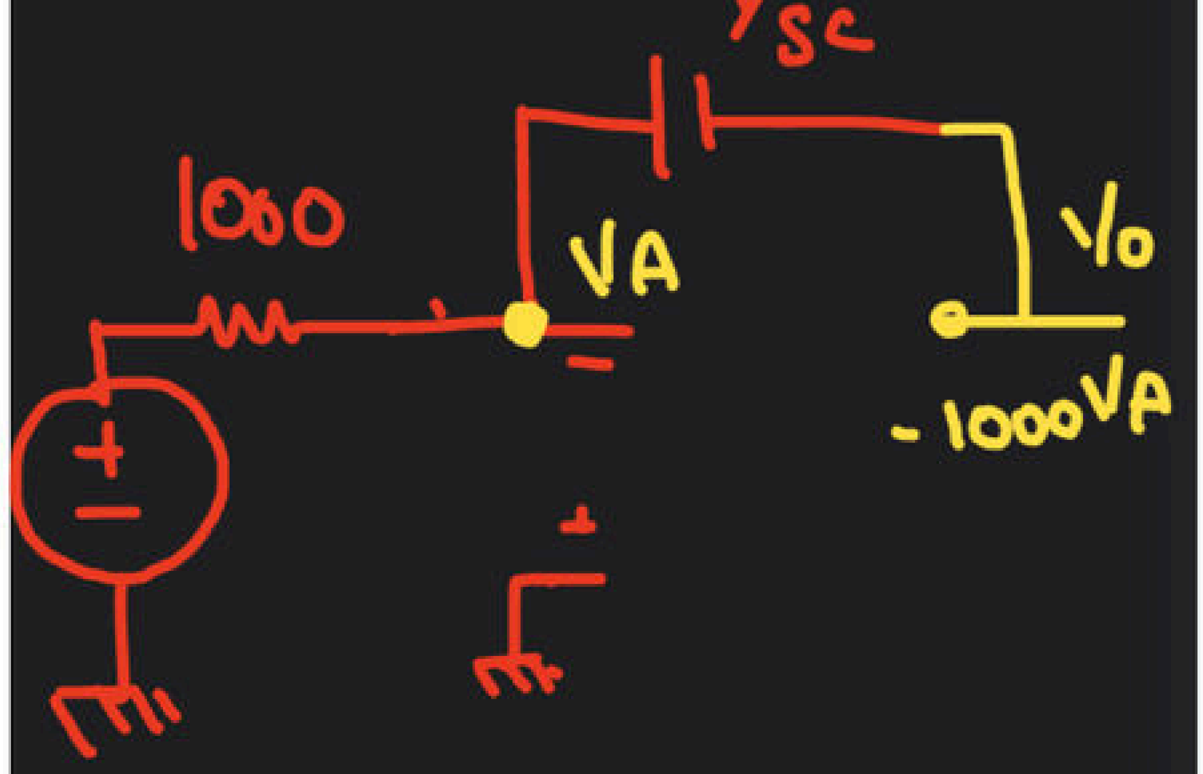
The op-amp shown in the figure has a finite gain $A = 1000$ and an infinite input resistance. A step voltage $V_i = 1$ mV is applied at the input at time $t = 0$ as shown. Assuming that the operational amplifier is not saturated, the time constant (in millisecond) of the output voltage, V_o, is

$\frac{1}{s}$



(a) 1001
(b) 101
(c) 11
~~(d) 1~~

[EE-2015 : 2 Marks]



$$\frac{V_i - V_A}{1000} = \frac{V_A + 1000 V_A}{1/sC}$$

$$V_i = V_A[1001 \times 1000]sC + V_A$$

$$V_i = V_A[1.001]s + V_A$$

$$V_A = \left[\frac{V_i}{1 + 1.001s}\right]$$

$$V_0 = -1000\,V_A = -\frac{1000\,V_{i0}}{(1+1.001\,s)}$$

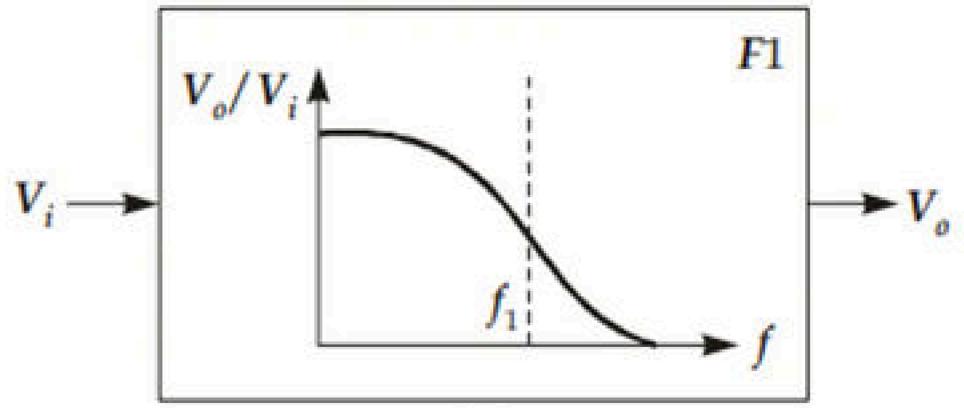
$$= -\frac{1000 \; 1\times10^{-3}}{s(1+1.001\,s)}$$

$$= \left[\frac{A}{s} + \frac{B}{s+\frac{1}{1.001}}\right]$$

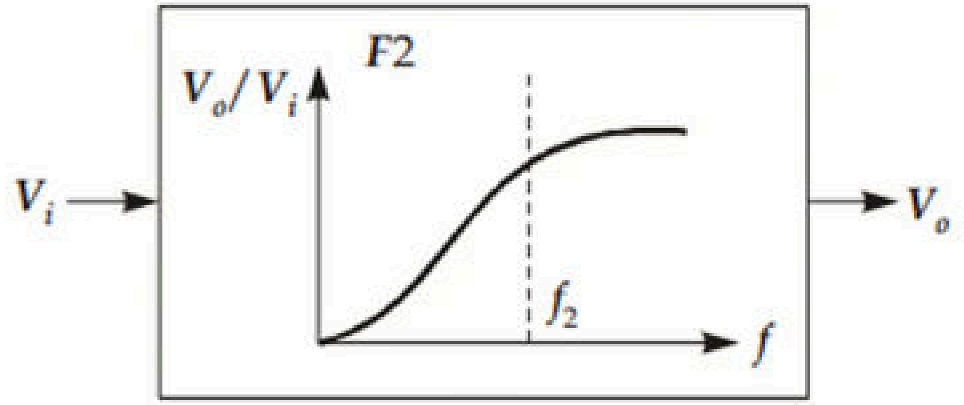
$$e^{-t/1.001}$$

Q

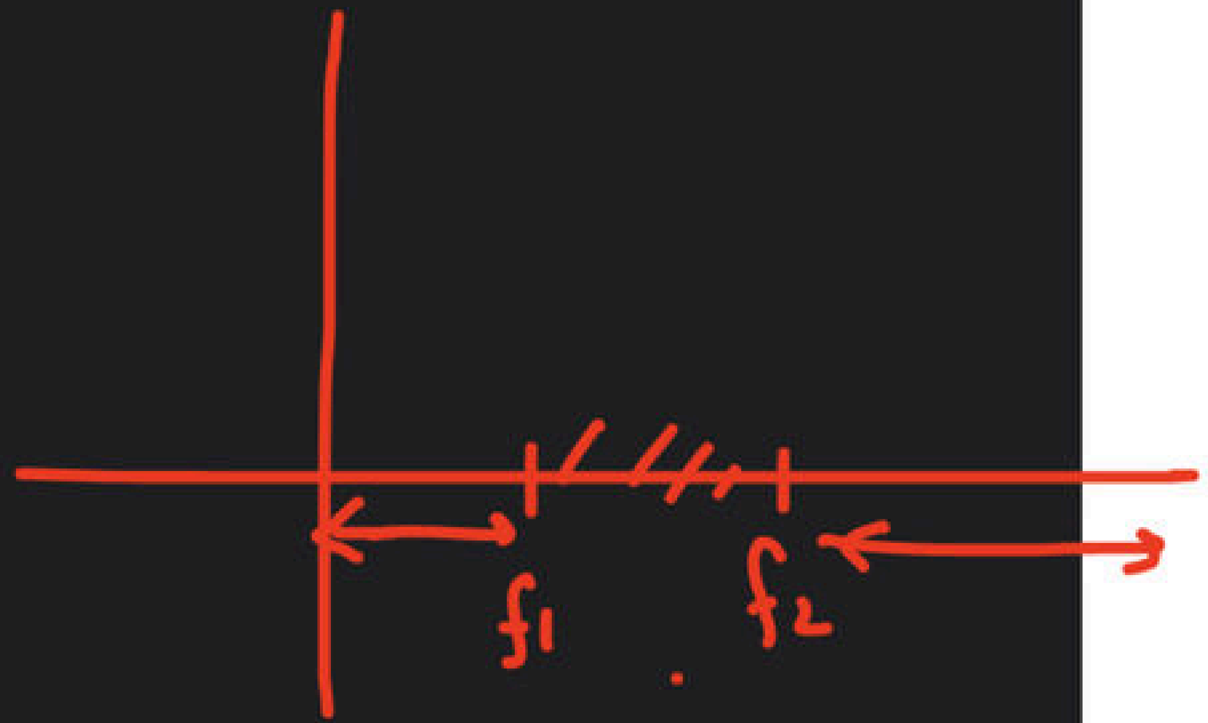
Q.41 The filters $F1$ and $F2$ having characteristics as shown in Fig. (a) and (b) are connected as shown in Fig. (c).

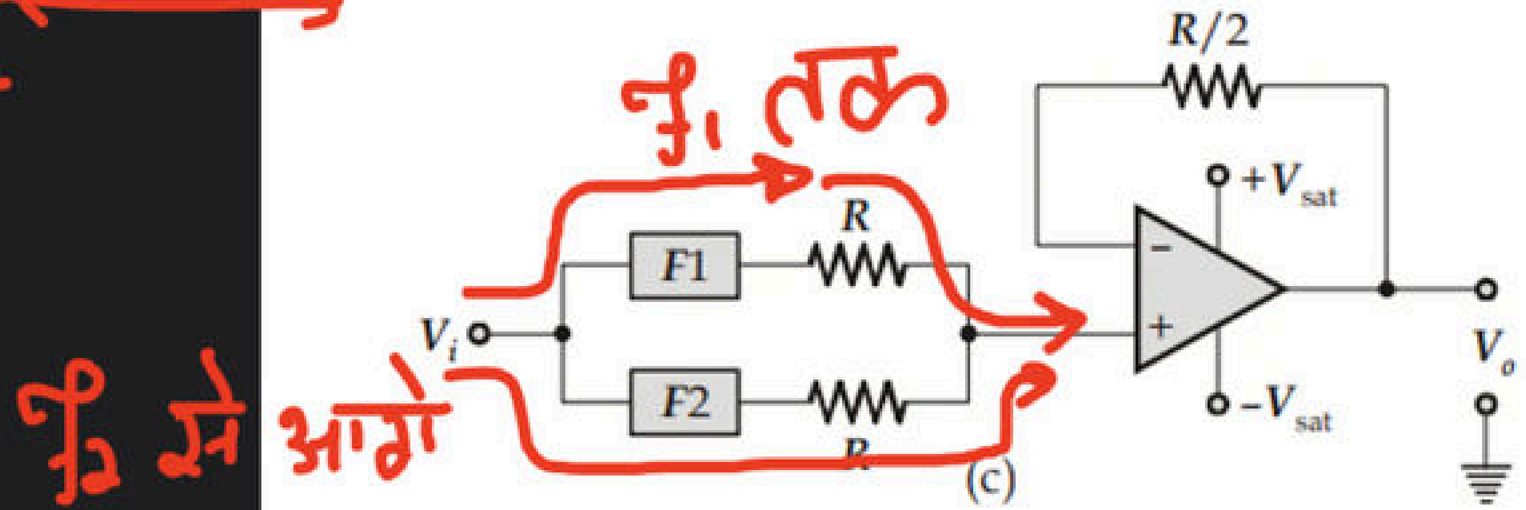


(a)



(b)





(c)

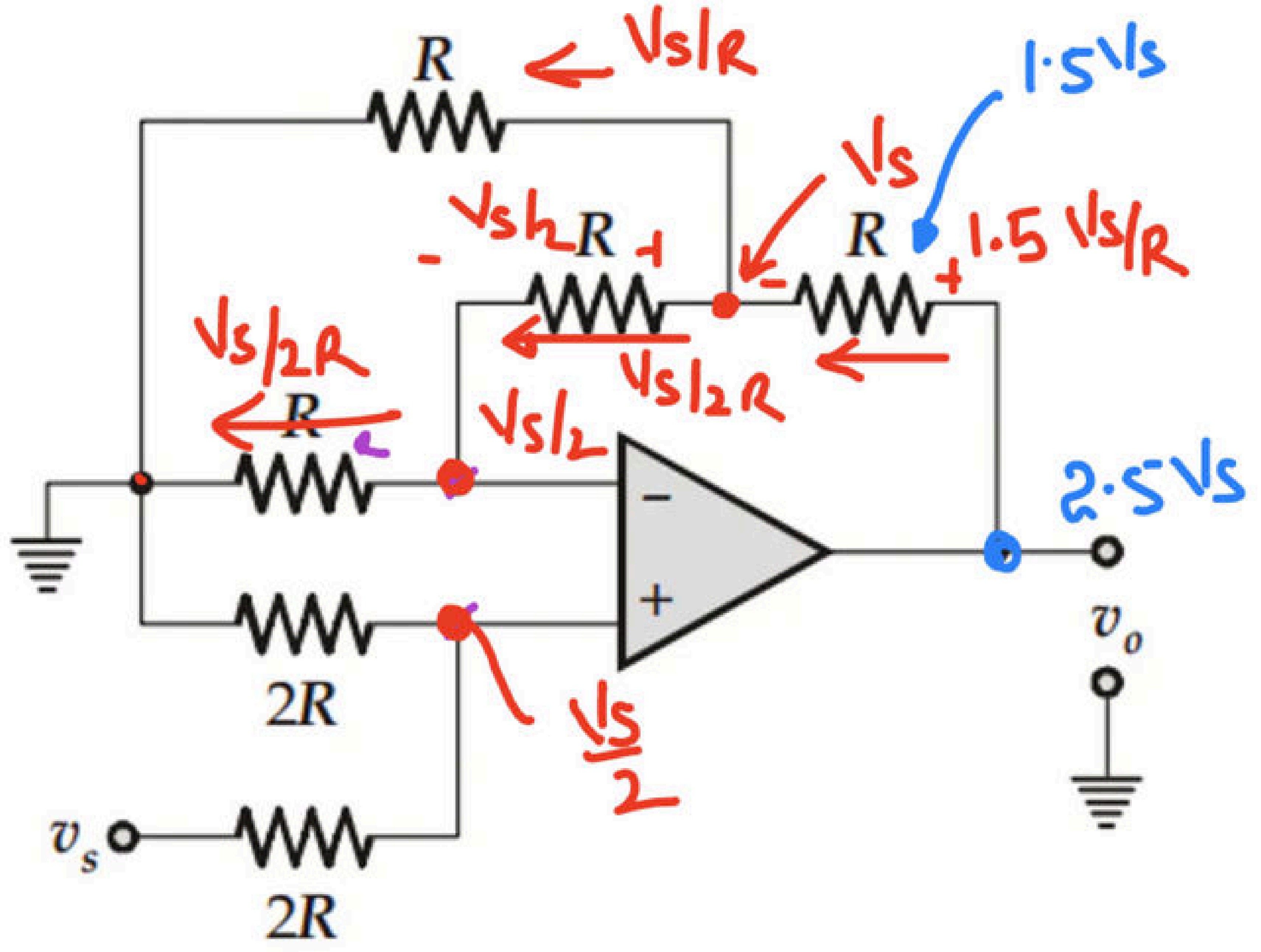
$Q = \frac{W_0}{B.W.}$ ← RLC

The cut-off frequencies of $F1$ and $F2$ are f_1 and f_2 respectively. If $f_1 < f_2$, the resultant circuit exhibits the characteristic of a

(a) Band-pass filter (b) Band-stop filter ✓
(c) All-pass filter (d) High Q-filter → BPF with Small B.W

[EE-2015 : 1 Mark]

For the circuit shown below, assume that the op-amp is ideal. Which one of the following is true?



(a) $v_o = v_s$

(b) $v_o = 1.5\ v_s$

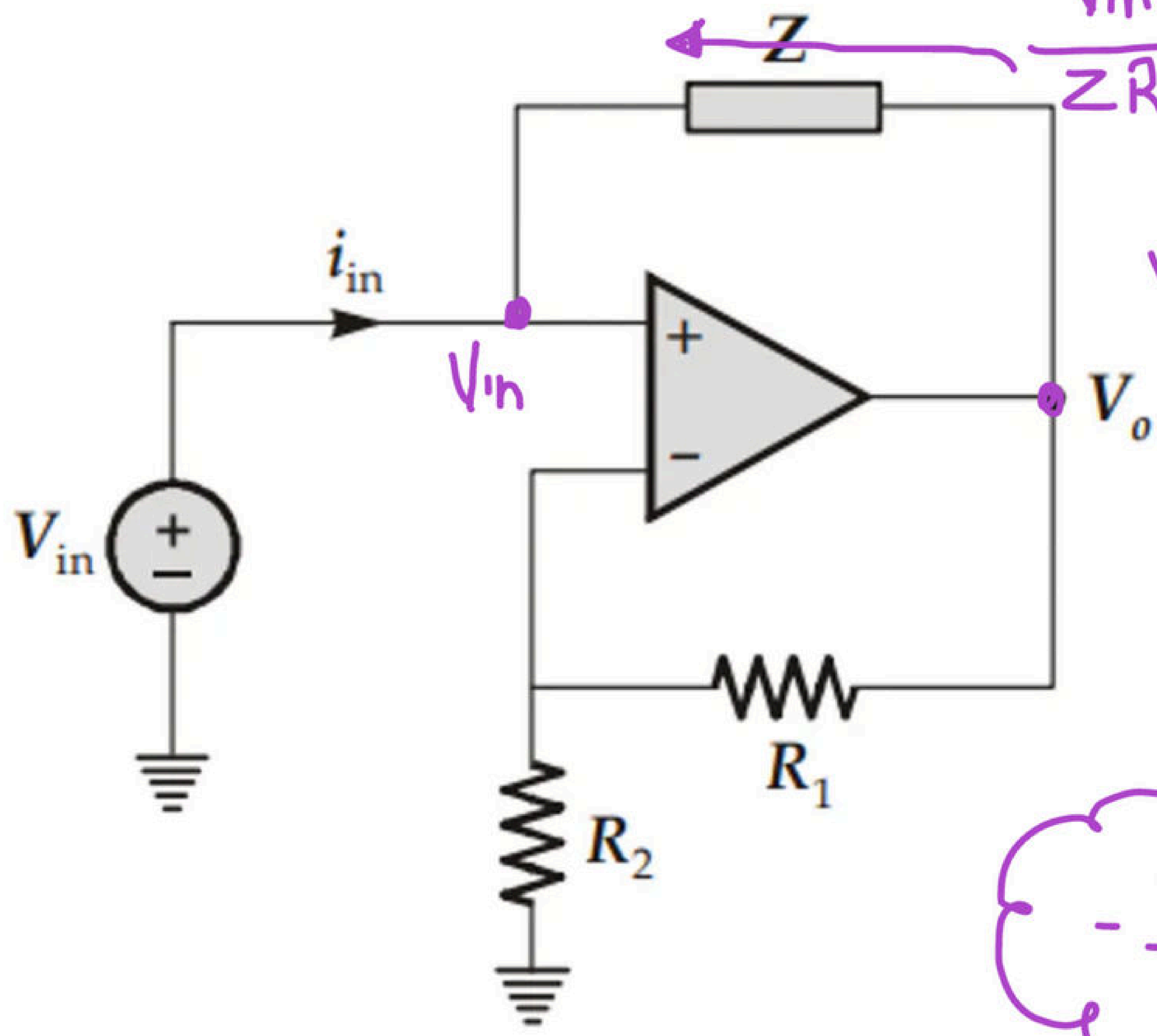
(c) $v_o = 2.5\ v_s$

(d) $v_o = 5\ v_s$

[EE-2017 : 2 Marks]

Q

The op-amp shown in the figure is ideal. The input impedance V_{in}/i_{in} is given by



$$\frac{V_{in}R_1}{ZR_2}$$

$$V_{in}\left(1+\frac{R_1}{R_2}\right)$$

$$i_{in} = -\frac{V_{in}R_1}{ZR_2}$$

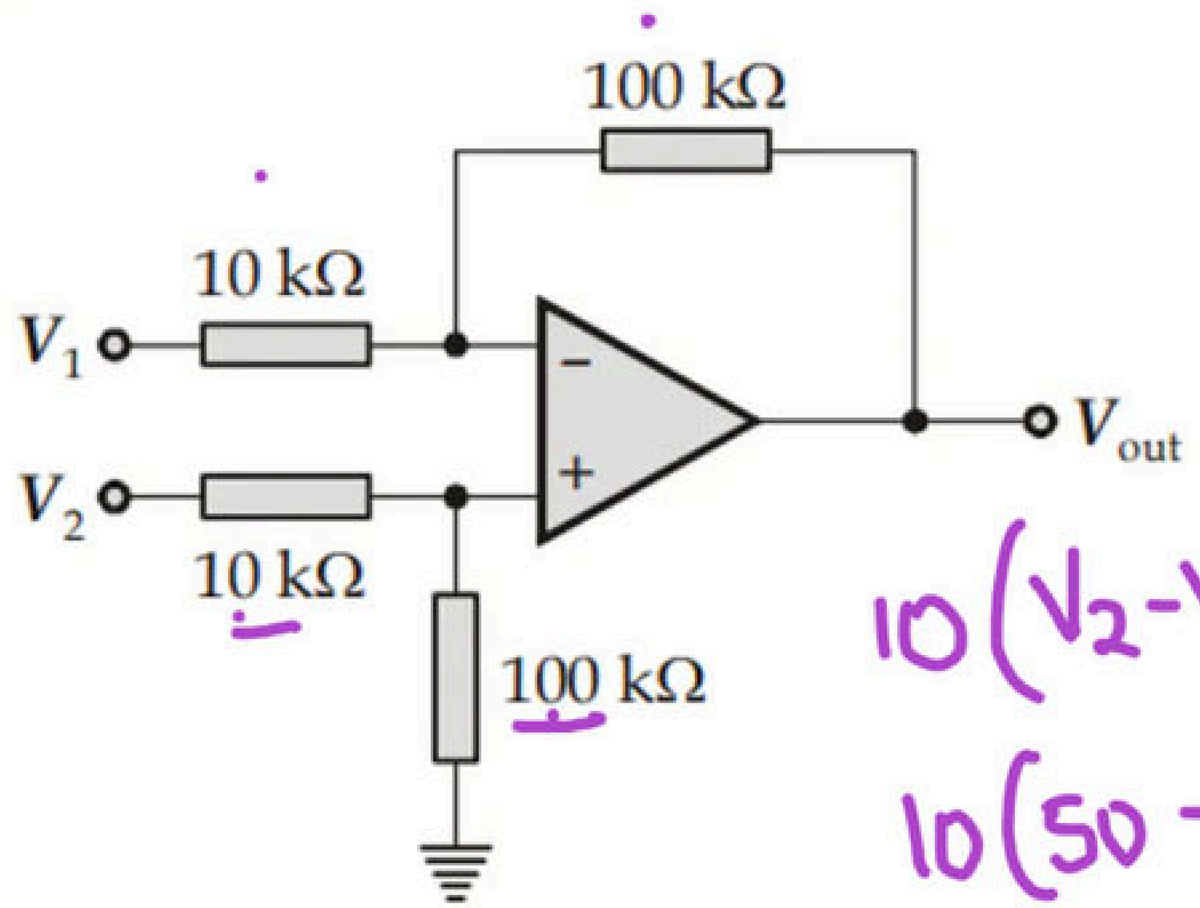
$$-\frac{ZR_2}{R_1}$$

(a) $Z\dfrac{R_1}{R_2}$ (b) $-Z\dfrac{R_2}{R_1}$

(c) Z (d) $-Z\dfrac{R_2}{R_1+R_2}$

[EE-2018 : 1 Mark]

Q.49 In the circuit below, the operational amplifier is ideal. If $V_1 = 10$ mV and $V_2 = 50$ mV, the output voltage (V_{out}), is



$10(V_2 - V_1)$

$10(50 - 10) = 400$

(a) 400 mV (b) 500 mV

(c) 600 mV (d) 100 mV

[EE-2019 : 2 Marks]

(a) –1 V to –2 V (b) –2 V to –4 V

(c) +1 V to –2 V (d) +2 V to –4 V

[EE-2014 : 2 Marks]

Q.26 A non-ideal diode is biased with a voltage of –0.03 V, and a diode current of I_1 is measured. The thermal voltage is 26 mV and the ideality factor for the diode is 15/13. The voltage, (in V), at which the measured current increases to $1.5I_1$ is closest to

(a) –4.50 (b) –0.09

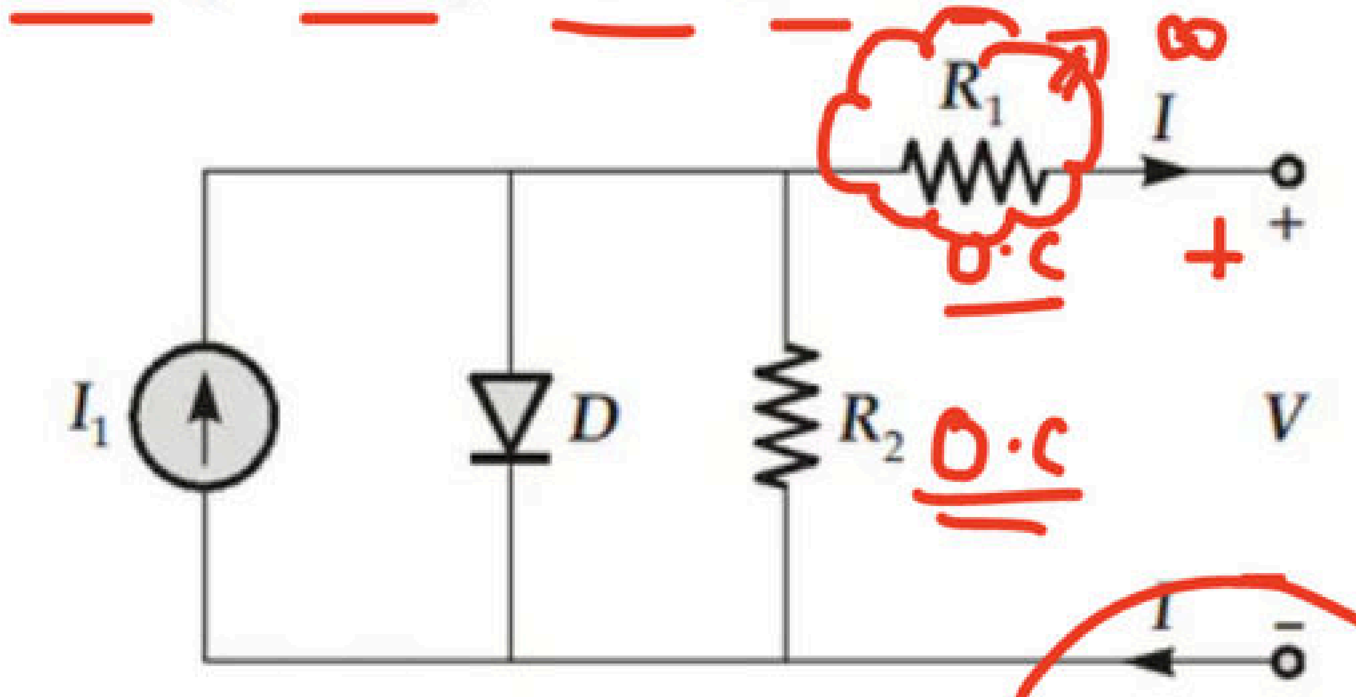
(c) –0.02 (d) –1.50

[EE-2020 : 2 Marks]

Q.27 Consider the diode circuit shown below. The diode, D, obeys the current-voltage characteristic,

$$I_D = I_s\left(\exp\left(\frac{V_D}{nV_T}\right)-1\right)$$

where $n > 1$, $V_T > 0$, V_D is the voltage across the diode and I_D is the current through it. The circuit is biased so that voltage, $V > 0$ and current, $I < 0$. If you had a design this circuit to transfer maximum power from the current source (I_1) to a resistive load (not shown) at the output, what values R_1 and R_2 would you choose?



(a) ~~Small R_1 and small R_2~~

(b) Large R_1 and large R_2

(c) $\boxed{\text{Small } R_1 \text{ and large } R_2}$

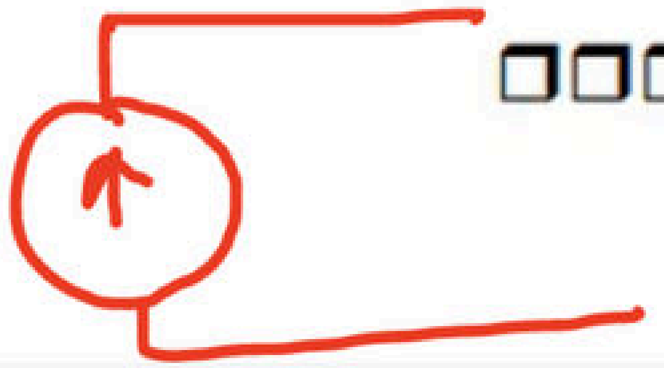
(d) ~~Large R_1 and small R_2~~

$R_1 = 0$

$R_2 = \infty$

[EE-2020 : 2 Marks]

$R_2 = 0$ large



$$I = I_s\left(e^{V/nV_T} - 1\right)$$

$$I_1 = -.632\, I_s$$

$$1.5\, I_1 = -.948\, \cancel{I_s} = \cancel{I_s}\left(e^{V/nV_T} - 1\right)$$

$$V = -.088\ldots$$

$$= -.09$$