Analog Electronics Session No XXXI

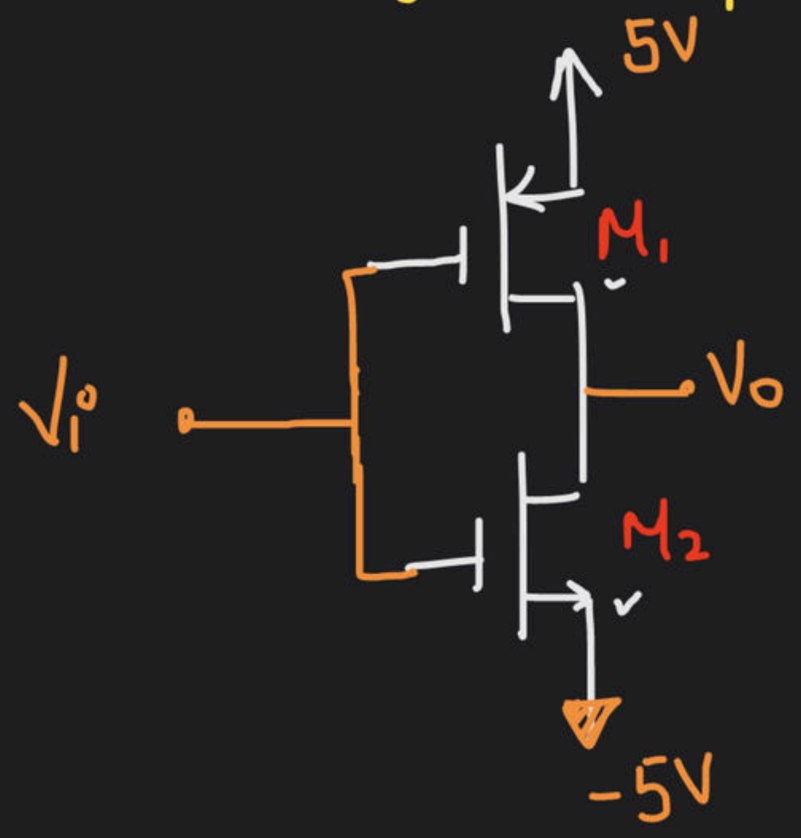
Lakshya GATE 2023: Course on Analog Electronics for ECE EE IN

Siddharth Sabharwal • Lesson 41 • June 6, 2022


SUCCESS
DOESN'T
COME TO YOU,
YOU GO TO IT.
MARVA COLLINS

Topic CMOS inverter :-

The combination of Pmos and NMOS :- $|V_{th}| = 1$



if $V_i = -5V$,

1) $V_{SG} = 10V$.

2) $V_{GS} = 0$.

So M_2 is off

and M_1 is ohmic

So we will get $V_o = 5$,

$V_{GS} < 1$

$V_i - (-5) < 1$

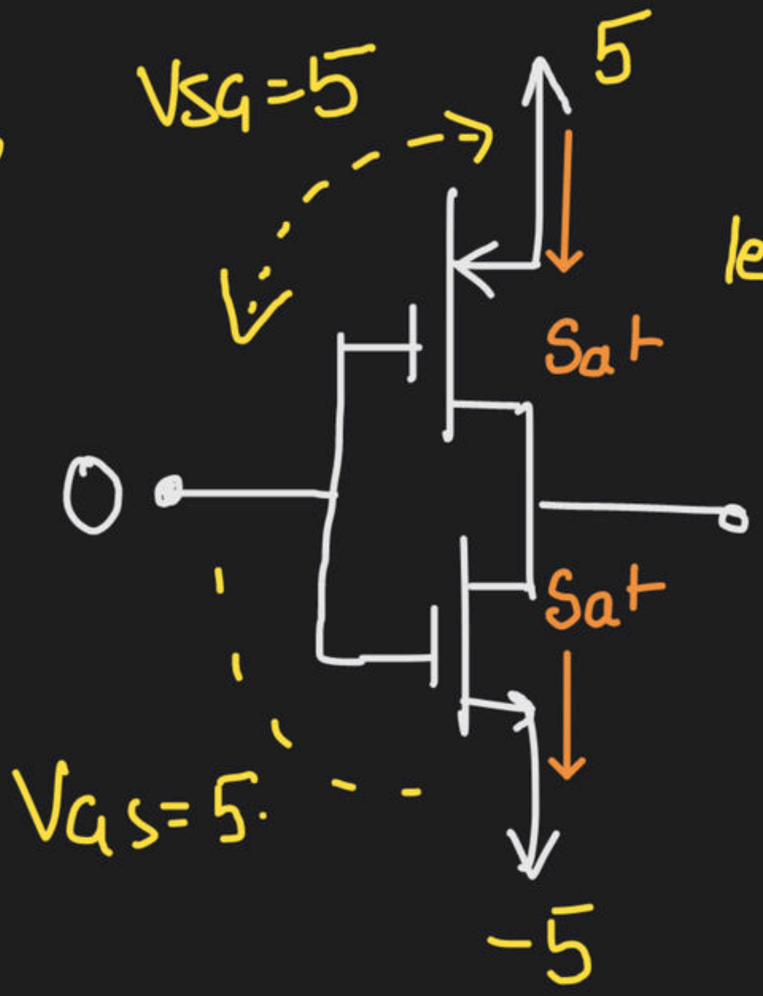
$V_i < -4$

Now when V_i is inc above -4 then M_2 will turn on and will enter sat mode

as V_i inc V_{SG} of M_1 dec and thus resistance of M_1 in ohmic mode $\left[R = \frac{1}{\mu_p C_{ox} \frac{W}{L}\left[V_{SG} - |V_{th}|\right]}\right]$

thus as V_{SG} dec R. of M_1 inc and thus V_o dec.

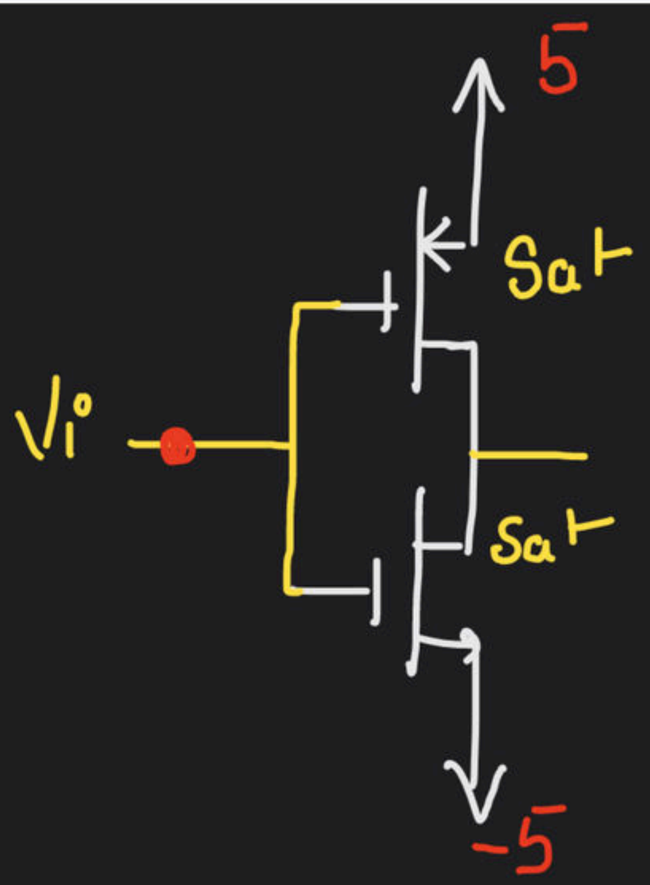
When $V_i = 0$ then



$$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} \left[V_{SG} + |V_{tp}| \right]^2$$

let $\mu_p = \mu_n$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(V_{gs} - V_{tn} \right)^2$$



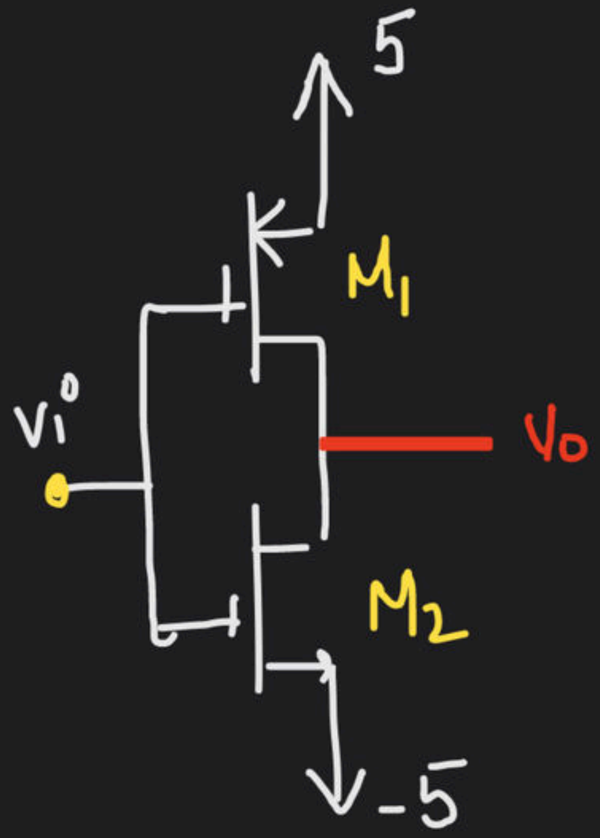
$V_{th} = 1, -1$

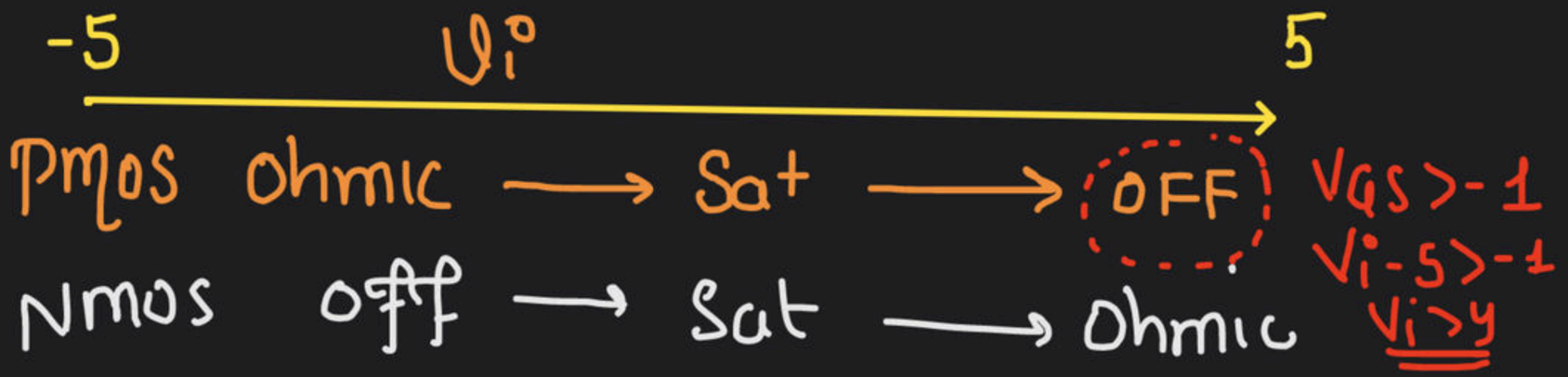
$I_{D1} = I_{D2}$ KCL

$\frac{1}{2} \cancel{\mu_n C_{ox}} \frac{W}{L} \left[V_{GS} - \cancel{V_{th}} \right]^2$

$= \frac{1}{2} \cancel{\mu_p C_{ox}} \frac{W}{L} \left[V_{SG} - \cancel{V_{th}} \right]^2$

$V_{GS} = V_{SG}$



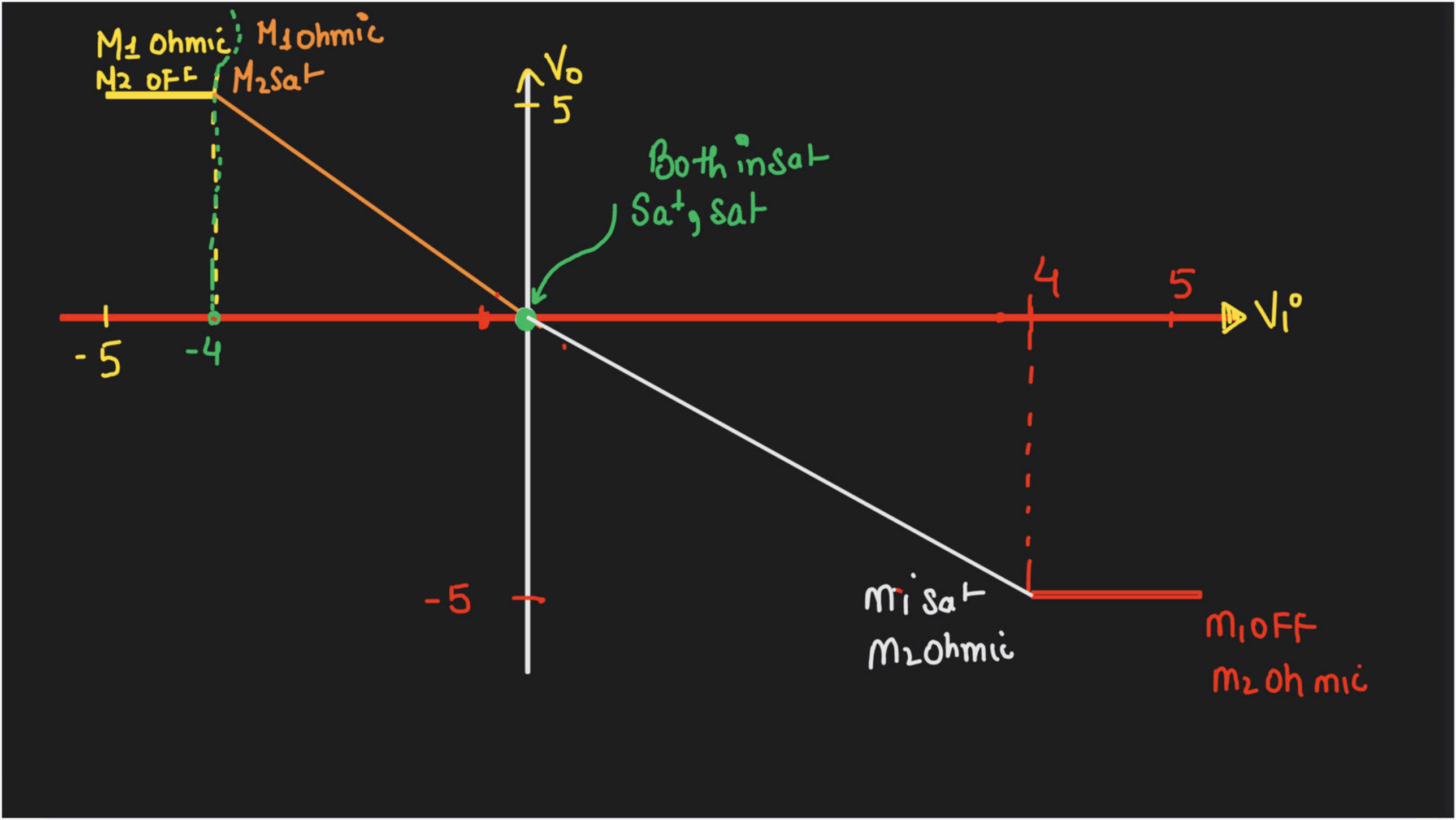


for Vi ⇒ 4 to 5

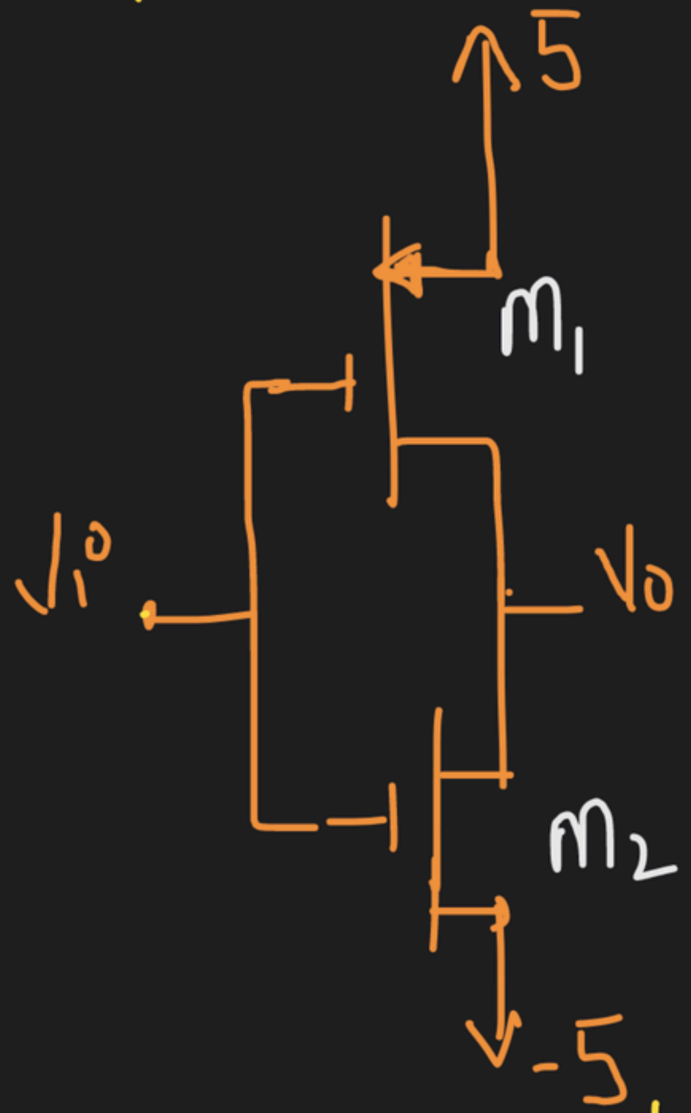
M_1 OFF

M_2 Vgs = 9 to 10

→ ohmic


M1 Ohmic
M2 OFF
M1 Ohmic
M2 Sat
Vo
5
Both in Sat
Sat, Sat
4
5
Vi°
-5
-4
-5
M1 Sat
M2 Ohmic
M1 OFF
M2 Ohmic

- Explanation



M_2 OFF $V_i^o < -4$.

M_1 ohmic as high value of V_{SG}

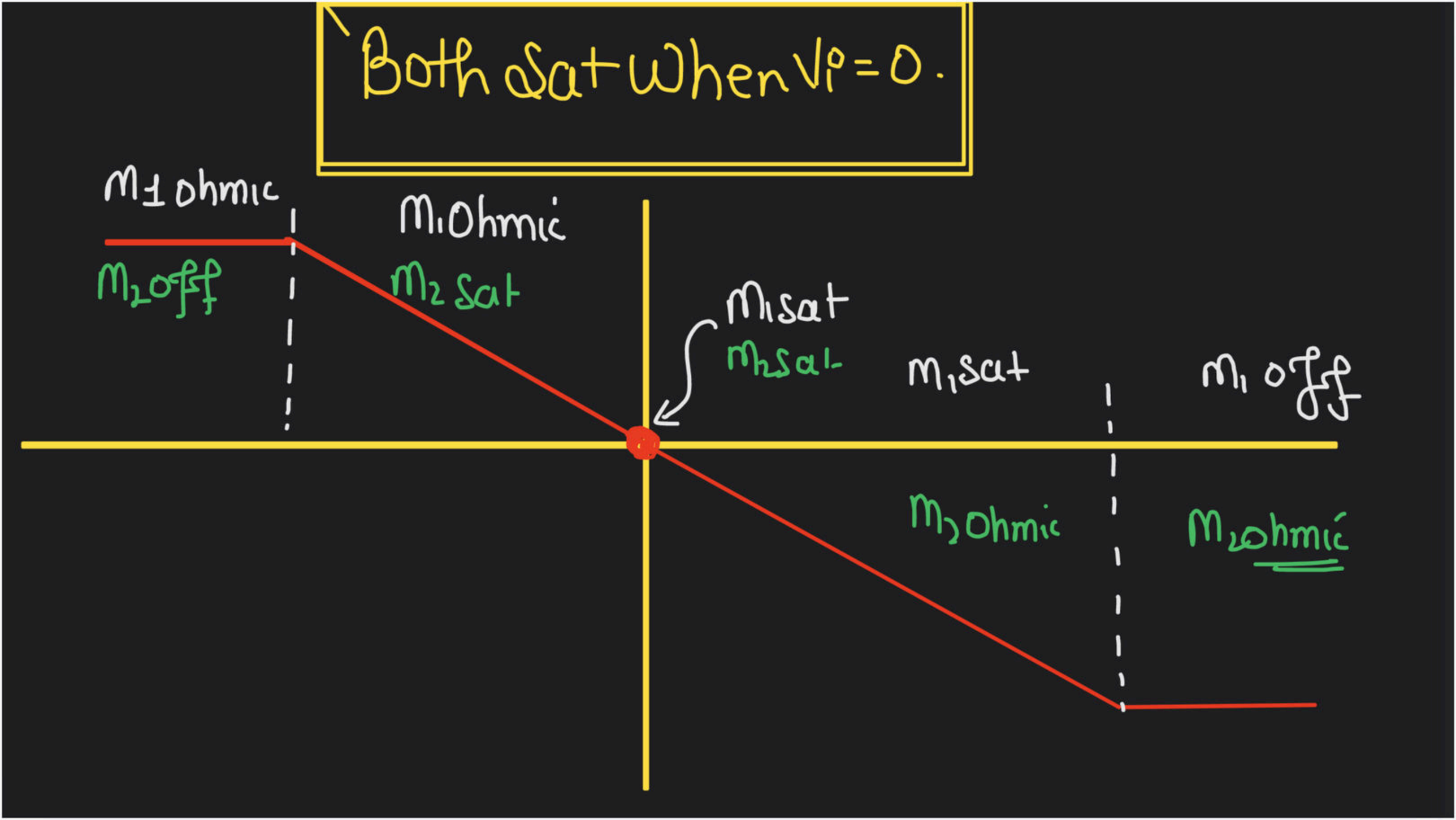
$V_o = 5$.

M_1 off $V_i^o > 4$

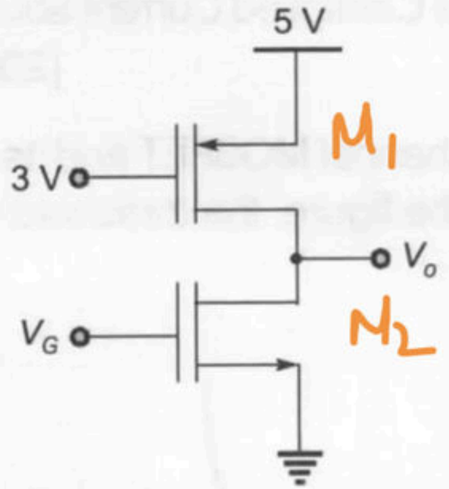
M_2 ohmic $V_o = -5$

M_1, M_2 both sat, $I_{D1} = I_{D2}$

$\frac{1}{2} u_n C_{ox} \frac{W}{L}(V_{as} - V_{th})^2 = \frac{1}{2} u_p C_{ox} \frac{W}{L}(V_{SG} - |V_{tm}|)^2$, $V_{GS} = V_{SG}$


Both Sat When Vi = 0.
M1 ohmic
M2 off
M1 Ohmic
M2 Sat
M1 sat
M2 sat
M1 sat
M1 off
M2 Ohmic
M2 ohmic

the gate voltage of the *p*-MOSFET is kept constant at 3 V. Assume that, for both transistors, the magnitude of the threshold voltage is 1 V and the product of the transconductance parameter and the (*W*/*L*) ratio, i.e. the quantity $\mu C_{ox}(W/L)$, is 1 mA · V^{-2}.



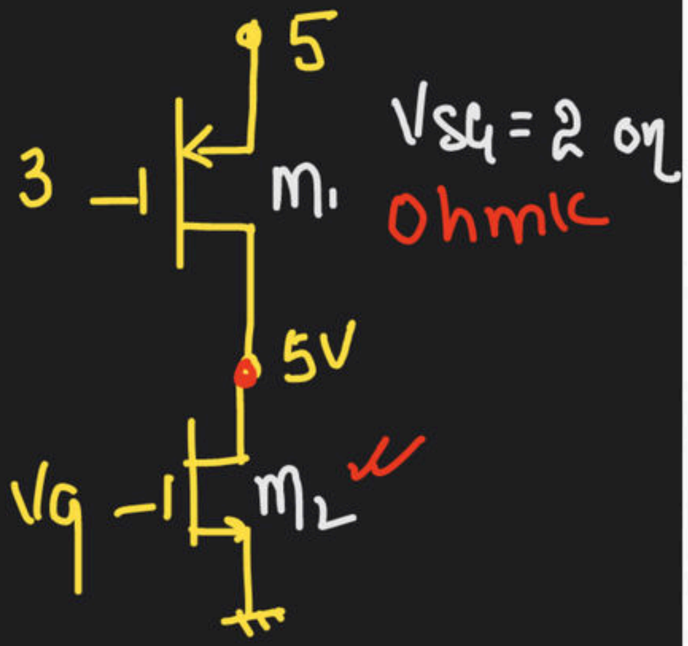
4.16 For small increase in V_G beyond 1 V, which of the following gives the correct description of the region of operation of each MOSFET?

(a) Both the MOSFETs are in saturation region
(b) Both the MOSFETs are in triode region
(c) *n*-MOSFET is in triode and *p*-MOSFET is in saturation region
(d) *n*-MOSFET is in saturation and *p*-MOSFET is in triode region

[2009 : 2 Marks]

Initally $V_G = 0$

M_2 is off



$V_{SG} = 2$ on

Ohmic

M_2 is turned on

$M_2 \rightarrow$ goin sat.

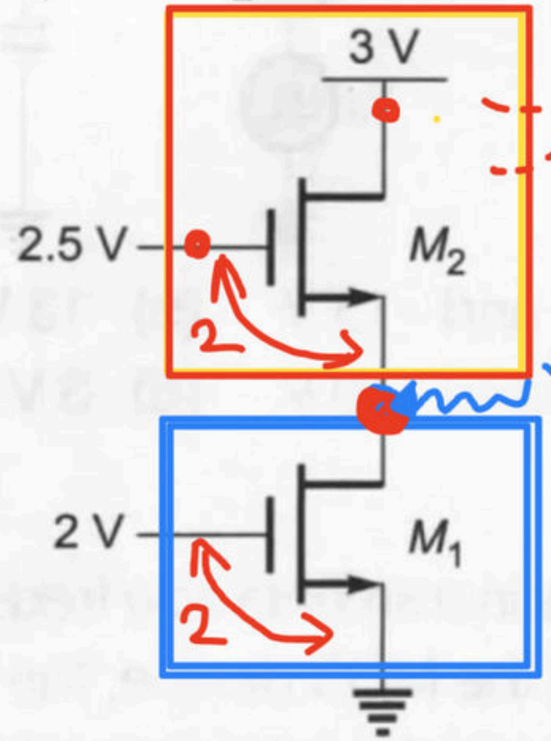
PMOS Sat

$V_{GD} > V_{th}$

$V_{GD} > -1$

$3 - 5 > -1$ No

Assuming that transistors M_1 and M_2 are identical and have a threshold voltage of 1 V, the state of transistors M_1 and M_2 are respectively



(a) Saturation, Saturation
(b) Linear, Linear
(c) Linear, Saturation
(d) Saturation, Linear

[2017 : 2 Marks, Set-2]

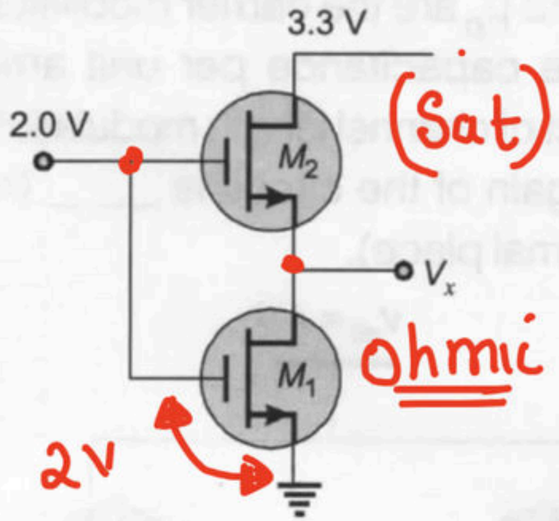
So M_2 is in sat for sure, Now for both in sat
So $I_{D1} = I_{D2}$
So $V_{GS1} = V_{GS2} = 2$
So $V_A = -.5$
Sat - Sat- not satisfied.

Sat. Sat $V_{GD} < V_{th}$
$2.5 - 3 < 1$ Yes

$V_A = -.5$

for sat $V_{GD} < V_{th}$
$2 - V_D < 1$
$V_D > 1$

In the circuit shown below, the (W/L) value for M_2 is twice that for M_1. The two nMOS transistors are otherwise identical. The threshold voltage V_T for both transistors is 1.0 V. Note that V_{GS} for M_2 must be > 1.0 V.



Current through the nMOS transistors can be modeled as

$$I_{DS} = \mu C_{ox}\left(\frac{W}{L}\right)\left((V_{GS} - V_T)\,V_{DS} - \frac{1}{2}V_{DS}^2\right) \quad \text{for } V_{DS} \le V_{GS} - V_T$$

$$I_{DS} = \mu C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2/2 \quad \text{for } V_{DS} \ge V_{GS} - V_T$$

The voltage (in volts, accurate to two decimal places) at V_x is _____.

So Solution method is easy :-

$I_{D2} = I_{D1}$

Sat ohmic

$$\frac{1}{2}\cancel{\mu_n C_{ox}}\left(\frac{W}{L}\right)_2 (V_{GS}-1)^2 = \cancel{\mu_n C_{ox}}\left(\frac{W}{L}\right)_1 \left[(V_{GS}-1)(V_{DS}) - \frac{V_{DS}^2}{2}\right]$$

$$\frac{1}{2}\cancel{\left(\frac{W}{L}\right)}_2 \left[2-V_x-1\right]^2 = \cancel{\left(\frac{W}{L}\right)}_1 \left[(2-1)V_x - \frac{V_x^2}{2}\right]$$

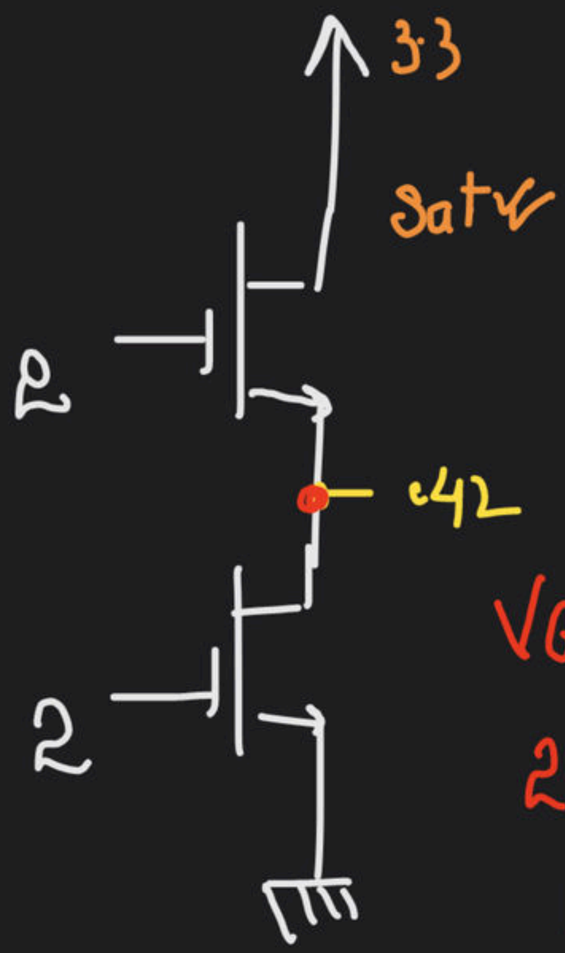
$$(W/L)_2 = 2(W/L)_1$$

$$(1-V_x)^2 = \left(V_x - \frac{V_x^2}{2}\right)$$

$$1+V_x^2-2V_x = V_x - \frac{V_x^2}{2} \;;\; 1.5V_x^2 - 3V_x + 1 = 0$$

$$V_x = 0.42,\ 1.57$$

$\therefore$ $V_x = 0.42$



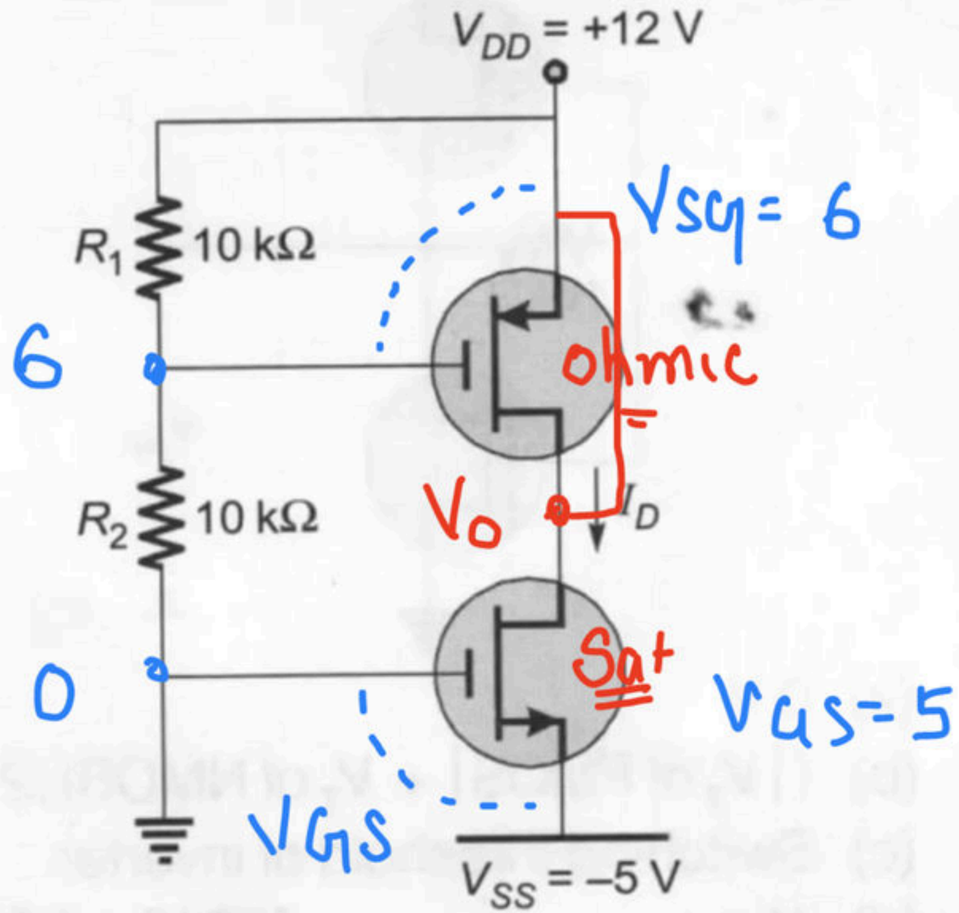
$V_{GD} < V_{th}$ x

$2 - 0.42 < V_{th}$ x

$1.58 < 1$ ✗ No

Satx ohmic mode

For the MOSFET shown in the figure, the threshold voltage $|V_t| = 2\,V$ and $K = \frac{1}{2}\mu C\left(\frac{W}{L}\right) = 0.1 mA/V^2$. The value of I_D (in mA) is _____.



[2014 : 2 Marks, Set-2]

So Sat - Sat ✗

but Vsg = 6

Vgs = 5

device with large input is in ohmic mode

✗ ✗

Sat / Sat

$I_{DP} = I_{DN}$

$\frac{1}{2}\mu C_{ox}\frac{W}{L}(6-2)^2$

$= \frac{1}{2}\mu C_{ox}\frac{W}{L}(5-2)$

So $I_{Dpoh} = I_{Dn\,sat}$

$$\cancel{\mu C_{ox}}\frac{W}{L}\left[(V_{SG}-|V_{thl}|)V_{SD}-\frac{V_{SD}^2}{2}\right]=\frac{1}{2}\cancel{\mu C_{ox}}\frac{W}{L}(5-2)^2$$

$$2\left[(6-2)(12-V_0)-\frac{(12-V_0)^2}{2}\right]=9$$

$$12-V_0=\alpha$$

$$2\left[4\alpha-\frac{\alpha^2}{2}\right]=9$$

$$8\alpha-\alpha^2=9 \qquad \alpha^2-8\alpha+9=0, \quad \alpha=6.64, 1.35$$

$12 - V_o = \alpha = 6.64, 1.35$

$V_o = 5.36$

Nmos in sat

$V_{GD} < V_{th}$

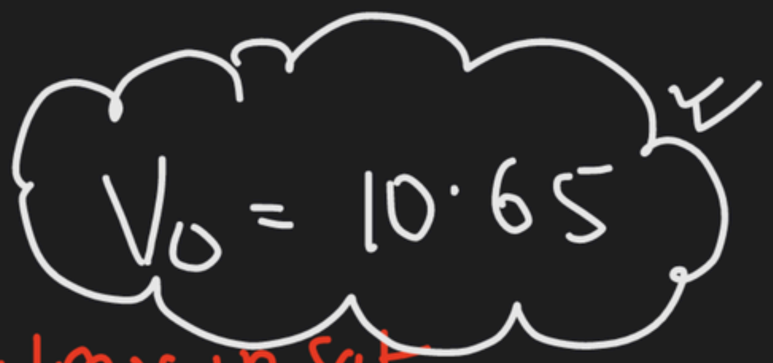
$0 - 5.36 < 2$

Yes

pmos in ohmic

$V_{GD} < V_{th}$

$6 - 5.36 < -2$ No



Nmos in sat

$V_{GD} < V_{th}$

$0 - 10.65 < 2$ Yes

pmos in ohmic

$V_{GD} < -2$

$6 - 10.65 < -2$ Yes

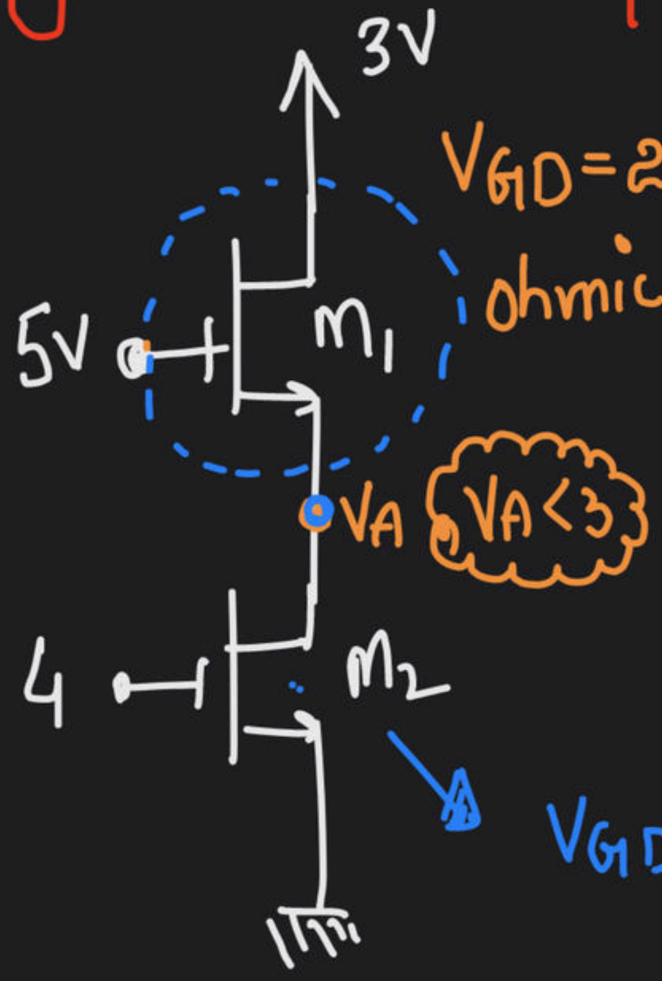
ohmic, Sat } Satisfied

$I_{D\,NMOS\,sat} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$

$= 1 \cdot (5-2)^2 \text{ mA}$

$= 9 \text{ mA}$ Ans

Q Find mode of op. of M_1, M_2



$V_{GD}=2V$ ohmic

$V_{th}=1v$. both identical find mode of op

a) ~~L L~~ b) S S

c) S L d) L S

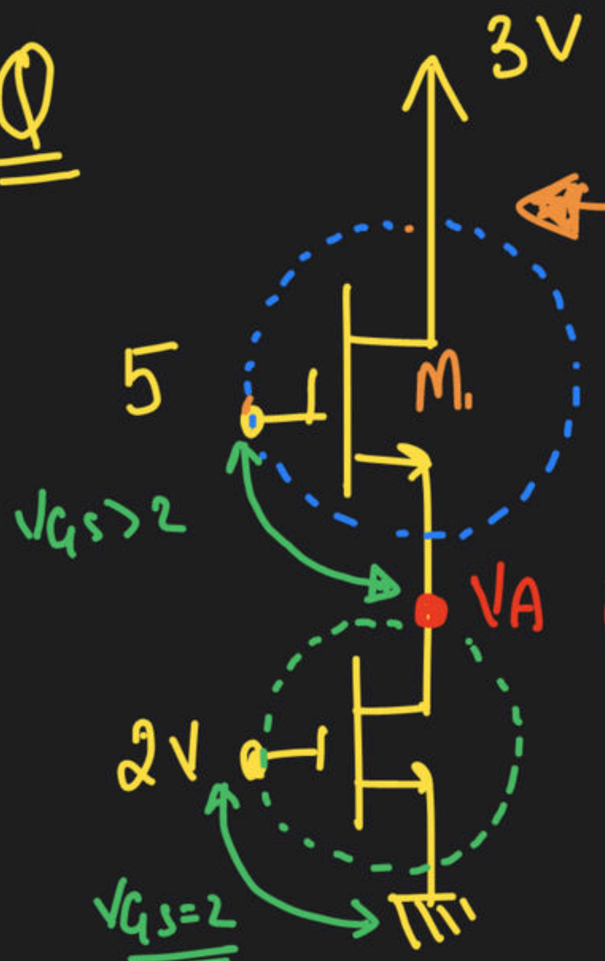
$V_{GD} = 4-V_A$ for sat

$4-V_A < 1$

$V_A > 3$

~~Sat~~

Q



Both are identical $V_{th} = 1$, find mode of op.

$V_{GD} = 2V$

$V_{GD} > V_{th}$ ohmic

$V_A < 3$

$V_{GD} = (2 - V_A) < 1$ Sat

$V_A > 1$ Sat

$V_A < 1$ ohmic

Since V_A will be close to 3 so we choose Sat

Linear Sat

Another way

$V_{GS_1} = 5 - V_A > 2$

$V_{GS_2} = 2 - 0 = 2$

So M_1 ohmic

M_2 sat.

So $I_{D1} = I_{D2}$

$$\cancel{\mu_n C_{ox}} \frac{W}{L}\left[\left(V_{GS1} - V_{th}\right) V_{DS} - \frac{V_{DS}^2}{2}\right] = \frac{1}{2}\cancel{\mu_n C_{ox}}\frac{W}{L}\left(V_{GS} - V_{th}\right)^2$$

$$2\left[\left(5 - V_A - 1\right)\left(3 - V_A\right) - \frac{\left(3 - V_A\right)^2}{2}\right] = \left(2 - 1\right)^2$$

$$2\left[\left(4 - V_A\right)\left(3 - V_A\right) - \frac{\left(3 - V_A\right)^2}{2}\right] = 1$$

$3 - V_A = \alpha$; $2\left[\left(1+\alpha\right)\alpha - \frac{\alpha^2}{2}\right] = 1$

$$2\alpha(1+\alpha) - \alpha^2 = 1$$

$$2\alpha + \alpha^2 - 1 = 0$$

$$\Rightarrow \boxed{\alpha^2 + 2\alpha - 1 = 0}$$

$$-2.41 \; , \; .414$$

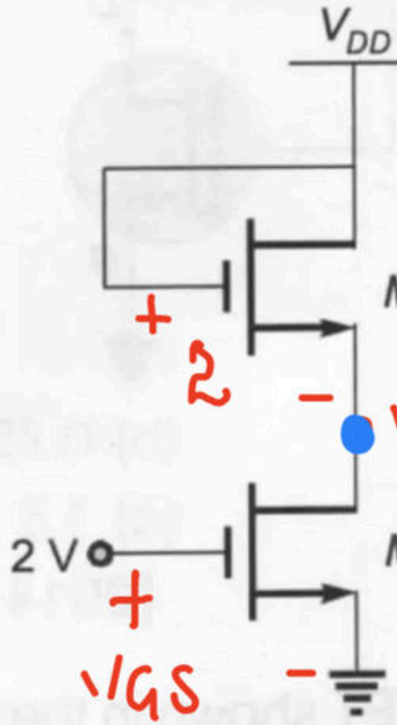
$3 - \sqrt{A} = -2.41$

$\sqrt{A} = 5.41$ X

$3 - \sqrt{A} = .414$

$\sqrt{A} = 2.586$ yes linear Sol-

In the circuit shown, both the enhancement mode NMOS transistors have the following characteristics: $k_n = \mu_n C_{ox}$ (W/L) = 1 mA/V^2; V_{TN} = 1 V. Assume that the channel length modulation parameter λ is zero and body is shorted to source. The minimum supply voltage V_{DD} (in volts) needed to ensure that transistor M_1 operates in saturation mode of operation is _____.



[2015 : 2 Marks, Set-3]

a) 2 b) 3 c) 4 d) 5

M_2 Sat ✓

$V_{DD} = 2 + V_A$

$V_{DD} > 3$

M_1 Sat ✓ ⟹ $V_{GD} < 1$

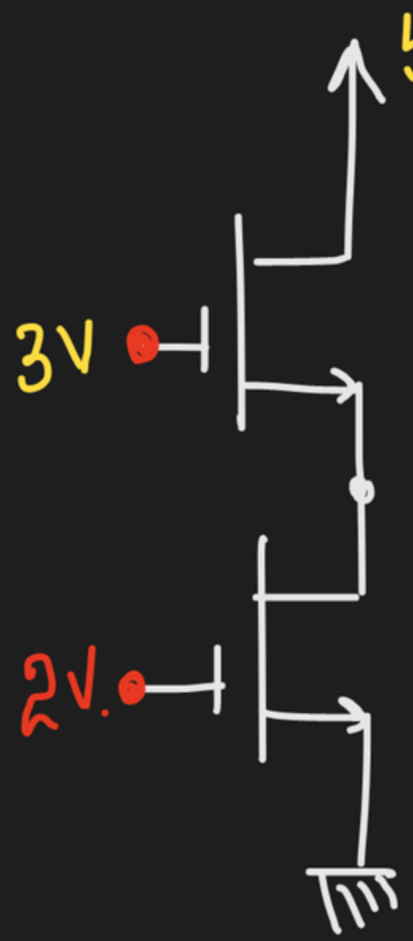
$2 - V_A < 1$

$V_A > 1$

- If all devices are identical and all in sat
  $\Rightarrow V_{GS}$ or V_{SG} is same in All
- device with large V_{GS}, V_{SG} is in ohmic mode

Find mode of op. of each device

Q1



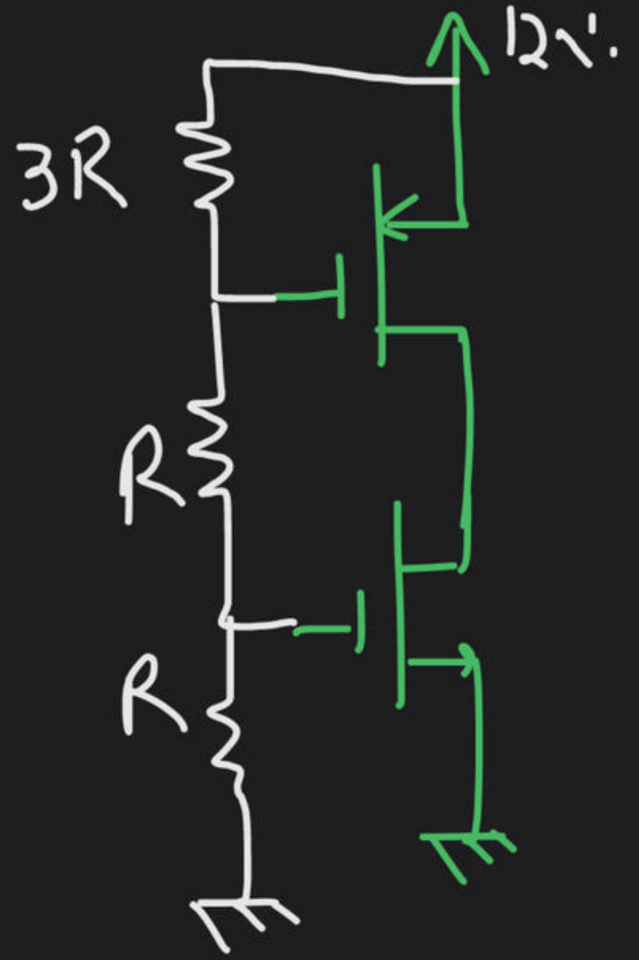
+ve all are identical

$\mu_p C_{ox} \frac{W}{L} = \mu_n C_{ox} \frac{W}{L}$

$V_{th} = 1$

Q2

Q3



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